Advanced Load Management Switch

FPF1504 / FPF1504L

Description

The FPF1504/FPF1504L are low- R_{DS} P-channel MOSFET load switches of the IntelliMAXTM family. Integrated slew-rate control prevents excessive inrush current from the supply rails with capacitive loads common in power applications. In addition, the FPF1504/FPF1504L feature output discharge capability.

The input voltage range operates from 1.0 V to 3.6 V to fulfill today's mobile device supply requirements. Switch control is by a logic input (ON pin) capable of interfacing directly with low-voltage CMOS control signals and GPIOs in embedded processors.

Features

- 1.0 V to 3.6 V Input Voltage Operating Range
- Typical R_{DS(ON)}:
 - 15 m Ω at $V_{IN} = 3.3 \text{ V}$
 - $20 \text{ m}\Omega$ at $V_{IN} = 1.8 \text{ V}$
 - $40 \text{ m}\Omega$ at $V_{IN} = 1.0 \text{ V}$
- Slew Rate Control
- Output Discharge Function
- Low <1 μA Quiescent Current at V_{ON} = V_{IN}
- ESD Protected: 4000 V HBM, 2000 V CDM
- GPIO/CMOS-Compatible Enable Circuitry
- Active HIGH and active LOW versions

Applications

- Mobile Devices and Smart Phones
- Portable Media Devices
- Digital Cameras
- Advanced Notebook, UMPC, and MID
- Portable Medical Devices
- GPS and Navigation Equipment

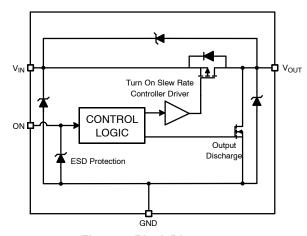


Figure 1. Block Diagram



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WLCSP4 CASE 567RH

MARKING DIAGRAM

G&K 4&2 &.&E&Z

G = 1st Digit of 2 Digit Device ID Mark
 &K = 2-Digits Lot Run Traceability Code
 4 = 2nd Digit of 2 Digit Device ID Mark

&2 = 2-digit Date Code Format

&. = Pin 1 Identifier&E = Space Designator&Z = Assembly Plant Code

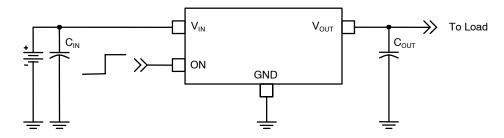
ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 2 of this data sheet.

ORDERING INFORMATION

Part Number	Top Mark	Switch (Typical) At 1.8 V _{IN}	Input Buffer	Output Discharge	ON Pin Activity	Package
FPF1504UCX	G4	20 mΩ	CMOS	YES	Active HIGH	4-Ball, WLCSP, 0.5 mm Pitch
FPF1504BUCX	G4	20 mΩ	CMOS	YES	Active HIGH	4-Ball, WLCSP with Backside Laminate, 0.5 mm Pitch
FPF1504LUCX	GZ	20 mΩ	CMOS	YES	Active LOW	4-Ball, WLCSP, 0.5 mm Pitch
FPF1504LBUCX	GZ	20 mΩ	CMOS	YES	Active LOW	4-Ball, WLCSP with Backside Laminate, 0.5 mm Pitch

Application Diagram



- NOTES: 1. C_{IN} =1 μ F, X5R, 0603, for example Murata GRM185R60J105KE26. 2. C_{OUT} = 1 μ F, X5R, 0805, for example Murata GRM216R61A105KA01.

Figure 2. Typical Application

Pin Configurations



Figure 3. 1 x 1 mm WLCSP Bumps Facing Down

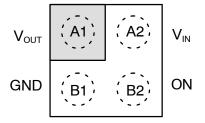


Figure 5. Pin Assignments (Top View)

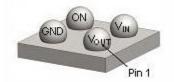


Figure 4. 1 x 1 mm WLCSP Bumps Facing Up

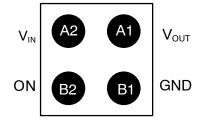


Figure 6. Pin Assignments (Bottom View)

PIN DEFINITIONS

Pin#	Name	Description
A1	V _{OUT}	Switch Output
A2	V _{IN}	Supply Input; Input to the Power Switch
B1	GND	Ground
B2	ON	ON/OFF Control

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter			Max.	Unit
V _{IN}	$V_{\text{IN}}, V_{\text{OUT}}, V_{\text{ON}}$ to GND	V _{IN} , V _{OUT} , V _{ON} to GND			V
I _{SW}	Maximum Continuous Switch Current	Maximum Continuous Switch Current			Α
P_{D}	Power Dissipation at T _A = 25°C		1.0	W	
T _{STG}	Storage Junction Temperature			+150	°C
T _A	Operating Temperature Range			+85	°C
θЈА	Thermal Resistance, Junction-to-Ambient	1S2P with 1 Thermal Via 1S2P without Thermal Via		95	°C/W
				187	
ESD	Electrostatic Discharge Capability	Human Body Model, JESD22-A114			kV
		Charged Device Model, JESD22-C101	2		

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

RECOMMENDED OPERATING CONDITIONS

Ī	Symbol	Parameter	Min.	Max.	Unit
	V _{IN}	Supply Voltage	1.0	3.6	V
	T _A	Ambient Operating Temperature	-40	+85	°C

Functional operation above the stresses listed in the Recommended Operating Ranges is not implied. Extended exposure to stresses beyond the Recommended Operating Ranges limits may affect device reliability.

ELECTRICAL CHARACTERISTICS

Unless otherwise noted, V_{IN} = 1.0 to 3.6 V, T_A = -40 to +85°C; Typical Values are at V_{IN} = 3.3 V and T_A = 25°C.

Symbol	Parameter		Conditions	Min.	Тур.	Max.	Unit
IC OPERAT	TION						
V _{IN}	Supply Voltage			1.0		3.6	٧
I _{Q(OFF)}	Off Supply Current	FPF1504	V _{ON} = GND, V _{OUT} = Open		0.25		μΑ
		FPF1504L	V _{ON} = V _{IN} , V _{OUT} = Open		0.3		
I _{SD(OFF)}	Off Switch Current	FPF1504	V _{ON} = GND, V _{OUT} = GND		0.25		
		FPF1504L	V _{ON} = V _{IN} , V _{OUT} = GND		0.3		_
IQ	Quiescent Current	FPF1504	I _{OUT} = 0 mA, V _{IN} = 3.6 V, V _{ON} = V _{IN}		0.08		
			IOUT = 0 mA, VON = VIH(MIN)		0.75		_
		FPF1504L	I_{OUT} = 0 mA, V_{IN} = 3.6 V, V_{ON} = GND		0.08		
			I _{OUT} = 0 mA, Von = VIL(MAX)		0.95		1
R _{ON}	On Resistance	I	V _{IN} = 3.3 V, I _{OUT} = 200 mA, T _A = 25°C		15	30	mΩ
			V _{IN} = 1.8 V, I _{OUT} = 200 mA, T _A = 25°C		20	40	
			V _{IN} = 1.5 V, I _{OUT} = 200 mA, T _A = 25°C		30		
			$V_{IN} = 1.0 \text{ V}, I_{OUT} = 200 \text{ mA},$ $T_A = 25^{\circ}\text{C}$		40	80	
			V_{IN} = 1.8 V, I_{OUT} = 200 mA, T_A = 85°C (Note 3)		35	50	
R _{PD}	Output Discharge Pull-Down Resistance		$V_{ON} = 0 \text{ V or } V_{IN}, I_{OUT} = -20 \text{ mA}$		65	95	Ω
V _{IH}	On Input Logic High Voltage	FPF1504		0.8			V
V_{IL}	On Input Logic Low Voltage	FPF1504				0.3	
I _{ON}	On Input Leakage		V _{ON} = V _{IN} or GND			1	μA
AMIC CHAI	RACTERISTICS					•	
t _{DON}	Turn-On Delay (Note 4)	FPF1504	$R_L = 10 \ \Omega, \ C_L = 0.1 \ \mu F,$		80		μs
t _R	V _{OUT} Rise Time (Note 4)	FPF1504	$V_{IN} = 3.3 \text{ V}, T_{A} = 25^{\circ}\text{C}$		130		
t _{ON}	Turn-On Time (Note 4)	FPF1504			210		1
t _{DON}	Turn-On Delay (Note 4)	FPF1504	$R_L = 500 \Omega$, $C_L = 0.1 \mu F$,		70	100	μs
		FPF1504L	$V_{IN} = 3.3 \text{ V}, T_A = 25^{\circ}\text{C}$		95		
t _R	V _{OUT} Rise Time (Note 4)	FPF1504			110	150	1
		FPF1504L			115		1
t _{ON}	Turn-On Time (Note 4)	FPF1504	-		180	250	1
		FPF1504L			210		1
t _{DOFF}	Turn-Off Delay (Note 4)	FPF1504	R _L =10 Ω, C _L = 0.1 μF,		25	30	μs
t _F	V _{OUT} Fall Time (Note 4)	FPF1504	$V_{IN} = 3.3 \text{ V}, T_A = 25^{\circ}\text{C}$		2		1
t _{OFF}	Turn-Off Time (Note 4)	FPF1504			27		1

ELECTRICAL CHARACTERISTICS (continued)

Unless otherwise noted, V_{IN} = 1.0 to 3.6 V, T_A = -40 to +85°C; Typical Values are at V_{IN} = 3.3 V and T_A = 25°C.

Symbol	Parameter		Conditions	Min.	Тур.	Max.	Units
DYNAMIC CHAF	RACTERISTICS						
t _{DOFF}	Turn-Off Delay	FPF1504	$R_L = 500 \Omega$, $C_L = 0.1 \mu F$,		25		μs
	(Note 4)	FPF1504L	$V_{IN} = 3.3 \text{ V}, T_A = 25^{\circ}\text{C}$		2		
t _F	V _{OUT} Fall Time	FPF1504			12		
	(Note 4)	FPF1504L	7		14		
t _{OFF}	Turn-Off Time	FPF1504			37		
1	(Note 4)	FPF1504L	7		16		

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

3. This parameter is guaranteed by design and characterization; not production tested.

- t_{DON}/t_{DOFF}/t_R/t_F are defined in Figure 7.
 Output discharge path is enabled during off.

Timing Diagram - FPF1504

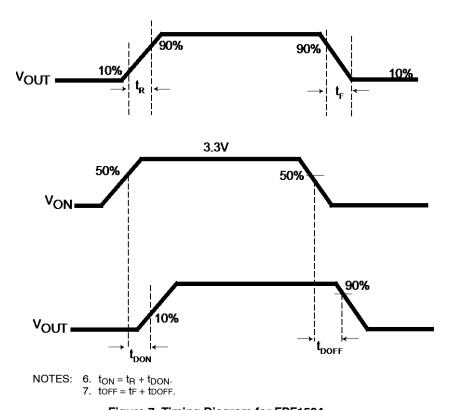
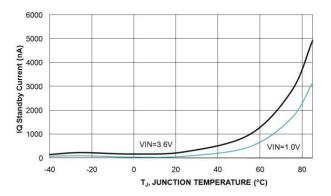


Figure 7. Timing Diagram for FPF1504

TYPICAL PERFORMANCE CHARACTERISTICS FOR FPF1504

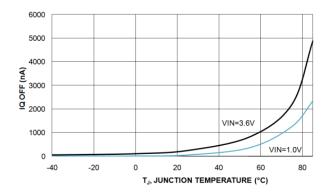
Applicable to active high version only.



4000 3500 3000 **85°C 2** 2500 **2** 2500 **2** 1500 **2** 1000 **2** 1000 **2** 1000 **3** 1000 **4** 25°C **5** 1000 **1** 1.5 2.0 2.5 3.0 3.5 **SUPPLY VOLTAGE (V)**

Figure 1. Shutdown Current vs. Temperature

Figure 2. Shutdown Current vs. Supply Voltage



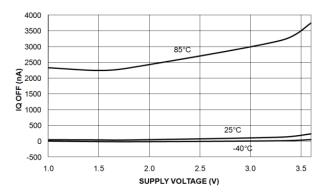
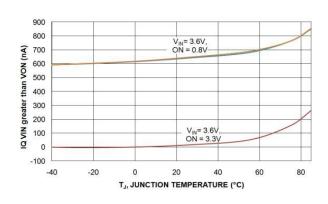


Figure 3. Off Supply Current vs. Temperature

Figure 4. Off Supply Current vs. Supply Voltage



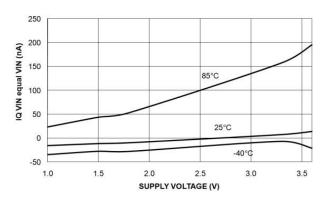
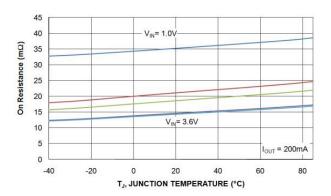


Figure 5. Quiescent Current vs. Temperature

Figure 6. Quiescent Current vs. Supply Voltage $(V_{ON} = V_{IN})$

TYPICAL PERFORMANCE CHARACTERISTICS FOR FPF1504

Applicable to active high version only.



45 40 Resistance (mQ) 35 30 25 85°C 25°C 20 9 15 10 5 I_{OUT} = 200mA 0 1.0 2.0 2.5 3.0 3.5 1.5 SUPPLY VOLTAGE (V)

Figure 7. R_{ON} vs. Temperature

Figure 8. R_{ON} vs. Temperature

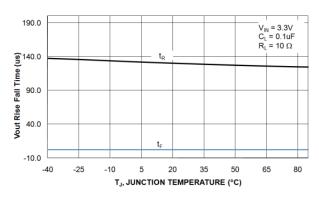


Figure 9. V_{OUT} Rise/Fall Times vs. Temperature (R_L = 10 Ω)

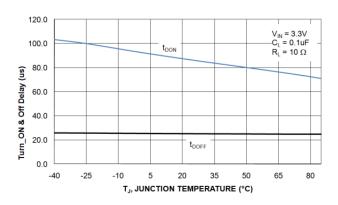


Figure 10. V_{OUT} Turn-On/Turn-Off Delays vs. Temperature (R_L = 10 Ω)

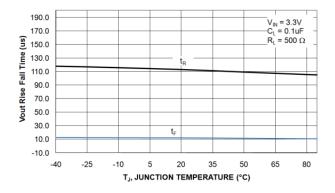


Figure 11. V_{OUT} Rise/Fall Time vs. Temperature (R_L = 500 Ω)

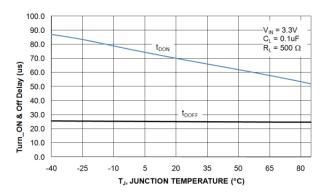


Figure 12. V_{OUT} Turn-On/Turn-Off Delays vs. Temperature (R_L = 500 Ω)

TYPICAL PERFORMANCE CHARACTERISTICS FOR FPF1504

Applicable to active high version only.

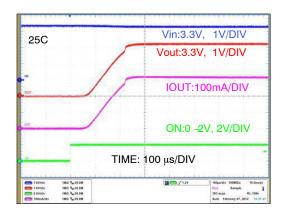


Figure 13. Turn–On Response (V_{IN} = 3.3 V, C_{OUT} = 0.1 μ F, R_L = 10 Ω)

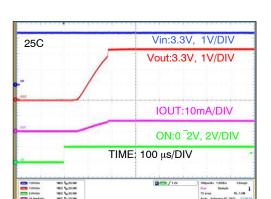


Figure 15. Turn–On Response (V_{IN} = 3.3 V, C_{OUT} = 0.1 μ F, R_L = 500 Ω)

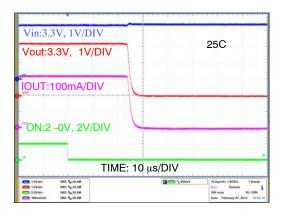


Figure 14. Turn–Off Response (V_{IN} = 3.3 V, C_{OUT} = 0.1 μ F, R_L = 10 Ω)

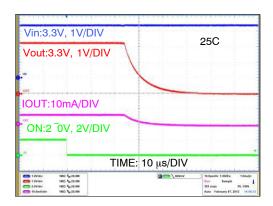


Figure 16. Turn–Off Response (V_{IN} = 3.3 V, C_{OUT} = 0.1 μ F, R_L = 500 Ω)

APPLICATION INFORMATION

Input Capacitor

IntelliMAX switches don't require an input capacitor. To reduce device inrush current, a 0.1 μF ceramic capacitor, C_{IN} , is recommended close to the VIN pin. A higher value of C_{IN} can be used to further reduce the voltage drop experienced as the switch is turned on into a large capacitive load.

Output Capacitor

IntelliMAX switches work without an output capacitor. If the applications parasitic board inductance forces V_{OUT} below GND when switching off, a 0.1 μF capacitor, C_{OUT} , should be placed between V_{OUT} and GND.

Fall Time

Device output fall time can be calculated based on RC constant of external components as follows:

$$t_F = R_L \times C_L \times 2.2$$
 (eq. 1)

where t_F is 90% to 10% fall time, R_L is output, load and C_L is output capacitor.

The same equation works for a device with a pull-down output resistor, then R_L is replaced by a parallel connected pull-down and external output resistor combination, as follows:

$$t_F = \frac{R_L \times R_{PD} \times C_L}{R_L + R_{PD}} \times 2.2$$
 (eq. 2)

where t_F is 90% to 10% fall time, R_L is output load, R_{PD} is output pull–down resistor (65 Ω typical), and C_L is the output capacitor.

RECOMMENDED LAND PATTERN AND LAYOUT

For best thermal performance and minimal inductance and parasitic effects, it is recommended to keep input and output traces short and the capacitors as close to the device as possible. Below is a recommended layout for this device to achieve optimum performance.

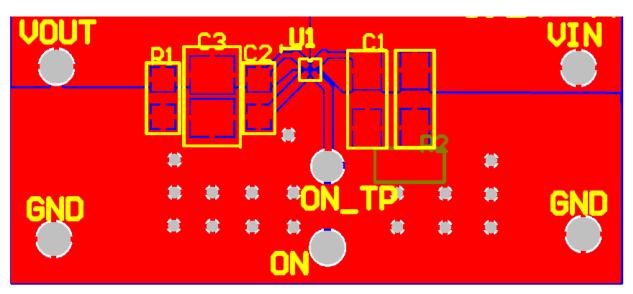


Figure 17. Recommended Land Pattern and Layout

The following information applies to the WLCSP package dimensions on the next page:

PRODUCT-SPECIFIC DIMENSIONS

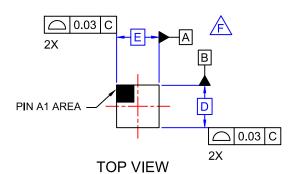
Product	D	E	Х	Υ	
FPF1504UCX					
FPF1504BUCX	960 μm ±30 μm	960 μm ±30 μm	0.230 mm	0.230 mm	
FPF1504LUCX				0.230 111111	
FPF1504LBUCX					

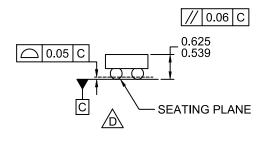
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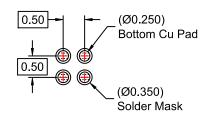
WLCSP4 0.96x0.96x0.582

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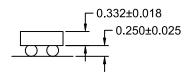
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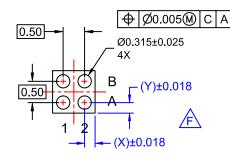




RECOMMENDED LAND PATTERN (NSMD PAD TYPE)



SIDE VIEWS



BOTTOM VIEW

NOTES:

- A. NO JEDEC REGISTRATION APPLIES.
- B. DIMENSIONS ARE IN MILLIMETERS.
- C. DIMENSIONS AND TOLERANCES PER ASME Y14.5M, 2009.
- D. DATUM C IS DEFINED BY THE SPHERICAL CROWNS OF THE BALLS.
- E. PACKAGE NOMINAL HEIGHT IS 582 MICRONS ±43 MICRONS (539-625 MICRONS).

FOR DIMENSIONS D, E, X, AND Y SEE PRODUCT DATASHEET.

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