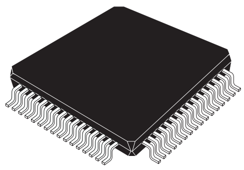
TDA7705

Highly integrated tuner for AM/FM car radio

Features

- Fully integrated VCO for world tuning
- High performance PLL for fast RDS system
- AM/FM mixers with high image rejection
- Integrated AM-LNA and AM-PINDIODE
- Automatic self alignment for preselection and image rejection
- Digital IF signal processing, high performance and drift-free
- Integrated IF-filters with high selectivity, high dynamic range and adaptive bandwidth control
- RDS demodulation with group and block synchronization
- High performance stereodecoder with noiseblanker
- I^{2}C/SPI bus controlled
- Single 5 V supply
- LQFP64 package



LQFP64

Description

The TDA7705 highly integrated tuner (HIT) is a new generation of high performance tuners for carradio applications.

It contains mixers and IF amplifiers for AM and FM, fully integrated VCO and PLL synthesizer, IF-processing including adaptive bandwidth control, stereo decoder and RDS decoder on a single chip.

The utilization of digital signal processing results in numerous advantages against today's tuners: very low number of external components, very small space occupation and easy application, very high selectivity due to digital filters, high flexibility by software control and automatic alignment.

Table 1. Device summary

Order code	Package	Packing
TDA7705	LQFP64 (10x10x1.4mm)	Tray
TDA7705TR	LQFP64 (10x10x1.4mm)	Tape and reel

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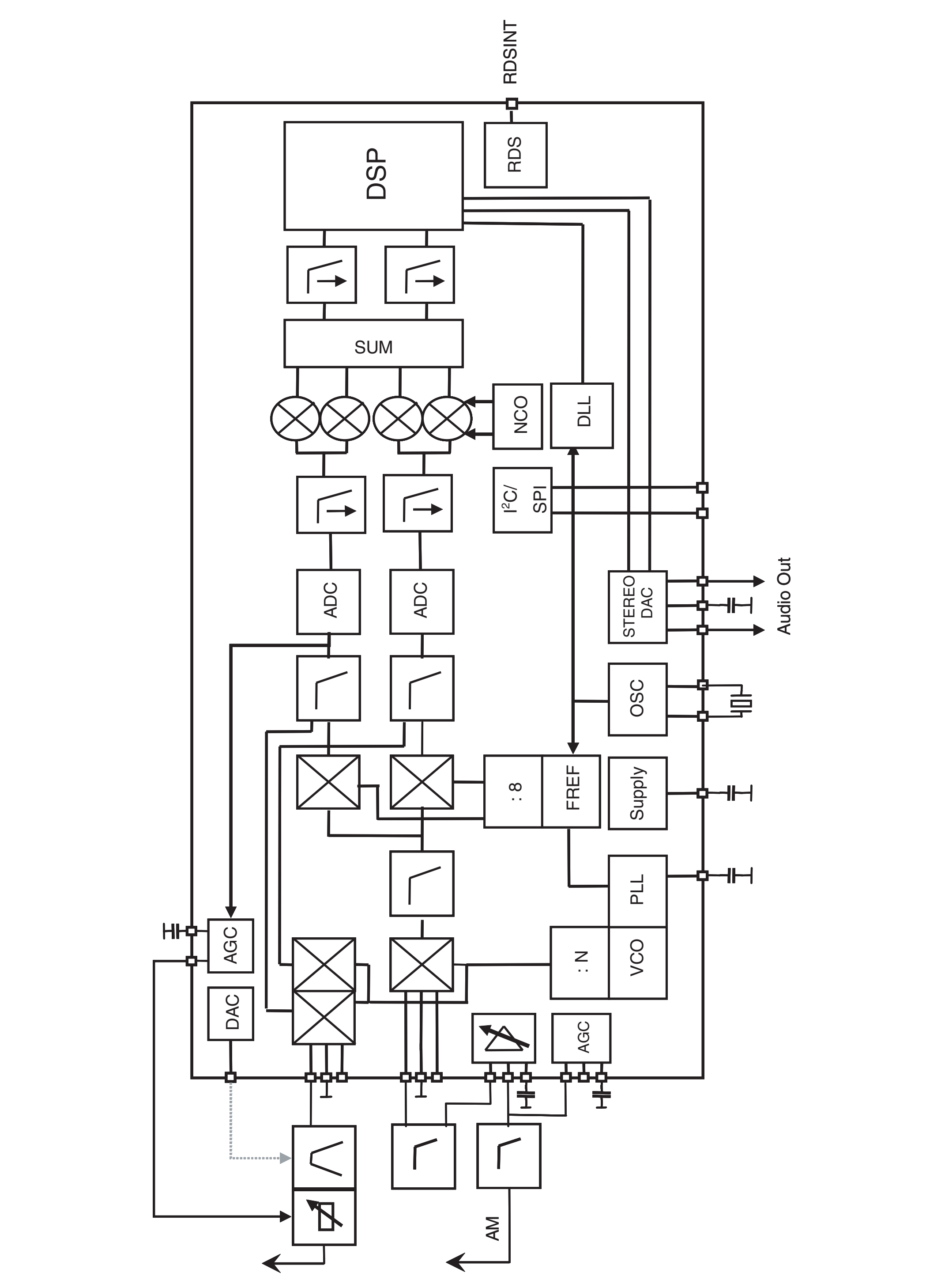
1 Block diagram and pins description

1.1 Block diagram

Figure 1. Functional block diagram



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1.2 Pin description

Figure 2. Pin connection (top view)

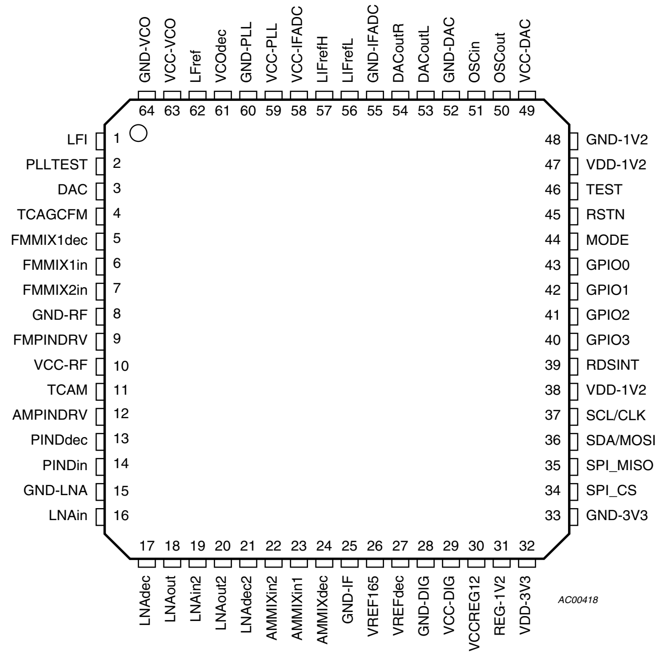

Table 2. Pin description

Pin #	Pin name	Function
1	LF1	PLL loopfilter output
2	PLLTEST	PLL test output / GPO
3	DAC	FM tuning DAC output
4	TCAGCFM	FM AGC time constant
5	FMMIX1dec	FM mixer decoupling
6	FMIX1in	FM mixer input 1
7	FMIX2in	FM mixer input 2
8	GND-RF	RF Ground
9	FMPINDRV	FM AGC PIN diode driver
10	VCC-RF	5V supply for RF section
11	TCAM	AM AGC time constant
12	AMPINDRV	AM AGC external PIN diode driver
13	PINDdec	AM AGC internal PIN diode decoupling
14	PINDin	AM AGC internal PIN diode input
15	GND-LNA	AM LNA and internal PIN diode GND
16	LNAin	AM LNA input

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Table 2. Pin description (continued)

Pin #	Pin name	Function
17	LNAdec	AM LNA decoupling
18	LNAout	AM LNA output first stage
19	LNAin2	AM LNA input 2^{nd} stage
20	LNAout2	AM LNA output
21	LNAdec2	AM LNA decoupling 2^{nd} stage
22	AMMIXin2	AM mixer input 2
23	AMMIXin1	AM mixer input 1
24	AMMIXdec	AM mixer decoupling
25	GND-IF	IF and Vref GND
26	VREF165	1.65V reference voltage decoupling
27	VREFdec	3.3V reference voltage decoupling
28	GND-DIG	Digital GND
29	VCC-DIG	5V supply for digital logic
30	VCCreg1V2	VCC of 1.2V regulator
31	REG1V2	1.2V regulator output
32	VDD-3V3	3.3V VDD output / decoupling
33	GND-3V3	3.3V VDD GND
34	SPI_CS	SPI chip select
35	SPI_MISO	SPI Data output
36	SDA / SPI_MOSI	I^2C bus data / SPI data input
37	SCL / SPI_CLK	I^2C bus Clock / SPI clock
38	VDD-1V2	1.2V DSP supply
39	RDSINT	RDS interrupt
40	GPIO3	Reserved
41	GPIO2	Reserved
42	GPIO 1	Reserved
43	GPIO 0	Reserved
44	MODE	For debug purpose only, connected to GND
45	RSTN	Reset pin (active low)
46	TEST	Test input
47	VDD-1V2	1.2V DSP supply
48	GND-1V2	Digital GND for 1.2V VDD
49	VCC-DAC	5V supply of audio DAC
50	OSCout	Xtal osc output
51	OSCin	Xtal osc input

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Table 2. Pin description (continued)

Pin #	Pin name	Function
52	GND-DAC	Audio DAC GND
53	DACoutL	Audio output left
54	DACoutR	Audio output right
55	GND-IFADC	IF ADC GND
56	LIFrefL	IF ADC reference low
57	LIFrefH	IF ADC reference high
58	VCC-IFADC	5V supply of IF ADC
59	VCC-PLL	5V supply of PLL
60	GND-PLL	PLL GND
61	VCO-dec	VCO decoupling
62	LFref	Loopfilter reference
63	VCC-VCO	5V supply of VCO
64	GND-VCO	VCO GND

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2 Function description

2.1 FM - mixers

The image-rejection mixer has two FM inputs, selectable through software. These inputs feed stages with different gains, noise figures, and IIP3. They are optimized for best performance in case of a passive tuned prestage and for a passive fixed bandpass without tuning for low-cost application respectively.

The second input offers also the possibility of an easy addition of a weather-band preselection filter.

The input frequency is downconverted to low IF with high image rejection.

The tuned application is supported by an 8-bit tuning DAC. The alignment of the DAC is performed automatically.

2.2 FM - AGC

The programmable RFAGC senses the mixer input whereas the IFAGC senses the IFADC input to avoid overload.

The PIN diode driver is able to drive external PIN diodes with a current value as high as 15mA.

The time constant of the FM-AGC is defined by an external capacitor.

2.3 AM - LNA

The AM-LNA is integrated with low noise and high IIP2 and IIP3. The gain of the LNA is controlled by the AGC. The maximum gain is set with an external resistor, typically 26 dB with 1 kΩ.

2.4 AM - AGC

The programmable AM-RF-AGC senses the mixer inputs and controls the internal PIN diode and LNA gain.

First the LNA gain is reduced by about 10dB, then the PIN diodes are activated to attenuate the signal.

The time constant of the AM-AGC is defined with an external capacitor and programmable internal currents.

2.5 AM - mixers

The image-rejection mixer has two AM inputs selectable via software. It easily supports low-cost applications for extended frequency bands like SW, DRM.

The input frequency is converted to low IF with high image rejection.

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2.6 IF A/D converters

A high performance IQ-IFADC converts the IF-signal to digital IF for subsequent digital signal processing.

2.7 Audio D/A converters

A stereo DAC provides the left / right audio signals after IF-processing and stereodecoding by the DSP.

2.8 VCO

The VCO is fully integrated without any external tuning component. It covers all FM frequency bands including EU, US , Japan, EastEU, Weatherband and AM-bands including LW, MW, SW.

2.9 PLL

The high speed tuning PLL is able to settle within about 300 µs for fast RDS applications.

The frequency step can be as low as 5 kHz in FM and 500 Hz in AM.

2.10 Crystal oscillator

The device works with a 37.05 MHz fundamental tone crystal, and can be used also with a 3^{rd} overtone 37.05 MHz crystal.

2.11 DSP

The DSP and its hardware accelerators perform all the digital signal processing. The main program is fixed in ROM. Control parameters are copied in RAM and are accessible and modifiable there, thus allowing parametric performance optimization.

It performs:

- digital down-conversion of IF
- bandwidth selection with variable controlled bandwidth
- FM and AM noiseblanking
- FM/AM demodulation with softmute, high-cut, weak signal processing and quality detection
- FM stereo decoding with stereo blend
- RDS demodulation including error correction and block synchronization with generation of an RDS interrupt for the main µP
- Autonomous control of RDS-AF tests
- Self alignment of preselection tuning

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2.12 IO interface pins

The TDA7705 has the following IO pins:

PLLTEST	pin 2	general purpose output
SPI_CS	pin 34	serial communication with µP
SPI_MISO	pin 35	serial communication with µP
SDA/MOSI	pin 36	serial communication with µP
SCL/CLK	pin 37	serial communication with µP
RDSINT	pin 39	serial communication with µP
RSTN	pin 45	reset pin driven by µP

The pins labeled GPIO0, 1, 2 and 3 (pins 43 to 40) are reserved.

The pin PLLTEST output voltage can be freely programmed via software and be used to drive switches if needed by the application.

All the inputs are voltage-tolerant up to 3.5 V . The outputs can drive currents up to 0.5 mA from the internal 3.3 V supply line.

2.13 Serial interface

The device is controlled with a standard I^2C bus or SPI interface.

Through the serial bus the processing parameters can be modifed and the signal quality parameters and the RDS information can be read out.

The operation of the device is handled through high level commands sent by the main car-radio µP through the serial interface, which allow to simplify the operations carried out in the main µP. The high level commands include among others:

- set frequency (which allows to avoid computing the PLL divider factors);
- start seek (the seek operation can be carried out by the TDA7705 in a completely autonomous fashion);
- RDS seek/search (jumps to AF and quality measurements are automatically sequenced).

2.13.1 Serial interface choice / boot mode

The device can communicate with the main µP with two different standard serial protocols: SPI and I^2C. The configuration is chosen by setting the proper value (0V or 3.3V) at pins 35 and 39 and it is latched (e.g. made effective) when the RSTN line transitions from low to high (when RSTN is low, the IC is in reset mode).

The voltage level forced to pins 35 and 39 must be released to start the system operation a suitable time after the RSTN line has gone high.

The list of configurations is shown in the following table:

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Table 3. Boot mode pin configuration

Configuration:		I^2C (addr. 0 x C2)		I^2C (addr. 0 x C8)		SPI	
Pin		at reset	operation	at reset	operation	at reset	operation
39	RDSINT	0 in	RDS interrupt out	0 in	RDS interrupt out	1 in	RDS interrupt out
37	SCL	x	I^2C SCL in	x	I^2C SCL in	x	SPI CLK in
36	SDA	x	I^2C SDA in/out	x	I^2C SDA in/out	x	SPI MOSI in
35	(SPI_MISO)	0 in	-	1 in	-	1 in	SPI MISO out
34	(SPI_CS)	x	-	x	-	x	SPI SS in

If I^2C serial bus is chosen as means of communication with the controlling device, two chip addresses are possible: 0xC2/C3 or 0xC8/C9, depending on the initial configuration of pins 35 and 39.

The status of pins 35 and 39 during the reset phase can be set to:

- **high**, through external <10 kΩ resistors tied to 3.3V (pin 32), or
- **low**, by not forcing any voltage on them from outside, as 50 kohm internal pull-down resistors are present on said pins.

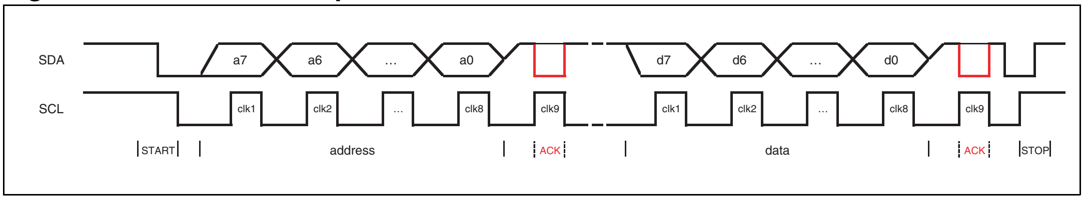
To make sure the boot mode is correctly latched up at start-up, it is advisable to keep the RSTN line low until the IC supply pins have reached their steady state, and then for an additional time T_{reset} (see *Section 3.4.8*).

2.13.2 I^2C bus protocol

I^2C requires two signals: clock (SCL) and data (SDA - bidirectional). The protocol requires an acknowledge after any 8-bit transmission.

A "write" communication example is shown in the figure below, for an unspecified number of data bytes (see the relevant technical documentation for frame structure description):

Figure 3. I^2C "write" sequence



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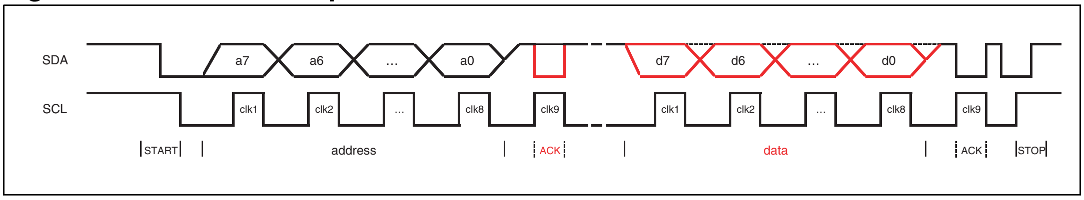
The sequence consists of the following phases:

- START: SDA line transitioning from H to L with SCL fixed H. This signifies a new transmission is starting;
- data latching: on the rising SCL edge. The SDA line can transition only when SCL is low (otherwise its transitions are interpreted as either a START or a STOP transition);
- ACKnowledge: on the 9th SCL pulse the µP keeps the SDA line H, and the TDA7705 pulls it down if communication has been successful. Lack of the acknowledge pulse generation from the TDA7705 means that the communication has failed;
- a chip address byte must be sent at the beginning of the transmission. The value can be C2 or C8 (according to the mode chosen at start-up during boot) for "write";
- as many data bytes as needed can follow the address before the communication is terminated. See the next section for details on the frame format;
- STOP: SDA line transitioning from L to H with SCL H. This signifies the end of the transmission.

Red lines represent transmissions from the TDA7705 to the µP.

A "read" communication example is shown in the figure below, for an unspecified number of data bytes (see later on for frame structure decription):

Figure 4. I^{2}C "read" sequence



The sequence is very similar to the "write" one and has the same constraints for start, stop, data latching. The differences follow:

- a chip address must always be sent by the µP to the TDA7705; the address must be C3 (if C2 had been selected at boot) or C9 (if C8 had been selected at boot);
- a header is transmitted after the chip address (the same happens for "write") before data are transferred from the TDA7705 to the µP. See the relevant technical documentation for details on the frame format;
- when data are transmitted from the TDA7705 to the µP, the µP keeps the SDA line H;
- the ACKnowledge pulse is generated by the µP for those data bytes that are sent by the TDA7705 to the µP. Failure of the µP to generate an ACK pulse on the 9th CLK pulse has the same effect on the TDA7705 as a STOP.

The max. clock speed is 500 kbit/s.

2.13.3 SPI bus protocol

SPI requires four signals: clock (CLK), master output/slave input (MOSI - for communication from the µP to the TDA7705), master input/slave output (MISO - for communication from the TDA7705 to the µP), chip select (CS). CLK is generated by the master device and is used for synchronization. MOSI and MISO are the data lines. The CS line is unique for each device in an SPI bus. The µP pulls low the TDA7705 CS line to select it for communication. The protocol does not foresee any transmission acknowledgement.

The SPI protocol has four possible modes of operation as far as data latching is concerned:

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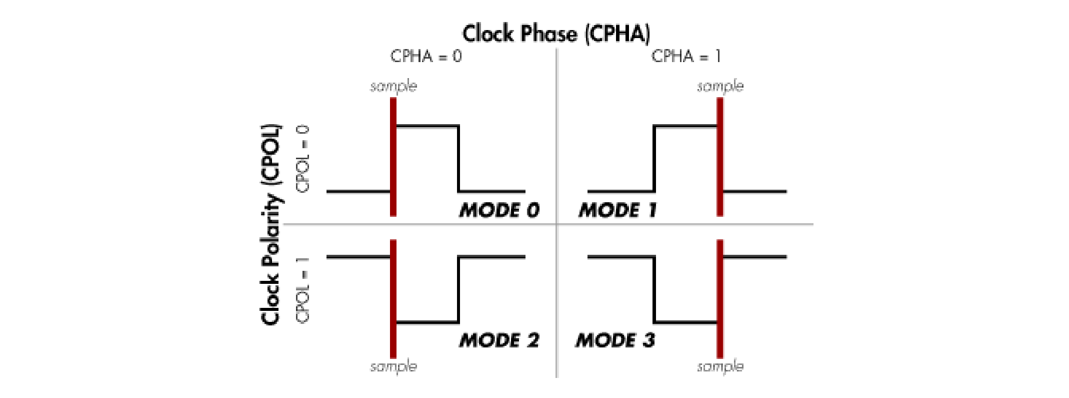
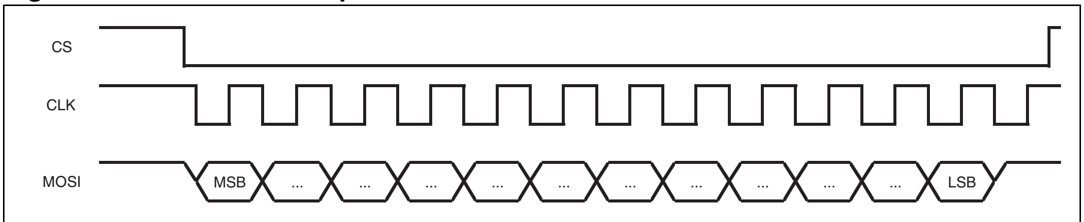
Figure 5. SPI modes



In the case of the TDA7705, the data are latched on the clock's rising edge, with CPOL = 1 and CPHA = 1 (mode 3 in the figure above). According to the specification of this mode, the polarity of the CLK line when no communication is taking place is high.

A "write" communication example is shown in the figure below, for an unspecified number of bits (see the relevant technical documentation for frame structure description):

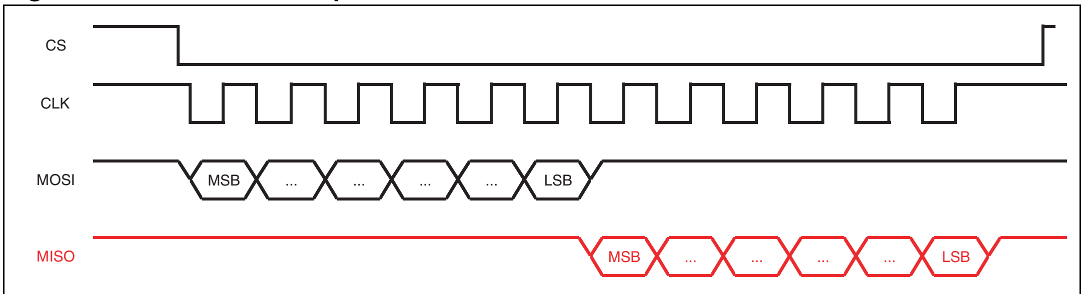
Figure 6. SPI "write" sequence



The start condition is signaled by the CS line going low, and the stop condition by the CS line going high. It is not allowed to toggle the CS line while the communication is going on.

A "read" communication example is shown in the figure below, for an unspecified number of bits (see the relevant technical documentation for frame structure description):

Figure 7. SPI "read" sequence



The red line is controlled by the TDA7705, whereas the black lines are controlled by the µP.

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3 Electrical specifications

3.1 Absolute maximum ratings

Table 4. Absolute maximum ratings

Symbol	Parameter	Test condition	Min	Typ	Max	Units
V_{CC}	Supply voltage	-	-	-	5.5	V
T_{stg}	Storage temperature	-	-55	-	150	°C
V_{ESD}	ESD withstand voltage	Human body model	≥ ±2000			V
		Charged device model	≥ ±450			
		Charged device model, corner pins	≥ ±750			
		Machine model	≥ ±150			

3.2 Thermal data

Table 5. Thermal data

Symbol	Parameter	Test condition	Value	Units
$R_{Th\ j\text{-}amb}$	Thermal resistance junction-to-ambient	LQFP64 10x10, double-layer JEDEC PCB	55	°C/W

3.3 General key parameters

Table 6. General key parameters

Symbol	Parameter	Test condition	Min	Typ	Max	Units
V_{CC}	5 V supply voltage	-	4.7	5	5.25	V
I_{CC}	Supply current @ 5 V	-	-	220	295	mA
T_{amb}	Ambient temperature range	-	-40	-	85	°C
$V_{VCCREG12}$	VCCREG12 supply voltage	see note(1)	2	-	-	V
V_{1V2}	Digital core 1.2V supply voltage	when supplied externally see note (2)	1.08	1.2	1.32	V
I_{1V2}	Digital core 1.2 V supply current	V_{1V2} = 1.08 V see note (2)	-	-	120	mA
		V_{1V2} = 1.2 V see note (2)	-	80	135	mA
		V_{1V2} = 1.32 V see note (2)	-	-	150	mA

1. In the typical application supplied from 5V with a series resistor.
2. When the 1.2 V supply is applied externally, and not using the internal 1.2 V regulator.

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3.4 Electrical characteristics

V_{CC} = 4.7 V to 5.25 V; T_{amb} = -40 °C to +85 °C; unless otherwise specified.

3.4.1 FM - section

Table 7. FM - section

Symbol	Parameter	Test condition	Min	Typ	Max	Units
FM IMR mixer						
R_{in}	Input resistance	-	90	130	170	kΩ
V_{noise}	Input noise voltage	Mix 1, R_{source} = 1.5 kΩ, noiseless	-	2.5	3.1	nV/√Hz
		Mix 2, R_{source} = 800 Ω, noiseless	-	2	2.5	
IIP3	3^{rd} order intercept point	Mix 1 up to $V_{in/tone}$ = 90 dBµV	122	125	-	dBµV
		Mix 2 up to $V_{in/tone}$ = 85 dBµV	118	121		dBµV
FM AGC						
RFAGC-Thr	RFAGC threshold, referred to mixer input; RF level	Mix 1, min setting	-	87	-	dBµV
		Mix 1, max setting	-	93	-	
		Mix 2, min setting	-	85	-	
		Mix 2, max setting	-	91	-	
	Threshold steps	-	-	2	-	dB
	Threshold error	@ T_{amb} = 27 °C	-1.5		1.5	dB
	Threshold temperature drift		-	0.016	-	dB/K
IFAGC-Thr	IFAGC threshold, referred to mixer input; at tuned frequency RF level	Mix 1, min setting	-	81	-	dBµV
		Mix 1, max setting	-	85	-	
		Mix 2, min setting	-	77	-	
		Mix 2, max setting	-	81	-	
	Threshold steps	-	-	2	-	dB
	Threshold error	@ T_{amb} = 27 °C	-1.5		1.5	dB
	Threshold temperature drift	-		0.016	-	dB/K
-	Pin diode source current	@ T_{amb} = 27 °C; see note[1]	12	-	-	mA
-	Pin diode sink current	-	3	-	20	µA
-	Pin diode source current in constant current mode	@ T_{amb} = 27 °C; see note[1]	0.4	-	-	mA

1. The current is generated by a PTAT (Proportional To Absolute Temperature) source, and has therefore a temperature dependency described by: $\Delta I/Io = \Delta T/To$, with Io being the current at ambient temperature (25 °C) and To the ambient temperature (25°C) expressed in Kelvin, that is 298 K.

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3.4.2 AM - section

Table 8. AM - section

Symbol	Parameter	Test condition	Min	Typ	Max	Units
AM IMR Mixer						
R_{in}	Input resistance	-	20	30	45	kΩ
V_{out_max}	Max. output voltage	without clipping	-	126	-	dBµV
$V_{N,in}$	Input noise voltage	Mix 1, R_{source} = 1 kΩ, noiseless	-	8.5	12	nV/√Hz
		Mix 2, R_{source} = 1 kΩ, noiseless	-	8.5	12	
IIP3	3rd order intercept point	Mix 1,2 up to $V_{in/tone}$ = 90 dBµV	126	129	-	dBµV
IIP2	2nd order intercept point	Mix1 1,2 up to $V_{in/tone}$ = 90 dBµV	-	158	-	dBµV
LO hsupp	LO harmonic suppression	N=2,3,4,5,6	-	100	-	dB
		N=7,9	-	85	-	
AM LNA						
Gain	Voltage gain	Max Gain, R_{ext} = 1 kΩ	21	25	28	dB
		Min Gain (AGC controlled)	-	12	-	
R_{in}	Input resistance	-	-	1000		kΩ
C_{in}	Input capacitance	-	-	20		pF
$V_{N,in}$	Input noise voltage	-	-	1.0	1.4	nV/√Hz
IIP3	3rd order intercept point	@ maximum LNA gain	-	125	-	dBµV
IIP2	2nd order intercept point	@ maximum LNA gain	-	143	-	dBµV
AM PIN diode						
IIP2	2nd order intercept point	Full attenuation, C_{source} = 80 pF, f=1 MHz	-	140	-	dBµV
R_{min}	Minimum resistance	-	-	50	80	Ω
C_{in}	Input capacitance	High ohmic	-	12	-	pF
AM AGC						
AGC-Thr	Referred to mixer input RF level	Mix 1,2 min setting	-	87	-	dBµV
		Mix 1,2 max setting	-	93	-	
Thr-steps	Threshold steps	-	-	1	-	dB
	Threshold error	@ T_{amb} = 27 °C	-2.5	-	2.5	
	Threshold temperature drift	-	-3	-	3	
-	Pin diode source current	@ T_{amb} = 27 °C; see note(1)	2	-	10	mA
-	Pin diode sink current	-	15	35	50	µA
-	Pin diode source current in constant current mode	@ T_{amb} = 27 °C; see note(1)	1.5	2.5	3.5	mA

1. The current is generated by a PTAT (Proportional To Absolute Temperature) source, and has therefore a temperature dependency described by: ΔI/Io = ΔT/To, with Io being the current at ambient temperature (25 °C) and To the ambient temperature (25 °C) expressed in Kelvin, that is 298 K.

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3.4.3 VCO

Table 9. VCO

Symbol	Parameter	Test condition	Min	Typ	Max	Units
F_{VCO}	Frequency range VCO	-	1100		1550	MHz
PN	Phase noise of LO	Locked VCO; values referred @ 100MHz @ 100 Hz @ 1 kHz @ 10 kHz	-	-100 -115 -115	-	dBc/Hz
dev	Deviation error (rms)	FM reception, deemphasis 50µs, f_{audio} = 20 Hz...20 kHz	-	5	-	Hz

3.4.4 Phase locked loop

Table 10. Phase locked loop

Symbol	Parameter	Test condition	Min	Typ	Max	Units
T_{settle}	Settling time FM	$\Delta f < 10$ kHz	-	300	-	µs
FM step	FM frequency step	-	-	5	-	kHz
AM step	AM frequency step	-	-	500	-	Hz

3.4.5 Tuning DAC

Table 11. Tuning DAC

Symbol	Parameter	Test condition	Min	Typ	Max	Units
Res	Resolution	8 bit	-	18	-	mV
V_{outmin}	Min output voltage	-	-	0.6	0.7	V
V_{outmax}	Max ouput voltage	-	VCC-0.2	VCC-0.1	-	V
R_{out}	Output impdedance	-	1.5	2.5	3.5	kΩ
DNL	Diff. Non linearity	-	-	-	0.5	LSB
T_{conv}	Conversion time	-	-	20	-	µs

3.4.6 IF ADC

Table 12. IF ADC

Symbol	Parameter	Test condition	Min	Typ	Max	Units
DR_{FM}	Dynamic range in FM	BW = ±200 kHz	-	90	-	dB
$V_{N,in\ FM}$	Input noise referred to mixer input	mixer 1 mixer 2	-	1.1 0.7	1.9 1.2	nV/√Hz
DR_{AM}	Dynamic range in AM	BW = ±4 kHz	-	103	-	dB
$V_{N,in\ AM}$	Input noise referred to mixer input	-	-	6.9	12	nV/√Hz

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3.4.7 Audio DAC

Table 13. Audio DAC

Symbol	Parameter	Test condition	Min	Typ	Max	Units
V_{out}	Max. output voltage	Full scale	-	1	-	Vrms
BW	Bandwidth	1dB attenuation	-	15	-	KHz
R_{out}	Output resistance	-	600	750	900	Ω
$V_{N, out}$	Output noise	-	-	60	95	µVrms
THD	Distortion	-6 dBFS	-	0.03	0.04	%

3.4.8 IO interface pins

Table 14. IO interface pins

Symbol	Parameter	Test condition	Min	Typ	Max	Units
-	High level output voltage (all IOs except GPO pin 2)	I_{out} = 500 µA	2.9	3.2	-	V
-	GPIOs source current (all IOs in source mode except pin 2)	Total sourced current by all GPIOs	-	-	1.25	mA
-	Low level output voltage (all IOs except GPO pin 2)	I_{out} = -1 mA	-	0.1	0.3	V
-	Input voltage range	-	0	-	3.5	V
-	High level input voltage	-	2.0	-	-	V
-	Low level input voltage	-	-	-	0.8	V
T_{reset}	Reset time	Minimum time during which pin RSTN must be low so as to reset the device	10	-	-	µs
T_{latch}	Boot mode configuration latch time	Minimum time during which the voltage applied at pins 25 and 39 must be kept in order to latch the correct boot mode (serial bus configuration)	10	-	-	µs
-	GPO PLLTEST (pin 2) max source current	-	-	-	1	mA
-	GPO PLLTEST (pin 2) max sink current	-	-1	-		mA
-	GPO PLLTEST (pin 2) minimum high level output voltage	I_{out} = 1 mA	2.8	3.1	-	V
	GPO PLLTEST (pin 2) maximum high level output voltage	I_{out} = 1 mA	-	0.1	0.3	V

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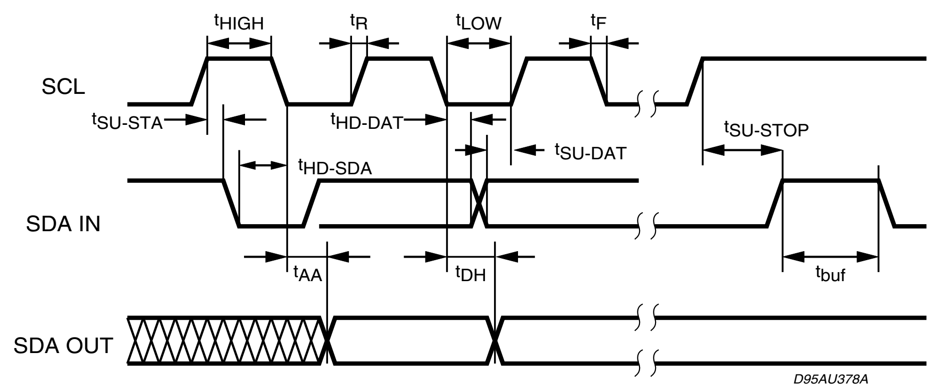
3.4.9 I²C interface

The following parameters apply to the serial bus communication when I²C protocol has been selected at start-up. For the other electrical characteristics of the pins, *Section 3.4.8* applies. The parameters of the following table are defined as in *Figure 8*.

Table 15. I²C interface

Symbol	Parameter	Min	Max	Units
f_{SCL}	SCL Clock frequency	-	500	kHz
t_{AA}	SCL low to SDA data valid	0.3	-	µs
t_{buf}	time the bus must be kept free before a new transmisison	1.3	-	µs
t_{HD-STA}	START condition hold time	0.6	-	µs
t_{LOW}	Clock low period	1.3	-	µs
t_{HIGH}	Clock high period	0.6	-	µs
t_{SU-SDA}	START condition setup time	0.1	-	µs
t_{HD-DAT}	Data input hold time	0	0.9	µs
t_{SU-DAT}	Data input setup time	0.1	-	µs
t_R	SDA & SCL rise time	-	0.3	µs
t_F	SDA & SCL fall time	-	0.3	µs
$t_{SU-STOP}$	Stop condition setup time	0.6	-	µs
t_{DH}	Data out time	-	0.3	µs

Figure 8. I²C bus timing diagram



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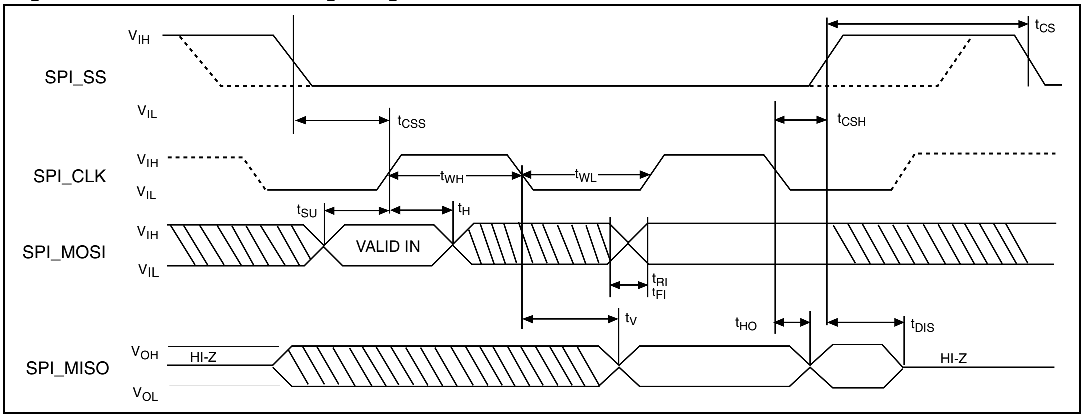
3.4.10 SPI interface

The following parameters apply to the serial bus communication when SPI protocol has been selected at start-up. For the other electrical characteristics of the pins, *Section 3.4.8* applies.

Table 16. SPI interface

Symbol	Parameter	Min	Max	Unit
f_{SCK}	Clock frequency	-	4.0	MHz
t_{SU}	Data setup time	25	-	ns
t_H	Data hold time	25	-	ns
t_{WH}	SCK high time	50	-	ns
t_{WL}	SCK low time	50	-	ns
t_{RI}	Input rise time	-	2	µs
t_{FI}	Input fall time	-	2	µs
t_V	Output valid from clock low	-	50	ns
t_{HO}	Output hold time	25	-	ns
t_{DIS}	Output disable time		25	ns
t_{CS}	CS high time	25	-	ns
t_{CSS}	CS setup time	25	-	ns
t_{CSH}	CS hold time	25	-	ns

Figure 9. SPI bus timing diagram



3.4.11 Warning

When the TDA7705 is not powered on, the internal ESD protection diodes pull-down keep the I^2C/SPI lines connected to ground. This implies that the I^2C/SPI bus connected to the TDA7705 may not be used to drive other devices when the TDA7705 is powered off.

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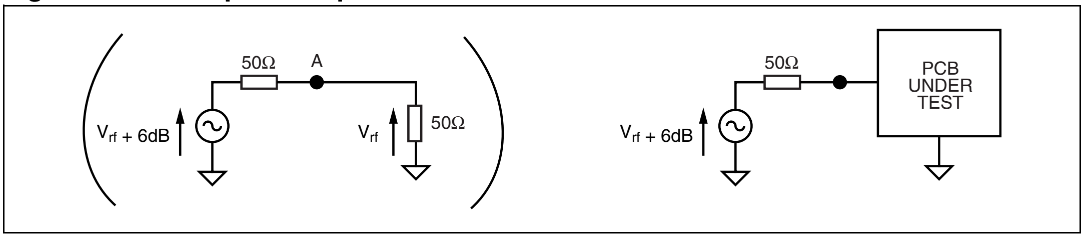
3.5 Overall system performance

All measurements obtained with application of *Figure 16* (FM tuned application / SPI control) unless otherwise specified.

3.5.1 FM overall system performance

Antenna level equivalence: 0 dBμV = 1 μV_{rms} (Antenna terminal voltage with 50 Ω source).

Figure 10. FM input set-up



Input level referred to signal generator loaded with 50 Ω (V_{rf}, node 'A'); no antenna dummy; AM input not connected. F_{rf} = 98.1 MHz, V_{rf} = 60 dBμV, mono modulation, f_{dev} = 40 kHz, f_{audio} = 1 kHz. De-emphasis = 50 μs. Unless otherwise specified

Table 17. FM overall system performance

Parameter	Test condition	Min	Typ	Max	Units
Tuning range FM Eu	(can be modified by the user) (automatic FE alignment available)	87.5	-	108	MHz
Tuning step FM Eu	(can be modified by the user)	-	100	-	kHz
Tuning range FM US	(can be modified by the user) (automatic FE alignment available)	87.5	-	107.9	MHz
Tuning step FM US	(can be modified by the user)	-	200	-	kHz
Tuning range FM Jp	(can be modified by the user) (automatic FE alignment available)	76	-	90	MHz
Tuning step FM Jp	(can be modified by the user)	-	100	-	kHz
Tuning range FM EEu	(can be modified by the user) (automatic FE alignment not available)	65	-	74	MHz
Tuning step FM EEu	(can be modified by the user)	-	100	-	kHz
Sensitivity	S/N =26dB	-	-7	-4	dBμV
S/N	@ 10 dBμV, no highcut, DISS BW = #3	-	55	-	dB
Ultimate S/N	@ 60 dBμV, mono	72	75	-	dB
	@ 60 dBμV, Deviation = 75 kHz, mono	78	81	-	dB
	@ 60 dBμV, stereo	70	73	-	dB

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Table 17. FM overall system performance (continued)

Parameter	Test condition	Min	Typ	Max	Units
Distortion	Deviation= 75 kHz	-	0.05	-	%
Max deviation	THD=3%	-	140	-	kHz
Adjacent channel selectivity	ΔF=100kHz, SINAD=30dB desired 40 dBµV, dev=40kHz, 400Hz undesired. dev=40kHz, 1KHz	-	25	-	dB
Alternate channel selectivity	ΔF=200 kHz, SINAD=30 dB desired 40 dB µV, dev=40kHz, 400 Hz undesired. dev=40kHz, 1kHz	-	63	-	dB
Max. strong signal interferer	Desired = 10 dBµV SINAD = 30 dB Undesired ΔF = 5 MHz dev = 40 kHz, 1 kHz	-	94	-	dBµV
Max. strong signal interferer no preselection (“wide-band”) application	Desired = 10 dBµV SINAD = 30 dB Undesired ΔF = 5 MHz dev = 40 kHz, 1 kHz	-	88	-	dBµV
3 signal performance(1)	Desired = 40 dBµV, dev = 40 kHz, 400 Hz, SINAD = 30 dB Undesired1 = ±400 kHz, dev = 40 kHz, 1 kHz Undesired2 = ±800 kHz, no mod	-	103	-	dBµV
	Desired = 40 dBµV, dev = 40 kHz, 400 Hz, SINAD = 30 dB Undesired1 = ±1 MHz, dev=40kHz, 1 kHz Undesired2=±2MHz, no mod	-	106	-	dBµV
3 signal performance(1) no preselection (“wide-band”) application	Desired = 40 dBµV, dev = 40 kHz, 400 Hz, SINAD = 30 dB Undesired1 = ±400 kHz, dev = 40 kHz, 1 kHz Undesired2 = ±800 kHz, no mod	-	103	-	dBµV
	Desired = 40 dBµV, dev=40kHz, 400 Hz, SINAD=30 dB Undesired1 =±1 MHz, dev=40kHz, 1 kHz Undesired2=±2MHz, no mod	-	104	-	dBµV
AM suppression	m =30 %	-	70	-	dB

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Table 17. FM overall system performance (continued)

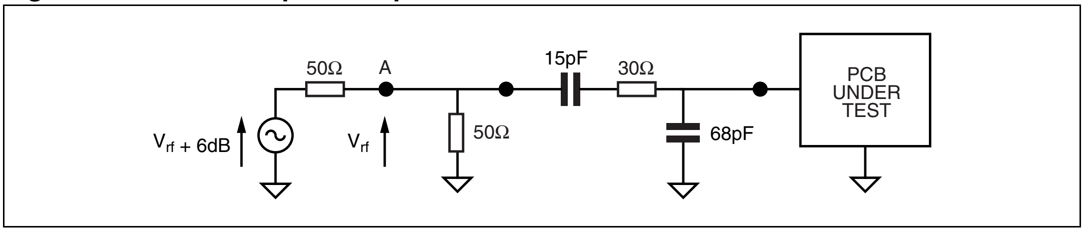
Parameter	Test condition	Min	Typ	Max	Units
Image rejection	-	-	80	-	dB
Logarithmic field strength indicator	@40 dBµV read "FM_Smeter_log"	-0.33 (equiv. to 37 dBµV)	-0.3	-0.27 (equiv. to 43 dBµV)	--

1. Signal levels referred to combiner output.

3.5.2 AM MW overall system performance

Antenna level equivalence: 0 dBµV = 1 µV_{rms}.

Figure 11. AM MW input set up



Level referred to SG output before antenna dummy (V_{rf}, node 'A'); capacitive dummy 15pF+68pF, FM input not connected. F_{rf} = 999 kHz (1000 kHz for US), V_{rf} =74 dBµV, mod = 30%, f_{audio} =400 Hz, unless otherwise specified.

Table 18. AM MW overall system performance

Parameter	Test condition	Min	Typ	Max	Units
Tuning range MW Eu/Jp	(can be modified by the user)	531	-	1629	kHz
Tuning step MW Eu/Jp	(can be modified by the user)	-	9	-	kHz
Tuning range MW US	(can be modified by the user)	530	-	1710	kHz
Tuning step MW US	(can be modified by the user)	-	10	-	kHz
Sensitivity	S/N = 20 dB	-	27	30	dBµV
Ultimate S/N	@ 80 dBµV	63	66	-	dB
AGC F.O.M.	Ref.=74 dBµV -10dB drop point	50	62	65	dB
Distortion	m = 80 %	-	0.1	-	%
Adjacent channel selectivity	ΔF=9 kHz, SINAD = 26 dB undesired. m=30%, 1 kHz	-	42	-	dB
Alternate channel selectivity	ΔF=18 kHz, SINAD=26 dB undesired. m=30%, 1kHz	-	50	-	dB

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Table 18. AM MW overall system performance (continued)

Parameter	Test condition	Min	Typ	Max	Units
Strong signal interferer SNR	ΔF= ±40 kHz desired = 40 dBµV undesired = 100 dBµV, m= 30%, 1 kHz	-	15	-	dB
	ΔF=±400kHz desired=40 dBµV undesired=100 dBµV, m=30%, 1kHz	17	-	-	dB
Strong signal interferer suppression	ΔF=±40 kHz desired=40 dBµV undesired=110 dBµV, m=30%, 1 kHz	-	4	-	dB
	ΔF=±400kHz desired=40 dBµV undesired=110 dBµV, m=30%, 1kHz	-	4	-	dB
Strong signal interferer cross-modulation	ΔF=±40kHz desired=80 dBµV undesired=100 dBµV, m=30%, 1kHz	-	-	10	dB
	ΔF=±400kHz desired=80 dBµV undesired=100 dBµV, m=30%, 1kHz	-	-	10	dB
Image rejection	-	-	80	-	dB
Logarithmic field strength indicator	@60 dBµV read “AM_Smeter_log”	0.50 (equiv. to 57 dBµV)	0.47	0.43 (equiv. to 63 dBµV)	-

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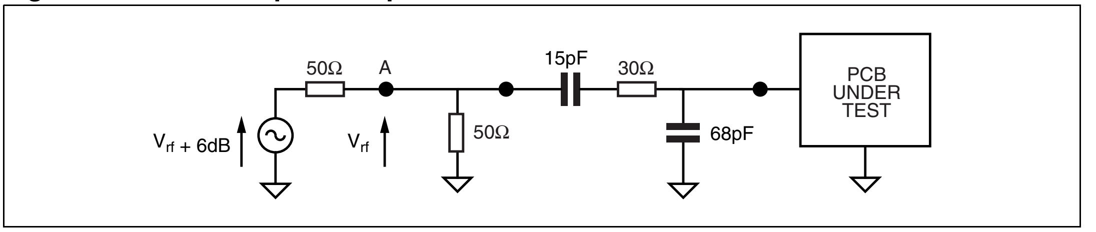
3.5.3 AM LW overall system performance

Antenna level equivalence: 0 dBμV = 1 μV_{rms}

Figure 12. AM LW input set-up



Level referred to SG output before antenna dummy (V_{rf}, node 'A'); capacitive dummy 15pF+68pF; FM input not connected. F_{rf} = 216 kHz, V_{rf} =74 dBμV, mod = 30 %, f_{audio} = 400 Hz, unless otherwise specified.

Table 19. AM LW overall system performance

Parameter	Test condition	Min	Typ	Max	Units
Tuning range LW	(can be modified by the user)	144	-	288	kHz
Tuning step LW	(can be modified by the user)	-	1	-	kHz
Sensitivity	S/N =20 dB	-	30	33	dBμV
Ultimate S/N	@ 80 dBμV	63	66	-	dB
AGC F.O.M.	Ref.=74 dBμV -10dB drop point	50	62	65	dB
Distortion	m = 80 %	-	0.1	-	%
Image rejection	-	-	80	-	dB

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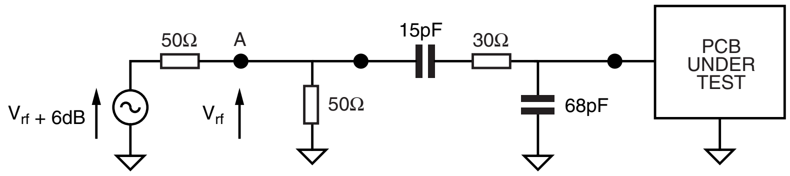
3.5.4 AM SW overall system performance

Antenna level equivalence: 0dBμV = 1μV_{rms}

Figure 13. AM SW input set-up



Level referred to SG output before antenna dummy (V_{rf}, node 'A'); capacitive dummy 15pF+68pF; FM input not connected. F_{rf} = 6000 kHz, V_{rf} =74 dBμV, mod = 30 %, f_{audio} = 400 Hz, unless otherwise specified.

Table 20. AM SW overall system performance

Parameter	Test condition	Min	Typ	Max	Units
Tuning range LW	(can be modified by the user)	2300	-	30000	kHz
Tuning step LW	(can be modified by the user)	-	1	-	kHz
Sensitivity	S/N =20dB	-	29	32	dBμV
Ultimate S/N	@ 80 dBμV	63	66	-	dB
AGC F.O.M.	Ref.=74 dBμV -10dB drop point	50	62	65	dB
Distortion	m = 80 %	-	0.3	-	%
Image rejection	-	-	80	-	dB

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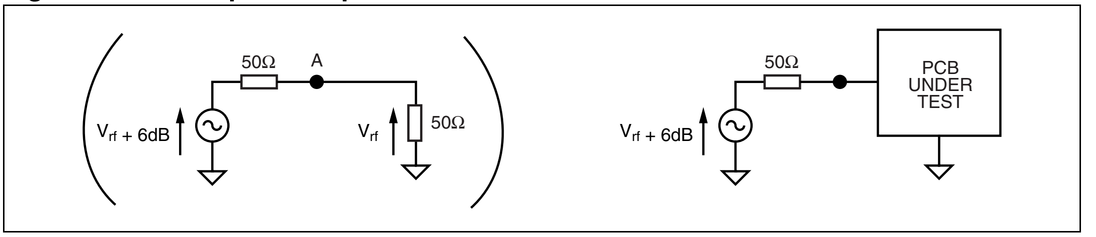
3.5.5 WX overall system performance

Antenna level equivalence: 0 dBµV = 1 μV_{rms} (Antenna terminal voltage with 50Ω source).

Figure 14. WX input set-up



Input level referred to signal generator loaded with 50 Ω (V_{rf}, node 'A'); no antenna dummy; AM input not connected. F_{rf} =162.475 MHz, V_{rf} = 60 dBµV, mono modulation, f_{dev} = 3 kHz, f_{audio} =400 Hz. De-emphasis = 75 µs. Application: WX using mixer input 2, in conjunction with FM narrow-band. Unless otherwise specified.

Table 21. WX overall system performance

Parameter	Test condition	Min	Typ	Max	Units
Sensitivity	S/N = 26 dB	-	-7	-	dBµV
Ultimate S/N	@ 60 dBµV	-	81	-	dB
Distortion	Deviation= 4.5 kHz	-	0.8	-	%
Max deviation	THD = 3 %	-	> 5 kHz	-	kHz
Adjacent channel Selectivity	∆F= 25 kHz, SINAD = 30 dB desired 40 dBµV, dev =2.0 kHz, 400 Hz undesired. dev= 3 kHz, 1 kHz	-	70	-	dB
Alternate Channel Selectivity	∆F=50kHz, SINAD=30dB desired 40 dBµV, dev=2.0kHz, 400Hz undesired. dev=2.0kHz, 1kHz	-	70	-	dB

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4 Front-end processing

All the parameters in this section refer to the programmability of the FE part of the device (registers). The part of the registers that are not described here have either fixed values or values written by the tuner drivers, and are described in the proper technical documentation.

Table 22. Register 0x00

Register number																								Register definition
MSB																							LSB	
23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	
																								AM mixer input selector
																						0	1	input #1
																						1	0	input #2
																								AM PIN diode
											0													internal
											1													external
																								AM AGC mode
										0														LNA and PIN diode
										1														PIN diode only
																								AM AGC time constant
								0	0															slow (125 ms with 1 µF)
								0	1															medium (25 ms with 1 µF)
								1	1															fast (5 ms with 1 µF)
																								AM AGC threshold @ mixin
					0	0	0																	90 dBµV
					0	0	1																	91 dBµV
					0	1	0																	92 dBµV
					0	1	1																	93 dBµV
					1	0	0																	90 dBµV
					1	0	1																	89 dBµV
					1	1	0																	88 dBµV
					1	1	1																	87 dBµV
																								AM AGC attack time constant
			0																					normal
			1																					fast

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Table 23. Register 0x01

Register number																								Register definition
MSB																							LSB	
23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	
																								FM mixer input selector
									0	1								1	0					input #1
									1	0								0	1					input #2
																								FM mixer gain
								0																high
								1																low
																								FM AGC time constant
		0																						normal
		1																						fast
																								FM AGC output mode
0	0																							normal
0	1																							constant 15 mA
1	0																							constant 1 mA

Table 24. Register 0x02

Register number																								Register definition
MSB																							LSB	
23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	
																								FM RF AGC threshold @ mixin
																						0	0	87 dBµV
																						0	1	89 dBµV
																						1	0	91 dBµV
																						1	1	93 dBµV
																								FM iF AGC threshold @ IFADC in
																				0	0			120 dBµV
																				0	1			122 dBµV
																				1	0			124 dBµV
																								Tuning DAC enable
																	0							off
																	1							on
																								Tuning DAC programming(1)
									0	0	0	0	0	0	0	0								0
									0	0	0	0	0	0	0	1								1
									…	…	…	…	…	…	…	…								…
									1	1	1	1	1	1	1	0								510
									1	1	1	1	1	1	1	1								511

1. Normally handled by tuner drivers.

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Table 25. Register 0x05

Register number																								Register definition
MSB																							LSB	
23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	
																								PLLTEST output status
																							0	low
																							1	high

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5 Weak signal processing

All the parameters in this section refer to the programmability of the DSP part of the device. The typical values are those set by default parameters (start-up without parametric change from main µP); the max and the min values refer to the programmability range. The values are referred to the typical application (*Figure 16: Example of FM tuned (narrow-band) application / SPI control*). Wherever the possible values are a discrete set, all the possible programmable values are displayed.

5.1 FM IF-processing

5.1.1 Dynamic channel selection filter (DISS)

Table 26. Dynamic channel selection filter (DISS)
(discrete set)

Symbol	Parameter	Test condition	Min	Typ	Max	Units
DISS BW	IF filter #6	response: - 3dB	-	±150	-	kHz
	IF filter #5		-	±110	-	kHz
	IF filter #4		-	±80	-	kHz
	IF filter #3		-	±60	-	kHz
	IF filter #2		-	±45	-	kHz
	IF filter #1		-	±35	-	kHz
	IF filter #0		-	±25	-	kHz

5.1.2 Soft mute

Table 27. Soft mute
(continuous set)

Symbol	Parameter	Test condition	Min	Typ	Max	Units
SMsp	Start point vs. field strength	audio atten = 1 dB read “FM_softmute” no adjacent channel present	0	6	20	dBµV
SMep	End point vs. field strength	audio atten = SMd + 1 dB read “FM_softmute” no adjacent channel present	-6	-6	10	dBµV
SMd	Depth	-	-30	-15	0	dB
SMtauatt	Field strength LPF cut-off frequency for soft mute activation	-	0.1	100	4000	Hz
SMtaurel	Field strength LPF cut-off frequency for soft mute release	-	0.1	1	4000	Hz

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5.1.3 Adjacent channel mute

Table 28. Adjacent channel mute
(continuous set)

Symbol	Parameter	Test condition	Min	Typ	Max	Units
ACMd	Depth		SMd	0	0	dB

5.1.4 Stereo blend-

Table 29. Stereo blend
(continuous set)

Symbol	Parameter	Test condition	Min	Typ	Max	Units
MaxSep	Maximum stereo separation	field strength = 80 dBµV, pilot deviation = 6.75 kHz	0	40	50	dB
SBFSsp	Start point vs. field strength	separation = MaxSep - 1 dB no multipath present	20	50	60	dBµV
SBFSep	End point vs. field strength	separation = 1 dB no multipath present	20	30	60	dBµV
SBFStM2S	Field strength-related transition time from mono to stereo	V_{rf} step-like variation from 20 dBµV to 80 dBµV	0.001	3	20	s
SBFStS2M	Field strength-related transition time from stereo to mono	V_{rf} step-like variation from 80 dBµV to 20 dBµV	0.001	0.5	20	s
SBMPsp	Start point vs. multipath	separation = MaxSep - 1 dB equivalent 19 kHz AM modulation depth; field strength = 80 dBµV	5	10	80	%
SBMPep	End point vs. multipath	separation = 1 dB equivalent 19 kHz AM modulation depth; field strength = 80 dBµV	5	30	80	%
SBMPtM2S	Multipath -related transition time from mono to stereo	V_{rf} step-like variation from 20 dBµV to 80 dBµV	0.001	1	20	s
SBMPtS2M	Multipath -related transition time from stereo to mono	V_{rf} step-like variation from 80 dBµV to 20 dBµV	0.001	0.001	20	s
Pil ThrM2S	Pilot detector stereo threshold	Threshold on pilot tone deviation for mono-stereo transition	0.8	2.74	7	kHz
Pil ThrHyst	Pilot detector threshold hysteresis	Difference in pil. det. deviation threshold for stereo to mono transition compared to PilThrM2S	-	0.01	-	kHz

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5.1.5 High cut control

Table 30. High cut control
(continuous set)

Symbol	Parameter	Test condition	Min	Typ	Max	Units
HCFSsp	Start point vs. field strength	minimum RF level for widest HC filter (filter # 7) no multipath present	0	50	50	dBµV
HCFSep	End point vs. field strength	maximum RF level for narrowest HC filter (filter # 0) no multipath present	0	30	40	dBµV
HCFStW2N	Field strength-related transition time from wide to narrow band	V_{rf} step-like variation from 60 dBµV to 10 dBµV		(1)		-
HCFStN2W	Field strength-related transition time from narrow to wide band	V_{rf} step-like variation from 0 dBµV to 60 dBµV	(1)	14	100	s
HCMPsp	Start point vs. multipath	minimum RF level for widest HC filter (filter # 7) equivalent 19 kHz AM modulation depth; field strength = 80 dBµV	5	10	150 (2)	%
HCMPep	End point vs. multipath	maximum RF level for narrowest HC filter (filter # 0) equivalent 19 kHz AM modulation depth; field strength = 80 dBµV	5	30	150 (2)	%
HCMPtN2W	Multipath -related transition time from narrow to wide band	V_{rf} step-like variation from 20 dBµV to 80 dBµV	0.001	0.001	20	s
HCMPtW2N	Multipath -related transition time from wide to narrow	V_{rf} step-like variation from 80 dBµV to 20 dBµV	0.001	0.001	20	s
HCmaxBW	Maximum cut-off frequency of high cut filter bank	Filter #7, -3 dB response frequency, input signal with pre-emphasis	HCmin BW	14	18	kHz
HCminBW	Minimum cut-off frequency of high cut filter bank	Filter #0, -3 dB response frequency, input signal with pre-emphasis	0.1	3	HCma xBW	kHz
HCnumFilt	Number of discrete HC filters	-	-	8 (3)	-	-

1. Depends only on field strength filter time constant.
2. Means that 100% equivalent 19 kHz AM modulation depth will not achieve full band narrowing.
3. Intermediate filters (#6 - #1) cut-off frequencies exponentially spaced between HCmaxBW and HCminBW.

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Table 31. De-emphasis filter
(continuous set)

Symbol	Parameter	Test condition	Min	Typ	Max	Units
DEtc	De-emphasis time constant 1	-	-	50	-	µs
	De-emphasis time constant 2	-	-	75	-	

5.1.6 Stereo decoder

Table 32. Stereo decoder

Symbol	Parameter	Test condition	Min	Typ	Max	Units
PilSup	Pilot signal suppression	Pilot 9%, 19 kHz, ref=40 kHz	-	60	-	dB
SubcSup	Subcarrier suppression	f = 38 kHz	-	70	-	dB
		f = 57 kHz	-	70	-	dB
		f = 76 kHz	-	80	-	dB

5.2 AM IF-processing

5.2.1 Channel selection filter

Table 33. Channel selection filter

Symbol	Parameter	Test condition	Min	Typ	Max	Units
CSF BW	Channel selection filter BW	response: - 3dB	-	±3.7	-	kHz

5.2.2 Soft mute

Table 34. Soft mute
(continuous set)

Symbol	Parameter	Test condition	Min	Typ	Max	Units
SMsp	Start point vs. field strength	audio atten = 1 dB read “FM_softmute” no adjacent channel present	0	25	40	dBµV
SMep	End point vs. field strength	audio atten = SMd + 1 dB read “FM_softmute” no adjacent channel present	0	0	30	dBµV
SMd	Depth	-	-40	-24	0	dB
SMtauatt	Transition time for field strength-dependent soft mute activation	-	0.001	0.1	10	s
SMtaurel	Transition time for field strength-dependent soft mute release	-	0.001	3	10	s

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5.2.3 High cut control

Table 35. High cut control
(continuous set)

Symbol	Parameter	Test condition	Min	Typ	Max	Units
HCFSsp	Start point vs. field strength	minimum RF level for widest HC filter (filter # 7) no multipath present	0	40	50	dBµV
HCFSep	End point vs. field strength	maximum RF level for narrowest HC filter (filter # 0) no multipath present	0	30	50	dBµV
HCFStW2N	Field strength-related transition time from wide to narrow band	V_{rf} step-like variation from 60 dBµV to 10 dBµV	0.001	0.2	20	s
HCFStN2W	Field strength-related transition time from narrow to wide band	V_{rf} step-like variation from 0 dBµV to 60 dBµV	0.001	10	20	s
HCmaxBW	Maximum cut-off frequency of high cut filter bank	Filter #7, -3 dB response frequency, input signal with pre-emphasis	HCmin BW	14	18	kHz
HCminBW	Minimum cut-off frequency of high cut filter bank	Filter #0, -3 dB response frequency, input signal with pre-emphasis	1	3	HCma xBW	kHz
HCnumFilt	Number of discrete HC filters		-	8	-	-

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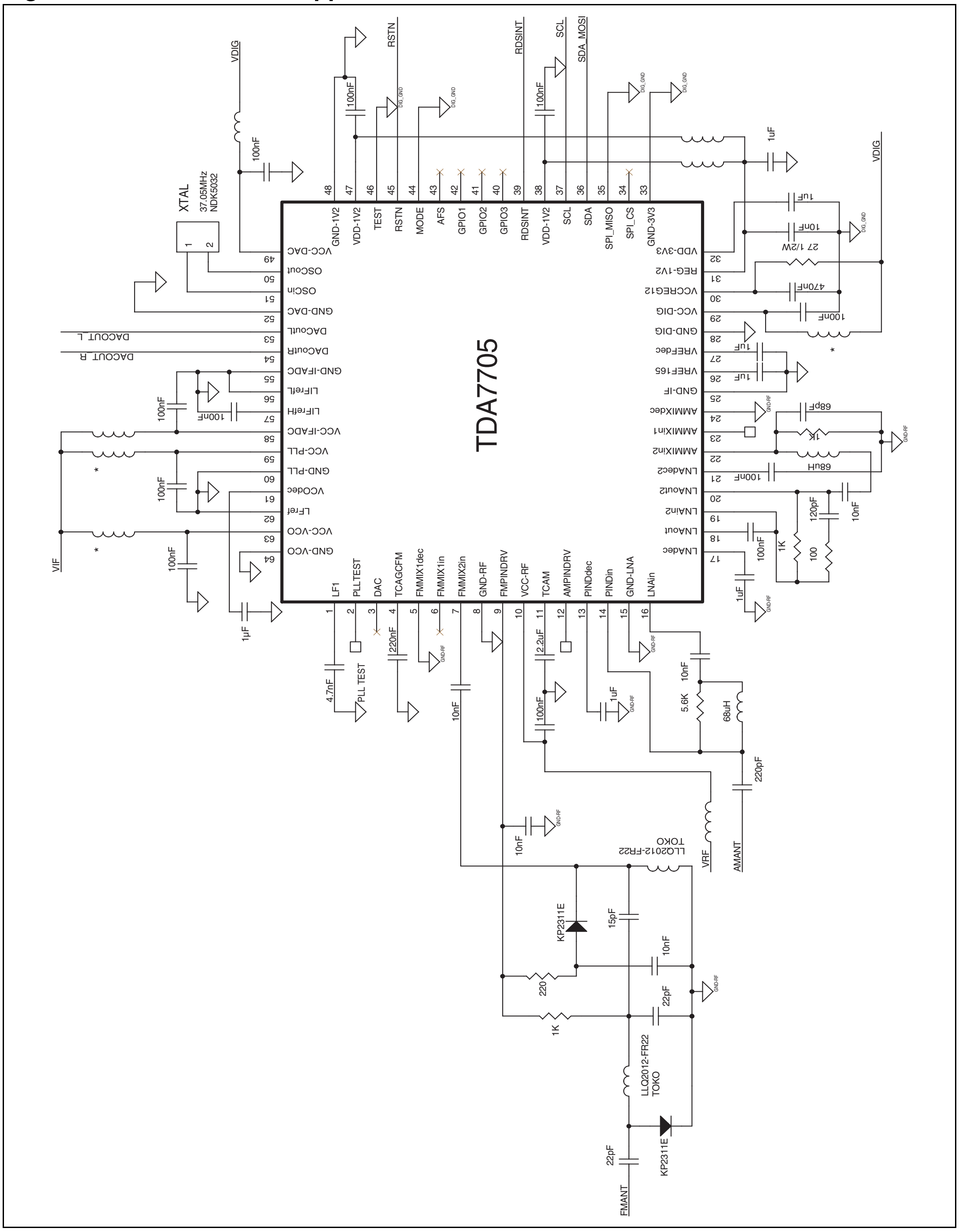
6 Application schematics

6.1 Basic application schematic

Figure 15. FM wide-band application / I^{2}C control



1. Note: components marked with a * are being considered for replacement with resistors, pending optimization test results.

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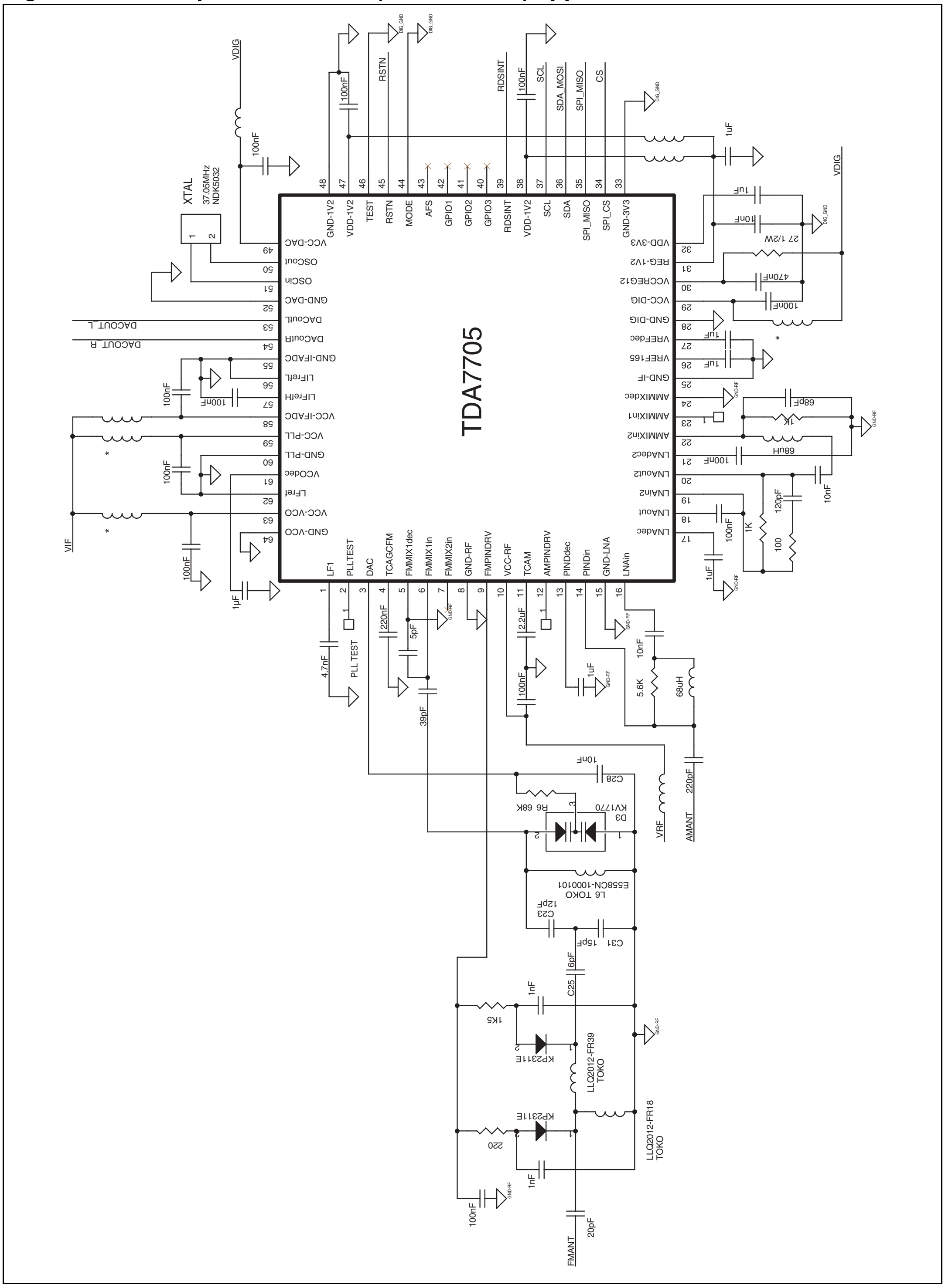
6.2 Application schematic example with SPI-bus and tuned preselection

Figure 16. Example of FM tuned (narrow-band) application / SPI control



1. Note: components marked with a * are being considered for replacement with resistors, pending optimization test results.

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7 Package information

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: *www.st.com*.

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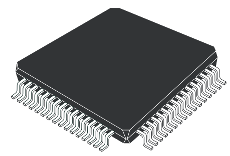
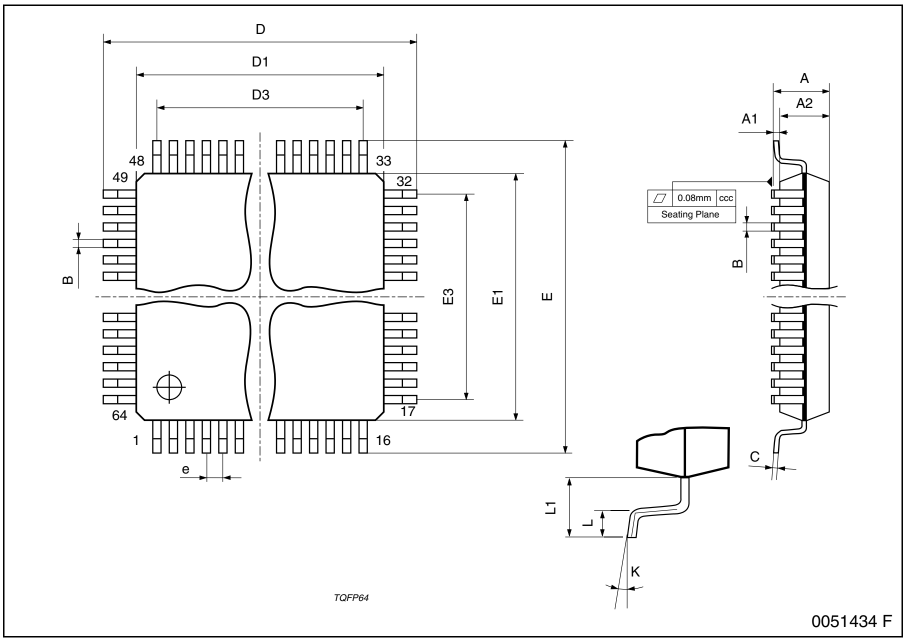
Figure 17. LQFP64 (10x10x1.4mm) mechanical data and package dimensions

DIM.	mm			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A			1.60			0.063
A1	0.05		0.15	0.002		0.006
A2	1.35	1.40	1.45	0.053	0.055	0.057
B	0.17	0.22	0.27	0.0066	0.0086	0.0106
C	0.09		0.20	0.0035		0.0079
D	11.80	12.00	12.20	0.464	0.472	0.480
D1	9.80	10.00	10.20	0.386	0.394	0.401
D3		7.50			0.295	
e		0.50			0.0197	
E	11.80	12.00	12.20	0.464	0.472	0.480
E1	9.80	10.00	10.20	0.386	0.394	0.401
E3		7.50			0.295	
L	0.45	0.60	0.75	0.0177	0.0236	0.0295
L1		1.00			0.0393	
K	0° (min.), 3.5° (min.), 7° (max.)					
ccc			0.080			0.0031

OUTLINE AND MECHANICAL DATA



LQFP64 (10 x 10 x 1.4mm)



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8 Revision history

Table 36. Document revision history

Date	Revision	Changes
31-Jul-2007	1	Initial release.
01-Aug-2008	2	Full update datasheet.
08-May-2009	3	Document status promoted from preliminary data to datasheet. Updated *Table 1: Device summary on page 1*. Updated *Section 3: Electrical specifications on page 16*. Updated *Section 4: Front-end processing on page 30*. Updated *Section 5: Weak signal processing on page 33*. Updated *Section 6: Application schematics on page 38*.
09-Jun-2009	4	Updated *Table 5: Thermal data on page 16*. Updated the value of “Adjacent channel selectivity” parameter in the *Table 17: FM overall system performance*.
01-Jul-2009	5	Updated *Figure 17: LQFP64 (10x10x1.4mm) mechanical data and package dimensions on page 40*.
13-Jan-2010	6	Modified *Table 1: Device summary on page 1* Modified *Table 5: Thermal data on page 16*. Modified *Section 3.5.5: WX overall system performance on page 29*. Modified *Section 7: Package information on page 40*.
29-Jan-2010	7	Minor text changes in *Section 2.13*. Modified min. value of “$t_{HD\text{-}DAT}$” parameter in *Table 15: I^2C interface on page 21*.
22-Mar-2010	8	Added *Section 3.4.11: Warning on page 22*.
17-Sep-2013	9	Updated Disclaimer

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