2 A/3 A, 20 V, 700 kHz, Nonsynchronous Step-Down Regulators

Data Sheet

ADP2302/ADP2303

FEATURES

- Wide input voltage range: 3.0 V to 20 V
- Maximum load current
  - 2 A for ADP2302
  - 3 A for ADP2303
- ±1.5% output accuracy over temperature
- Output voltage down to 0.8 V
- 700 kHz switching frequency
- Current-mode control architecture
- Automatic PFM/PWM mode
- Precision enable pin with hysteresis
- Integrated high-side MOSFET
- Integrated bootstrap diode
- Internal compensation and soft start
- Power-good output
- Undervoltage lockout (UVLO)
- Overcurrent protection (OCP)
- Thermal shutdown (TSD)
- 8-lead SOIC package with exposed paddle
- Supported by ADIsimPower™ design tool

APPLICATIONS

- Intermediate power rail conversion
- DC-to-DC point of load applications
- Communications and networking
- Industrial and instrumentation
- Healthcare and medical
- Consumer

TYPICAL APPLICATIONS CIRCUIT

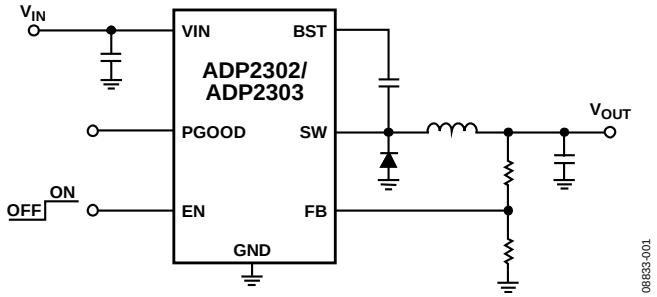

Figure 1. Typical Application Circuit

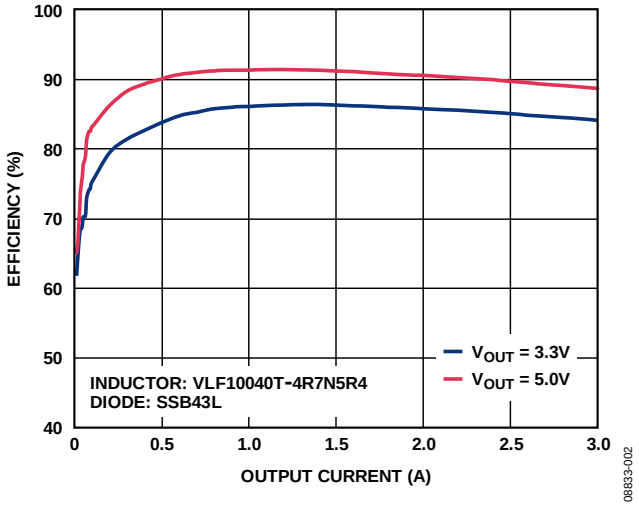

Figure 2. ADP2303 Efficiency vs. Output Current at V_{IN} = 12 V

GENERAL DESCRIPTION

The ADP2302/ADP2303 are fixed frequency, current-mode control, step-down, dc-to-dc regulators with an integrated power MOSFET. The ADP2302/ADP2303 can run from an input voltage of 3.0 V to 20 V, which makes them suitable for a wide range of applications. The output voltage of the ADP2302/ADP2303 can be down to 0.8 V for the adjustable version, while the fixed output version is available in preset output voltage options of 5.0 V, 3.3 V, and 2.5 V. The 700 kHz operating frequency allows small inductor and ceramic capacitors to be used, providing a compact solution. Current mode control provides fast and stable line and load transient performance.

The ADP2302/ADP2303 have integrated soft start circuitry to prevent a large inrush current at power-up. The power-good signal can be used to sequence devices that have an enable input. The precision enable threshold voltage allows the part to be easily sequenced from other input/output supplies. Other key features include undervoltage lockout (UVLO), overvoltage protection (OVP), thermal shutdown (TSD), and overcurrent protection (OCP).

The ADP2302/ADP2303 devices are available in the 8-lead, SOIC package with exposed paddle and are rated for the −40°C to +125°C junction temperature range.

Rev. A

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7/10—Revision 0: Initial Version

SPECIFICATIONS

V_{IN} = 3.3 V, T_J = −40°C to +125°C for minimum/maximum specifications, and T_A = 25°C for typical specifications, unless otherwise noted.

Table 1.

Parameters	Symbol	Test Conditions	Min	Typ	Max	Unit
VIN						
Voltage Range	V_{IN}		3.0		20	V
Supply Current	I_{VIN}	No switching, V_{IN} = 12 V		720	950	µA
Shutdown Current	I_{SHDN}	V_{EN} = 0 V, V_{IN} = 12 V		24	45	µA
Undervoltage Lockout Threshold	UVLO	V_{IN} rising		2.7	2.9	V
		V_{IN} falling	2.2	2.4		V
FB						
Regulation Voltage	V_{FB}	ADP230xARDZ (adjustable)	0.788	0.8	0.812	V
		ADP230xARDZ-2.5	2.463	2.5	2.538	V
		ADP230xARDZ-3.3	3.25	3.3	3.35	V
		ADP230xARDZ-5.0	4.925	5.0	5.075	V
Bias Current	I_{FB}	ADP230xARDZ (adjustable)		0.01	0.1	µA
SW						
On Resistance[1]		$V_{BST} - V_{SW}$ = 5 V, I_{SW} = 200 mA	80	120	160	mΩ
Peak Current Limit		ADP2302, $V_{BST} - V_{SW}$ = 5 V	2.7	3.5	4.4	A
		ADP2303, $V_{BST} - V_{SW}$ = 5 V	4.6	5.5	6.4	A
Leakage Current		$V_{EN} = V_{SW}$ = 0 V, V_{IN} = 12 V		0.1	5	µA
Minimum On Time				126	170	ns
Minimum Off Time				210	280	ns
OSCILLATOR FREQUENCY	f_{SW}		595	700	805	kHz
SOFT START TIME				2048		Clock cycles
EN						
Input Threshold	V_{EN}		1.12	1.2	1.28	V
Input Hysteresis				100		mV
Pull-Down Current				1.2		µA
BOOTSTRAP VOLTAGE	V_{BOOT}	V_{IN} = 12 V	4.7	5.0	5.3	V
PGOOD						
PGOOD Rising Threshold			82.5	87.5	92.5	%
PGOOD Hysteresis				2.5		%
PGOOD Deglitch Time[2]				32		Clock cycles
PGOOD Output Low Voltage				150	300	mV
PGOOD Leakage Current		V_{PGOOD} = 5 V		0.1	1	µA
THERMAL SHUTDOWN						
Threshold		Rising temperature		150		°C
Hysteresis				15		°C

[1] Pin-to-Pin measurements.
[2] Guaranteed by design.

ABSOLUTE MAXIMUM RATINGS

Table 2.

Parameter	MAX Rating
VIN, EN, PGOOD	−0.3 V to +24 V
SW	−1.0 V to +24 V
BST to SW	−0.6 V to +6 V
FB, NC	−0.3 V to +6 V
Operating Junction Temperature Range	−40°C to +125°C
Storage Temperature Range	−65°C to +150°C
Soldering Conditions	JEDEC J-STD-020

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Absolute maximum ratings apply individually only, not in combination. Unless otherwise specified, all voltages are referenced to GND.

THERMAL RESISTANCE

θ_{JA} is specified for the worst-case conditions, that is, a device soldered in a circuit board for surface-mount packages.

Table 3. Thermal Resistance[1]

Package Type	θ_{JA}	Unit
8-Lead SOIC_N_EP	58.5	°C/W

[1] θ_{JA} is measured using natural convection on JEDEC 4-layer board.

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

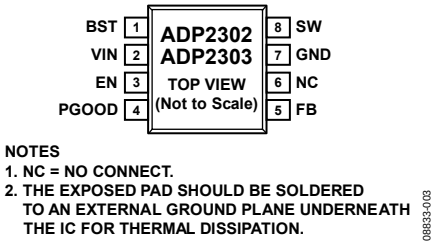

Figure 3. Pin Configuration (Top View)

Table 4. Pin Function Descriptions

Pin No.	Mnemonic	Description
1	BST	Bootstrap Supply for the High-Side MOSFET Driver. A 0.1 µF capacitor is connected between SW and BST to provide a floating driver voltage for the power switch.
2	VIN	Power Input. Connect to the input power source with a ceramic bypass capacitor to GND directly from this pin.
3	EN	Output Enable. Pull this pin high to enable the output. Pull this pin low to disable the output. This pin can also be used as a programmable UVLO input. This pin has an internal 1.2 µA pull-down current to GND.
4	PGOOD	Power-Good Open-Drain Output.
5	FB	Feedback Voltage Sense Input. For the adjustable version, connect this pin to a resistive divider from V_{OUT}. For the fixed output version, connect this pin to V_{OUT} directly.
6	NC	Used for internal testing. Connect to GND or leave this pin floating to ensure proper operation.
7	GND	Ground. Connect this pin to the ground plane.
8	SW	Switch Node Output. Connect an inductor to V_{OUT} and a catch diode to GND from this pin.
9 (EPAD)	Exposed Pad	The exposed pad should be soldered to an external ground plane underneath the IC for thermal dissipation.

TYPICAL PERFORMANCE CHARACTERISTICS

V_{IN} = 3.3 V, T_A = 25°C, unless otherwise noted.

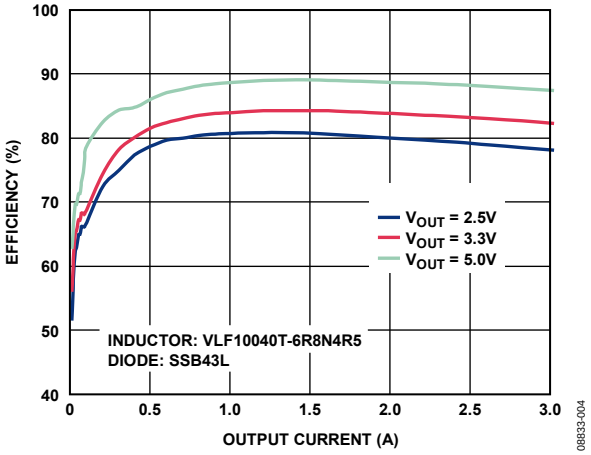

Figure 4. ADP2303 Efficiency, V_{IN} = 18 V

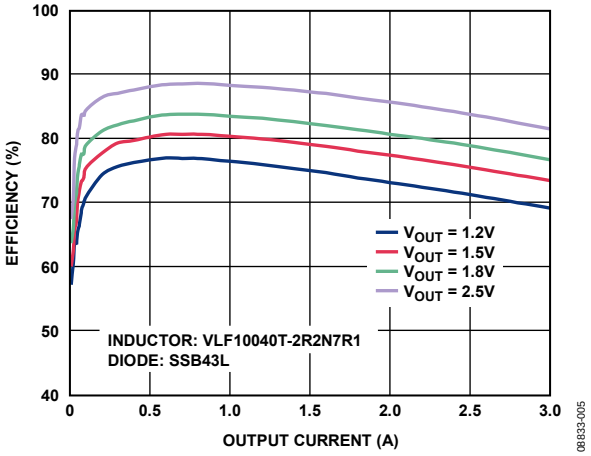

Figure 5. ADP2303 Efficiency, V_{IN} = 5 V

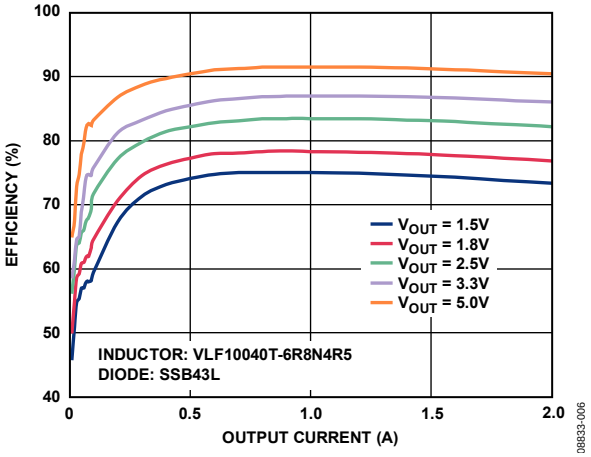

Figure 6. ADP2302 Efficiency, V_{IN} = 12 V

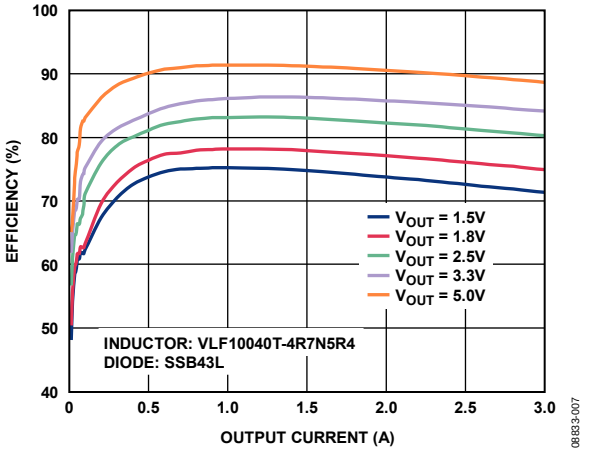

Figure 7. ADP2303 Efficiency, V_{IN} = 12 V

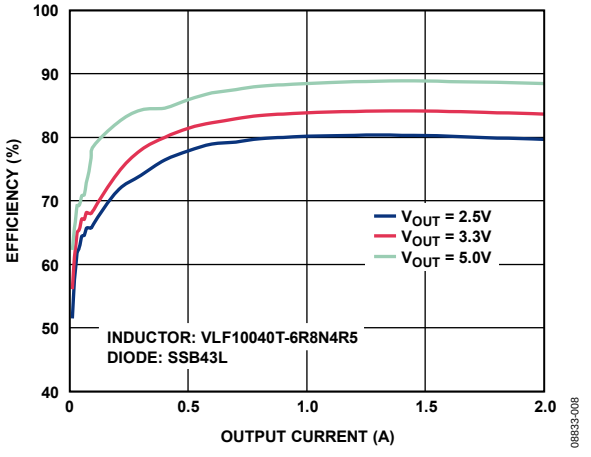

Figure 8. ADP2302 Efficiency, V_{IN} = 18 V

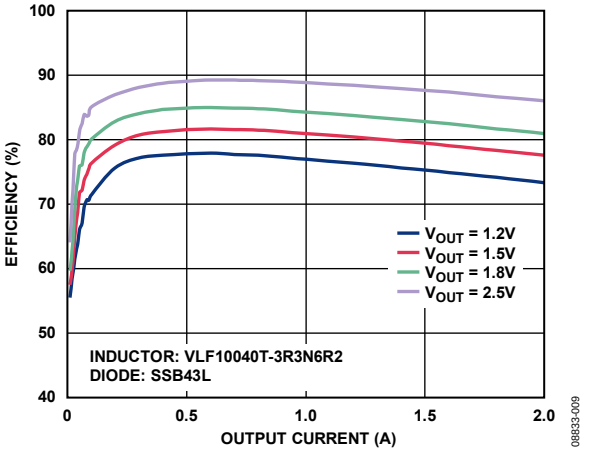

Figure 9. ADP2302 Efficiency, V_{IN} = 5 V

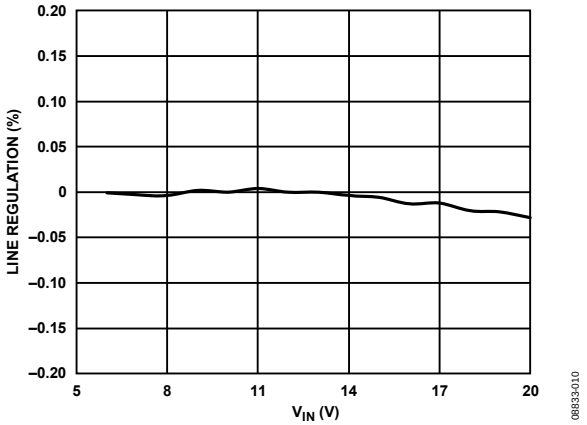

Figure 10. ADP2302 Line Regulation, V_{OUT} = 3.3 V, I_{OUT} = 2 A

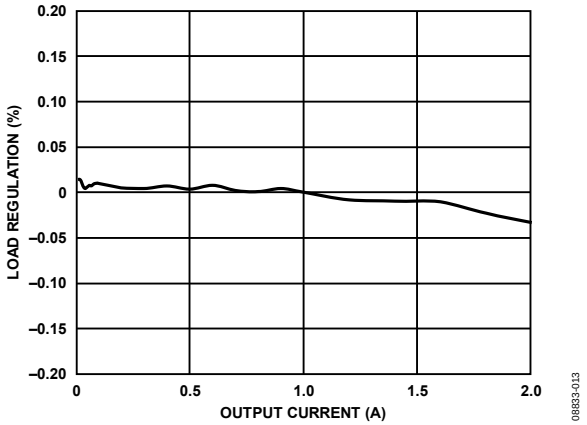

Figure 13. ADP2302 Load Regulation, V_{OUT} = 3.3V, V_{IN} = 12 V

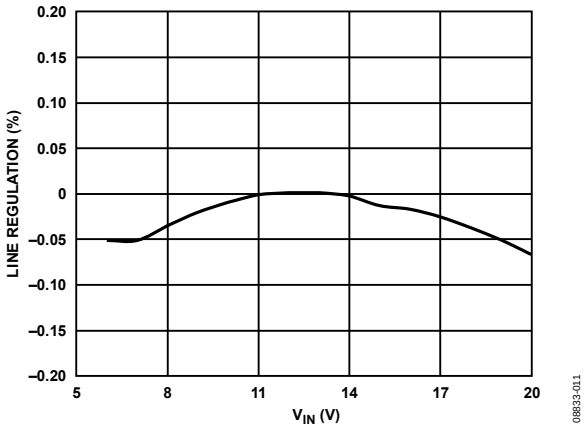

Figure 11. ADP2303 Line Regulation, V_{OUT} = 3.3 V , I_{OUT} = 3 A

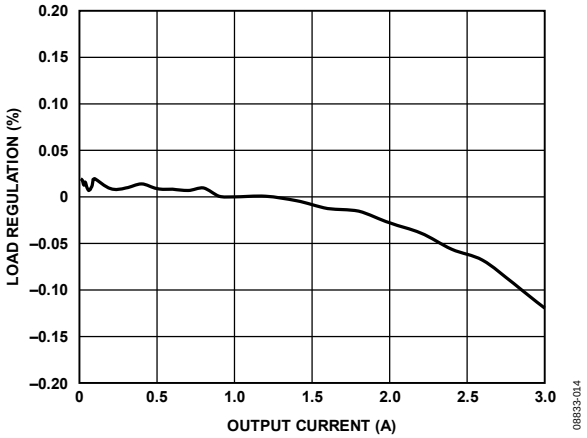

Figure 14. ADP2303 Load Regulation, V_{OUT} = 3.3 V, V_{IN} = 12 V

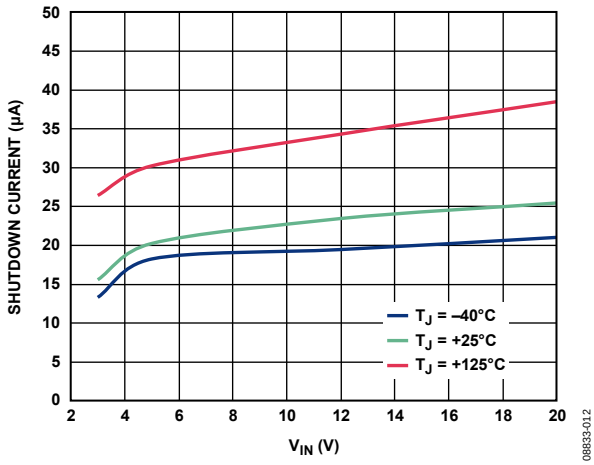

Figure 12. Shutdown Current vs. V_{IN}

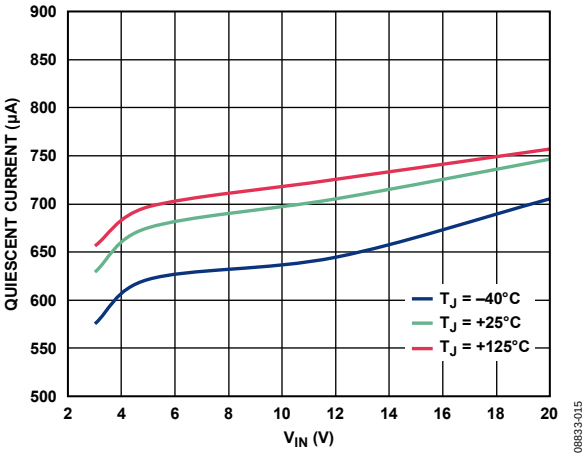

Figure 15. Quiescent Current vs. V_{IN}

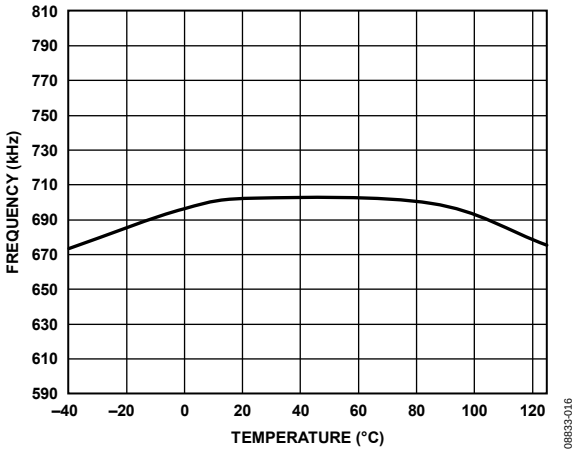

Figure 16. Frequency vs. Temperature

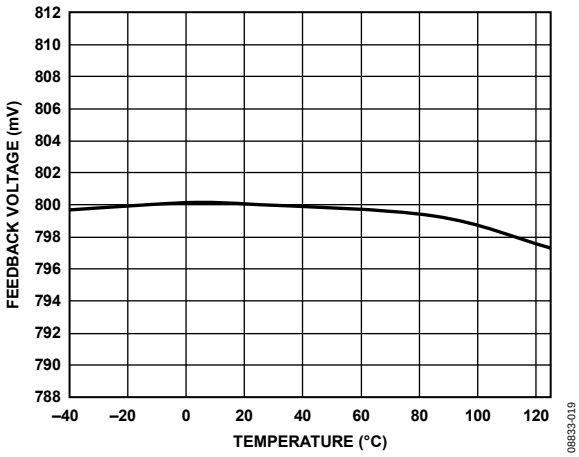

Figure 19. 0.8 V Feedback Voltage vs. Temperature

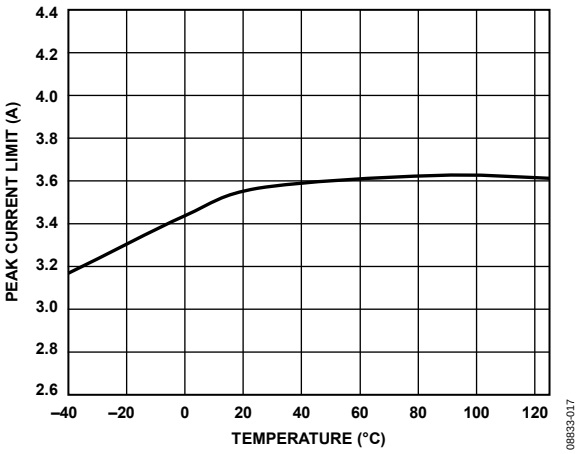

Figure 17. ADP2302 Current-Limit Threshold vs. Temperature, $V_{BST} - V_{SW} = 5$ V

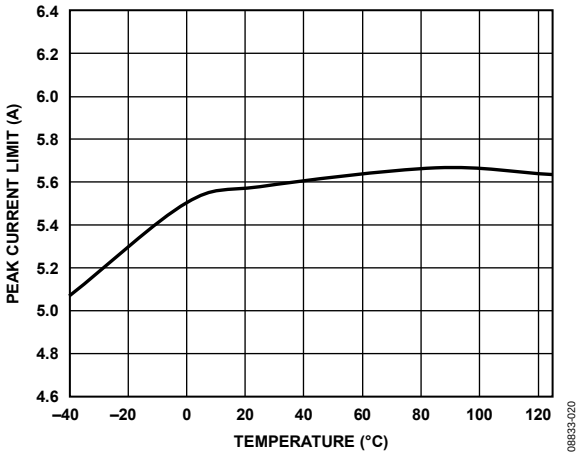

Figure 20. ADP2303 Current-Limit Threshold vs. Temperature, $V_{BST} - V_{SW} = 5$ V

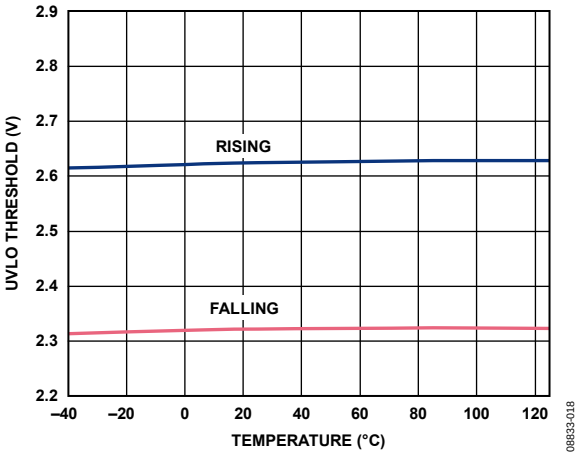

Figure 18. UVLO Threshold vs. Temperature

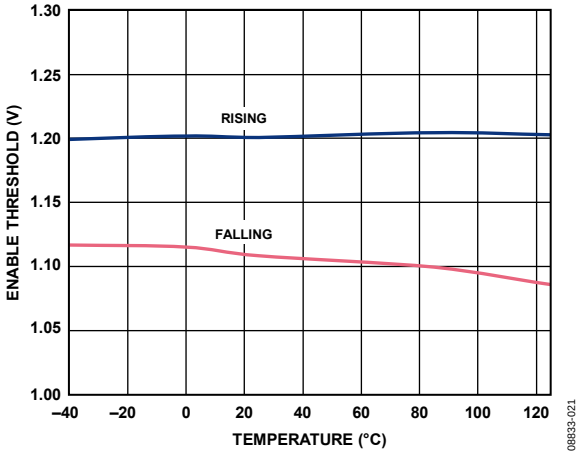

Figure 21. Enable Threshold vs. Temperature

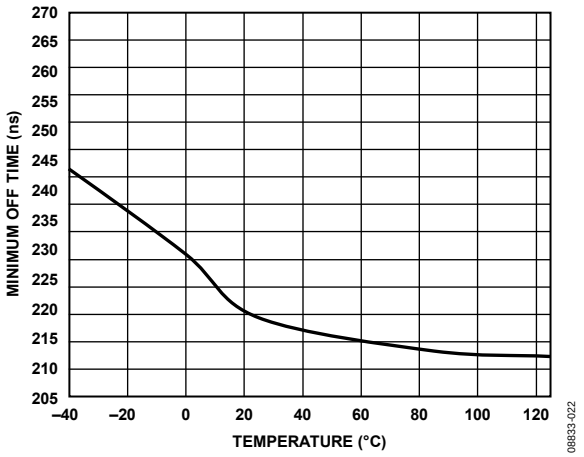

Figure 22. Minimum Off Time vs. Temperature

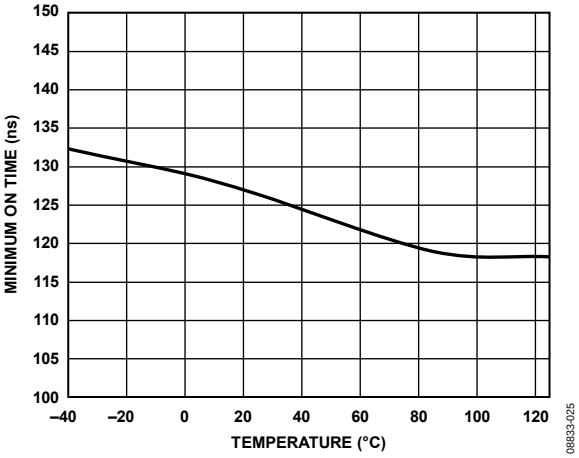

Figure 25. Minimum On Time vs. Temperature

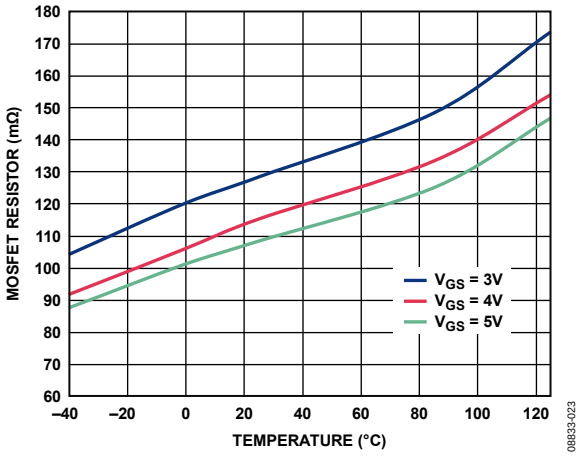

Figure 23. MOSFET R_{DSON} vs. Temperature (Pin-to-Pin Measurement)

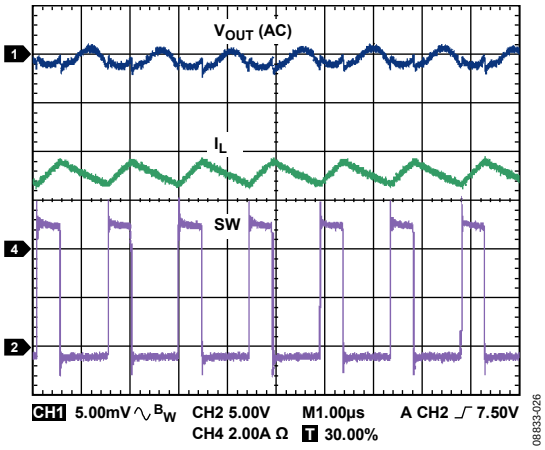

Figure 26. Continuous Conduction Mode (CCM), V_{OUT} = 3.3 V, V_{IN} = 12 V

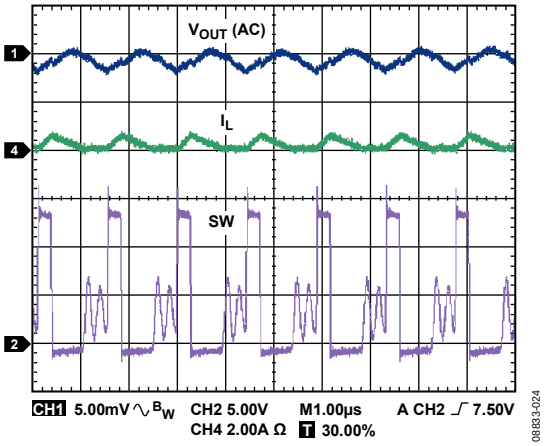

Figure 24. Discontinuous Conduction Mode (DCM), V_{OUT} = 3.3 V, V_{IN} = 12 V

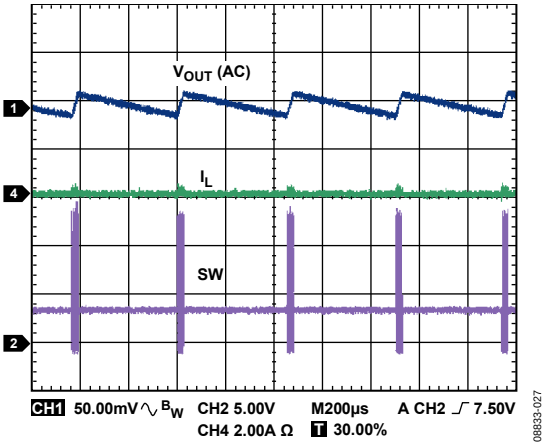

Figure 27. Power Saving Mode, V_{OUT} = 3.3 V, V_{IN} = 12 V

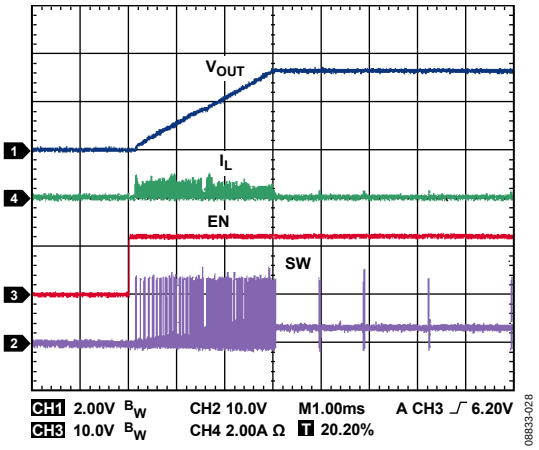

Figure 28. Soft Start Without Load, V_{OUT} = 3.3 V, V_{IN} = 12 V

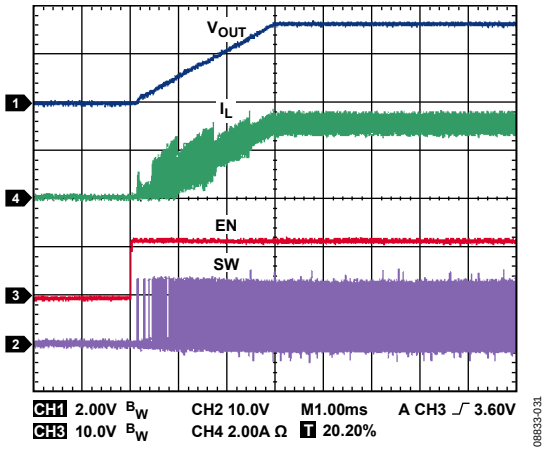

Figure 31. Soft Start with Full Load, V_{OUT} = 3.3 V, V_{IN} = 12 V

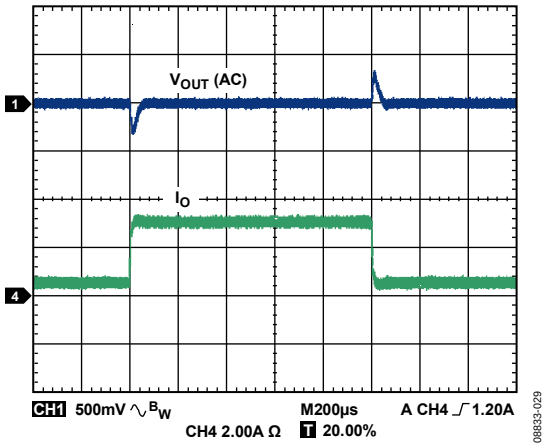

Figure 29. ADP2303 Load Transient, 0.5 A to 3.0 A, V_{OUT} = 5.0 V, V_{IN} = 12 V, L = 4.7 µH, C_{OUT} = 47 µF

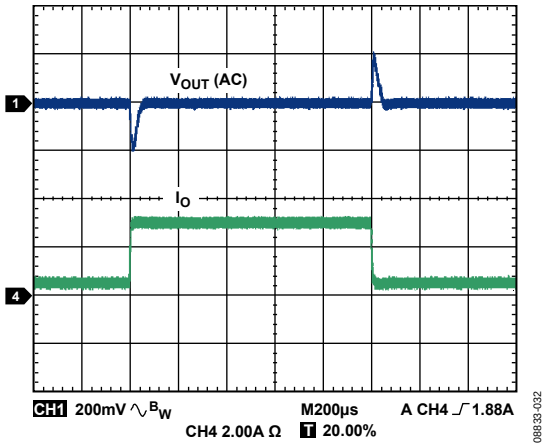

Figure 32. ADP2303 Load Transient, 0.5 A to 3.0 A, V_{OUT} = 3.3 V, V_{IN} = 12 V, L = 4.7 µH, C_{OUT} = 2 × 47 µF

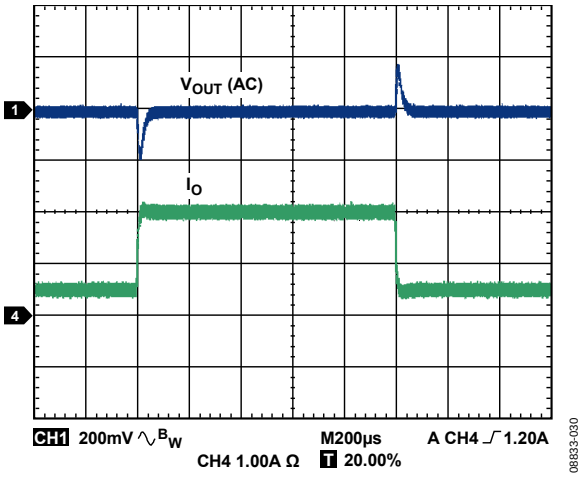

Figure 30. ADP2302 Load Transient, 0.5 A to 2.0 A, V_{OUT} = 5.0 V, V_{IN} = 12 V, L = 6.8 µH, C_{OUT} = 2 × 22 µF

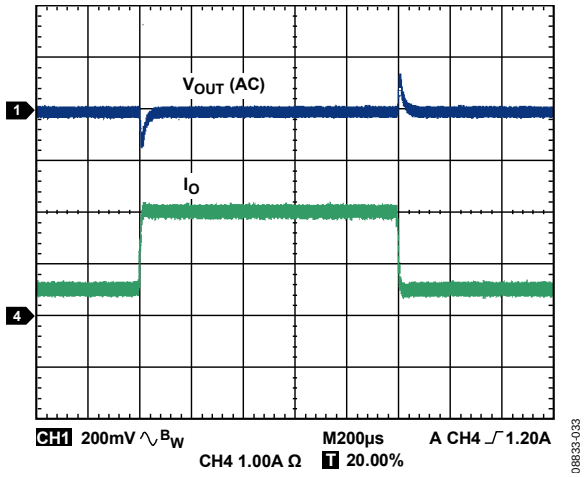

Figure 33. ADP2302 Load Transient, 0.5 A to 2.0 A, V_{OUT} = 3.3 V, V_{IN} = 12 V, L = 6.8 µH, C_{OUT} = 2 × 22 µF

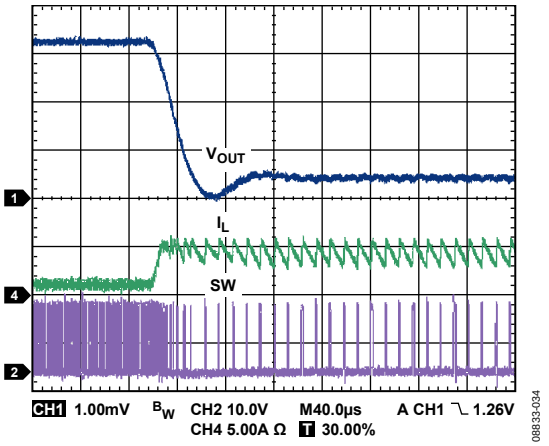

Figure 34. Output Short, V_{OUT} = 3.3 V, V_{IN} = 12 V, L = 4.7 µH, C_{OUT} = 2 × 47 µF

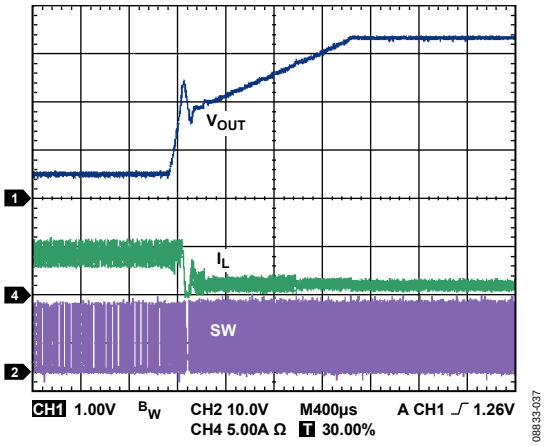

Figure 37. Output Short Recovery, V_{OUT} = 3.3 V, V_{IN} = 12 V, L = 4.7 µH, C_{OUT} = 2 × 47 µF

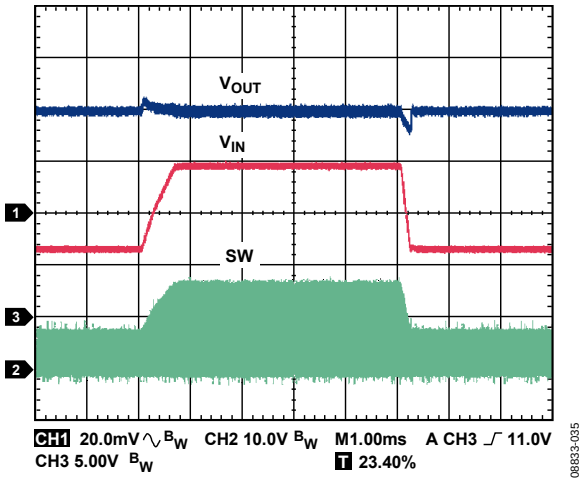

Figure 35. ADP2303 Line Transient, 7 V to 15 V, V_{OUT} = 3.3 V, I_{OUT} = 3 A, L = 4.7 µH, C_{OUT} = 2 × 47 µF

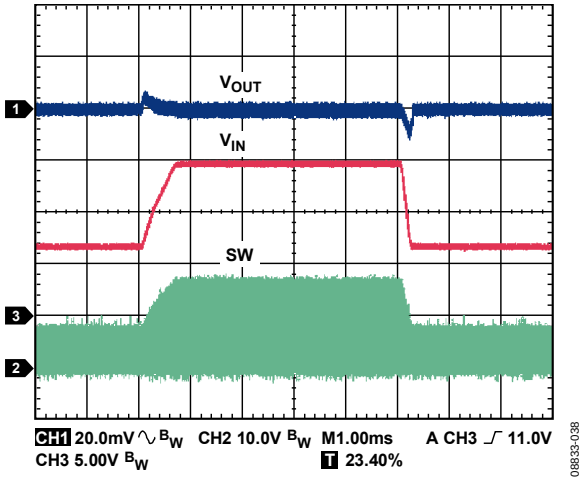

Figure 38. ADP2302 Line Transient, 7 V to 15 V, V_{OUT} = 3.3 V, I_{OUT} = 2 A, L = 6.8 µH, C_{OUT} = 2 × 22 µF

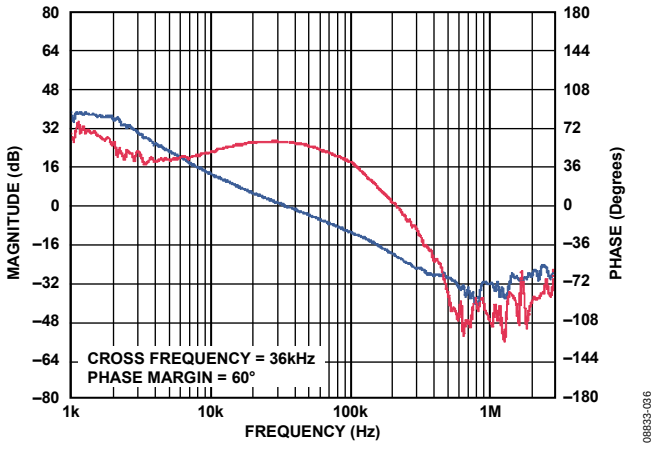

Figure 36. ADP2302 Bode Plot, V_{OUT} = 2.5 V, V_{IN} = 12 V, L = 4.7 µH, C_{OUT} =3 × 22 µF

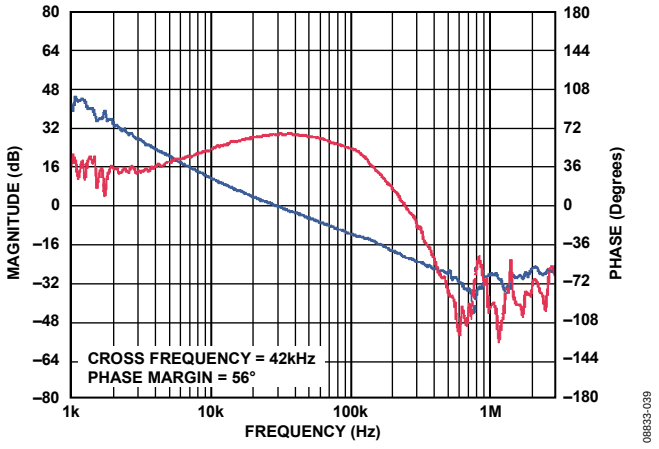

Figure 39. ADP2302 Bode Plot, V_{OUT} = 3.3 V, V_{IN} = 12 V, L = 6.8 µH, C_{OUT} = 2 × 22 µF

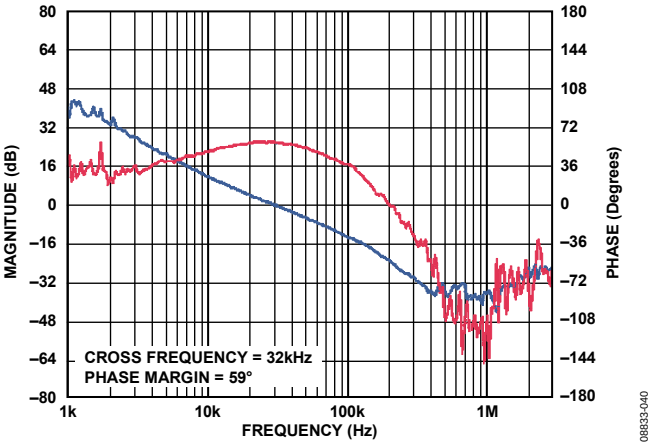

Figure 40. ADP2302 Bode Plot, V_{OUT} = 5 V, V_{IN} = 12 V, L = 6.8 µH, C_{OUT} = 2 × 22 µF

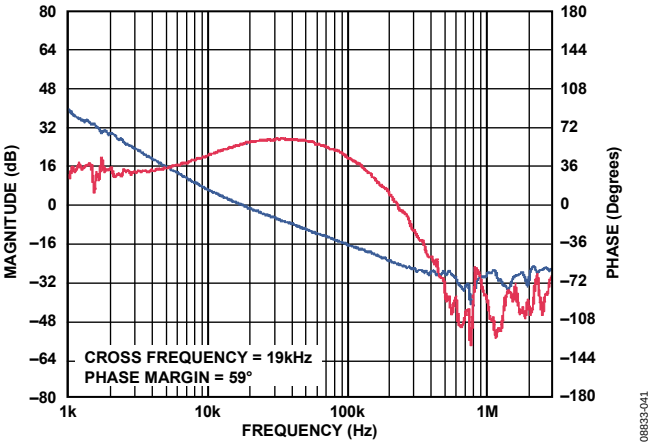

Figure 41. ADP2303 Bode Plot, V_{OUT} = 3.3 V, V_{IN} = 12 V, L = 4.7 µH, C_{OUT} = 2 × 47 µF

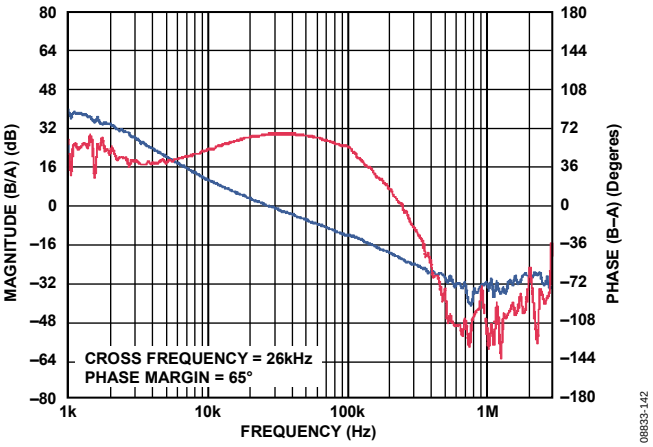

Figure 42. ADP2303 Bode Plot, V_{OUT} = 2.5 V, V_{IN} = 12 V, L = 3.3 µH, C_{OUT} = 2 × 47 µF

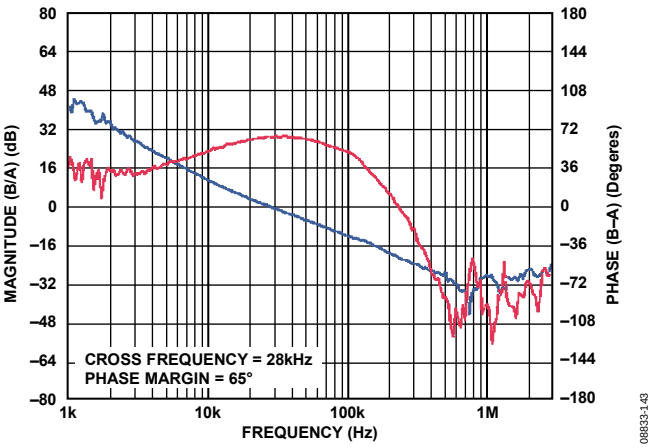

Figure 43. ADP2303 Bode Plot, V_{OUT} = 5 V, V_{IN} = 12 V, L = 4.7 µH, C_{OUT} = 47 µF

FUNCTIONAL BLOCK DIAGRAM

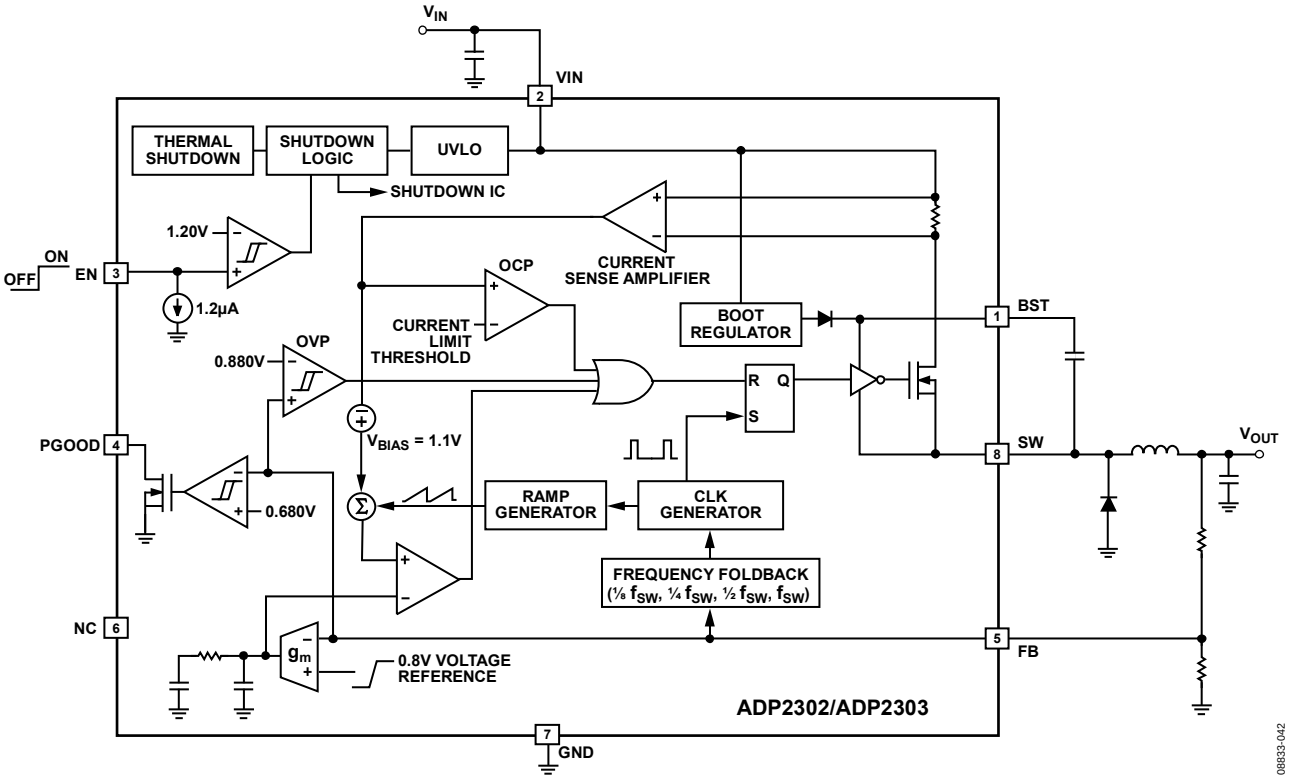

Figure 44. Functional Block Diagram

THEORY OF OPERATION

The ADP2302/ADP2303 are nonsynchronous, step-down, dc-to-dc regulators, each with an integrated high-side power MOSFET. The high switching frequency and 8-lead SOIC package provide a small, step-down, dc-to-dc regulator solution.

The ADP2302/ADP2303 can operate with an input voltage from 3.0 V to 20 V while regulating an output voltage down to 0.8 V.

The ADP2302 can provide 2 A maximum continuous output current, and the ADP2303 can provide 3 A maximum continuous output current.

BASIC OPERATION

The ADP2302/ADP2303 use the fixed-frequency, peak current-mode PWM control architecture from medium to high loads, but shift to a pulse-skip mode control scheme at light loads to reduce the switching power losses and improve efficiency. When these devices operate in fixed-frequency PWM mode, output regulation is achieved by controlling the duty cycle of the integrated MOSFET. While the devices are operating in pulse-skip mode at light loads, the output voltage is controlled in a hysteretic manner with higher output ripple. In this mode of operation, the regulator periodically stops switching for a few cycles, thus keeping the conversion losses minimal to improve efficiency.

PWM MODE

In PWM mode, the ADP2302/ADP2303 operate at a fixed frequency, set by an internal oscillator. At the start of each oscillator cycle, the MOSFET switch is turned on, providing a positive voltage across the inductor. The inductor current increases until the current-sense signal crosses the peak inductor current threshold that turns off the MOSFET switch; this threshold is set by the error amplifier output. During the MOSFET off time, the inductor current declines through the external diode until the next oscillator clock pulse comes and a new cycle starts.

POWER SAVING MODE

To achieve higher efficiency, the ADP2302/ADP2303 smoothly transition to the pulse-skip mode when the output load decreases below the pulse-skip current threshold. When the output voltage dips below the regulation, the ADP2302/ADP2303 enter PWM mode for a few oscillator cycles until the voltage increases to regulation range. During the idle time between bursts, the MOSFET switch is turned off, and the output capacitor supplies all the output current.

Because the pulse-skip mode comparator monitors the internal compensation node, which represents the peak inductor current information, the average pulse-skip load current threshold depends on the input voltage (V_{IN}), the output voltage (V_{OUT}), the inductor, and the output capacitor.

Because the output voltage occasionally dips below regulation and then recovers, the output voltage ripple in the power saving mode is larger than the ripple in the PWM mode of operation.

BOOTSTRAP CIRCUITRY

The ADP2302/ADP2303 each have an integrated boot regulator, which requires that a 0.1 µF ceramic capacitor (X5R or X7R) be placed between the BST and SW pins to provide the gate drive voltage for the high-side MOSFET. There is at least a 1.2 V difference between the BST and SW pins to turn on the high-side MOSFET. This voltage should not exceed 5.5 V in case the BST pin is supplied with the external voltage source through a diode.

The ADP2302/ADP2303 generate a typical 5.0 V bootstrap voltage for the gate drive circuit by differentially sensing and regulating the voltage between the BST and SW pins. There is a diode integrated on the chip that blocks the reverse voltage between the VIN and BST pins when the MOSFET switch is turned on.

PRECISION ENABLE

The ADP2302/ADP2303 provide a precision enable circuit that has 1.2 V reference threshold with 100 mV hysteresis. When the voltage at the EN pin is greater than 1.2 V (typical), the part is enabled. If the EN voltage falls below 1.1 V (typical), the chip is disabled. The precision enable threshold voltage allows the ADP2302/ADP2303 to be easily sequenced from other input/output supplies. It also can be used as a programmable UVLO input by using a resistive divider. An internal 1.2 µA pull-down current prevents errors if the EN pin is left floating.

INTEGRATED SOFT START

The ADP2302/ADP2303 have an internal digital soft start circuitry to limit the output voltage rise time and reduce the inrush current at power up. The soft start time is fixed at 2048 clock cycles.

CURRENT LIMIT

The ADP2302/ADP2303 include current-limit protection circuitry to limit the amount of positive current flowing through the high-side MOSFET switch. The positive current limit on the power switch limits the amount of current that can flow from the input to the output.

SHORT-CIRCUIT PROTECTION

The ADP2302/ADP2303 include frequency foldback to prevent output current runaway when there is a hard short on the output. The switching frequency is reduced when the voltage at the FB pin drops below a certain value, which allows more time for the inductor current to decline, but increases the ripple current while regulating the peak current. This results in a reduction in average output current and prevents output current runaway. The correlation between the switching frequency and the FB pin voltage is shown in Table 5.

Table 5. Correlation Between f_{SW} and V_{FB}

FB Pin Voltage	Switching Frequency
$V_{FB} \geq 0.6$ V	f_{SW}
0.4 V < V_{FB} < 0.6 V	1/2 f_{SW}
0.2 V < $V_{FB} \leq$ 0.4 V	1/4 f_{SW}
$V_{FB} \leq 0.2$ V	1/8 f_{SW}

When a hard short ($V_{FB} \leq 0.2$ V) is removed, a soft start cycle is initiated to regulate the output back to its level during normal operation, which helps to limit the inrush current and prevent possible overshoot on the output voltage.

UNDERVOLTAGE LOCKOUT (UVLO)

The ADP2302/ADP2303 have fixed, internally set undervoltage lockout circuitry (UVLO). If the input voltage drops below 2.4 V, the ADP2302/ADP2303 shut down and the MOSFET switch turns off. After the voltage rises above 2.7 V, the soft start period is initiated, and the part is enabled.

THERMAL SHUTDOWN (TSD)

If the ADP2302/ADP2303 junction temperature rises above 150°C, the thermal shutdown circuit disables the chip. Extreme junction temperature can be the result of high current operation, poor circuit board design, or high ambient temperature. A 15°C hysteresis is included so that when thermal shutdown occurs, the ADP2302/ADP2303 do not return to operation until the on-chip temperature drops below 135°C. When the devices recover from thermal shutdown, a soft start is initiated.

OVERVOLTAGE PROTECTION (OVP)

The ADP2302/ADP2303 provide an overvoltage protection feature to protect the system against an output short to a higher voltage supply. If the feedback voltage is above 0.880 V, the internal high-side MOSFET is turned off, until the voltage at FB decreases to 0.850 V. At that time, the ADP2302/ADP2303 resume normal operation.

POWER GOOD

The PGOOD pin is an active high, open-drain output and requires a resistor to pull it up to a voltage (<20.0 V). A high indicates that the voltage on the FB pin (and therefore the output voltage) is above 87.5% of the reference voltage. A low indicates that the voltage on the FB pin is below 85% of the reference voltage. There is a 32-cycle waiting period after FB is detected as being in or out of bounds.

CONTROL LOOP

The ADP2302/ADP2303 are internally compensated to minimize external component count and cost. In addition, the built-in slope compensation helps to prevent subharmonic oscillations when the ADP2302/ADP2303 operate at a duty cycle greater than or close to 50%.

APPLICATIONS INFORMATION

ADIsimPower DESIGN TOOL

The ADP2302/ADP2303 are supported by the ADIsimPower design tool set. ADIsimPower is a collection of tools that produce complete power designs optimized for a specific design goal. The tools enable the user to generate a full schematic and bill of materials, and calculate performance in minutes. ADIsimPower can optimize designs for cost, area, efficiency, and parts count while taking into consideration the operating conditions and limitations of the IC and all real external components. For more information about ADIsimPower design tools, refer to www.analog.com/ADIsimPower. The tool set is available from this website, and users can request an unpopulated board through the tool.

PROGRAMMING OUTPUT VOLTAGE

ADP2302/ADP2303 have an adjustable version where the output voltage is programmed through an external resistive divider, as shown in Figure 45. Suggested resistor values for the typical output voltage setting are listed in Table 6. The output voltages are calculated using the following equation:

$$V_{OUT} = 0.800\ \text{V} \times \left(1 + \frac{R_{TOP}}{R_{BOT}}\right)$$

where:
V_{OUT} is the output voltage.
R_{TOP} is the feedback resistor from V_{OUT} to FB.
R_{BOT} is the feedback resistor from FB to GND.

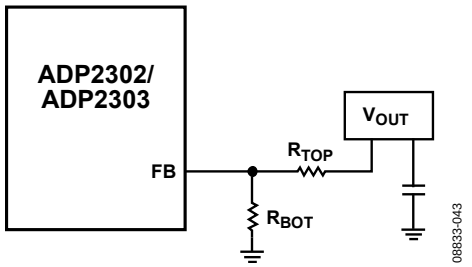

Figure 45. Programming the Output Voltage Using a Resistive Voltage Divider

Table 6. Suggested Values for Resistive Voltage Divider

V_{OUT} (V)	R_{TOP} (kΩ), ±1%	R_{BOT} (kΩ), ±1%
1.2	10	20
1.5	10	11.3
1.8	12.7	10.2
2.5	21.5	10.2
3.3	31.6	10.2
5.0	52.3	10

VOLTAGE CONVERSION LIMITATIONS

There are both lower and upper output voltage limitations for a given input voltage due to the minimum on time, the minimum off time, and the bootstrap dropout voltage.

The lower limit of the output voltage is constrained by the controllable minimum on time, which can be as high as 170 ns for the worst case. By considering the variation of both the switching frequency and the input voltage, the equation for the lower limit of the output voltage is

$$V_{OUT(min)} = t_{MIN\text{-}ON} \times f_{SW(max)} \times (V_{IN(max)} + V_D) - V_D$$

where:
$V_{IN(max)}$ is the maximum input voltage.
$f_{SW(max)}$ is the maximum switching frequency for the worst case.
$t_{MIN\text{-}ON}$ is the minimum controllable on time.
V_D is the diode forward drop.

The upper limit of the output voltage is constrained by the minimum controllable off time, which can be as high as 280 ns in ADP2302/ADP2303 for the worst case. By considering the variation of both the switching frequency and the input voltage, the equation for the upper limit of the output voltage is

$$V_{OUT(max)} = (1 - t_{MIN\text{-}OFF} \times f_{SW(max)}) \times (V_{IN(min)} + V_D) - V_D$$

where:
$V_{IN(min)}$ is the minimum input voltage.
$f_{SW(max)}$ is the maximum switching frequency for the worst case.
V_D is the diode forward drop.
$t_{MIN\text{-}OFF}$ is the minimum controllable off time.

In addition, the bootstrap circuit limits the minimum input voltage for the desired output due to the internal dropout voltage. To attain stable operation at light loads and ensure proper startup for the prebiased condition, the ADP2302/ADP2303 require the voltage difference between the input voltage and the regulated output voltage (or between the input voltage and the prebias voltage) to be greater than 2.1 V for the worst case. If the voltage difference is smaller, the bootstrap circuit relies on some minimum load current to charge the boost capacitor for startup. Figure 46 shows the typical required minimum input voltage vs. load current for the 3.3 V output voltage.

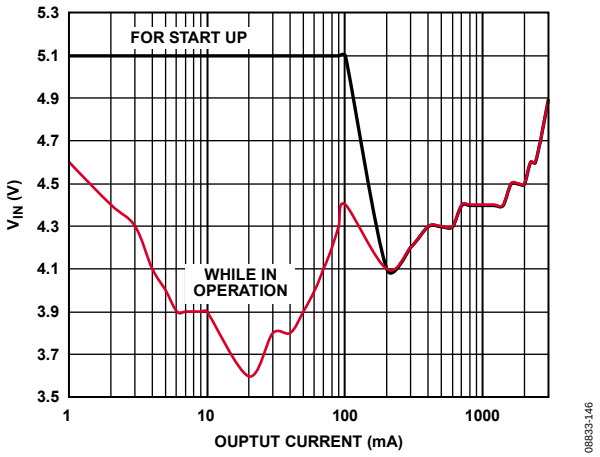

Figure 46. Minimum Input Voltage vs. Load Current

Based on three conversion limitations (the minimum on time, the minimum off time, and the bootstrap dropout voltage), Figure 47 shows the voltage conversion limitations.

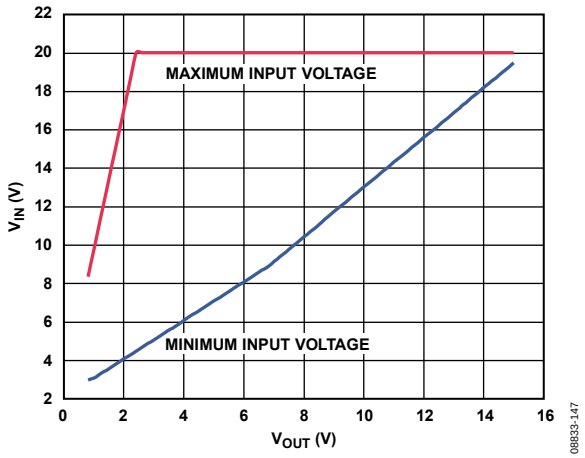

Figure 47. Voltage Conversion Limitations

LOW INPUT VOLTAGE CONSIDERATIONS

For low input voltage between 3 V and 5 V, the internal boot regulator cannot provide enough bootstrap voltage due to the internal dropout voltage. As a result, the increased MOSFET $R_{DS(ON)}$ reduces the available load current. To prevent this, add an external small-signal Schottky diode from a 5.0 V external bootstrap bias voltage. Because the absolute maximum rating between the BST and SW pins is 6.0 V, the bias voltage should be less than 5.5 V. Figure 48 shows the application diagram for the external bootstrap circuit.

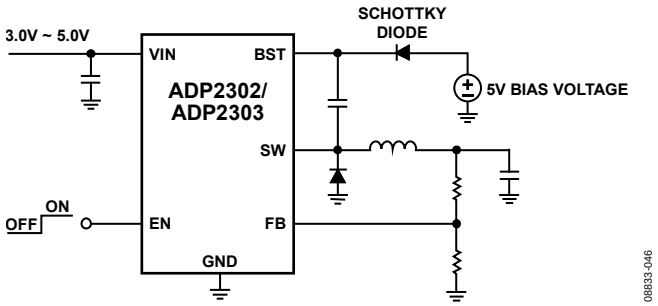

Figure 48. External Bootstrap Circuit for Low Input Voltage Application

PROGRAMMING THE PRECISION ENABLE

Generally, the EN pin can connect to the VIN pin so that the device automatically starts up when the input power is applied. However, the precision enabling feature allows the ADP2302/ ADP2303 to be used as a programmable UVLO by connecting a resistive voltage divider to VIN, as shown in Figure 49. This configuration prevents the start-up problems that can occur when VIN ramps up slowly in soft start with a relatively high load current.

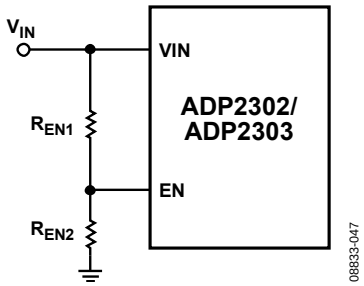

Figure 49. Precision Enable Used as a Programmable UVLO

The precision enable feature also allows the ADP2302/ADP2303 to be sequenced precisely by using a resistive voltage divider from another dc-to-dc power supply, as shown in Figure 50.

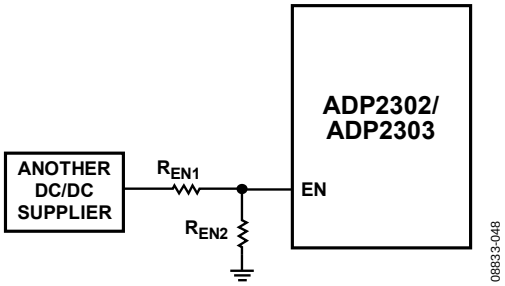

Figure 50. Precision Enable Used as a Sequencing Control from Another DC-to-DC Power Supply

With a 1.2 µA pull-down current on the EN pin, the equation for the start-up voltage in Figure 49 and Figure 50 is

$$V_{STARTUP} = \left(\frac{1.2\ \text{V}}{R_{EN2}} + 1.2\ \mu\text{A} \right) \times R_{EN1} + 1.2\ \text{V}$$

where:
$V_{STARTUP}$ is the start-up voltage to enable the chip.
R_{EN1} is the resistor from the dc source to EN.
R_{EN2} is the resistor from EN to GND.

INDUCTOR

The high switching frequency of the ADP2302/ADP2303 allows the use of small inductors. For best performance, use inductor values between 1 µH and 15 µH.

The peak-to-peak inductor ripple current is calculated using the following equation:

$$\Delta I_{RIPPLE} = \frac{(V_{IN} - V_{OUT})}{L \times f_{sw}} \times \left(\frac{V_{OUT} + V_D}{V_{IN} + V_D} \right)$$

where:
f_{SW} is the switching frequency.
L is the inductor value.
V_D is the diode forward drop.
V_{IN} is the input voltage.
V_{OUT} is the output voltage.

Inductors of smaller values are usually smaller in size but increase the ripple current and the output ripple voltage. As a guideline, the inductor peak-to-peak ripple current is typically set to 30% of the maximum load current for optimal transient

response and efficiency. Therefore, the inductor value is calculated using the following equation:

$$L = \frac{(V_{IN} - V_{OUT})}{0.3 \times I_{LOAD(\max)} \times f_{sw}} \times \left(\frac{V_{OUT} + V_D}{V_{IN} + V_D} \right)$$

where $I_{LOAD(max)}$ is the maximum load current.

The inductor peak current is calculated using the following equation:

$$I_{PEAK} = I_{LOAD(\max)} + \frac{\Delta I_{RIPPLE}}{2}$$

The minimum current rating of the inductor must be greater than the inductor peak current. For ferrite core inductors with a quick saturation characteristic, the inductor saturation current rating should be higher than the switch current limit threshold to prevent the inductor from reaching its saturation point. Be sure to validate the worst-case condition, in which there is a shorted output, over the intended temperature range.

Inductor conduction loss is caused by the flow of current through internal dc resistance (DCR). Larger sized inductors have smaller DCR of the inductor and, therefore, may reduce inductor conduction losses. Inductor core loss is related to the core material and the ac flux swing, which are affected by the peak-to-peak inductor ripple current. Because the ADP2302/ADP2303 are high frequency switching regulators, shielded ferrite core materials are recommended for their low core losses and low EMI. Some recommended inductors are shown in Table 8.

CATCH DIODE

The catch diode conducts the inductor current during the off time of the internal MOSFET. The average current of the diode in normal operation is, therefore, dependent on the duty cycle of the regulator as well as the output load current.

$$I_{DIODE(AVG)} = \left(1 - \frac{V_{OUT} + V_D}{V_{IN} + V_D}\right) \times I_{LOAD(\max)}$$

where V_D is the diode forward drop.

The only reason to select a diode with a higher current rating than necessary in normal operation is for the worst-case condition, in which there is a shorted output. In this case, the diode current increases up to the typical peak current limit threshold. Be sure to consult the diode data sheet to ensure that the diode can operate well within the thermal and electrical limits.

The reverse breakdown voltage rating of the diode must be higher than the highest input voltage and allow an appropriate margin for the ringing that may be present on the SW node. A Schottky diode is recommended for the best efficiency because it has a low forward voltage drop and fast switching speed. Table 7 provides a list of recommended Schottky diodes.

Table 7. Recommended Schottky Diodes

Vendor	Part No.	V_{RRM} (V)	I_{AVG} (A)
Vishay	SSB43L	30	4
	SSA33L	30	3
ON Semiconductor	MBRS330T3	30	3
Diodes Inc.	B330B	30	3

Table 8. Recommended Inductors

Vendor	Value (µH)	Part No.	DCR (mΩ)	I_{SAT} (A)	Dimensions L × W × H (mm)
Sumida	2.5	CDRH104RNP-2R5N	7.8	7.5	10.5 × 10.3 × 3.8
	3.8	CDRH104RNP-3R8N	9.6	6	10.5 × 10.3 × 3.8
	5.2	CDRH104RNP-5R2N	16	5.5	10.5 × 10.3 × 3.8
	7	CDRH104RNP-7R0N	20	4.8	10.5 × 10.3 × 3.8
	10	CDRH104RNP-100N	26	4.4	10.5 × 10.3 × 3.8
Coilcraft	2.5	MSS1038-252NL	10	7.62	10 × 10.2 × 3.8
	3.8	MSS1038-382NL	13	6.5	10 × 10.2 × 3.8
	5.2	MSS1038-522NL	22	5.28	10 × 10.2 × 3.8
	7	MSS1038-702NL	27	4.74	10 × 10.2 × 3.8
	10	MSS1038103NL	35	3.9	10 × 10.2 × 3.8
Toko	2.8	#919AS-2R8M	10.7	8.3	10.3 × 10.3 × 4.5
	3.7	#919AS-3R7M	14.2	7	10.3 × 10.3 × 4.5
	4.7	#919AS-4R7M	16.2	6.1	10.3 × 10.3 × 4.5
	6.4	#919AS-6R4M	22.9	5.2	10.3 × 10.3 × 4.5
	10	#919AS-100M	26.5	4.3	10.3 × 10.3 × 4.5
TDK	2.2	VLF10040T-2R2N7R1	7.9	8.2	10 × 9.7 × 4.0
	3.3	VLF10040T-3R3N6R2	10.5	6.7	10 × 9.7 × 4.0
	4.7	VLF10040T-4R7N5R4	12.7	5.4	10 × 9.7 × 4.0
	6.8	VLF10040T-6R8N4R5	19.8	4.6	10 × 9.7 × 4.0
	10	VLF10040T-100M3R8	28	3.8	10 × 9.7 × 4.0

INPUT CAPACITOR

The input capacitor must be able to support the maximum input operating voltage and the maximum RMS input current. The rms ripple current flowing through the input capacitor is, at maximum, $I_{LOAD(max)}/2$. Select an input capacitor capable of withstanding the rms ripple current for an application's maximum load current using the following equation:

$$I_{IN(RMS)} = I_{LOAD(\max)} \times \sqrt{D \times (1-D)}$$

where D is the duty cycle and is equal to

$$D = \frac{V_{OUT} + V_D}{V_{IN} + V_D}$$

The recommended input capacitance is ceramic with X5R or X7R dielectrics due to its low ESR and small temperature coefficients. A capacitance of 10 µF should be adequate for most applications. To minimize supply noise, place the input capacitor as close as possible to the VIN pin of the ADP2302/ADP2303.

OUTPUT CAPACITOR

The output capacitor selection affects both the output voltage ripple and the loop dynamics of the regulator. The ADP2302/ADP2303 are designed to operate with small ceramic capacitors that have low ESR and equivalent series inductance (ESL) and are, therefore, easily able to meet stringent output voltage ripple specifications.

When the regulator operates in continuous conduction mode, the overall output voltage ripple is the sum of the voltage spike caused by the output capacitor equivalent series resistance (ESR) plus the voltage ripple caused by the charging and discharging of the output capacitor

$$\Delta V_{RIPPLE} = \Delta I_{RIPPLE} \times \left(\frac{1}{8 \times f_{sw} \times C_{OUT}} + ESR_{C_{OUT}} \right)$$

Capacitors with lower ESR are preferable to guarantee low output voltage ripple, as shown in the following equation:

$$ESR_{Cout} \le \frac{\Delta V_{RIPPLE}}{\Delta I_{RIPPLE}}$$

Ceramic capacitors are manufactured with a variety of dielectrics, each with different behavior over temperature and applied voltage. X5R or X7R dielectrics are recommended for best performance, due to their low ESR and small temperature coefficients. Y5V and Z5U dielectrics are not recommended because of their poor temperature and dc bias characteristics.

In general, most applications require a minimum output capacitor value of 2 × 22 µF.

Some recommended output capacitors for $V_{OUT} \le 5.0$ V are provided in Table 9.

THERMAL CONSIDERATION

ADP2302/ADP2303 have an internal high-side MOSFET and its drive circuit. Only a small amount of power dissipates inside the ADP2302/ADP2303 package under typical load conditions, which reduces thermal constraints.

However, in applications with maximum loads at high ambient temperature and high duty cycle, the heat dissipated in the package may cause the junction temperature of the die to exceed the maximum junction temperature of 125°C. If the junction temperature exceeds 150°C, the regulator goes into thermal shutdown and recovers when the junction temperature drops below 135°C.

The junction temperature of the die is the sum of the ambient temperature and the temperature rise of the package due to power dissipation, as indicated in the following equation:

$$T_J = T_A + T_R$$

where:
T_J is the junction temperature.
T_A is the ambient temperature.
T_R is the rising temperature of the package due to power dissipation.

The rising temperature of the package is directly proportional to the power dissipation in the package. The proportionality constant for this relationship is the thermal resistance from the junction of the die to the ambient temperature, as shown in the following equation:

$$T_R = \theta_{JA} \times P_D$$

where:
T_R is the rising temperature of the package.
θ_{JA} is the thermal resistance from the junction of the die to the ambient temperature of the package.
P_D is the power dissipation in the package.

Table 9. Recommended Capacitors for $V_{OUT} \le 5.0$ V

Vendor	Value	Part No.	Dimensions L × W × H (mm)
Murata	22 µF, 6.3 V, X5R	GRM31CR60J226KE19	3.2 × 2.5 × 2.0
	47 µF, 6.3 V, X5R	GRM32ER60J476ME20	3.2 × 2.5 × 2.0
TDK	22 µF, 6.3 V, X5R	C3216X5R0J226MB	3.2 × 1.6 × 0.85
	33 µF, 6.3 V, X5R	C3216X5R0J336MB	3.2 × 1.6 × 1.3
	47 µF, 6.3 V, X5R	C3225X5R0J476MB	3.2 × 2.5 × 2.5

DESIGN EXAMPLE

This section provides the procedures to select the external components, based on the example specifications listed in Table 10. The schematic for this design example is shown in Figure 51. Because the output current is 3 A, the ADP2303 is chosen for this application.

Table 10. Step-Down DC-to-DC Regulator Requirements

Parameter	Specification	Additional Requirements
Input Voltage, V_{IN}	12.0 V ± 10%	None
Output Voltage, V_{OUT}	3.3 V, 3 A, 1% V_{OUT} ripple at full load condition	None
Programmable UVLO Voltage	V_{IN} start-up voltage approximately 7.8 V	None
PGOOD	Not used	None

CATCH DIODE SELECTION

Select the catch diode. A Schottky diode is recommended for best efficiency because it has a low forward voltage drop and faster switching speed. The average current of the catch diode in normal operation, with a typical Schottky diode forward voltage, can be calculated using the following equation:

$$I_{DIODE(AVG)} = \left(1 - \frac{V_{OUT} + V_D}{V_{IN} + V_D}\right) \times I_{LOAD(\max)}$$

where:
V_{OUT} = 3.3 V.
V_{IN} = 12 V.
$I_{LOAD(max)}$ = 3 A.
V_D = 0.4 V.

Therefore, $I_{DIODE(AVG)}$ = 2.1 A.

In this case, selecting a SSB43L, 4.0 A, 30 V surface-mount Schottky diode results in more reliable operation.

INDUCTOR SELECTION

Select the inductor by using the following equation:

$$L = \frac{(V_{IN} - V_{OUT})}{0.3 \times I_{LOAD(\max)} \times f_{sw}} \times \left(\frac{V_{OUT} + V_D}{V_{IN} + V_D}\right)$$

where:
V_{OUT} = 3.3 V.
V_{IN} = 12 V.
$I_{LOAD(max)}$ = 3 A.
V_D = 0.4 V.
f_{SW} = 700 kHz.

This results in L = 4.12 µH. The closest standard value is 4.7 µH; therefore, ΔI_{RIPPLE} = 0.7 A.

The inductor peak current is calculated using the following equation:

$$I_{PEAK} = I_{LOAD(\max)} + \frac{\Delta I_{RIPPLE}}{2}$$

where:
$I_{LOAD(max)}$ = 3 A.
ΔI_{RIPPLE} = 0.7 A.

The calculated peak current for the inductor is 3.4 A. Therefore, in this application, select VLF10040T-4R7N5R4 as the inductor.

OUTPUT CAPACITOR SELECTION

Select the output capacitor based on the minimum output voltage ripple requirement, according to the following equation:

$$\Delta V_{RIPPLE} = \Delta I_{RIPPLE} \times \left(\frac{1}{8 \times f_{sw} \times C_{OUT}} + ESR_{C_{OUT}}\right)$$

where:
ΔI_{RIPPLE} = 0.7 A.
f_{SW} = 700 kHz.
ΔV_{RIPPLE} = 33 mV (1% of output voltage).

If ESR of the ceramic capacitor is 3 mΩ, then C_{OUT} = 4 µF.

Because the output capacitor is one of two external components that control the loop stability and according to the recommended external components in Table 11, choose two 47 µF capacitor with a 6.3 V voltage rating in this application.

RESISTIVE VOLTAGE DIVIDER SELECTION

The output feedback resistive voltage divider is

$$V_{OUT} = 0.800\ \text{V} \times \left(1 + \frac{R_{TOP}}{R_{BOT}}\right)$$

For the 3.3 V output voltage, choose R_{TOP} = 31.6 kΩ and R_{BOT} = 10.2 kΩ as the feedback resistive voltage divider according to the recommended values in Table 11.

The resistive voltage divider for the programmable V_{IN} start-up voltage is

$$V_{STARTUP} = \left(\frac{1.2\ \text{V}}{R_{EN2}} + 1.2\ \mu\text{A}\right) \times R_{EN1} + 1.2\ \text{V}$$

If $V_{STARTUP}$ = 7.8 V, choose R_{EN2} = 10.2 kΩ, and then calculate R_{EN1}, which, in this case, is 56 kΩ.

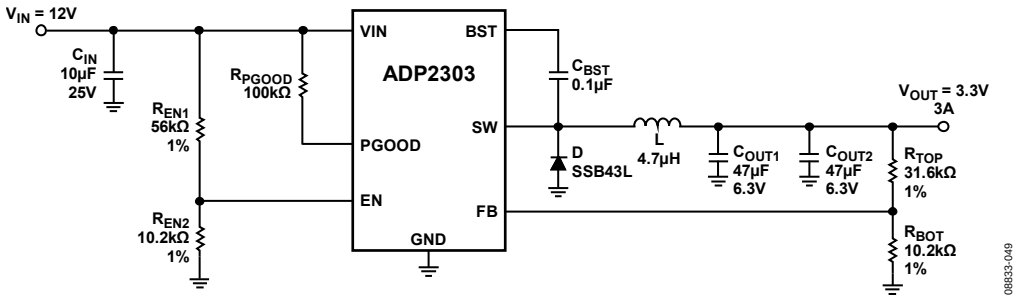

Figure 51. Schematic for the Design Example

Table 11. Recommended External Components for Typical Applications at 2 A/3 A Output Load

Part Number	V_{IN} (V)	V_{OUT} (V)	$I_{LOAD(max)}$ (A)	L (µH)	C_{OUT}	R_{TOP} (kΩ), ±1%	R_{BOT} (kΩ), ±1%
ADP2302	18	3.3	2	6.8	2 × 22 µF	31.6	10.2
	18	5.0	2	10	2 × 22 µF	52.3	10
	12	1.5	2	4.7	2 × 47 µF	10	11.3
	12	1.8	2	4.7	3 × 22 µF	12.7	10.2
	12	2.5	2	4.7	3 × 22 µF	21.5	10.2
	12	3.3	2	6.8	2 × 22 µF	31.6	10.2
	12	5.0	2	6.8	2 × 22 µF	52.3	10
	5	1.5	2	3.3	2 × 47 µF	10	11.3
	5	1.8	2	3.3	2 × 47 µF	12.7	10.2
	5	2.5	2	3.3	2 × 22 µF	21.5	10.2
ADP2303	18	3.3	3	4.7	2 × 47 µF	31.6	10.2
	18	5.0	3	6.8	47 µF	52.3	10
	12	1.5	3	2.5	3 × 47 µF	10	11.3
	12	1.8	3	3.3	3 × 47 µF	12.7	10.2
	12	2.5	3	3.3	2 × 47 µF	21.5	10.2
	12	3.3	3	4.7	2 × 47 µF	31.6	10.2
	12	5.0	3	4.7	47 µF	52.3	10
	5	1.5	3	2.2	3 × 47 µF	10	11.3
	5	1.8	3	2.2	3 × 47 µF	12.7	10.2
	5	2.5	3	2.2	3 × 47 µF	21.5	10.2

CIRCUIT BOARD LAYOUT RECOMMENDATIONS

Good circuit board layout is essential to obtaining the best performance for ADP2302/ADP2303. Poor layout can affect the regulation and stability, as well as the electromagnetic interface (EMI) and electromagnetic compatibility (EMC) performance. A PCB layout example is shown in Figure 53. Refer to the following guidelines for a good PCB layout:

- Place the input capacitor, the inductor, catch diode, output capacitor, and bootstrap capacitor close to the IC using short traces.
- Ensure that the high current loop traces are as short and wide as possible. The high current path is shown Figure 52.
- Maximize the size of ground metal on the component side to improve thermal dissipation.
- Use a ground plane with several vias connecting to the component side ground to further reduce noise on sensitive circuit nodes.
- Minimize the length of the FB trace connecting the top of the feedback resistive voltage divider to the output. In addition, keep these traces away from the high current traces and the switch node to avoid noise pickup.

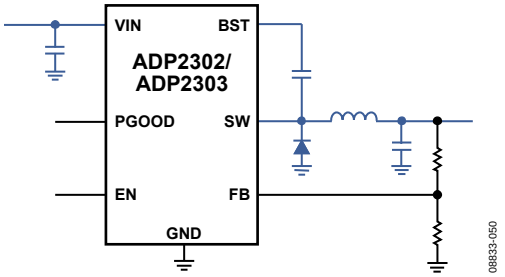

Figure 52. Typical Application Circuit with High Current Lines Shown in Blue

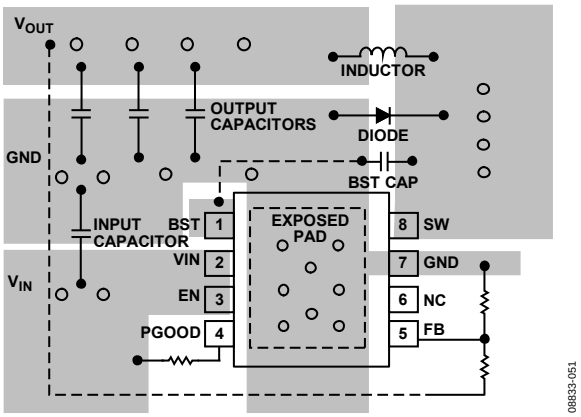

Figure 53. Recommended Layout for ADP2302/ADP2303

TYPICAL APPLICATION CIRCUITS

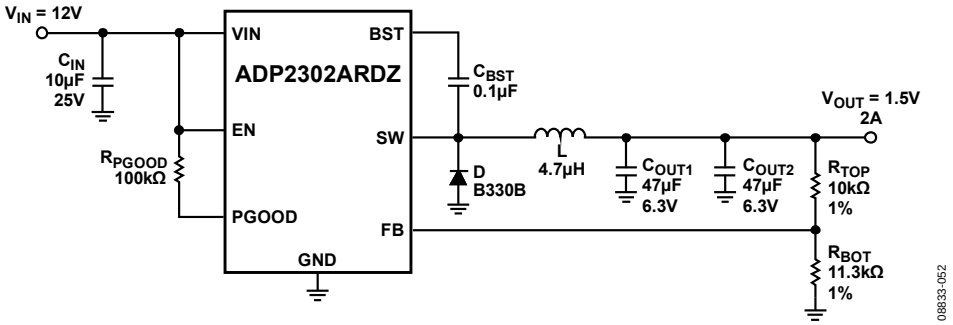

Figure 54. ADP2302 Typical Application, V_{IN} = 12 V, V_{OUT} = 1.5 V, 2 A

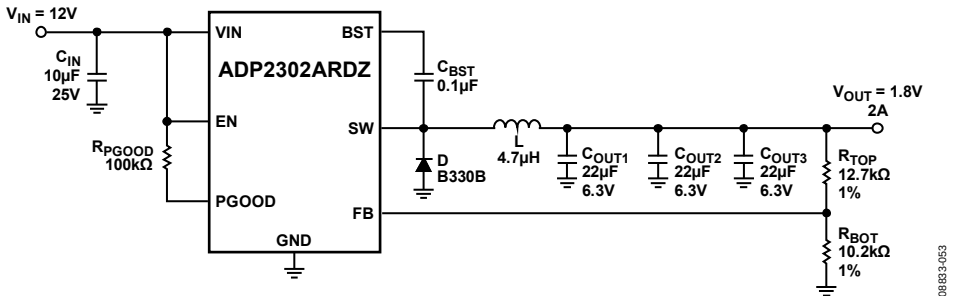

Figure 55. ADP2302 Typical Application, V_{IN} = 12 V, V_{OUT} = 1.8 V, 2 A

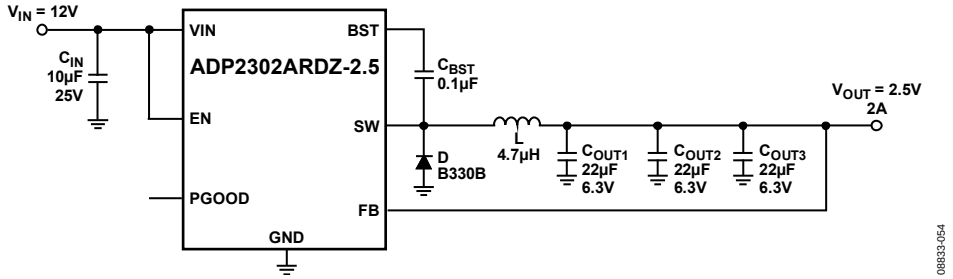

Figure 56. ADP2302 Typical Application, V_{IN} = 12 V, V_{OUT} = 2.5 V, 2 A

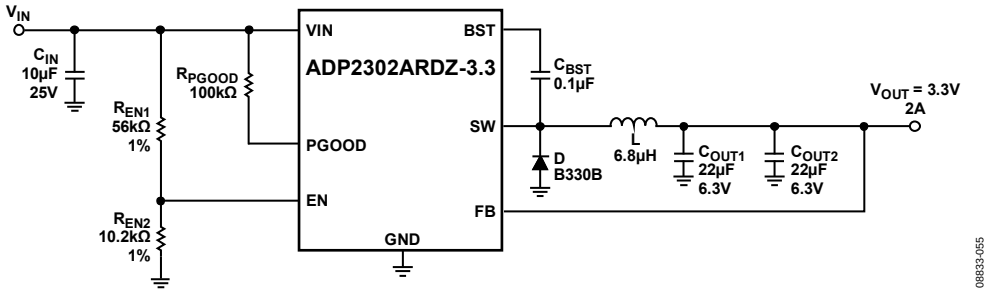

Figure 57. ADP2302 Typical Application, V_{IN} = 12 V, V_{OUT} = 3.3 V, 2 A, with Programmable 7.8 V UVLO

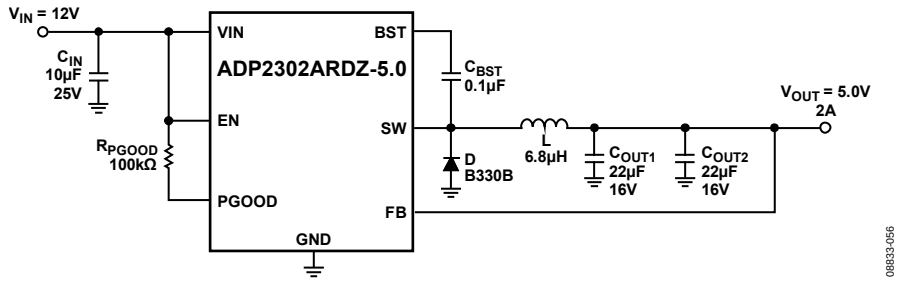

Figure 58. ADP2302 Typical Application, V_{IN} = 12 V, V_{OUT} = 5 V, 2 A

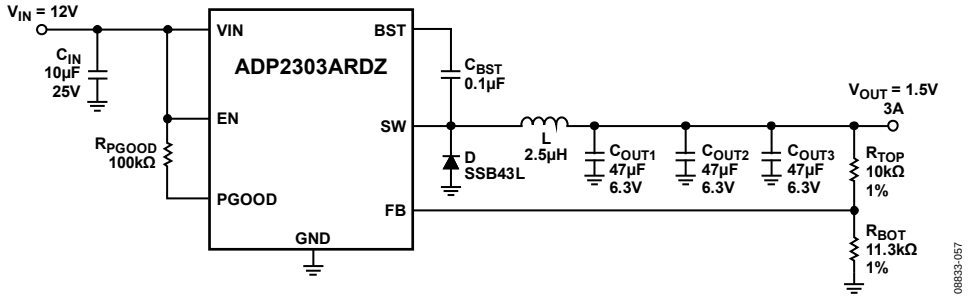

Figure 59. ADP2303 Typical Application, V_{IN} = 12 V, V_{OUT} = 1.5 V, 3 A

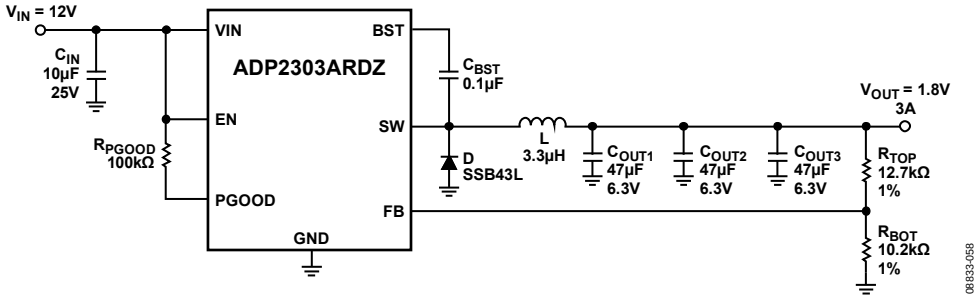

Figure 60. ADP2303 Typical Application, V_{IN} = 12 V, V_{OUT} = 1.8 V, 3 A

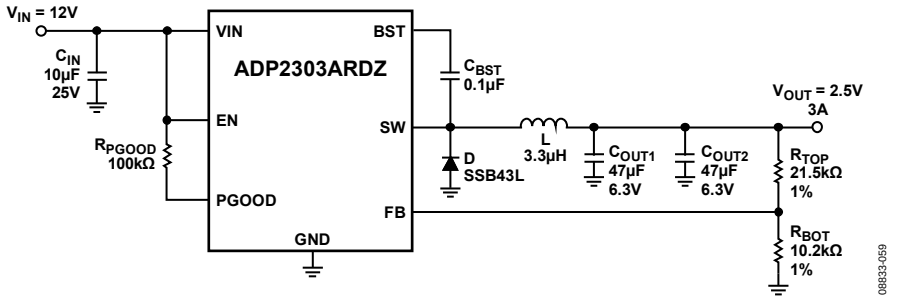

Figure 61. ADP2303 Typical Application, V_{IN} = 12 V, V_{OUT} = 2.5 V, 3 A

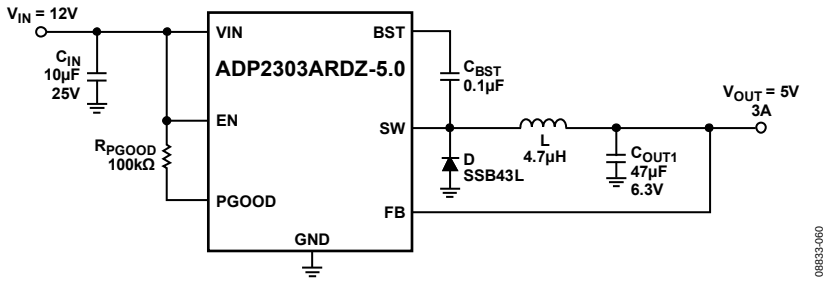

Figure 62. ADP2303 Typical Application, V_{IN} = 12 V, V_{OUT} = 5 V, 3 A

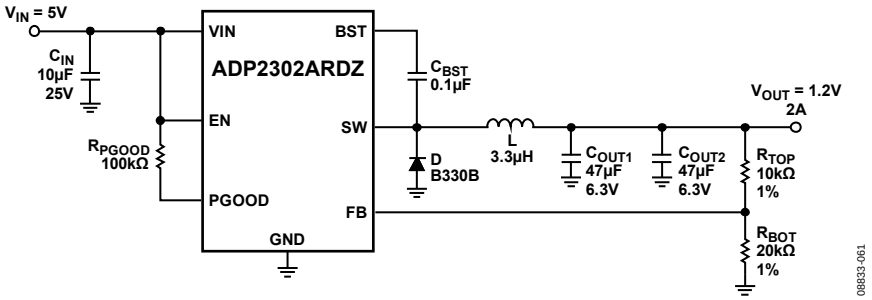

Figure 63. ADP2302 Typical Application, V_{IN} = 5V, V_{OUT} = 1.2 V, 2 A

OUTLINE DIMENSIONS

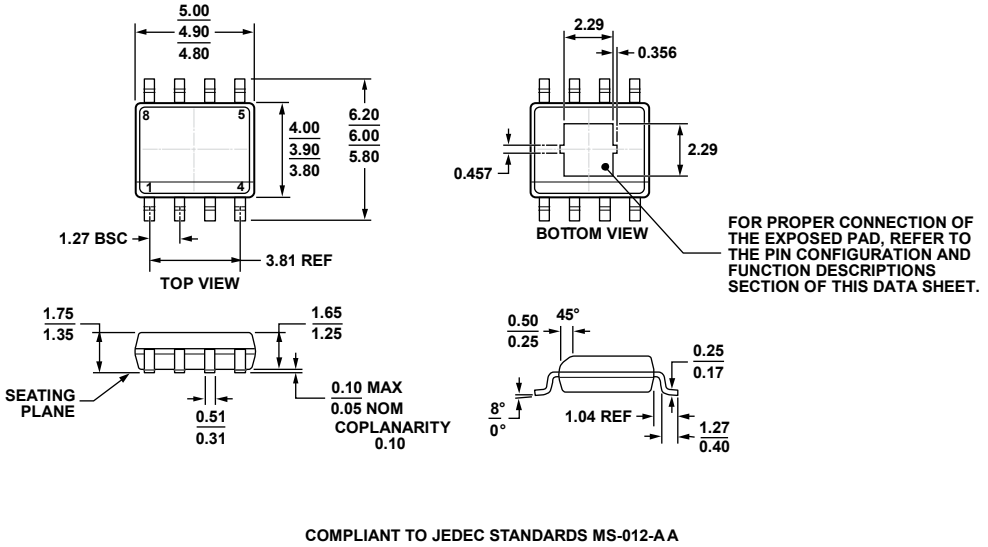

Figure 64. 8-Lead Standard Small Outline Package, with Exposed Pad [SOIC_N_EP]
Narrow Body
(RD-8-1)
Dimensions shown in millimeters

ORDERING GUIDE

Model[1]	Output Voltage	Temperature Range	Package Description	Package Option
ADP2302ARDZ	Adjustable	−40°C to +125°C	8-Lead SOIC_N_EP, Tube	RD-8-1
ADP2302ARDZ-2.5	2.5 V	−40°C to +125°C	8-Lead SOIC_N_EP, Tube	RD-8-1
ADP2302ARDZ-3.3	3.3 V	−40°C to +125°C	8-Lead SOIC_N_EP, Tube	RD-8-1
ADP2302ARDZ-5.0	5.0 V	−40°C to +125°C	8-Lead SOIC_N_EP, Tube	RD-8-1
ADP2302ARDZ-R7	Adjustable	−40°C to +125°C	8-Lead SOIC_N_EP, 7″ Tape and Reel	RD-8-1
ADP2302ARDZ-2.5-R7	2.5 V	−40°C to +125°C	8-Lead SOIC_N_EP, 7″ Tape and Reel	RD-8-1
ADP2302ARDZ-3.3-R7	3.3 V	−40°C to +125°C	8-Lead SOIC_N_EP, 7″ Tape and Reel	RD-8-1
ADP2302ARDZ-5.0-R7	5.0 V	−40°C to +125°C	8-Lead SOIC_N_EP, 7″ Tape and Reel	RD-8-1
ADP2302-EVALZ			Evaluation Board	
ADP2303ARDZ	Adjustable	−40°C to +125°C	8-Lead SOIC_N_EP, Tube	RD-8-1
ADP2303ARDZ-2.5	2.5 V	−40°C to +125°C	8-Lead SOIC_N_EP, Tube	RD-8-1
ADP2303ARDZ-3.3	3.3 V	−40°C to +125°C	8-Lead SOIC_N_EP, Tube	RD-8-1
ADP2303ARDZ-5.0	5.0 V	−40°C to +125°C	8-Lead SOIC_N_EP, Tube	RD-8-1
ADP2303ARDZ-R7	Adjustable	−40°C to +125°C	8-Lead SOIC_N_EP, 7″ Tape and Reel	RD-8-1
ADP2303ARDZ-2.5-R7	2.5 V	−40°C to +125°C	8-Lead SOIC_N_EP, 7″ Tape and Reel	RD-8-1
ADP2303ARDZ-3.3-R7	3.3 V	−40°C to +125°C	8-Lead SOIC_N_EP, 7″ Tape and Reel	RD-8-1
ADP2303ARDZ-5.0-R7	5.0 V	−40°C to +125°C	8-Lead SOIC_N_EP, 7″ Tape and Reel	RD-8-1
ADP2303-EVALZ			Evaluation Board	

[1] Z = RoHS Compliant Part.

NOTES

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D08833-0-6/12(A)