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# FDS89161LZ

## Dual N-Channel Shielded Gate PowerTrench<sup>®</sup> MOSFET 100 V, 2.7 A, 105 mΩ

### Features

- Shielded Gate MOSFET Technology
- Max  $r_{DS(on)}$  = 105 mΩ at  $V_{GS} = 10\text{ V}$ ,  $I_D = 2.7\text{ A}$
- Max  $r_{DS(on)}$  = 160 mΩ at  $V_{GS} = 4.5\text{ V}$ ,  $I_D = 2.1\text{ A}$
- High performance trench technology for extremely low  $r_{DS(on)}$
- High power and current handling capability in a widely used surface mount package
- CDM ESD protection level > 2KV typical (Note 4)
- 100% UIL Tested
- RoHS Compliant

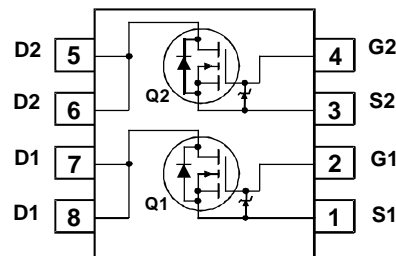
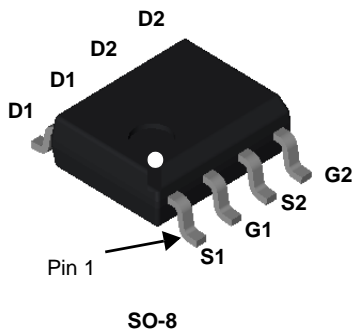


### General Description

This N-Channel logic Level MOSFETs are produced using Fairchild Semiconductor's advanced PowerTrench<sup>®</sup> process that incorporates Shielded Gate technology. This process has been optimized for the on-state resistance and yet maintain superior switching performance. G-S zener has been added to enhance ESD voltage level.

### Application

- DC-DC conversion



### MOSFET Maximum Ratings $T_A = 25\text{ °C}$ unless otherwise noted

Symbol	Parameter	Ratings	Units
$V_{DS}$	Drain to Source Voltage	100	V
$V_{GS}$	Gate to Source Voltage	$\pm 20$	V
$I_D$	Drain Current -Continuous	2.7	A
	-Pulsed	15	
$E_{AS}$	Single Pulse Avalanche Energy (Note 3)	13	mJ
$P_D$	Power Dissipation $T_C = 25\text{ °C}$	31	W
	Power Dissipation $T_A = 25\text{ °C}$ (Note 1a)	1.6	
$T_J, T_{STG}$	Operating and Storage Junction Temperature Range	-55 to +150	$^{\circ}\text{C}$

### Thermal Characteristics

$R_{\theta JC}$	Thermal Resistance, Junction to Case (Note 1)	40	$^{\circ}\text{C}/\text{W}$
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient (Note 1a)	78	

### Package Marking and Ordering Information

Device Marking	Device	Package	Reel Size	Tape Width	Quantity
FDS89161LZ	FDS89161LZ	SO-8	13"	12 mm	2500 units

## Electrical Characteristics $T_J = 25^\circ\text{C}$ unless otherwise noted

Symbol	Parameter	Test Conditions	Min	Typ	Max	Units
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### Off Characteristics

$BV_{DSS}$	Drain to Source Breakdown Voltage	$I_D = 250 \mu\text{A}, V_{GS} = 0 \text{ V}$	100			V
$\frac{\Delta BV_{DSS}}{\Delta T_J}$	Breakdown Voltage Temperature Coefficient	$I_D = 250 \mu\text{A}$ , referenced to $25^\circ\text{C}$		68		mV/°C
$I_{DSS}$	Zero Gate Voltage Drain Current	$V_{DS} = 80 \text{ V}, V_{GS} = 0 \text{ V}$			1	$\mu\text{A}$
$I_{GSS}$	Gate to Source Leakage Current	$V_{GS} = \pm 20 \text{ V}, V_{DS} = 0 \text{ V}$			$\pm 10$	$\mu\text{A}$

### On Characteristics

$V_{GS(th)}$	Gate to Source Threshold Voltage	$V_{GS} = V_{DS}, I_D = 250 \mu\text{A}$	1	1.7	2.2	V
$\frac{\Delta V_{GS(th)}}{\Delta T_J}$	Gate to Source Threshold Voltage Temperature Coefficient	$I_D = 250 \mu\text{A}$ , referenced to $25^\circ\text{C}$		-6		mV/°C
$r_{DS(on)}$	Static Drain to Source On Resistance	$V_{GS} = 10 \text{ V}, I_D = 2.7 \text{ A}$		81	105	m $\Omega$
		$V_{GS} = 4.5 \text{ V}, I_D = 2.1 \text{ A}$		110	160	
		$V_{GS} = 10 \text{ V}, I_D = 2.7 \text{ A}, T_J = 125^\circ\text{C}$		140	182	
$g_{FS}$	Forward Transconductance	$V_{DS} = 10 \text{ V}, I_D = 2.7 \text{ A}$		7.8		S

### Dynamic Characteristics

$C_{iss}$	Input Capacitance	$V_{DS} = 50 \text{ V}, V_{GS} = 0 \text{ V}, f = 1\text{MHz}$		227	302	pF
$C_{oss}$	Output Capacitance			44	58	pF
$C_{rss}$	Reverse Transfer Capacitance			3	4	pF
$R_g$	Gate Resistance			0.9		$\Omega$

### Switching Characteristics

$t_{d(on)}$	Turn-On Delay Time	$V_{DD} = 50 \text{ V}, I_D = 2.7 \text{ A}, V_{GS} = 10 \text{ V}, R_{GEN} = 6 \Omega$		3.8	10	ns	
$t_r$	Rise Time			1.2	10	ns	
$t_{d(off)}$	Turn-Off Delay Time			9.5	17	ns	
$t_f$	Fall Time			1.6	10	ns	
$Q_{g(TOT)}$	Total Gate Charge		$V_{GS} = 0 \text{ V to } 10 \text{ V}$		3.8	5.3	nC
$Q_{g(TOT)}$	Total Gate Charge	$V_{GS} = 0 \text{ V to } 5 \text{ V}$	$V_{DD} = 50 \text{ V}, I_D = 2.7 \text{ A}$		2.1	2.9	nC
$Q_{gs}$	Gate to Source Charge				0.7		nC
$Q_{gd}$	Gate to Drain "Miller" Charge				0.7		nC

### Drain-Source Diode Characteristics

$V_{SD}$	Source to Drain Diode Forward Voltage	$V_{GS} = 0 \text{ V}, I_S = 2.7 \text{ A}$ (Note 2)		0.8	1.3	V
		$V_{GS} = 0 \text{ V}, I_S = 2 \text{ A}$ (Note 2)		0.8	1.2	
$t_{rr}$	Reverse Recovery Time	$I_F = 2.7 \text{ A}, di/dt = 100 \text{ A}/\mu\text{s}$		31	56	ns
$Q_{rr}$	Reverse Recovery Charge			20	36	nC

#### NOTES:

1.  $R_{\theta JA}$  is determined with the device mounted on a  $1 \text{ in}^2$  pad 2 oz copper pad on a  $1.5 \times 1.5 \text{ in.}$  board of FR-4 material.  $R_{\theta JC}$  is guaranteed by design while  $R_{\theta CA}$  is determined by the user's board design.



a)  $78^\circ\text{C}/\text{W}$  when mounted on a  $1 \text{ in}^2$  pad of 2 oz copper



b)  $135^\circ\text{C}/\text{W}$  when mounted on a minimum pad

2. Pulse Test: Pulse Width  $< 300 \mu\text{s}$ , Duty cycle  $< 2.0\%$ .

3. Starting  $T_J = 25^\circ\text{C}$ ,  $L = 0.3 \text{ mH}$ ,  $I_{AS} = 25 \text{ A}$ ,  $V_{DD} = 27 \text{ V}$ ,  $V_{GS} = 10 \text{ V}$ .

4. The diode connected between gate and source serves only as protection against ESD. No gate overvoltage rating is implied.

**Typical Characteristics ( N-Channel)**  $T_J = 25^\circ\text{C}$  unless otherwise noted

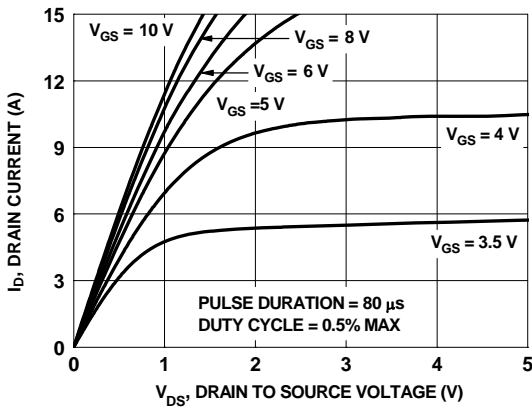


Figure 1. On-Region Characteristics

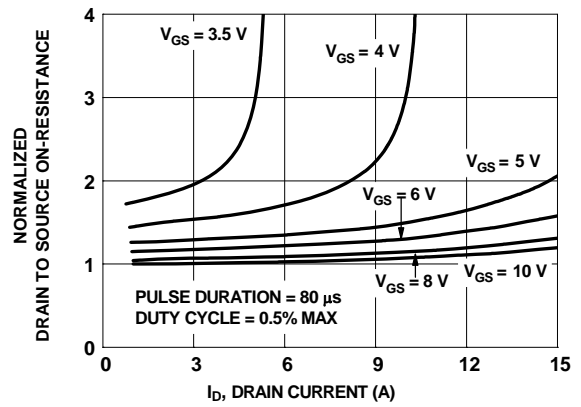


Figure 2. Normalized On-Resistance vs Drain Current and Gate Voltage

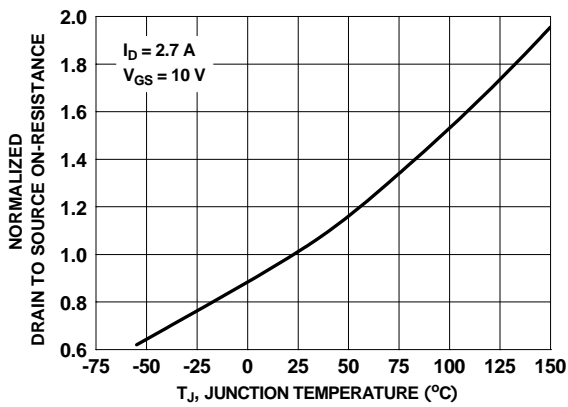


Figure 3. Normalized On-Resistance vs Junction Temperature

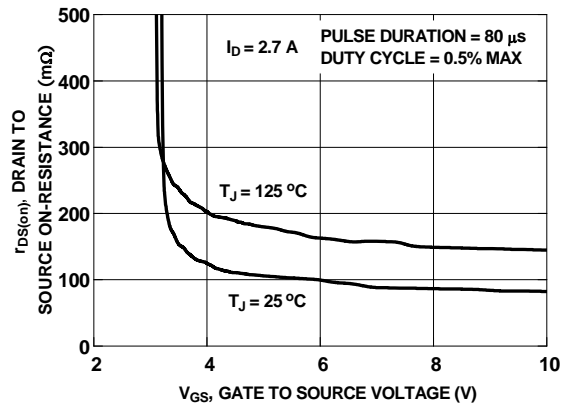


Figure 4. On-Resistance vs Gate to Source Voltage

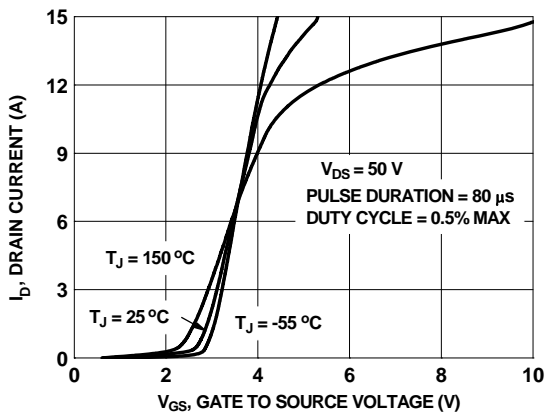


Figure 5. Transfer Characteristics

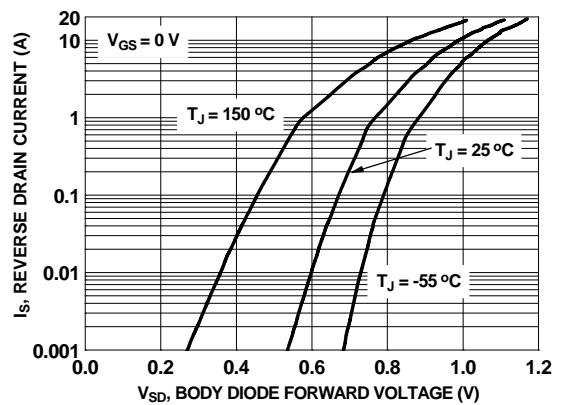
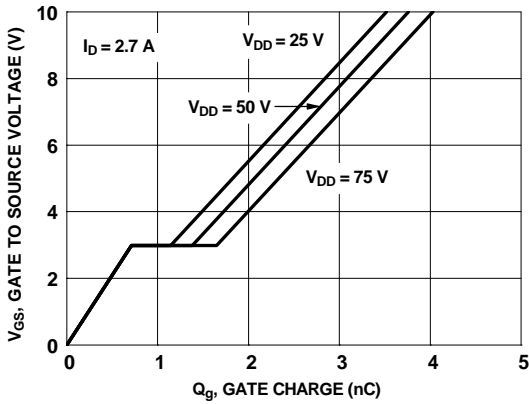
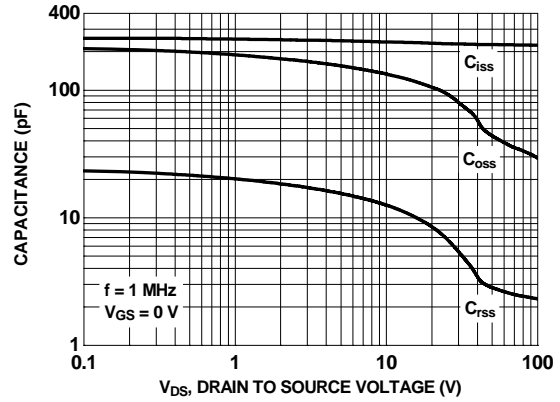


Figure 6. Source to Drain Diode Forward Voltage vs Source Current

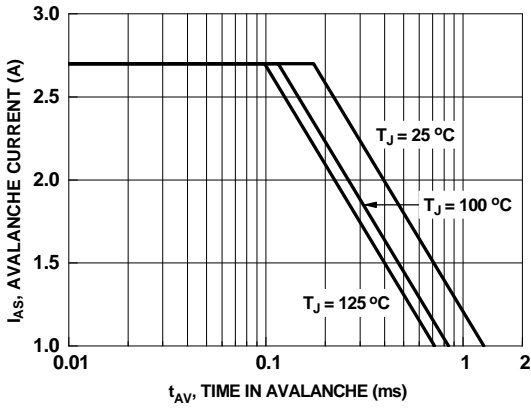
**Typical Characteristics ( N-Channel)**  $T_J = 25^\circ\text{C}$  unless otherwise noted



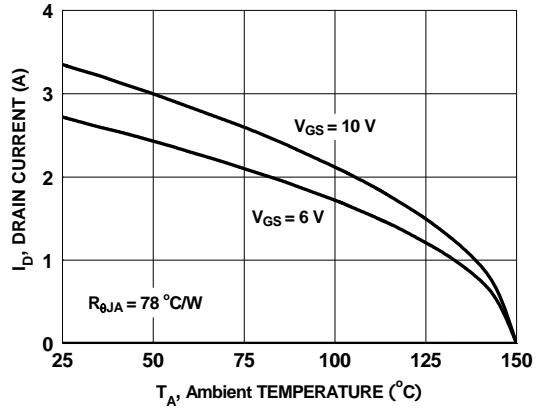
**Figure 7. Gate Charge Characteristics**



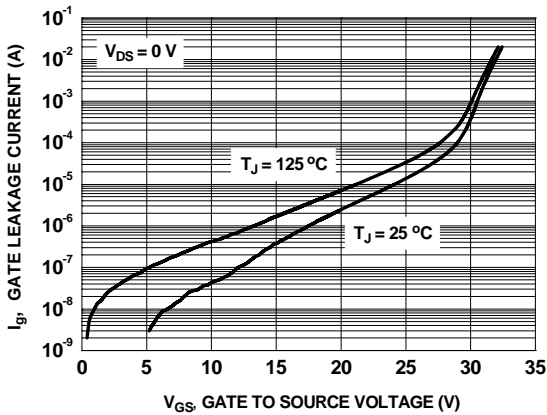
**Figure 8. Capacitance vs Drain to Source Voltage**



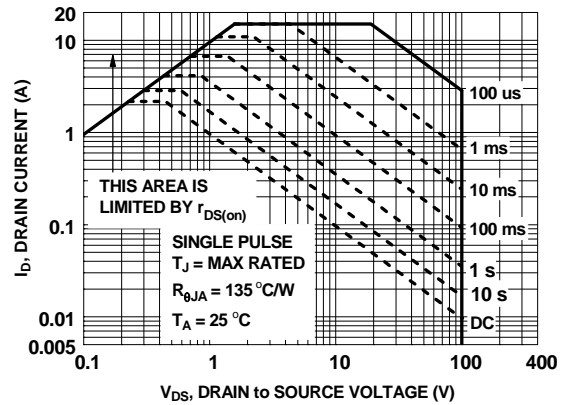
**Figure 9. Unclamped Inductive Switching Capability**



**Figure 10. Maximum Continuous Drain Current vs Ambient Temperature**

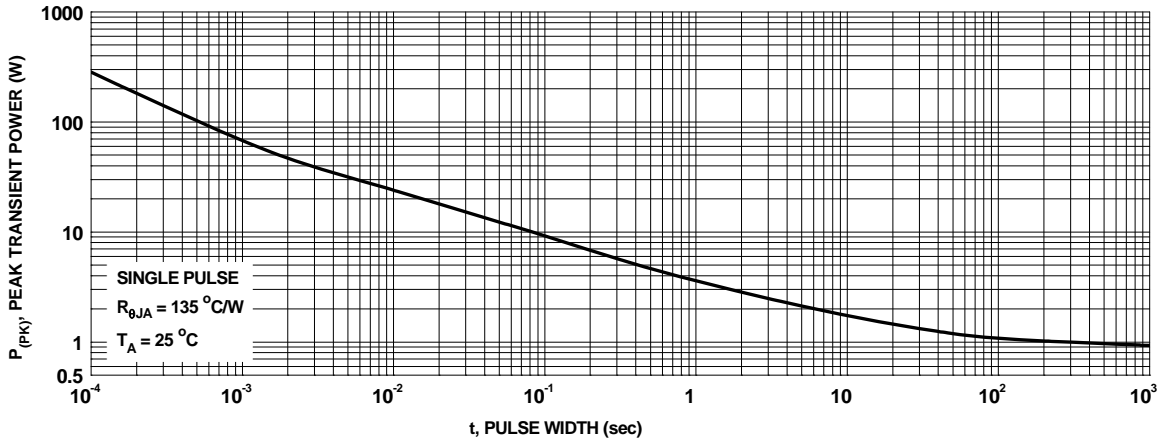


**Figure 11. Gate Leakage Current vs Gate to Source Voltage**

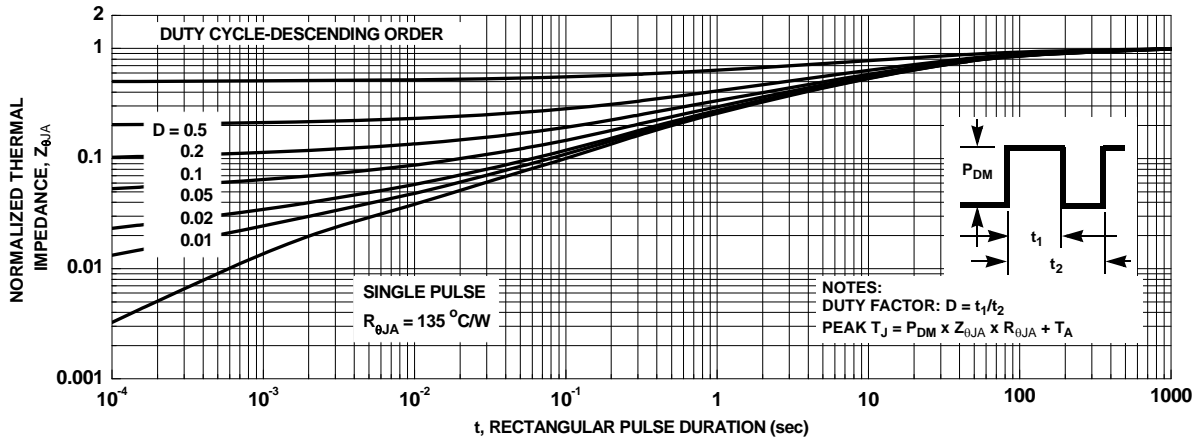


**Figure 12. Forward Bias Safe Operating Area**

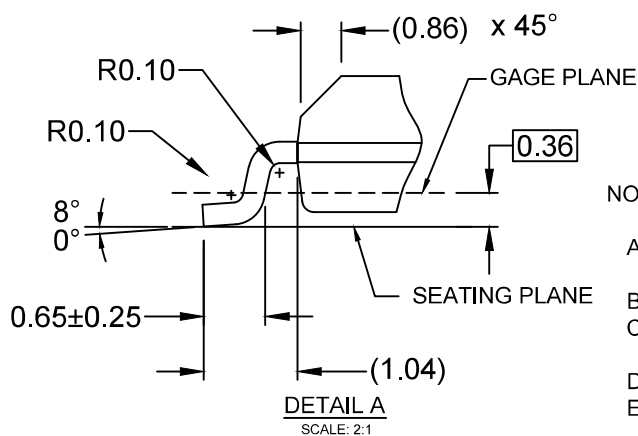
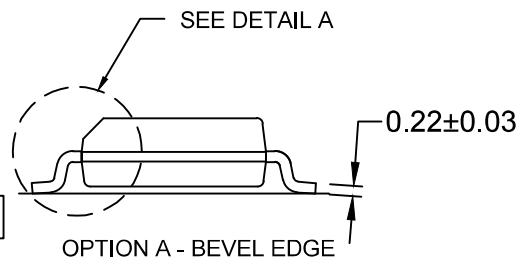
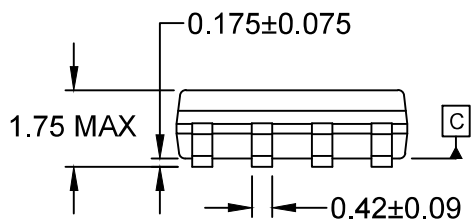
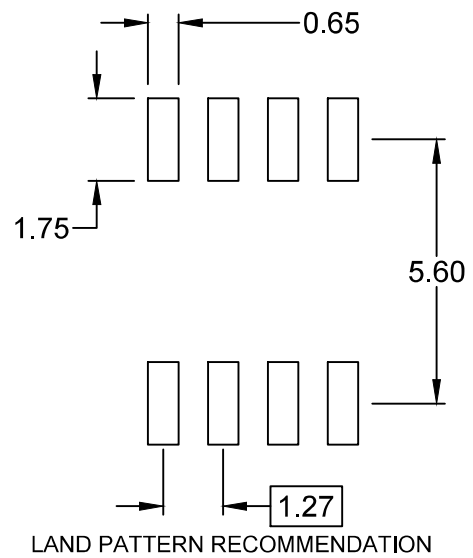
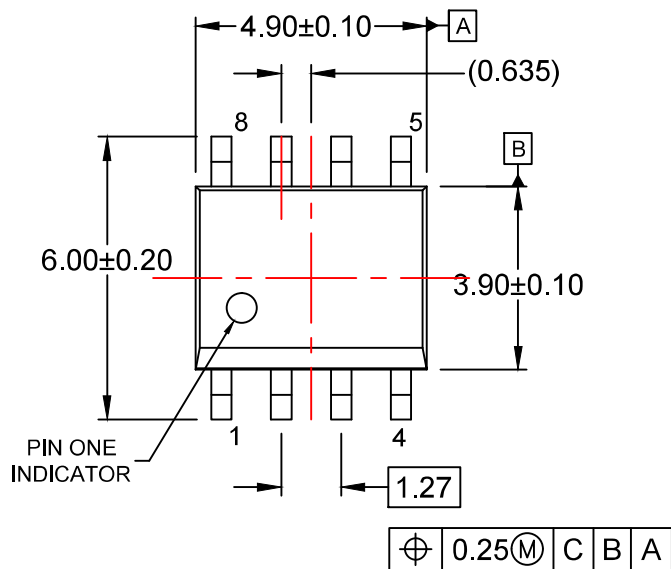
**Typical Characteristics ( N-Channel)**  $T_J = 25^\circ\text{C}$  unless otherwise noted



**Figure 13. Single Pulse Maximum Power Dissipation**



**Figure 14. Junction-to-Ambient Transient Thermal Response Curve**



NOTES:

- A) THIS PACKAGE CONFORMS TO JEDEC MS-012, VARIATION AA.
- B) ALL DIMENSIONS ARE IN MILLIMETERS.
- C) DIMENSIONS DO NOT INCLUDE MOLD FLASH OR BURRS.
- D) LANDPATTERN STANDARD: SOIC127P600X175-8M
- E) DRAWING FILENAME: M08Arev16



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