

FEATURES

- <0.5 pC charge injection over full signal range
- Off capacitance: 2 pF
- Off leakage: 2 pA
- Supply range: 33 V
- On resistance: 120 Ω
- Fully specified at ±15 V, +12 V
- No V_L supply required
- 3 V logic-compatible inputs
- Rail-to-rail operation
- 10-lead MSOP package

APPLICATIONS

- Automatic test equipment
- Data acquisition systems
- Battery-powered systems
- Sample-and-hold systems
- Audio signal routing
- Video signal routing
- Communication systems

GENERAL DESCRIPTION

The ADG1221/ADG1222/ADG1223 are monolithic, complementary metal-oxide semiconductor (CMOS) devices containing four independently selectable switches designed on an *i*CMOS (industrial CMOS) process. *i*CMOS is a modular manufacturing process combining high voltage CMOS and bipolar technologies. It enables the development of a wide range of high performance analog ICs, capable of 33 V operation, in a footprint that no previous generation of high voltage parts has been able to achieve. Unlike analog ICs using conventional CMOS processes, *i*CMOS components can tolerate high supply voltages while providing increased performance, dramatically lower power consumption, and reduced package size.

The ultralow capacitance and exceptionally low charge injection of these switches make them ideal solutions for data acquisition and sample-and-hold applications, where low glitch and fast settling are required. Figure 2 shows that there is minimum charge injection over the full signal range of the device.

The ADG1221/ADG1222/ADG1223 contain two independent single-pole/single-throw (SPST) switches. The ADG1221 and ADG1222 differ only in that the digital control logic is inverted. The ADG1221 switches are turned on with Logic 1 on the appropriate control input, and Logic 0 is required for the

FUNCTIONAL BLOCK DIAGRAM

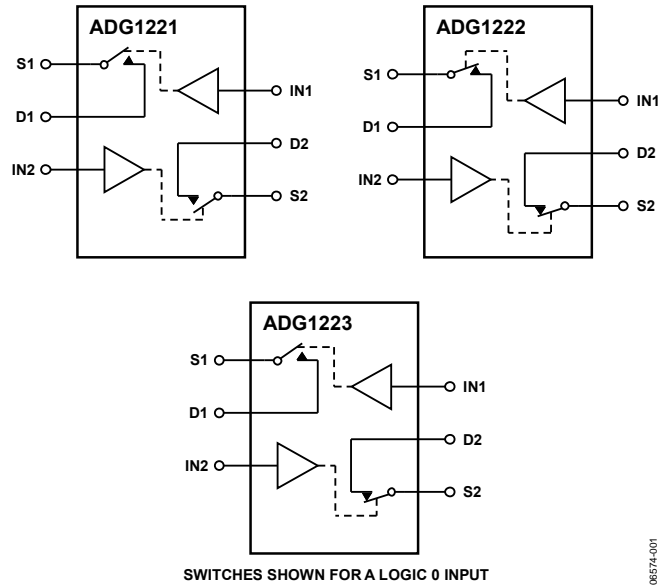


Figure 1.

ADG1222. The ADG1223 has one switch with digital control logic similar to that of the ADG1221; the logic is inverted on the other switch. The ADG1223 exhibits break-before-make switching action for use in multiplexer applications. Each switch conducts equally well in both directions when on and has an input signal range that extends to the supplies. In the off condition, signal levels up to the supplies are blocked.

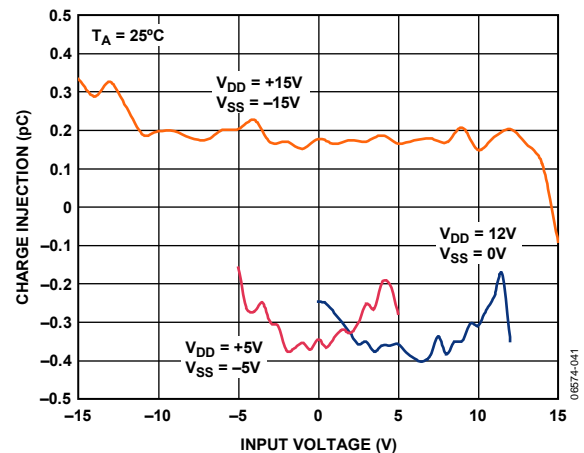


Figure 2. Charge Injection vs. Input Voltage

Rev. B

Document Feedback

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REVISION HISTORY

9/2017—Rev. A to Rev. B

| | |
|----------------------------------|---|
| Change to Features Section | 1 |
|----------------------------------|---|

3/2009—Rev. 0 to Rev. A

| | |
|--|---|
| Changes to Power Requirements, I _{DD} , Digital Inputs = 5 V Parameter, Table 1..... | 4 |
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2/2007—Rev. 0: Initial Version

SPECIFICATIONS

DUAL SUPPLY

$V_{DD} = 15\text{ V} \pm 10\%$, $V_{SS} = -15\text{ V} \pm 10\%$, GND = 0 V, unless otherwise noted.

Table 1.

| Parameter | Temperature | | | Unit | Test Conditions/Comments |
|---|--------------------------|----------------|----------------------|--|--|
| | 25°C | -40°C to +85°C | -40°C to +125°C | | |
| ANALOG SWITCH | | | | | |
| Analog Signal Range | | | V_{DD} to V_{SS} | V | $V_{DD} = +13.5\text{ V}$, $V_{SS} = -13.5\text{ V}$, $V_S = \pm 10\text{ V}$, $I_S = -1\text{ mA}$ (see Figure 23) |
| On Resistance, R_{ON} | 120 200 | 240 | 270 | Ω typ Ω max | |
| On Resistance Match Between Channels, ΔR_{ON} | 2.5 6 | 10 | 12 | Ω typ Ω max | $V_S = \pm 10\text{ V}$, $I_S = -1\text{ mA}$ |
| On Resistance Flatness, $R_{FLAT(ON)}$ | 20 64 | 76 | 83 | Ω typ Ω max | $V_S = -5\text{ V}/0\text{ V}/+5\text{ V}$; $I_S = -1\text{ mA}$ |
| LEAKAGE CURRENTS | | | | | |
| Source Off Leakage, I_S (Off) | ± 0.002 ± 0.1 | ± 0.6 | ± 1 | nA typ nA max | $V_{DD} = +16.5\text{ V}$, $V_{SS} = -16.5\text{ V}$ $V_S = \pm 10\text{ V}$, $V_D = \pm 10\text{ V}$ (see Figure 24) |
| Drain Off Leakage, I_D (Off) | ± 0.002 ± 0.1 | ± 0.6 | ± 1 | nA typ nA max | $V_S = \pm 10\text{ V}$, $V_D = \pm 10\text{ V}$ (see Figure 24) |
| Channel On Leakage, I_D , I_S (On) | ± 0.01 ± 0.2 | ± 0.6 | ± 1 | nA typ nA max | $V_S = V_D = \pm 10\text{ V}$ (see Figure 25) |
| DIGITAL INPUTS | | | | | |
| Input High Voltage, V_{INH} | | | 2.0 | V min | $V_{IN} = V_{INL}$ or V_{INH} |
| Input Low Voltage, V_{INL} | | | 0.8 | V max | |
| Input Current, I_{INL} or I_{INH} | 0.005 | | ± 0.1 | μA typ μA max | |
| Digital Input Capacitance, C_{IN} | 2.5 | | | pF typ | |
| DYNAMIC CHARACTERISTICS¹ | | | | | |
| t_{ON} | 130 170 | 210 | 240 | ns typ ns max | $R_L = 300\ \Omega$, $C_L = 35\text{ pF}$, $V_S = 10\text{ V}$ (see Figure 26) |
| t_{OFF} | 85 105 | 130 | 140 | ns typ ns max | $R_L = 300\ \Omega$, $C_L = 35\text{ pF}$, $V_S = 10\text{ V}$ (see Figure 26) |
| Break-Before-Make Time Delay (ADG1223 Only), t_{BBM} | 40 | | | ns typ | $R_L = 300\ \Omega$, $C_L = 35\text{ pF}$, $V_{S1} = V_{S2} = 10\text{ V}$ (see Figure 27) |
| Charge Injection, Q_{INJ} | 0.1 | | 10 | ns min | $V_S = 0\text{ V}$, $R_S = 0\ \Omega$, $C_L = 1\text{ nF}$ (see Figure 28) |
| Off Isolation | 75 | | | pC typ dB typ | $R_L = 50\ \Omega$, $C_L = 1\text{ pF}$, $f = 1\text{ MHz}$ (see Figure 29) |

| Parameter | Temperature | | | Unit | Test Conditions/Comments |
|--|-------------|----------------|------------------|-------------------|---|
| | 25°C | -40°C to +85°C | -40°C to +125°C | | |
| Channel-to-Channel Crosstalk | 90 | | | dB typ | $R_L = 50 \Omega$, $C_L = 1 \text{ pF}$, $f = 1 \text{ MHz}$ (see Figure 30) |
| Total Harmonic Distortion + Noise, THD + N | 0.15 | | | % typ | $R_L = 10 \text{ k}\Omega$, 5 V rms, $f = 20 \text{ Hz}$ to 20 kHz |
| -3 dB Bandwidth | 960 | | | MHz typ | $R_L = 50 \Omega$, $C_L = 1 \text{ pF}$ (see Figure 31) |
| C_S (Off) | 1.7 | | | pF typ | $V_S = 0 \text{ V}$, $f = 1 \text{ MHz}$ |
| | 2.2 | | | pF max | |
| C_D (Off) | 1.7 | | | pF typ | $V_S = 0 \text{ V}$, $f = 1 \text{ MHz}$ |
| | 2.2 | | | pF max | |
| C_D, C_S (On) | 3 | | | pF typ | $V_S = 0 \text{ V}$, $f = 1 \text{ MHz}$ |
| | 4 | | | pF max | |
| POWER REQUIREMENTS | | | | | $V_{DD} = +16.5 \text{ V}$, $V_{SS} = -16.5 \text{ V}$ |
| I_{DD} | 0.001 | | 1.0 | μA typ | Digital inputs = 0 V or V_{DD} |
| | 140 | | 190 | μA max | Digital inputs = 0 V or V_{DD} |
| | | | | μA typ | Digital inputs = 5 V |
| | | | | μA max | Digital inputs = 5 V |
| I_{SS} | 0.001 | | 1.0 | μA typ | Digital inputs = 0 V, 5 V, or V_{DD} |
| | | | | μA max | |
| V_{DD}/V_{SS} | | | $\pm 5/\pm 16.5$ | V min/max | GND = 0 V |

¹ Guaranteed by design, not subject to production test.

SINGLE SUPPLY

$V_{DD} = 12 \text{ V} \pm 10\%$, $V_{SS} = 0 \text{ V}$, GND = 0 V, unless otherwise noted.

Table 2.

| Parameter | Temperature | | | Unit | Test Conditions/Comments |
|---|-------------|----------------|-----------------|--------------|--|
| | 25°C | -40°C to +85°C | -40°C to +125°C | | |
| ANALOG SWITCH | | | | | |
| Analog Signal Range | | | 0 V to V_{DD} | V | $V_{DD} = 10.8 \text{ V}$, $V_{SS} = 0 \text{ V}$, $V_S = 0 \text{ V}$ to 10 V, $I_S = -1 \text{ mA}$ (see Figure 23) |
| On Resistance, R_{ON} | 300 | | | Ω typ | |
| | 475 | 567 | 625 | Ω max | $V_S = 0 \text{ V}$ to 10 V, $I_S = -1 \text{ mA}$ |
| On Resistance Match Between Channels, ΔR_{ON} | 4.5 | | | Ω typ | |
| | 16 | 26 | 27 | Ω max | |
| On Resistance Flatness, $R_{FLAT(ON)}$ | 60 | | | Ω typ | $V_S = 3 \text{ V}/6 \text{ V}/9 \text{ V}$, $I_S = -1 \text{ mA}$ |
| LEAKAGE CURRENTS | | | | | |
| Source Off Leakage, I_S (Off) | ± 0.002 | | | nA typ | $V_{DD} = 13.2 \text{ V}$, $V_{SS} = 0 \text{ V}$ $V_S = 1 \text{ V}/10 \text{ V}$, $V_D = 10 \text{ V}/1 \text{ V}$ (see Figure 24) |
| | ± 0.1 | ± 0.6 | ± 1 | nA max | |

| Parameter | Temperature | | | Unit | Test Conditions/Comments |
|---|----------------|----------------|-----------------|------------------|---|
| | 25°C | -40°C to +85°C | -40°C to +125°C | | |
| Drain Off Leakage, I_D (Off) | ±0.002 ±0.1 | ±0.6 | ±1 | nA typ nA max | $V_S = 1\text{ V}/10\text{ V}, V_D = 10\text{ V}/1\text{ V}$ (see Figure 24) |
| Channel On Leakage, I_D, I_S (On) | ±0.01 ±0.2 | ±0.6 | ±1 | nA typ nA max | $V_S = V_D = 1\text{ V}$ or 10 V (see Figure 25) |
| DIGITAL INPUTS | | | | | |
| Input High Voltage, V_{INH} | | | 2.0 | V min | $V_{IN} = V_{INL}$ or V_{INH} |
| Input Low Voltage, V_{INL} | | | 0.8 | V max | |
| Input Current, I_{INL} or I_{INH} | 0.001 | | ±0.1 | µA typ µA max | |
| Digital Input Capacitance, C_{IN} | 3 | | | pF typ | |
| DYNAMIC CHARACTERISTICS ¹ | | | | | |
| t_{ON} | 190 250 | 300 | 345 | ns typ ns max | $R_L = 300\ \Omega, C_L = 35\text{ pF}, V_S = 8\text{ V}$ (see Figure 26) |
| t_{OFF} | 120 150 | 190 | 225 | ns typ ns max | $R_L = 300\ \Omega, C_L = 35\text{ pF}, V_S = 8\text{ V}$ (see Figure 26) |
| Break-Before-Make Time Delay (ADG1223 Only), t_{BBM} | 70 | | 10 | ns typ ns min | $R_L = 300\ \Omega, C_L = 35\text{ pF}, V_{S1} = V_{S2} = 8\text{ V}$ (see Figure 27) |
| Charge Injection, Q_{INJ} | 0.2 | | | pC typ | $V_S = 6\text{ V}, R_S = 0\ \Omega, C_L = 1\text{ nF}$ (see Figure 28) |
| Off Isolation | 75 | | | dB typ | $R_L = 50\ \Omega, C_L = 1\text{ pF}, f = 1\text{ MHz}$ (see Figure 29) |
| Channel-to-Channel Crosstalk | 90 | | | dB typ | $R_L = 50\ \Omega, C_L = 1\text{ pF}, f = 1\text{ MHz}$ (see Figure 30) |
| -3 dB Bandwidth C_S (Off) | 550 | | | MHz typ | $R_L = 50\ \Omega, C_L = 1\text{ pF}$ (see Figure 31) $V_S = 6\text{ V}, f = 1\text{ MHz}$ |
| C_D (Off) | 2.1 2.6 | | | pF typ pF max | $V_S = 6\text{ V}, f = 1\text{ MHz}$ |
| C_D, C_S (On) | 2.1 2.6 | | | pF typ pF max | $V_S = 6\text{ V}, f = 1\text{ MHz}$ |
| C_D, C_S (On) | 3.8 4.6 | | | pF typ pF max | $V_S = 6\text{ V}, f = 1\text{ MHz}$ |
| POWER REQUIREMENTS | | | | | $V_{DD} = 13.2\text{ V}$ |
| I_{DD} | 0.001 | | 1.0 | µA typ µA max | Digital inputs = 0 V or V_{DD} Digital inputs = 0 V or V_{DD} |
| | 140 | | 190 | µA typ µA max | Digital inputs = 5 V Digital inputs = 5 V |
| V_{DD} | | | 5/16.5 | V min/max | $V_{SS} = 0\text{ V}, GND = 0\text{ V}$ |

¹ Guaranteed by design, not subject to production test.

ABSOLUTE MAXIMUM RATINGS

$T_A = 25^\circ\text{C}$, unless otherwise noted.

Table 3.

| Parameter | Rating |
|---|--|
| V_{DD} to V_{SS} | 35 V |
| V_{DD} to GND | -0.3 V to +25 V |
| V_{SS} to GND | +0.3 V to -25 V |
| Analog Inputs ¹ | $V_{SS} - 0.3\text{ V}$ to $V_{DD} + 0.3\text{ V}$ or 30 mA, whichever occurs first |
| Digital Inputs ¹ | GND - 0.3 V to $V_{DD} + 0.3\text{ V}$ or 30 mA, whichever occurs first |
| Peak Current, S or D | 100 mA (pulsed at 1 ms, 10% duty cycle max) |
| Continuous Current per Channel, S or D | 30 mA |
| Operating Temperature Range | -40°C to +125°C |
| Storage Temperature Range | -65°C to +150°C |
| Junction Temperature | 150°C |
| Reflow Soldering Peak Temperature, Pb free | 260°C |

¹ Overvoltages at IN, S, or D are clamped by internal diodes. Current must be limited to the maximum ratings given.

Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

THERMAL RESISTANCE

θ_{JA} is specified for the worst-case conditions, that is, a device soldered in a circuit board for surface-mount packages.

Table 4. Thermal Resistance

| Package Type | θ_{JA} | θ_{JC} | Unit |
|------------------------------|---------------|---------------|------|
| 10-Lead MSOP (4-Layer Board) | 206 | 44 | °C/W |

ESD CAUTION



ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

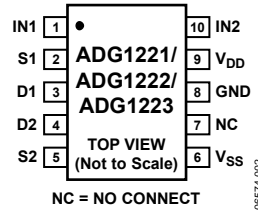


Figure 3. 10-Lead MSOP Pin Configuration

Table 5. Pin Function Descriptions

| Pin No. | Mnemonic | Description |
|---------|-----------------|---|
| 1 | IN1 | Logic Control Input. |
| 2 | S1 | Source Terminal. Can be an input or output. |
| 3 | D1 | Drain Terminal. Can be an input or output. |
| 4 | D2 | Drain Terminal. Can be an input or output. |
| 5 | S2 | Source Terminal. Can be an input or output. |
| 6 | V _{SS} | Most Negative Power Supply Potential. |
| 7 | NC | No Connect. |
| 8 | GND | Ground (0 V) Reference. |
| 9 | V _{DD} | Most Positive Power Supply Potential. |
| 10 | IN2 | Logic Control Input. |

Table 6. ADG1221/ADG1222 Truth Table

| ADG1221 INx | ADG1222 INx | Switch Condition |
|-------------|-------------|------------------|
| 1 | 0 | On |
| 0 | 1 | Off |

Table 7. ADG1223 Truth Table

| ADG1223 INx | Switch 1 Condition | Switch 2 Condition |
|-------------|--------------------|--------------------|
| 0 | Off | On |
| 1 | On | Off |

TERMINOLOGY

I_{DD}

The positive supply current.

I_{SS}

The negative supply current.

V_D (V_S)

The analog voltage on Terminal D and Terminal S.

R_{ON}

The ohmic resistance between Terminal D and Terminal S.

$R_{FLAT(ON)}$

Flatness is defined as the difference between the maximum and minimum value of on resistance, as measured over the specified analog signal range.

I_S (Off)

The source leakage current with the switch off.

I_D (Off)

The drain leakage current with the switch off.

I_D, I_S (On)

The channel leakage current with the switch on.

V_{INL}

The maximum input voltage for Logic 0.

V_{INH}

The minimum input voltage for Logic 1.

I_{INL} (I_{INH})

The input current of the digital input.

C_S (Off)

The off switch source capacitance, measured with reference to ground.

C_D (Off)

The off switch drain capacitance, measured with reference to ground.

C_D, C_S (On)

The on switch capacitance, measured with reference to ground.

C_{IN}

The digital input capacitance.

t_{ON}

The delay between applying the digital control input and the output switching on (see Figure 26).

t_{OFF}

The delay between applying the digital control input and the output switching off (see Figure 26).

t_{BBM}

Off time or on time measured between the 90% points of both switches, when switching from one address state to another (ADG1223 only).

Q_{INJ} (Charge Injection)

A measure of the glitch impulse transferred from the digital input to the analog output during switching.

Off Isolation

A measure of unwanted signal coupling through an off switch.

Crosstalk

A measure of unwanted signal that is coupled through from one channel to another as a result of parasitic capacitance.

-3 dB Bandwidth

The frequency at which the output is attenuated by 3 dB.

On Response

The frequency response of the on switch.

Insertion Loss

The loss due to the on resistance of the switch.

THD + N (Total Harmonic Noise Plus Distortion)

The ratio of the harmonic amplitude plus noise of the signal to the fundamental.

ACPSRR (AC Power Supply Rejection Ratio)

Measures the ability of a part to avoid coupling noise and spurious signals that appear on the supply voltage pin to the output of the switch. The dc voltage on the device is modulated by a sine wave of 0.62 V p-p. The ratio of the amplitude of signal on the output to the amplitude of the modulation is the ACPSRR.

TYPICAL PERFORMANCE CHARACTERISTICS

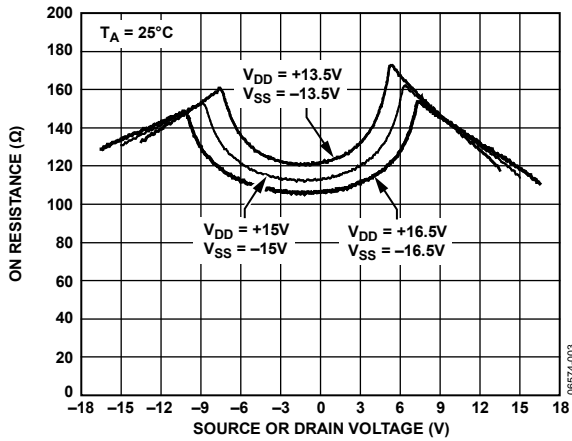


Figure 4. On Resistance as a Function of V_S (V_D), Dual Supply

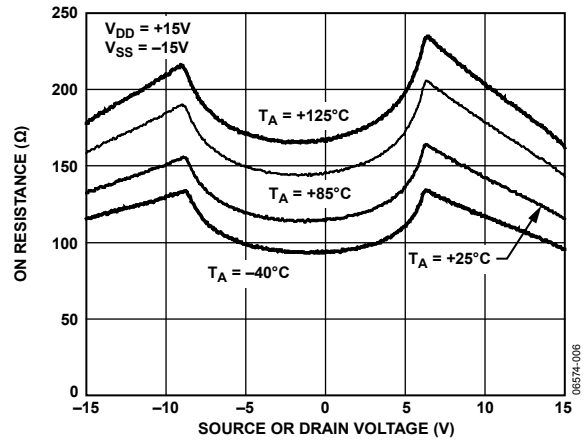


Figure 7. On Resistance as a Function of V_S (V_D) for Different Temperatures, Dual Supply

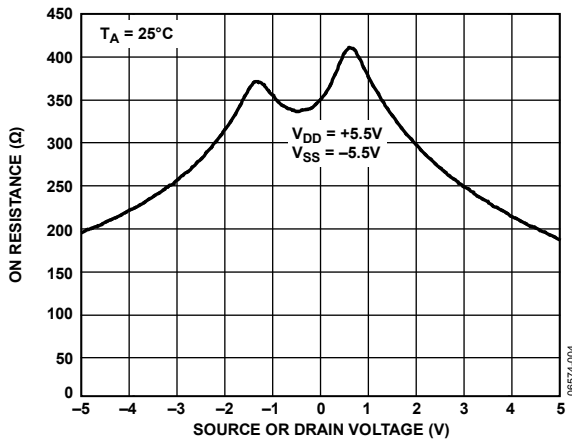


Figure 5. On Resistance as a Function of V_S (V_D), Dual Supply

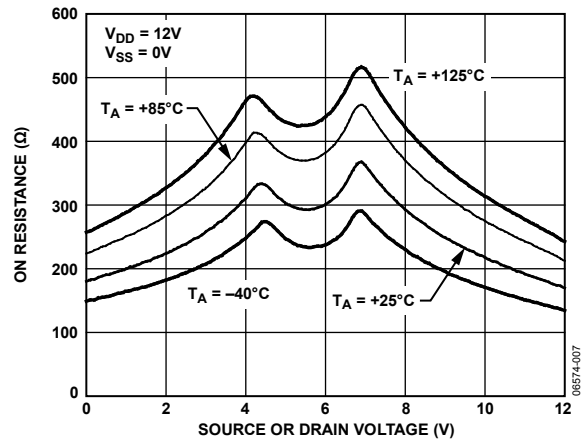


Figure 8. On Resistance as a Function of V_S (V_D) for Different Temperatures, Single Supply

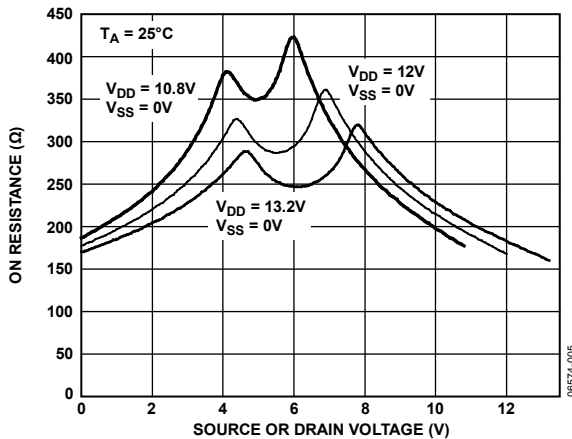


Figure 6. On Resistance as a Function of V_S (V_D), Single Supply

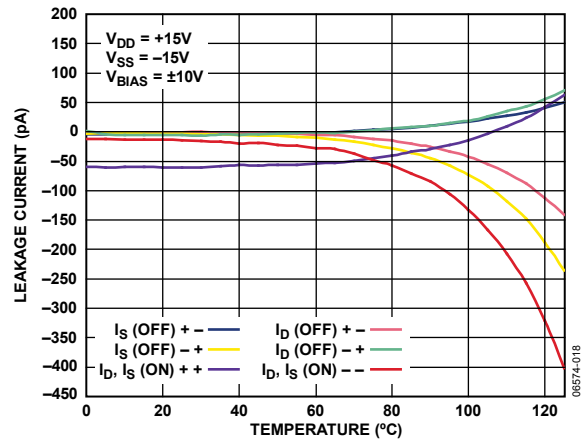


Figure 9. Leakage Current as a Function of Temperature, Dual Supply

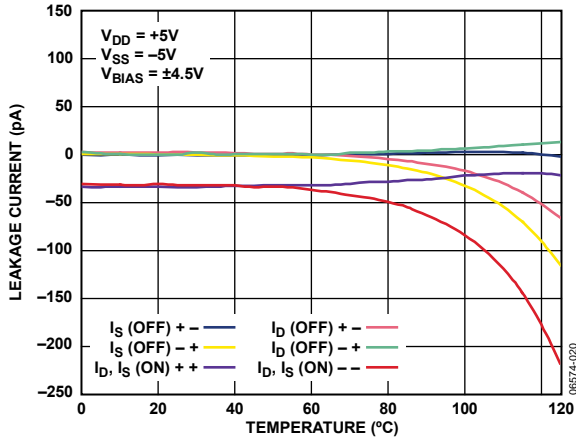


Figure 10. Leakage Current as a Function of Temperature, Dual Supply

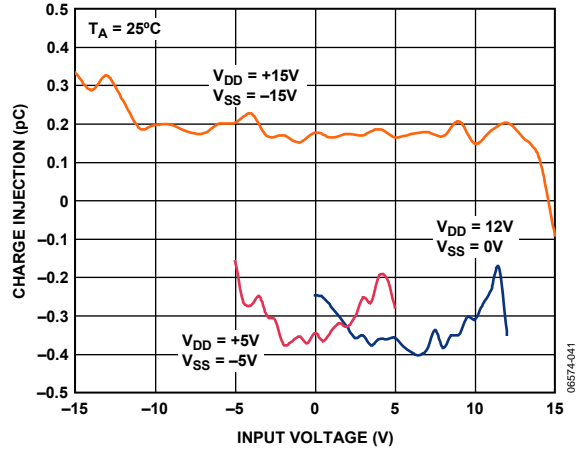


Figure 13. Charge Injection vs. Input Voltage

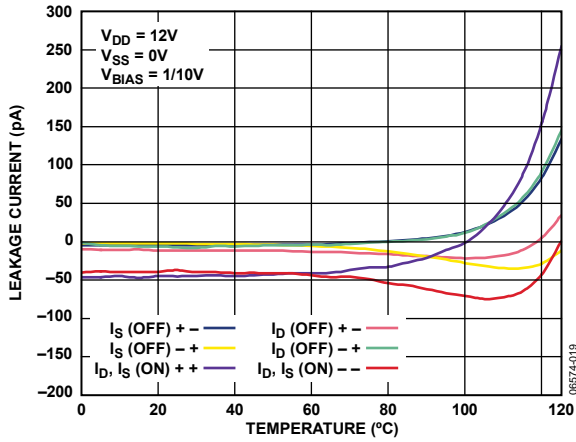


Figure 11. Leakage Current as a Function of Temperature, Single Supply

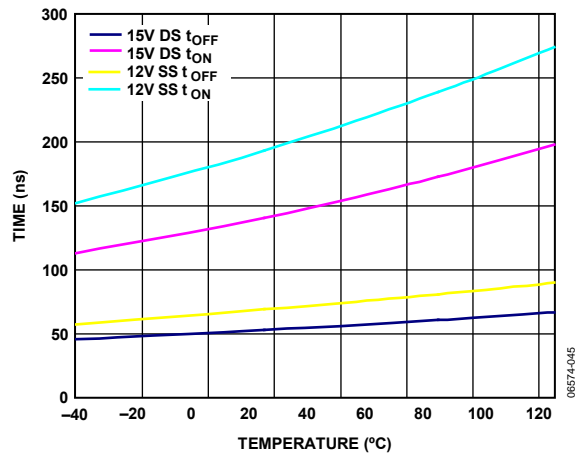


Figure 14. t_{ON}/t_{OFF} vs. Temperature

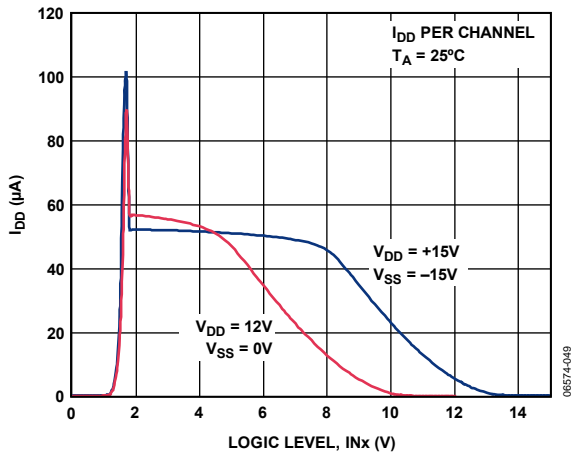


Figure 12. I_{DD} vs. Logic Level

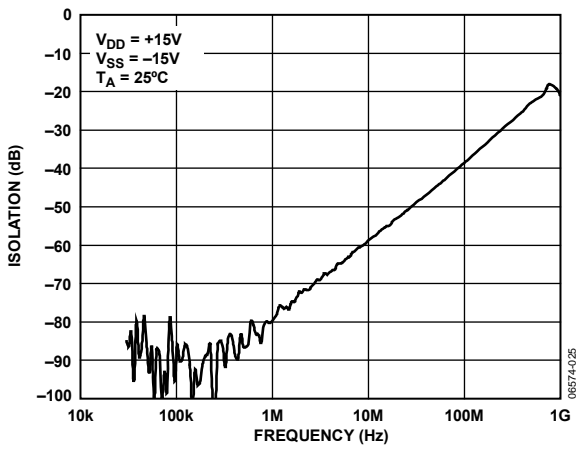


Figure 15. Off Isolation vs. Frequency

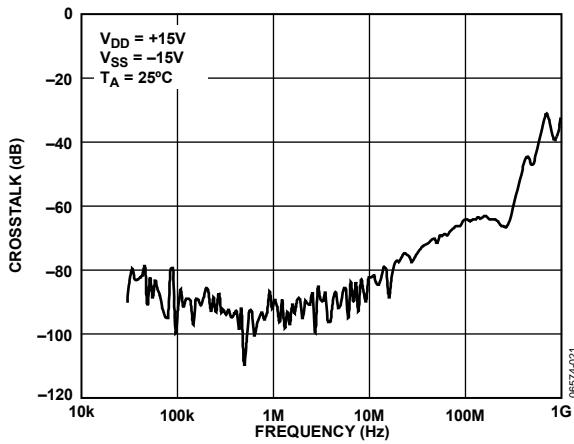


Figure 16. Crosstalk vs. Frequency

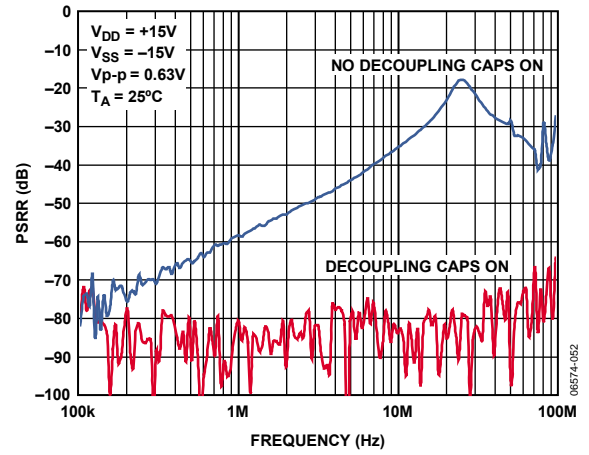


Figure 18. ACPSRR vs. Frequency

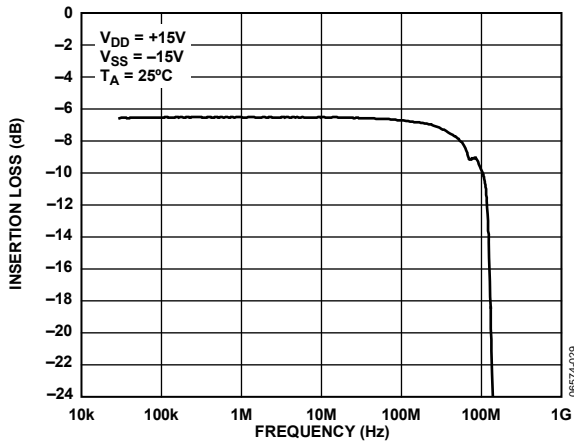


Figure 17. Insertion Loss vs. Frequency

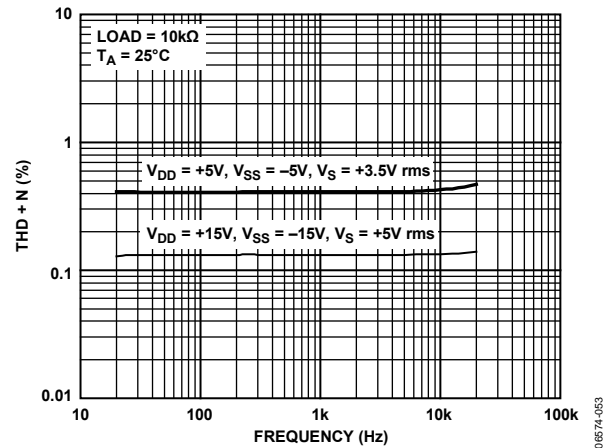


Figure 19. THD + N vs. Frequency

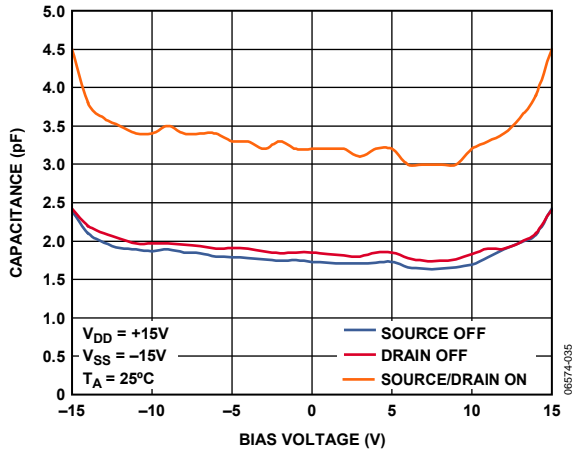


Figure 20. Capacitance vs. Bias Voltage

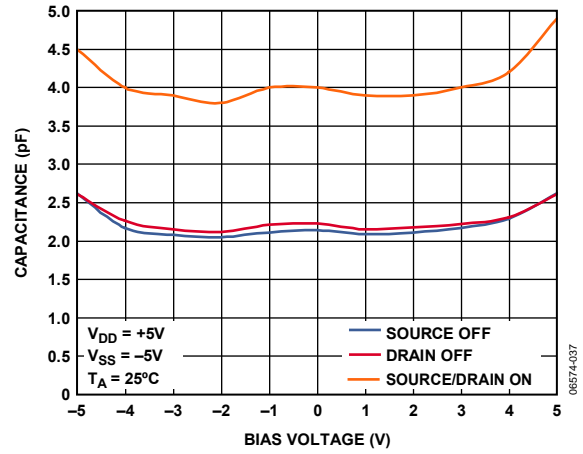


Figure 22. Capacitance vs. Bias Voltage

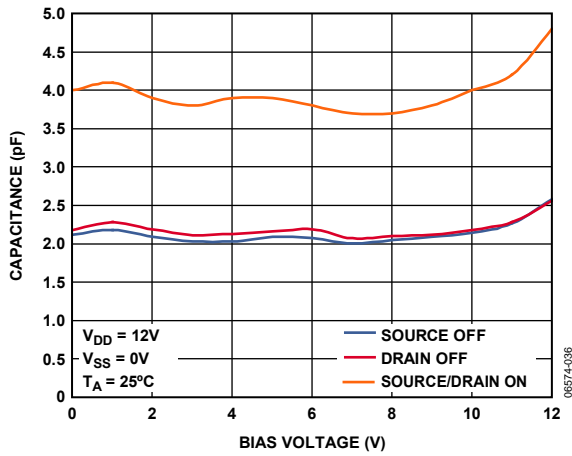


Figure 21. Capacitance vs. Bias Voltage

TEST CIRCUITS

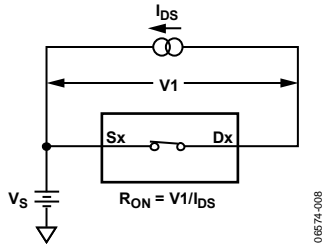


Figure 23. Test Circuit 1—On Resistance

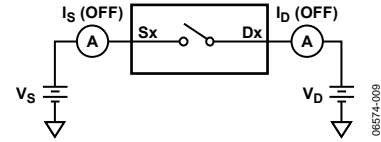


Figure 24. Test Circuit 2—Off Leakage

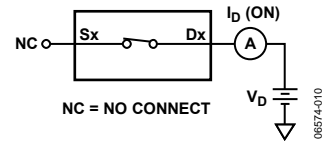


Figure 25. Test Circuit 3—On Leakage

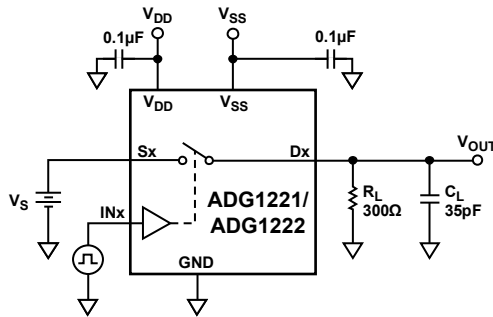


Figure 26. Test Circuit 4—Switching Times

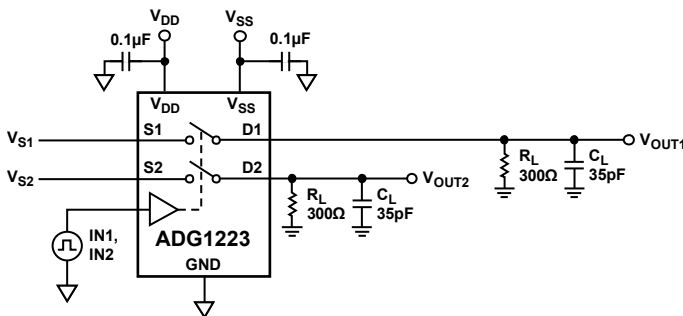
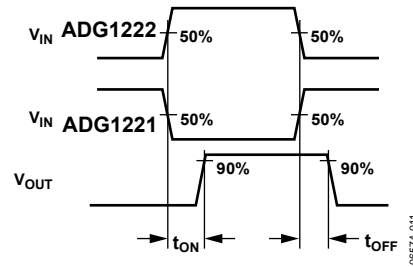


Figure 27. Test Circuit 5—Break-Before-Make Time Delay

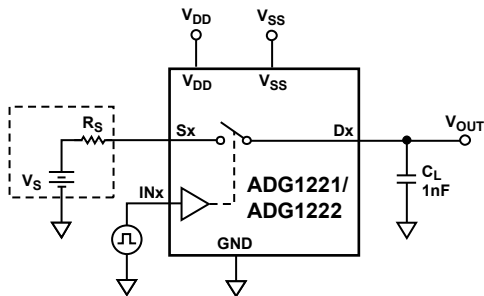
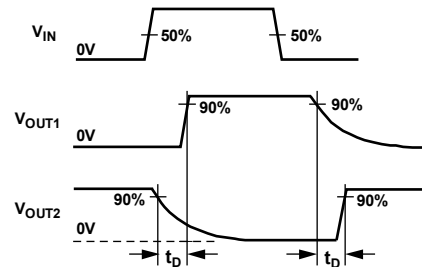
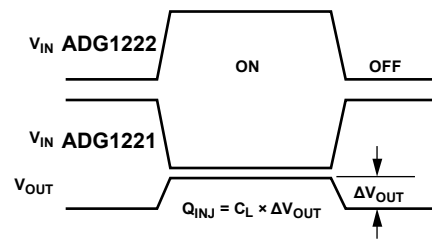


Figure 28. Test Circuit 6—Charge Injection



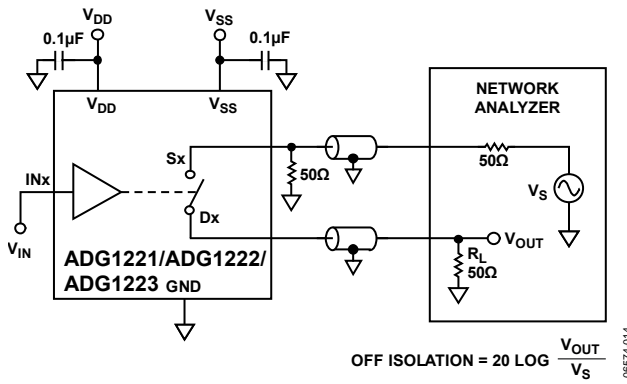


Figure 29. Test Circuit 7—Off Isolation

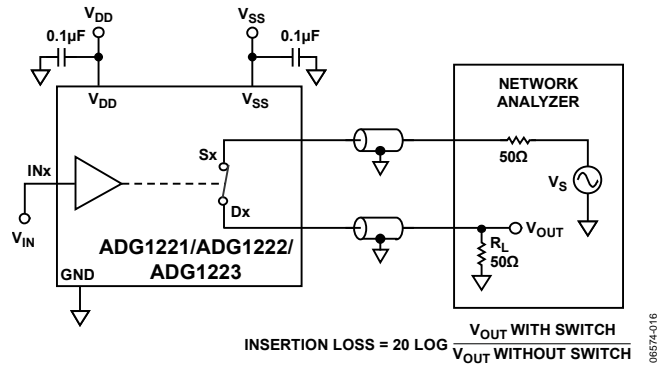


Figure 31. Test Circuit 9—Bandwidth

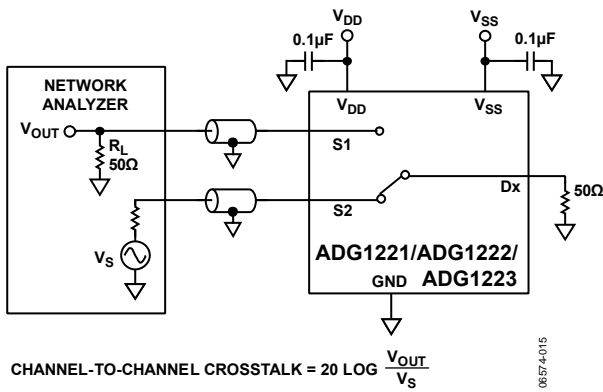


Figure 30. Test Circuit 8—Channel-to-Channel Crosstalk

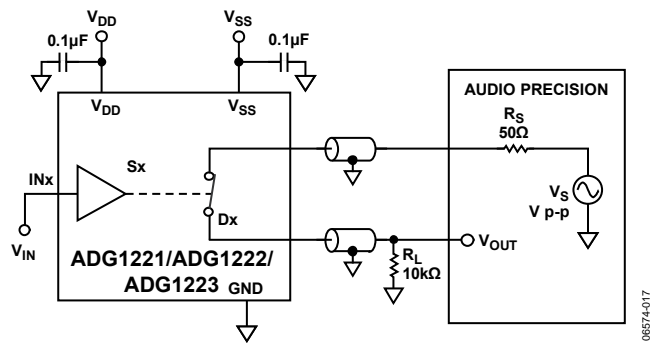
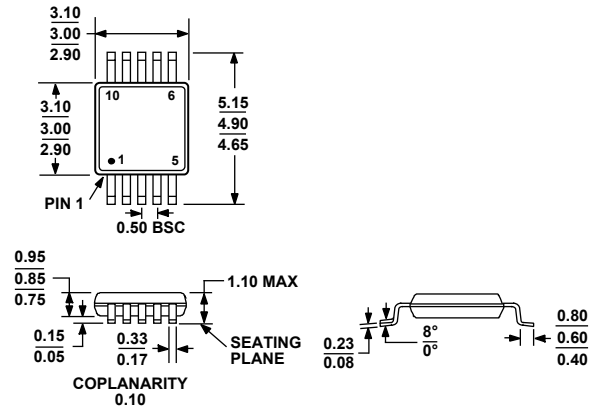


Figure 32. Test Circuit 10—Total Harmonic Distortion + Noise

OUTLINE DIMENSIONS



COMPLIANT TO JEDEC STANDARDS MO-187-BA

Figure 33. 10-Lead Mini Small Outline Package [MSOP] (RM-10)

Dimensions shown in millimeters

ORDERING GUIDE

| Model ¹ | Temperature Range | Package Description | Package Option | Branding |
|--------------------|-------------------|---|----------------|----------|
| ADG1221BRMZ | -40°C to +125°C | 10-Lead Mini Small Outline Package (MSOP) | RM-10 | S27 |
| ADG1221BRMZ-REEL7 | -40°C to +125°C | 10-Lead Mini Small Outline Package (MSOP) | RM-10 | S27 |
| ADG1222BRMZ | -40°C to +125°C | 10-Lead Mini Small Outline Package (MSOP) | RM-10 | S28 |
| ADG1222BRMZ-REEL7 | -40°C to +125°C | 10-Lead Mini Small Outline Package (MSOP) | RM-10 | S28 |
| ADG1223BRMZ | -40°C to +125°C | 10-Lead Mini Small Outline Package (MSOP) | RM-10 | S2J |
| ADG1223BRMZ-REEL7 | -40°C to +125°C | 10-Lead Mini Small Outline Package (MSOP) | RM-10 | S2J |

¹ Z = Pb-free part.

NOTES