

## 8K-256K SPI Serial EEPROM High Temp Family Data Sheet

### Features:

- Max. Clock 5 MHz
- Low-power CMOS Technology:
  - Max. Write Current: 5 mA at 5.5V, 5 MHz
  - Read Current: 5 mA at 5.5V, 5 MHz
  - Standby Current: 10  $\mu$ A at 5.5V
- 1024 x 8 through 32768 x 8-bit Organization
- Byte and Page-level Write Operations
- Self-timed Erase and Write Cycles (6 ms max.)
- Block Write Protection:
  - Protect none, 1/4, 1/2 or all of array
- Built-in Write Protection:
  - Power-on/off data protection circuitry
  - Write enable latch
  - Write-protect pin
- Sequential Read
- High Reliability:
  - Endurance: >100K erase/write cycles
  - Data retention: > 200 years
  - ESD protection: > 4000V
- Temperature Range Supported:
  - Extended (H): -40°C to +150°C
- Package is Pb-free and Halogen free

### Pin Function Table

Name	Function
$\overline{\text{CS}}$	Chip Select Input
SO	Serial Data Output
$\overline{\text{WP}}$	Write-Protect
Vss	Ground
SI	Serial Data Input
SCK	Serial Clock Input
$\overline{\text{HOLD}}$	Hold Input
Vcc	Supply Voltage

### Description:

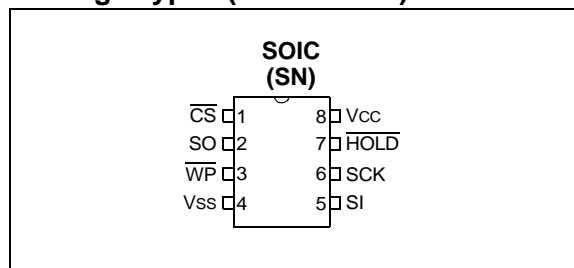
Microchip Technology Inc. 25LCXXX\* devices are Mid-density 8 through 256 Kbit Serial Electrically Erasable PROMs (EEPROM). The devices are organized in blocks of x8-bit memory and support the Serial Peripheral Interface (SPI) compatible serial bus architecture. Byte-level and page-level functions are supported.

The bus signals required are a clock input (SCK) plus separate data in (SI) and data out (SO) lines. Access to the device is controlled through a Chip Select ( $\overline{\text{CS}}$ ) input.

Communication to the device can be paused via the hold pin (HOLD). While the device is paused, transitions on its inputs will be ignored, with the exception of Chip Select, allowing the host to service higher priority interrupts.

The 25LCXXX is available in a standard 8-lead SOIC package. The package is Pb-free.

### Package Types (not to scale)



\*25LCXXX is used in this document as a generic part number for the 25 series devices.

# 25LCXXX

---

---

**Device Selection Table**

Part Number	Density (bits)	Organization	Vcc Range	Max Speed (MHz)	Page Size (Bytes)	Temp. Range	Package
25LC080C	8K	1,024 x 8	2.5V - 5.5V	5	16	H	SN
25LC080D	8K	1,024 x 8	2.5V - 5.5V	5	32	H	SN
25LC160C	16K	2,048 x 8	2.5V - 5.5V	5	16	H	SN
25LC160D	16K	2,048 x 8	2.5V - 5.5V	5	32	H	SN
25LC320A	32K	4,096 x 8	2.5V - 5.5V	5	32	H	SN
25LC640A	64K	8,192 x 8	2.5V - 5.5V	5	32	H	SN
25LC128	128K	16,384 x 8	2.5V - 5.5V	5	64	H	SN
25LC256	256K	32,768 x 8	2.5V - 5.5V	5	64	H	SN

## 1.0 ELECTRICAL CHARACTERISTICS

### Absolute Maximum Ratings<sup>(†)</sup>

V <sub>CC</sub> .....	6.5V
All inputs and outputs w.r.t. V <sub>SS</sub> .....	-0.6V to V <sub>CC</sub> +1.0V
Storage temperature.....	-65°C to 155°C
Ambient temperature under bias.....	-40°C to 150°C <sup>(1)</sup>
ESD protection on all pins.....	4 kV

**Note 1:** AEC-Q100 reliability testing for devices intended to operate at 150°C is 1,000 hours. Any design in which the total operating time between 125°C and 150°C will be greater than 1,000 hours is not warranted without prior written approval from Microchip Technology Inc.

† NOTICE: Stresses above those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device at those or any other conditions above those indicated in the operational listings of this specification is not implied. Exposure to maximum rating conditions for an extended period of time may affect device reliability.

**TABLE 1-1: DC CHARACTERISTICS**

DC CHARACTERISTICS			Extended (H): TA = -40°C to +150°C			V <sub>CC</sub> = 2.5V to 5.5V
Param. No.	Sym.	Characteristic	Min.	Max.	Units	Test Conditions
D001	V <sub>IH1</sub>	High-level input voltage	.7 V <sub>CC</sub>	V <sub>CC</sub> +1	V	
D002	V <sub>IL1</sub>	Low-level input voltage	-0.3	0.3V <sub>CC</sub>	V	V <sub>CC</sub> ≥ 2.7V
D003	V <sub>IL2</sub>		-0.3	0.2V <sub>CC</sub>	V	V <sub>CC</sub> < 2.7V
D004	V <sub>OL1</sub>	Low-level output voltage	—	0.4	V	I <sub>OL</sub> = 2.1 mA
D005	V <sub>OL2</sub>		—	0.2	V	I <sub>OL</sub> = 1.0 mA
D006	V <sub>OH</sub>	High-level output voltage	V <sub>CC</sub> -0.5	—	V	I <sub>OH</sub> = -400 μA
D007	I <sub>LI</sub>	Input leakage current	—	±2	μA	$\overline{CS} = V_{CC}, V_{IN} = V_{SS} \text{ OR } V_{CC}$
D008	I <sub>LO</sub>	Output leakage current	—	±2	μA	$\overline{CS} = V_{CC}, V_{OUT} = V_{SS} \text{ OR } V_{CC}$
D009	C <sub>INT</sub>	Internal Capacitance (all inputs and outputs)	—	7	pF	TA = 25°C, CLK = 1.0 MHz, V <sub>CC</sub> = 5.0V ( <b>Note</b> )
D010	I <sub>CC</sub> Read	Operating Current	—	5	mA	V <sub>CC</sub> = 5.5V; F <sub>CLK</sub> = 5.0 MHz; SO = Open
			—	2.5	mA	V <sub>CC</sub> = 2.5V; F <sub>CLK</sub> = 3.0 MHz; SO = Open
D011	I <sub>CC</sub> Write		—	5	mA	V <sub>CC</sub> = 5.5V
			—	3	mA	V <sub>CC</sub> = 2.5V
D012	I <sub>CCS</sub>	Standby Current	—	10	μA	$\overline{CS} = V_{CC} = 5.5V$ , Inputs tied to V <sub>CC</sub> or V <sub>SS</sub> , 150°C

**Note:** This parameter is periodically sampled and not 100% tested.

# 25LCXXX

**TABLE 1-2: AC CHARACTERISTICS**

AC CHARACTERISTICS			Extended (H): $T_A = -40^{\circ}\text{C}$ to $+150^{\circ}\text{C}$ $V_{CC} = 2.5\text{V}$ to $5.5\text{V}$			
Param. No.	Sym.	Characteristic	Min.	Max.	Units	Test Conditions
1	FCLK	Clock Frequency	—	5	MHz	$4.5\text{V} \leq V_{CC} \leq 5.5\text{V}$
			—	3	MHz	$2.5\text{V} \leq V_{CC} < 4.5\text{V}$
2	T <sub>CSS</sub>	$\overline{\text{CS}}$ Setup Time	100	—	ns	$4.5\text{V} \leq V_{CC} \leq 5.5\text{V}$
			150	—	ns	$2.5\text{V} \leq V_{CC} < 4.5\text{V}$
3	T <sub>CSH</sub>	$\overline{\text{CS}}$ Hold Time	200	—	ns	$4.5\text{V} \leq V_{CC} \leq 5.5\text{V}$
			250	—	ns	$2.5\text{V} \leq V_{CC} < 4.5\text{V}$
4	T <sub>CSD</sub>	$\overline{\text{CS}}$ Disable Time	50	—	ns	—
5	T <sub>SU</sub>	Data Setup Time	20	—	ns	$4.5\text{V} \leq V_{CC} \leq 5.5\text{V}$
			30	—	ns	$2.5\text{V} \leq V_{CC} < 4.5\text{V}$
6	T <sub>HD</sub>	Data Hold Time	40	—	ns	$4.5\text{V} \leq V_{CC} \leq 5.5\text{V}$
			50	—	ns	$2.5\text{V} \leq V_{CC} < 4.5\text{V}$
7	T <sub>R</sub>	CLK Rise Time	—	2	$\mu\text{s}$	<b>(Note 1)</b>
8	T <sub>F</sub>	CLK Fall Time	—	2	$\mu\text{s}$	<b>(Note 1)</b>
9	T <sub>HI</sub>	Clock High Time	100	—	ns	$4.5\text{V} \leq V_{CC} \leq 5.5\text{V}$
			150	—	ns	$2.5\text{V} \leq V_{CC} < 4.5\text{V}$
10	T <sub>LO</sub>	Clock Low Time	100	—	ns	$4.5\text{V} \leq V_{CC} \leq 5.5\text{V}$
			150	—	ns	$2.5\text{V} \leq V_{CC} < 4.5\text{V}$
11	T <sub>CLD</sub>	Clock Delay Time	50	—	ns	—
12	T <sub>CLE</sub>	Clock Enable Time	50	—	ns	—
13	T <sub>V</sub>	Output Valid from Clock Low	—	100	ns	$4.5\text{V} \leq V_{CC} \leq 5.5\text{V}$
			—	160	ns	$2.5\text{V} \leq V_{CC} < 4.5\text{V}$
14	T <sub>HO</sub>	Output Hold Time	0	—	ns	<b>(Note 1)</b>
15	T <sub>DIS</sub>	Output Disable Time	—	80	ns	$4.5\text{V} \leq V_{CC} \leq 5.5\text{V}$ <b>(Note 1)</b>
			—	160	ns	$2.5\text{V} \leq V_{CC} \leq 4.5\text{V}$ <b>(Note 1)</b>
16	T <sub>HS</sub>	$\overline{\text{HOLD}}$ Setup Time	40	—	ns	$4.5\text{V} \leq V_{CC} \leq 5.5\text{V}$
			80	—	ns	$2.5\text{V} \leq V_{CC} < 4.5\text{V}$
17	T <sub>HH</sub>	$\overline{\text{HOLD}}$ Hold Time	40	—	ns	$4.5\text{V} \leq V_{CC} \leq 5.5\text{V}$
			80	—	ns	$2.5\text{V} \leq V_{CC} < 4.5\text{V}$
18	T <sub>HZ</sub>	$\overline{\text{HOLD}}$ Low to Output High-Z	60	—	ns	$4.5\text{V} \leq V_{CC} \leq 5.5\text{V}$ <b>(Note 1)</b>
			160	—	ns	$2.5\text{V} \leq V_{CC} < 4.5\text{V}$ <b>(Note 1)</b>
19	T <sub>HV</sub>	$\overline{\text{HOLD}}$ High to Output Valid	60	—	ns	$4.5\text{V} \leq V_{CC} \leq 5.5\text{V}$
			160	—	ns	$2.5\text{V} \leq V_{CC} < 4.5\text{V}$
20	T <sub>WC</sub>	Internal Write Cycle Time	—	6	ms	<b>(Note 2)</b>
21	—	Endurance	100K	—	E/W Cycles	<b>(Note 3)</b>

**Note 1:** This parameter is periodically sampled and not 100% tested.

**2:** T<sub>WC</sub> begins on the rising edge of  $\overline{\text{CS}}$  after a valid write sequence and ends when the internal write cycle is complete.

**3:** This parameter is not tested but ensured by characterization. For endurance estimates in a specific application, please consult the Total Endurance™ Model which can be obtained from our web site: [www.microchip.com](http://www.microchip.com).

**TABLE 1-3: AC TEST CONDITIONS**

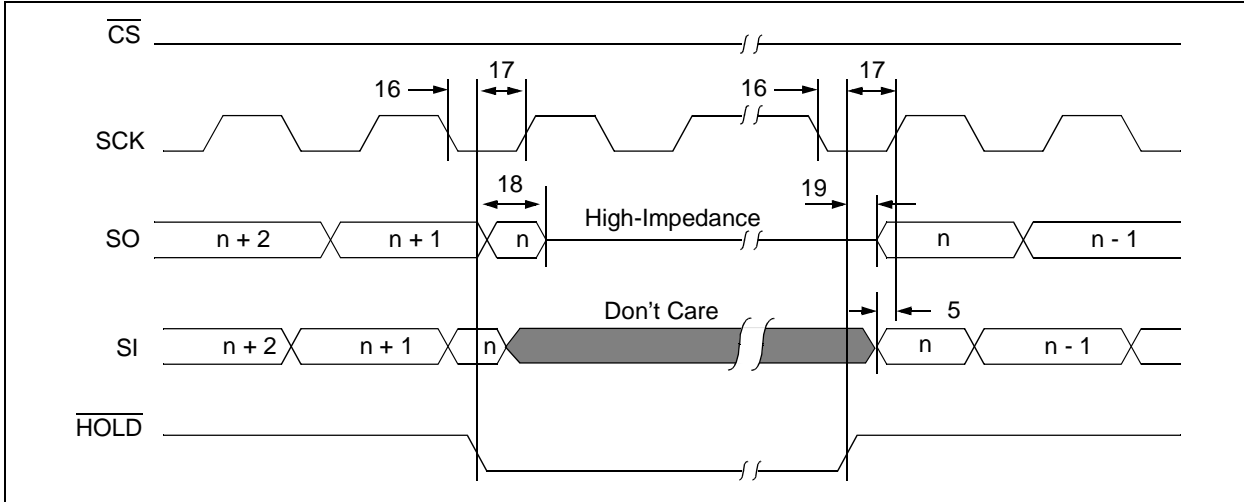
<b>AC Waveform:</b>	
$V_{LO} = 0.2V$	—
$V_{HI} = V_{CC} - 0.2V$	<b>(Note 1)</b>
$V_{HI} = 4.0V$	<b>(Note 2)</b>
$CL = 50\text{ pF}$	—
<b>Timing Measurement Reference Level</b>	
Input	0.5 $V_{CC}$
Output	0.5 $V_{CC}$

**Note 1:** For  $V_{CC} \leq 4.0V$

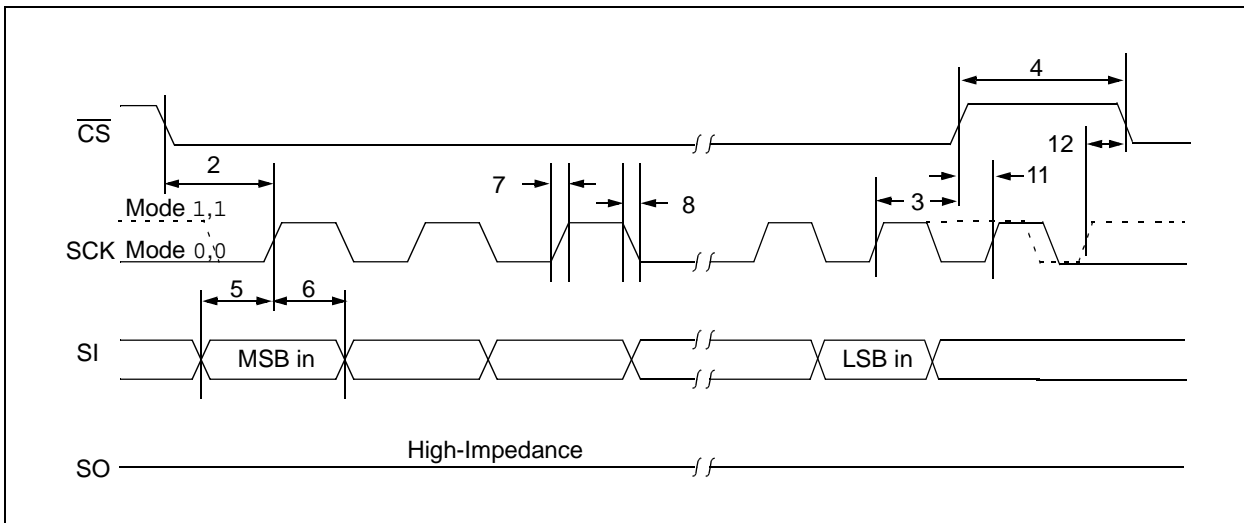
**2:** For  $V_{CC} > 4.0V$

# 25LCXXX

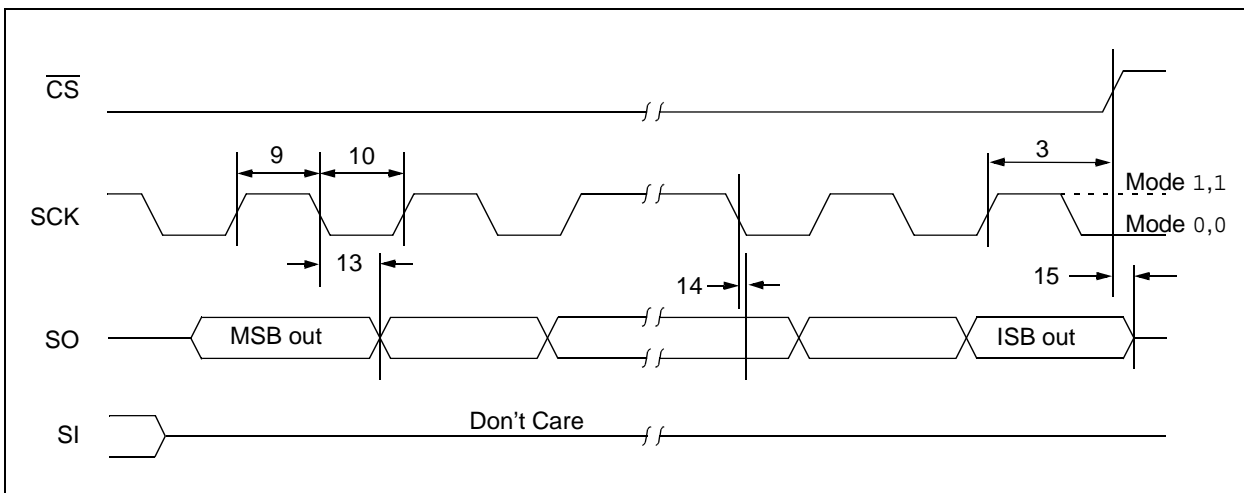
**FIGURE 1-1: HOLD TIMING**



**FIGURE 1-2: SERIAL INPUT TIMING**



**FIGURE 1-3: SERIAL OUTPUT TIMING**



## 2.0 PIN DESCRIPTIONS

The descriptions of the pins are listed in Table 2-1.

**TABLE 2-1: PIN FUNCTION TABLE**

Name	Pin Number	Function
$\overline{\text{CS}}$	1	Chip Select Input
SO	2	Serial Data Output
$\overline{\text{WP}}$	3	Write-Protect Pin
Vss	4	Ground
SI	5	Serial Data Input
SCK	6	Serial Clock Input
$\overline{\text{HOLD}}$	7	Hold Input
Vcc	8	Supply Voltage

### 2.1 Chip Select ( $\overline{\text{CS}}$ )

A low level on this pin selects the device. A high level deselects the device and forces it into Standby mode. However, a programming cycle which is already initiated or in progress will be completed, regardless of the  $\overline{\text{CS}}$  input signal. If  $\overline{\text{CS}}$  is brought high during a program cycle, the device will go into Standby mode as soon as the programming cycle is complete. When the device is deselected, SO goes to the high-impedance state, allowing multiple parts to share the same SPI bus. A low-to-high transition on  $\overline{\text{CS}}$  after a valid write sequence initiates an internal write cycle. After power-up, a low level on  $\overline{\text{CS}}$  is required prior to any sequence being initiated.

### 2.2 Serial Output (SO)

The SO pin is used to transfer data out of the 25LCXXX. During a read cycle, data is shifted out on this pin after the falling edge of the serial clock.

### 2.3 Write-Protect ( $\overline{\text{WP}}$ )

This pin is used in conjunction with the WPEN bit in the STATUS register to prohibit writes to the nonvolatile bits in the STATUS register. When  $\overline{\text{WP}}$  is low and WPEN is high, writing to the nonvolatile bits in the STATUS register is disabled. All other operations function normally. When  $\overline{\text{WP}}$  is high, all functions, including writes to the nonvolatile bits in the STATUS register operate normally. If the WPEN bit is set,  $\overline{\text{WP}}$  low during a STATUS register write sequence will disable writing to the STATUS register. If an internal write cycle has already begun,  $\overline{\text{WP}}$  going low will have no effect on the write.

The  $\overline{\text{WP}}$  pin function is blocked when the WPEN bit in the STATUS register is low. This allows the user to install the 25LCXXX in a system with  $\overline{\text{WP}}$  pin grounded and still be able to write to the STATUS register. The  $\overline{\text{WP}}$  pin functions will be enabled when the WPEN bit is set high.

### 2.4 Serial Input (SI)

The SI pin is used to transfer data into the device. It receives instructions, addresses and data. Data is latched on the rising edge of the serial clock.

### 2.5 Serial Clock (SCK)

The SCK is used to synchronize the communication between a master and the 25LCXXX. Instructions, addresses or data present on the SI pin are latched on the rising edge of the clock input, while data on the SO pin is updated after the falling edge of the clock input.

### 2.6 Hold ( $\overline{\text{HOLD}}$ )

The  $\overline{\text{HOLD}}$  pin is used to suspend transmission to the 25LCXXX while in the middle of a serial sequence without having to retransmit the entire sequence again. It must be held high any time this function is not being used. Once the device is selected and a serial sequence is underway, the  $\overline{\text{HOLD}}$  pin may be pulled low to pause further serial communication without resetting the serial sequence. The  $\overline{\text{HOLD}}$  pin must be brought low while SCK is low, otherwise the  $\overline{\text{HOLD}}$  function will not be invoked until the next SCK high-to-low transition. The 25LCXXX must remain selected during this sequence. The SI, SCK and SO pins are in a high-impedance state during the time the device is paused and transitions on these pins will be ignored. To resume serial communication,  $\overline{\text{HOLD}}$  must be brought high while the SCK pin is low, otherwise serial communication will not resume. Lowering the  $\overline{\text{HOLD}}$  line at any time will tri-state the SO line.

# 25LCXXX

## 3.0 FUNCTIONAL DESCRIPTION

### 3.1 Principles of Operation

The 25LCXXX are Mid-Density Serial EEPROMs designed to interface directly with the Serial Peripheral Interface (SPI) port of many of today's popular microcontroller families, including Microchip's PIC® microcontrollers. It may also interface with microcontrollers that do not have a built-in SPI port by using discrete I/O lines programmed properly in firmware to match the SPI protocol.

The 25LCXXX contains an 8-bit instruction register. The device is accessed via the SI pin, with data being clocked in on the rising edge of SCK. The  $\overline{CS}$  pin must be low and the HOLD pin must be high for the entire operation.

Table 3-1 contains a list of the possible instruction bytes and format for device operation. All instructions, addresses, and data are transferred MSB first, LSB last.

Data (SI) is sampled on the first rising edge of SCK after  $\overline{CS}$  goes low. If the clock line is shared with other peripheral devices on the SPI bus, the user can assert the HOLD input and place the 25LCXXX in 'HOLD' mode. After releasing the HOLD pin, operation will resume from the point when the HOLD was asserted.

### Block Diagram

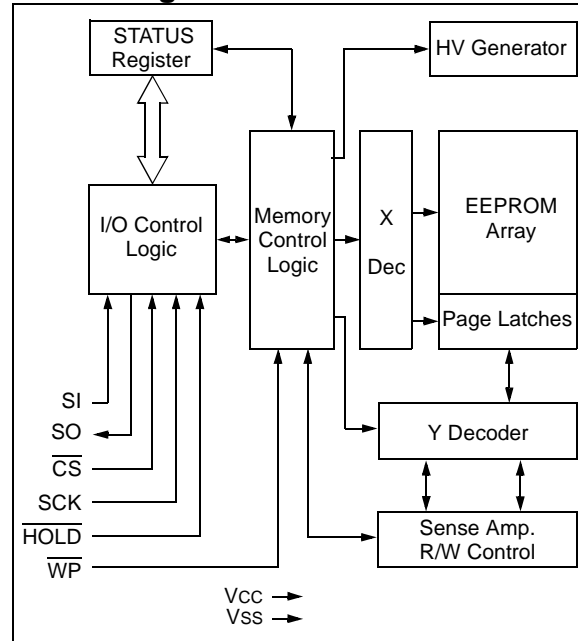


TABLE 3-1: INSTRUCTION SET

Instruction Name	Instruction Format	Description
READ	0000 0011	Read data from memory array beginning at selected address
WRITE	0000 0010	Write data to memory array beginning at selected address
WRDI	0000 0100	Reset the write enable latch (disable write operations)
WREN	0000 0110	Set the write enable latch (enable write operations)
RDSR	0000 0101	Read STATUS register
WRSR	0000 0001	Write STATUS register



## 3.2 Read Sequence

The device is selected by pulling  $\overline{CS}$  low. The 8-bit READ instruction is transmitted to the 25LCXXX followed by the 16-bit address. After the correct READ instruction and address are sent, the data stored in the memory at the selected address is shifted out on the SO pin. The data stored in the memory at the next address can be read sequentially by continuing to provide clock pulses. The internal Address Pointer is automatically incremented to the next higher address after each byte of data is shifted out. When the highest address is reached, the address counter rolls over to address 0000h allowing the read cycle to be continued indefinitely. The read operation is terminated by raising the  $\overline{CS}$  pin (Figure 3-1).

## 3.3 Write Sequence

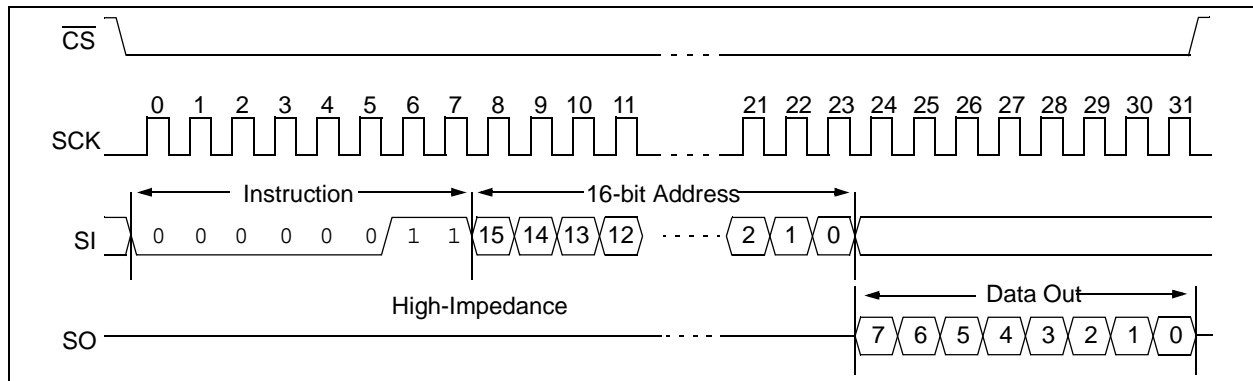
Prior to any attempt to write data to the 25LCXXX, the write enable latch must be set by issuing the WREN instruction (Figure 3-4). This is done by setting  $\overline{CS}$  low and then clocking out the proper instruction into the 25LCXXX. After all eight bits of the instruction are transmitted, the  $\overline{CS}$  must be brought high to set the write enable latch. If the write operation is initiated immediately after the WREN instruction without  $\overline{CS}$  being brought high, the data will not be written to the array because the write enable latch will not have been properly set.

Once the write enable latch is set, the user may proceed by setting the  $\overline{CS}$  low, issuing a WRITE instruction, followed by the 16-bit address, and then the data to be written. Depending upon the density, a page of data that ranges from 16 bytes to 64 bytes can be sent to the device before a write cycle is necessary. The only restriction is that all of the bytes must reside in the same page.

**Note:** Page write operations are limited to writing bytes within a single physical page, **regardless** of the number of bytes actually being written. Physical page boundaries start at addresses that are integer multiples of the page buffer size (or 'page size') and, end at addresses that are integer multiples of page size - 1. If a Page Write command attempts to write across a physical page boundary, the result is that the data wraps around to the beginning of the current page (overwriting data previously stored there), instead of being written to the next page as might be expected. It is therefore necessary for the application software to prevent page write operations that would attempt to cross a page boundary.

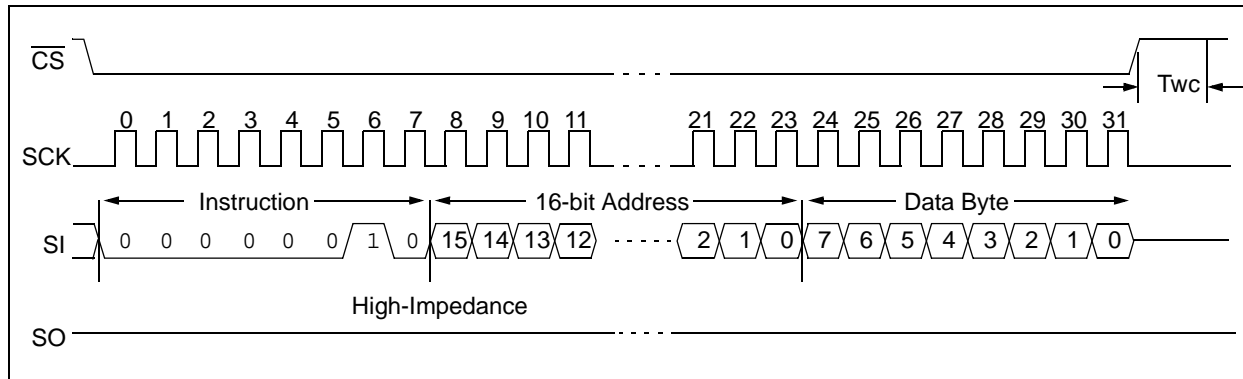
For the data to be actually written to the array, the  $\overline{CS}$  must be brought high after the Least Significant bit (D0) of the  $n^{th}$  data byte has been clocked in. If  $\overline{CS}$  is brought high at any other time, the write operation will not be completed. Refer to Figure 3-2 and Figure 3-3 for more detailed illustrations on the byte write sequence and the page write sequence, respectively. While the write is in progress, the STATUS register may be read to check the status of the WPEN, WIP, WEL, BP1 and BP0 bits (Figure 3-6). A read attempt of a memory array location will not be possible during a write cycle. When the write cycle is completed, the write enable latch is reset.

**FIGURE 3-1: READ SEQUENCE**

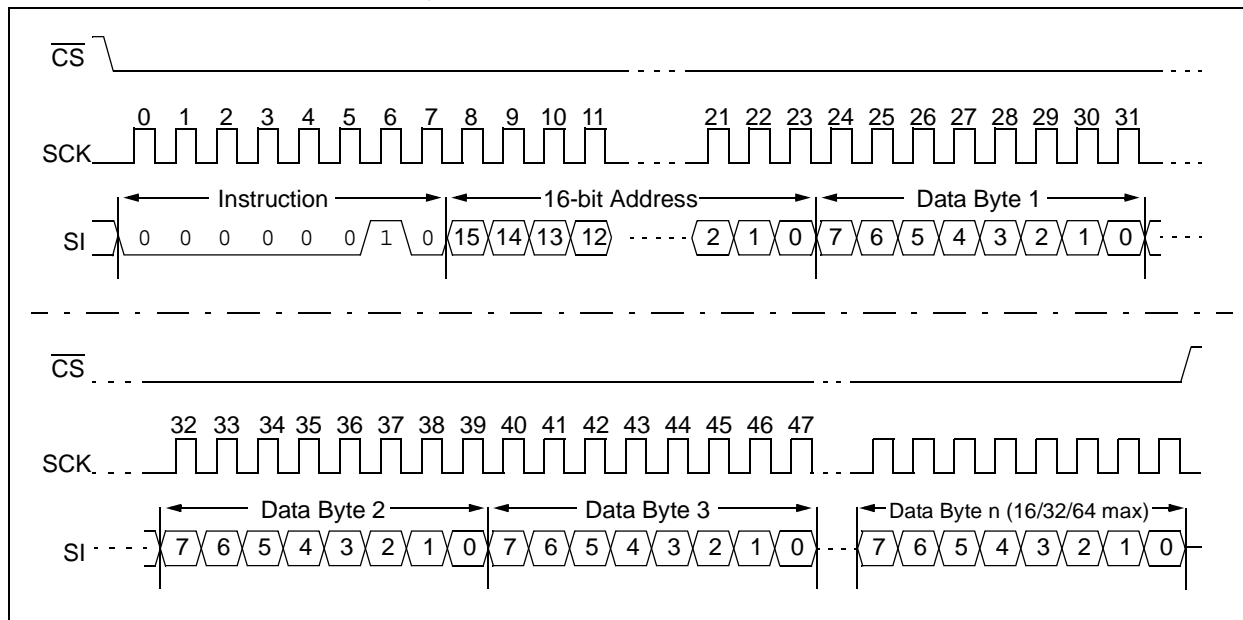


# 25LCXXX

**FIGURE 3-2: BYTE WRITE SEQUENCE**



**FIGURE 3-3: PAGE WRITE SEQUENCE**



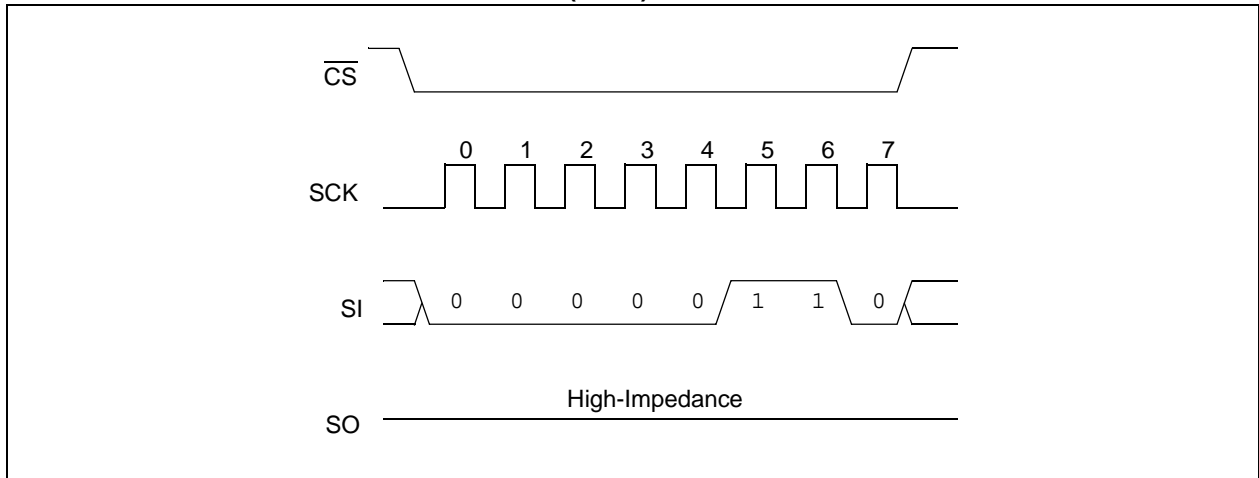
### 3.4 Write Enable ( $\overline{\text{WREN}}$ ) and Write Disable ( $\overline{\text{WRDI}}$ )

The 25LCXXX contains a write enable latch. See Table 5-1 for the write-protect functionality matrix. This latch must be set before any write operation will be completed internally. The  $\overline{\text{WREN}}$  instruction will set the latch, and the  $\overline{\text{WRDI}}$  will reset the latch.

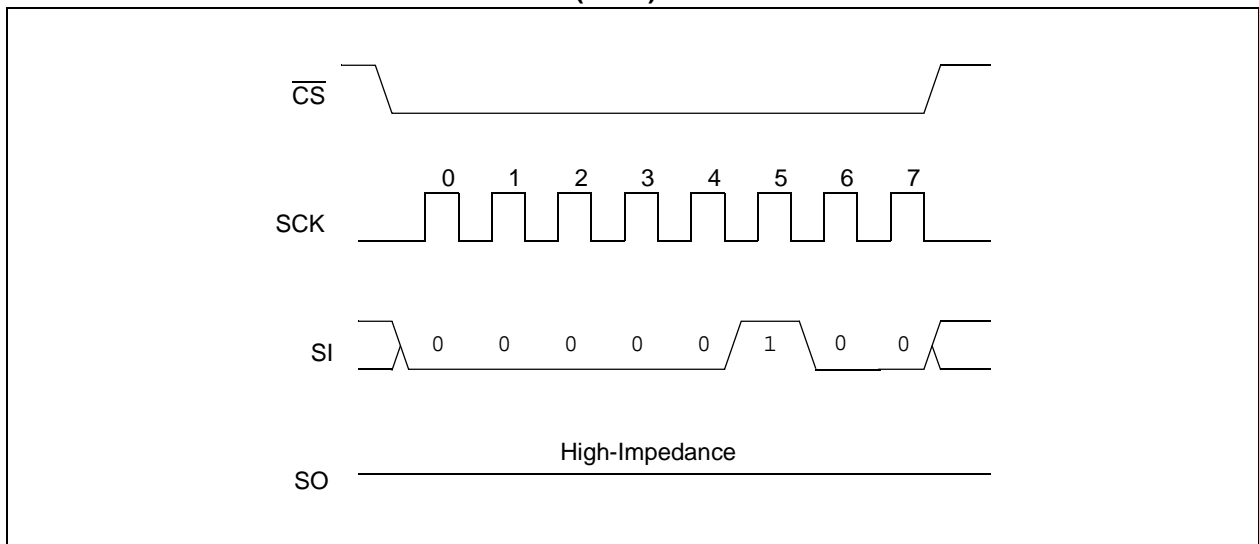
The following is a list of conditions under which the write enable latch will be reset:

- Power-up
- $\overline{\text{WRDI}}$  instruction successfully executed
- $\overline{\text{WRSR}}$  instruction successfully executed
- $\overline{\text{WRITE}}$  instruction successfully executed

**FIGURE 3-4: WRITE ENABLE SEQUENCE ( $\overline{\text{WREN}}$ )**



**FIGURE 3-5: WRITE DISABLE SEQUENCE ( $\overline{\text{WRDI}}$ )**



# 25LCXXX

## 3.5 Read Status Register Instruction (RDSR)

The Read Status Register instruction (RDSR) provides access to the STATUS register. The STATUS register may be read at any time, even during a write cycle. The STATUS register is formatted as follows:

**TABLE 3-2: STATUS REGISTER**

7	6	5	4	3	2	1	0
W/R	-	-	-	W/R	W/R	R	R
WPEN	X	X	X	BP1	BP0	WEL	WIP
W/R = writable/readable. R = read-only.							

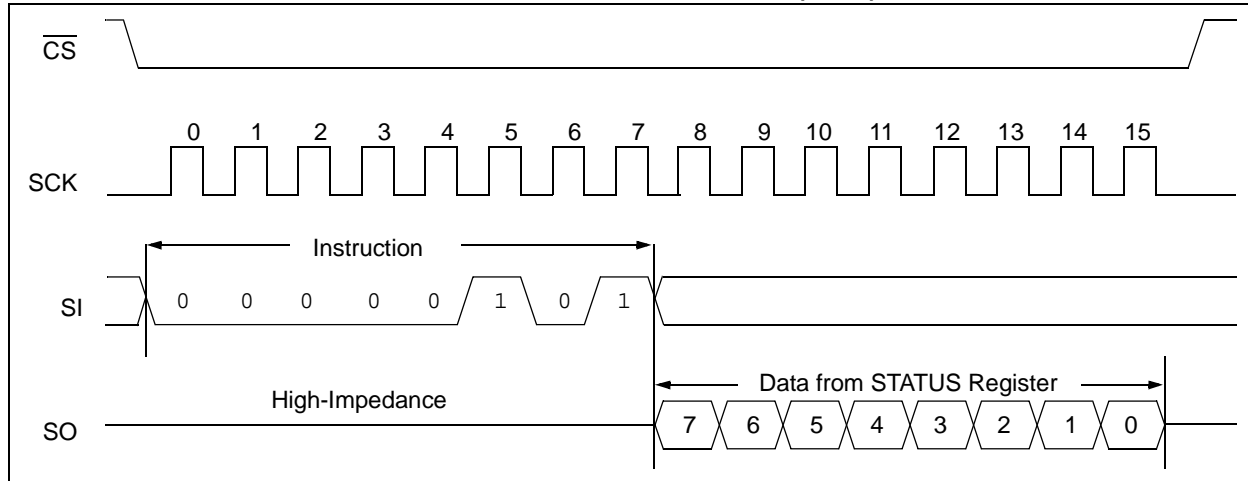
The **Write-In-Process (WIP)** bit indicates whether the 25LCXXX is busy with a write operation. When set to a '1', a write is in progress, when set to a '0', no write is in progress. This bit is read-only.

The **Write Enable Latch (WEL)** bit indicates the status of the write enable latch and is read-only. When set to a '1', the latch allows writes to the array, when set to a '0', the latch prohibits writes to the array. The state of this bit can always be updated via the WREN or WRDI commands regardless of the state of write protection on the STATUS register. These commands are shown in Figure 3-4 and Figure 3-5.

The **Block Protection (BP0 and BP1)** bits indicate which blocks are currently write-protected. These bits are set by the user issuing the WRSR instruction. These bits are nonvolatile, and are shown in Table 3-3.

See Figure 3-6 for the RDSR timing sequence.

**FIGURE 3-6: READ STATUS REGISTER TIMING SEQUENCE (RDSR)**



## 3.6 Write Status Register Instruction (WRSR)

The Write Status Register instruction (WRSR) allows the user to write to the nonvolatile bits in the STATUS register as shown in Table 3-2. The user is able to select one of four levels of protection for the array by writing to the appropriate bits in the STATUS register. The array is divided up into four segments. The user has the ability to write-protect none, one, two or all four of the segments of the array. The partitioning is controlled as shown in Table 3-3.

The Write-Protect Enable (WPEN) bit is a nonvolatile bit that is available as an enable bit for the  $\overline{WP}$  pin. The Write-Protect ( $\overline{WP}$ ) pin and the Write-Protect Enable (WPEN) bit in the STATUS register control the programmable hardware write-protect feature. Hardware write protection is enabled when  $\overline{WP}$  pin is low and the WPEN bit is high. Hardware write protection is disabled when either the  $\overline{WP}$  pin is high or the WPEN bit is low. When the chip is hardware write-protected, only writes to nonvolatile bits in the STATUS register are disabled. See Table 5-1 for a matrix of functionality on the WPEN bit.

See Figure 3-7 for the WRSR timing sequence.

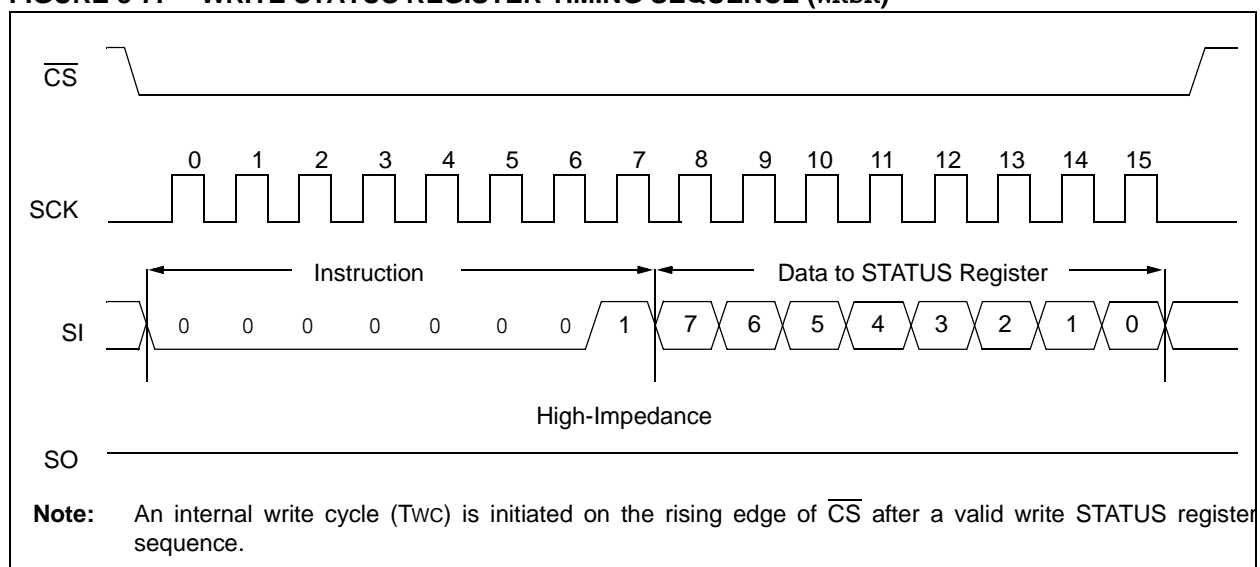
**TABLE 3-3: ARRAY PROTECTION**

BP1	BP0	Array Addresses Write-Protected	Array Addresses Unprotected
0	0	None	All
0	1	Upper 1/4	Lower 3/4
1	0	Upper 1/2	Lower 1/2
1	1	All	None

**TABLE 3-4: ARRAY PROTECTED ADDRESS LOCATIONS**

Density	Upper 1/4	Upper 1/2	All
8K	300h - 3FFh	200h - 3FFh	000h - 3FFh
16K	600h - 7FFh	400h - 7FFh	000h - 7FFh
32K	C00h - FFFh	800h - FFFh	000h - FFFh
64K	1800h - 1FFFh	1000h - 1FFFh	0000h - 1FFFh
128K	3000h - 3FFFh	2000h - 3FFFh	0000h - 3FFFh
256K	6000h - 7FFFh	4000h - 7FFFh	0000h - 7FFFh

**FIGURE 3-7: WRITE STATUS REGISTER TIMING SEQUENCE (WRSR)**



# 25LCXXX

## 4.0 DATA PROTECTION

The following protection has been implemented to prevent inadvertent writes to the array:

- The write enable latch is reset on power-up
- A write enable instruction must be issued to set the write enable latch
- After a byte write, page write or STATUS register write, the write enable latch is reset
- $\overline{CS}$  must be set high after the proper number of clock cycles to start an internal write cycle
- Access to the array during an internal write cycle is ignored and programming is continued

## 5.0 POWER-ON STATE

The 25LCXXX powers on in the following state:

- The device is in low-power Standby mode ( $\overline{CS} = 1$ )
- The write enable latch is reset
- SO is in high-impedance state
- A high-to-low-level transition on  $\overline{CS}$  is required to enter active state

TABLE 5-1: WRITE-PROTECT FUNCTIONALITY MATRIX

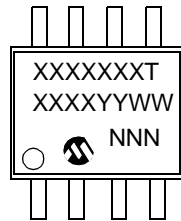
WEL (SR bit 1)	WPEN (SR bit 7)	$\overline{WP}$ (pin 3)	Protected Blocks	Unprotected Blocks	STATUS Register
0	x	x	Protected	Protected	Protected
1	0	x	Protected	Writable	Writable
1	1	0 (low)	Protected	Writable	Protected
1	1	1 (high)	Protected	Writable	Writable

x = don't care

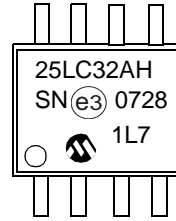
## 6.0 PACKAGING INFORMATION

### 6.1 Package Marking Information

8-Lead SOIC



Example:



8-Lead SOIC Package Marking (Pb-Free)	
Device	Line 1 Marking
25LC080C	25LC80CT
25LC080D	25LC80DT
25LC160C	25LC16CT
25LC160D	25LC16DT
25LC320A	25LC32AT
25LC640A	25L640AT
25LC128	25LC128T
25LC256	25LC256T

**Note 1:** T = Temperature Grade (H).

<b>Legend:</b>	XX...X	Customer-specific information
	Y	Year code (last digit of calendar year)
	YY	Year code (last 2 digits of calendar year)
	WW	Week code (week of January 1 is week '01')
	NNN	Alphanumeric traceability code
	(e3)	Pb-free JEDEC designator for Matte Tin (Sn)
	*	This package is Pb-free. The Pb-free JEDEC designator (e3) can be found on the outer packaging for this package.

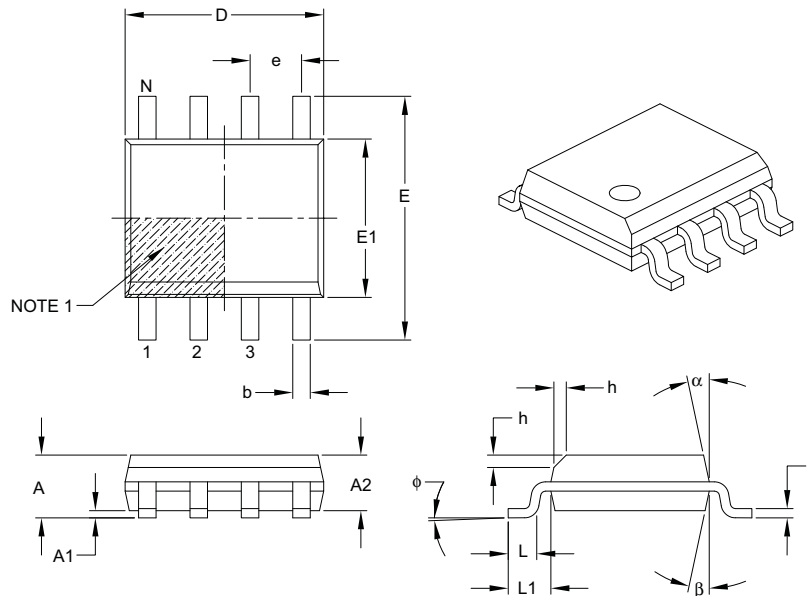
**Note:** In the event the full Microchip part number cannot be marked on one line, it will be carried over to the next line, thus limiting the number of available characters for customer-specific information.

**Note:** Custom marking available.

# 25LCXXX

## 8-Lead Plastic Small Outline (SN) – Narrow, 3.90 mm Body [SOIC]

**Note:** For the most current package drawings, please see the Microchip Packaging Specification located at <http://www.microchip.com/packaging>



Dimension Limits	Units	MILLIMETERS		
		MIN	NOM	MAX
Number of Pins	N	8		
Pitch	e	1.27 BSC		
Overall Height	A	–	–	1.75
Molded Package Thickness	A2	1.25	–	–
Standoff §	A1	0.10	–	0.25
Overall Width	E	6.00 BSC		
Molded Package Width	E1	3.90 BSC		
Overall Length	D	4.90 BSC		
Chamfer (optional)	h	0.25	–	0.50
Foot Length	L	0.40	–	1.27
Footprint	L1	1.04 REF		
Foot Angle	$\phi$	0°	–	8°
Lead Thickness	c	0.17	–	0.25
Lead Width	b	0.31	–	0.51
Mold Draft Angle Top	$\alpha$	5°	–	15°
Mold Draft Angle Bottom	$\beta$	5°	–	15°

**Notes:**

- Pin 1 visual index feature may vary, but must be located within the hatched area.
- § Significant Characteristic.
- Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.15 mm per side.
- Dimensioning and tolerancing per ASME Y14.5M.

BSC: Basic Dimension. Theoretically exact value shown without tolerances.

REF: Reference Dimension, usually without tolerance, for information purposes only.

Microchip Technology Drawing C04-057B



## 8-Lead Plastic Small Outline (SN) – Narrow, 3.90 mm Body [SOIC]

**Note:** For the most current package drawings, please see the Microchip Packaging Specification located at <http://www.microchip.com/packaging>



RECOMMENDED LAND PATTERN

Dimension Limits	Units	MILLIMETERS		
		MIN	NOM	MAX
Contact Pitch	E	1.27 BSC		
Contact Pad Spacing	C		5.40	
Contact Pad Width (X8)	X1			0.60
Contact Pad Length (X8)	Y1			1.55

**Notes:**

1. Dimensioning and tolerancing per ASME Y14.5M

BSC: Basic Dimension. Theoretically exact value shown without tolerances.

Microchip Technology Drawing No. C04-2057A

# 25LCXXX

---

## REVISION HISTORY

### Revision A (01/2009)

Original Release.

### Revision B (04/2009)

Revised part number from 25XX to 25LCXXX; Added Note 1 to Electrical Characteristics.

## THE MICROCHIP WEB SITE

Microchip provides online support via our WWW site at [www.microchip.com](http://www.microchip.com). This web site is used as a means to make files and information easily available to customers. Accessible by using your favorite Internet browser, the web site contains the following information:

- **Product Support** – Data sheets and errata, application notes and sample programs, design resources, user's guides and hardware support documents, latest software releases and archived software
- **General Technical Support** – Frequently Asked Questions (FAQ), technical support requests, online discussion groups, Microchip consultant program member listing
- **Business of Microchip** – Product selector and ordering guides, latest Microchip press releases, listing of seminars and events, listings of Microchip sales offices, distributors and factory representatives

## CUSTOMER CHANGE NOTIFICATION SERVICE

Microchip's customer notification service helps keep customers current on Microchip products. Subscribers will receive e-mail notification whenever there are changes, updates, revisions or errata related to a specified product family or development tool of interest.

To register, access the Microchip web site at [www.microchip.com](http://www.microchip.com), click on Customer Change Notification and follow the registration instructions.

## CUSTOMER SUPPORT

Users of Microchip products can receive assistance through several channels:

- Distributor or Representative
- Local Sales Office
- Field Application Engineer (FAE)
- Technical Support
- Development Systems Information Line

Customers should contact their distributor, representative or field application engineer (FAE) for support. Local sales offices are also available to help customers. A listing of sales offices and locations is included in the back of this document.

**Technical support is available through the web site at: <http://support.microchip.com>**

# 25LCXXX

---

---

## READER RESPONSE

It is our intention to provide you with the best documentation possible to ensure successful use of your Microchip product. If you wish to provide your comments on organization, clarity, subject matter, and ways in which our documentation can better serve you, please FAX your comments to the Technical Publications Manager at (480) 792-4150.

Please list the following information, and use this outline to provide us with your comments about this document.

To: Technical Publications Manager  
RE: Reader Response  
Total Pages Sent \_\_\_\_\_

From: Name \_\_\_\_\_  
Company \_\_\_\_\_  
Address \_\_\_\_\_  
City / State / ZIP / Country \_\_\_\_\_  
Telephone: (\_\_\_\_\_) \_\_\_\_\_ - \_\_\_\_\_ FAX: (\_\_\_\_\_) \_\_\_\_\_ - \_\_\_\_\_

Application (optional):

Would you like a reply? \_\_\_Y \_\_\_N

Device: 25LCXXX

Literature Number: DS22131B

Questions:

1. What are the best features of this document?

---

---

2. How does this document meet your hardware and software development needs?

---

---

3. Do you find the organization of this document easy to follow? If not, why?

---

---

4. What additions to the document do you think would enhance the structure and subject?

---

---

5. What deletions from the document could be made without affecting the overall usefulness?

---

---

6. Is there any incorrect or misleading information (what and where)?

---

---

7. How would you improve this document?

---

---

## PRODUCT IDENTIFICATION SYSTEM

To order or obtain information, e.g., on pricing or delivery, refer to the factory or the listed sales office.

<u>PART NO.</u>		<u>X</u>	-	<u>X</u>	<u>/XX</u>
Device		Tape & Reel		Temp Range	Package
<b>Device:</b>	25LC080C =			8k-bit, 2.5V, 16 Byte Page, SPI Serial EEPROM	
	25LC080D =			8k-bit, 2.5V, 32 Byte Page, SPI Serial EEPROM	
	25LC160C =			16k-bit, 2.5V, 16 Byte Page, SPI Serial EEPROM	
	25LC160D =			16k-bit, 2.5V, 32 Byte Page, SPI Serial EEPROM	
	25LC320A =			32k-bit, 2.5V, 32 Byte Page, SPI Serial EEPROM	
	25LC640A =			64k-bit, 2.5V, 32 Byte Page, SPI Serial EEPROM	
	25LC128 =			128k-bit, 2.5V, 64 Byte Page, SPI Serial EEPROM	
	25LC256 =			256k-bit, 2.5V, 64 Byte Page, SPI Serial EEPROM	
<b>Tape &amp; Reel:</b>	Blank =			Standard packaging	
	T =			Tape & Reel	
<b>Temperature Range:</b>	H =			-40°C to +150°C	
<b>Package:</b>	SN =			Plastic SOIC (3.90 mm body), 8-lead	

**Examples:**

- a) 25LC080CT-H/SN = 8k-bit, 16-byte page, 2.5V Serial EEPROM, Extended temp., Tape & Reel, SOIC package
- b) 25LC080D-H/SN = 8k-bit, 32-byte page, 2.5V Serial EEPROM, Extended temp., SOIC package
- c) 25LC160CT-H/SN = 16k-bit, 16-byte page, 2.5V Serial EEPROM, Extended temp., Tape & Reel, SOIC package
- d) 25LC160D-H/SN = 16k-bit, 32-byte page, 2.5V Serial EEPROM, Extended temp., SOIC package
- e) 25LC320AT-H/SN = 32k-bit, 32-byte page, 2.5V Serial EEPROM, Extended temp., Tape & Reel, SOIC package
- f) 25LC640A-H/SN = 64k-bit, 32-byte page, 2.5V Serial EEPROM, Extended temp., SOIC package
- g) 25LC128T-H/SN = 128k-bit, 64-byte page, 2.5V Serial EEPROM, Extended temp., Tape & Reel, SOIC package
- h) 25LC256-H/SN = 256k-bit, 64-byte page, 2.5V Serial EEPROM, Extended temp., SOIC package

# 25LCXXX

---

NOTES:

---

**Note the following details of the code protection feature on Microchip devices:**

- Microchip products meet the specification contained in their particular Microchip Data Sheet.
- Microchip believes that its family of products is one of the most secure families of its kind on the market today, when used in the intended manner and under normal conditions.
- There are dishonest and possibly illegal methods used to breach the code protection feature. All of these methods, to our knowledge, require using the Microchip products in a manner outside the operating specifications contained in Microchip's Data Sheets. Most likely, the person doing so is engaged in theft of intellectual property.
- Microchip is willing to work with the customer who is concerned about the integrity of their code.
- Neither Microchip nor any other semiconductor manufacturer can guarantee the security of their code. Code protection does not mean that we are guaranteeing the product as “unbreakable.”

Code protection is constantly evolving. We at Microchip are committed to continuously improving the code protection features of our products. Attempts to break Microchip's code protection feature may be a violation of the Digital Millennium Copyright Act. If such acts allow unauthorized access to your software or other copyrighted work, you may have a right to sue for relief under that Act.

---

Information contained in this publication regarding device applications and the like is provided only for your convenience and may be superseded by updates. It is your responsibility to ensure that your application meets with your specifications. MICROCHIP MAKES NO REPRESENTATIONS OR WARRANTIES OF ANY KIND WHETHER EXPRESS OR IMPLIED, WRITTEN OR ORAL, STATUTORY OR OTHERWISE, RELATED TO THE INFORMATION, INCLUDING BUT NOT LIMITED TO ITS CONDITION, QUALITY, PERFORMANCE, MERCHANTABILITY OR FITNESS FOR PURPOSE. Microchip disclaims all liability arising from this information and its use. Use of Microchip devices in life support and/or safety applications is entirely at the buyer's risk, and the buyer agrees to defend, indemnify and hold harmless Microchip from any and all damages, claims, suits, or expenses resulting from such use. No licenses are conveyed, implicitly or otherwise, under any Microchip intellectual property rights.

**Trademarks**

The Microchip name and logo, the Microchip logo, Accuron, dsPIC, KEELOQ, KEELOQ logo, MPLAB, PIC, PICmicro, PICSTART, rfPIC, SmartShunt and UNI/O are registered trademarks of Microchip Technology Incorporated in the U.S.A. and other countries.

FilterLab, Hampshire, Linear Active Thermistor, MXDEV, MXLAB, SEEVAL, SmartSensor and The Embedded Control Solutions Company are registered trademarks of Microchip Technology Incorporated in the U.S.A.

Analog-for-the-Digital Age, Application Maestro, CodeGuard, dsPICDEM, dsPICDEM.net, dsPICworks, dsSPEAK, ECAN, ECONOMONITOR, FanSense, In-Circuit Serial Programming, ICSP, ICEPIC, Mindi, MiWi, MPASM, MPLAB Certified logo, MPLIB, MPLINK, mTouch, nanoWatt XLP, PICkit, PICDEM, PICDEM.net, PICtail, PIC<sup>32</sup> logo, PowerCal, PowerInfo, PowerMate, PowerTool, REAL ICE, rfLAB, Select Mode, Total Endurance, TSHARC, WiperLock and ZENA are trademarks of Microchip Technology Incorporated in the U.S.A. and other countries.

SQTP is a service mark of Microchip Technology Incorporated in the U.S.A.

All other trademarks mentioned herein are property of their respective companies.

© 2009, Microchip Technology Incorporated, Printed in the U.S.A., All Rights Reserved.

 Printed on recycled paper.

**QUALITY MANAGEMENT SYSTEM**  
**CERTIFIED BY DNV**  
**== ISO/TS 16949:2002 ==**

*Microchip received ISO/TS-16949:2002 certification for its worldwide headquarters, design and wafer fabrication facilities in Chandler and Tempe, Arizona; Gresham, Oregon and design centers in California and India. The Company's quality system processes and procedures are for its PIC® MCUs and dsPIC® DSCs, KEELOQ® code hopping devices, Serial EEPROMs, microperipherals, nonvolatile memory and analog products. In addition, Microchip's quality system for the design and manufacture of development systems is ISO 9001:2000 certified.*



## WORLDWIDE SALES AND SERVICE

### AMERICAS

#### Corporate Office

2355 West Chandler Blvd.  
Chandler, AZ 85224-6199  
Tel: 480-792-7200  
Fax: 480-792-7277  
Technical Support:  
<http://support.microchip.com>  
Web Address:  
[www.microchip.com](http://www.microchip.com)

#### Atlanta

Duluth, GA  
Tel: 678-957-9614  
Fax: 678-957-1455

#### Boston

Westborough, MA  
Tel: 774-760-0087  
Fax: 774-760-0088

#### Chicago

Itasca, IL  
Tel: 630-285-0071  
Fax: 630-285-0075

#### Cleveland

Independence, OH  
Tel: 216-447-0464  
Fax: 216-447-0643

#### Dallas

Addison, TX  
Tel: 972-818-7423  
Fax: 972-818-2924

#### Detroit

Farmington Hills, MI  
Tel: 248-538-2250  
Fax: 248-538-2260

#### Kokomo

Kokomo, IN  
Tel: 765-864-8360  
Fax: 765-864-8387

#### Los Angeles

Mission Viejo, CA  
Tel: 949-462-9523  
Fax: 949-462-9608

#### Santa Clara

Santa Clara, CA  
Tel: 408-961-6444  
Fax: 408-961-6445

#### Toronto

Mississauga, Ontario,  
Canada  
Tel: 905-673-0699  
Fax: 905-673-6509

### ASIA/PACIFIC

#### Asia Pacific Office

Suites 3707-14, 37th Floor  
Tower 6, The Gateway  
Harbour City, Kowloon  
Hong Kong  
Tel: 852-2401-1200  
Fax: 852-2401-3431

#### Australia - Sydney

Tel: 61-2-9868-6733  
Fax: 61-2-9868-6755

#### China - Beijing

Tel: 86-10-8528-2100  
Fax: 86-10-8528-2104

#### China - Chengdu

Tel: 86-28-8665-5511  
Fax: 86-28-8665-7889

#### China - Hong Kong SAR

Tel: 852-2401-1200  
Fax: 852-2401-3431

#### China - Nanjing

Tel: 86-25-8473-2460  
Fax: 86-25-8473-2470

#### China - Qingdao

Tel: 86-532-8502-7355  
Fax: 86-532-8502-7205

#### China - Shanghai

Tel: 86-21-5407-5533  
Fax: 86-21-5407-5066

#### China - Shenyang

Tel: 86-24-2334-2829  
Fax: 86-24-2334-2393

#### China - Shenzhen

Tel: 86-755-8203-2660  
Fax: 86-755-8203-1760

#### China - Wuhan

Tel: 86-27-5980-5300  
Fax: 86-27-5980-5118

#### China - Xiamen

Tel: 86-592-2388138  
Fax: 86-592-2388130

#### China - Xian

Tel: 86-29-8833-7252  
Fax: 86-29-8833-7256

#### China - Zhuhai

Tel: 86-756-3210040  
Fax: 86-756-3210049

### ASIA/PACIFIC

#### India - Bangalore

Tel: 91-80-3090-4444  
Fax: 91-80-3090-4080

#### India - New Delhi

Tel: 91-11-4160-8631  
Fax: 91-11-4160-8632

#### India - Pune

Tel: 91-20-2566-1512  
Fax: 91-20-2566-1513

#### Japan - Yokohama

Tel: 81-45-471- 6166  
Fax: 81-45-471-6122

#### Korea - Daegu

Tel: 82-53-744-4301  
Fax: 82-53-744-4302

#### Korea - Seoul

Tel: 82-2-554-7200  
Fax: 82-2-558-5932 or  
82-2-558-5934

#### Malaysia - Kuala Lumpur

Tel: 60-3-6201-9857  
Fax: 60-3-6201-9859

#### Malaysia - Penang

Tel: 60-4-227-8870  
Fax: 60-4-227-4068

#### Philippines - Manila

Tel: 63-2-634-9065  
Fax: 63-2-634-9069

#### Singapore

Tel: 65-6334-8870  
Fax: 65-6334-8850

#### Taiwan - Hsin Chu

Tel: 886-3-6578-300  
Fax: 886-3-6578-370

#### Taiwan - Kaohsiung

Tel: 886-7-536-4818  
Fax: 886-7-536-4803

#### Taiwan - Taipei

Tel: 886-2-2500-6610  
Fax: 886-2-2508-0102

#### Thailand - Bangkok

Tel: 66-2-694-1351  
Fax: 66-2-694-1350

### EUROPE

#### Austria - Wels

Tel: 43-7242-2244-39  
Fax: 43-7242-2244-393

#### Denmark - Copenhagen

Tel: 45-4450-2828  
Fax: 45-4485-2829

#### France - Paris

Tel: 33-1-69-53-63-20  
Fax: 33-1-69-30-90-79

#### Germany - Munich

Tel: 49-89-627-144-0  
Fax: 49-89-627-144-44

#### Italy - Milan

Tel: 39-0331-742611  
Fax: 39-0331-466781

#### Netherlands - Drunen

Tel: 31-416-690399  
Fax: 31-416-690340

#### Spain - Madrid

Tel: 34-91-708-08-90  
Fax: 34-91-708-08-91

#### UK - Wokingham

Tel: 44-118-921-5869  
Fax: 44-118-921-5820

03/26/09



# Mouser Electronics

Authorized Distributor

Click to View Pricing, Inventory, Delivery & Lifecycle Information:

## Microchip:

[25LC320AT-H/SN](#) [25LC128T-H/SN](#) [25LC640A-H/SN](#) [25LC320A-H/SN](#) [25LC128-H/SN](#) [25LC640AT-H/SN](#)  
[25LC080C-E/MS](#) [25LC080C-E/P](#) [25LC080C-E/ST](#) [25LC080C-I/MS](#) [25LC080C-I/P](#) [25LC080C-I/SN](#) [25LC080C-I/ST](#)  
[25LC080CT-E/MNY](#) [25LC080CT-E/MS](#) [25LC080CT-E/SN](#) [25LC080CT-E/ST](#) [25LC080CT-I/MNY](#) [25LC080CT-I/MS](#)  
[25LC080CT-I/SN](#) [25LC080CT-I/ST](#) [25LC080D-E/MS](#) [25LC080D-E/P](#) [25LC080D-E/SN](#) [25LC080D-E/ST](#) [25LC080D-](#)  
[I/MS](#) [25LC080D-I/P](#) [25LC080D-I/SN](#) [25LC080D-I/ST](#) [25LC080DT-E/MNY](#) [25LC080DT-E/MS](#) [25LC080DT-E/SN](#)  
[25LC080DT-E/ST](#) [25LC080DT-I/MNY](#) [25LC080DT-I/MS](#) [25LC080DT-I/SN](#) [25LC080DT-I/ST](#) [25LC160C-E/MS](#)  
[25LC160C-E/P](#) [25LC160C-E/SN](#) [25LC160C-E/ST](#) [25LC160C-I/MS](#) [25LC160C-I/P](#) [25LC160C-I/SN](#) [25LC160C-I/ST](#)  
[25LC160CT-E/MNY](#) [25LC160CT-E/MS](#) [25LC160CT-E/SN](#) [25LC160CT-E/ST](#) [25LC160CT-I/MNY](#) [25LC160CT-I/MS](#)  
[25LC160CT-I/SN](#) [25LC160CT-I/ST](#) [25LC160D-E/MS](#) [25LC160D-E/P](#) [25LC160D-E/SN](#) [25LC160D-E/ST](#) [25LC160D-](#)  
[I/MS](#) [25LC160D-I/P](#) [25LC160D-I/SN](#) [25LC160D-I/ST](#) [25LC160DT-E/MNY](#) [25LC160DT-E/MS](#) [25LC160DT-E/SN](#)  
[25LC160DT-E/ST](#) [25LC160DT-I/MNY](#) [25LC160DT-I/MS](#) [25LC160DT-I/SN](#) [25LC160DT-I/ST](#)