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FDB024N08BL7 N-Channel PowerTrench[®] MOSFET 80 V, 229 A, 2.4 mΩ

Features

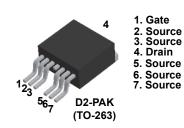
- R_{DS(on)} = 1.7 mΩ (Typ.) @ V_{GS} = 10 V, I_D = 100 A
- Low FOM R_{DS(on)} *Q_G
- Low Reverse Recovery Charge, Q_{rr} = 112 nC
- Soft Reverse Recovery Body Diode
- Enables Highly Efficiency in Synchronous Rectification
- · Fast Switching Speed
- RoHS Compliant
- Qualified according to JEDEC Standards JESD22-A113F and IPC/JEDEC J-STD-020D.1

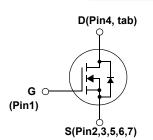
Description

This N-Channel MOSFET is produced using Fairchild Semiconductor's advance PowerTrench[®] process that has been tailored to minimize the on-state resistance while maintaining superior switching performance.

Applications

- Synchronous Rectification for ATX / Server / Telecom PSU
- Battery Protection Circuit
- Motor drives and Uninterruptible Power Supplies





MOSFET Maximum Ratings T_C = 25°C unless otherwise noted

Symbol		FDB024N08BL7	Unit		
V _{DSS}	Drain to Source Voltage	80	V		
V _{GSS}	Gate to Source Voltage	±20	V		
I _D		- Continuous (T _C = 25 ^o C, Silicon Limited)	229*	A	
	Drain Current	- Continuous (T _C = 100 ^o C, Silicon Limited)	162*		
		- Continuous (T _C = 25 ^o C, Package Limited)	120		
I _{DM}	Drain Current	- Pulsed (Note 1)	916	Α	
E _{AS}	Single Pulsed Avalanche En	917	mJ		
dv/dt	Peak Diode Recovery dv/dt	6.0	V/ns		
P _D	Devues Discipation	(T _C = 25°C)	246	W	
	Power Dissipation	- Derate Above 25°C	1.64	W/ºC	
T _J , T _{STG}	Operating and Storage Tem	-55 to +175	°C		
TL	Maximum Lead Temperature 1/8" from Case for 5 Second	300	°C		

*Calculated continuous current based on maximum allowable junction temperature. Package limitation current is 120 A.

Thermal Characteristics

Symbol	Parameter	FDB024N08BL7	Unit
$R_{\theta JC}$	Thermal Resistance, Junction to Case, Max.	0.61	°C/W
$R_{ extsf{ heta}JA}$	Thermal Resistance, Junction to Ambient, Max.	62.5	-0/00

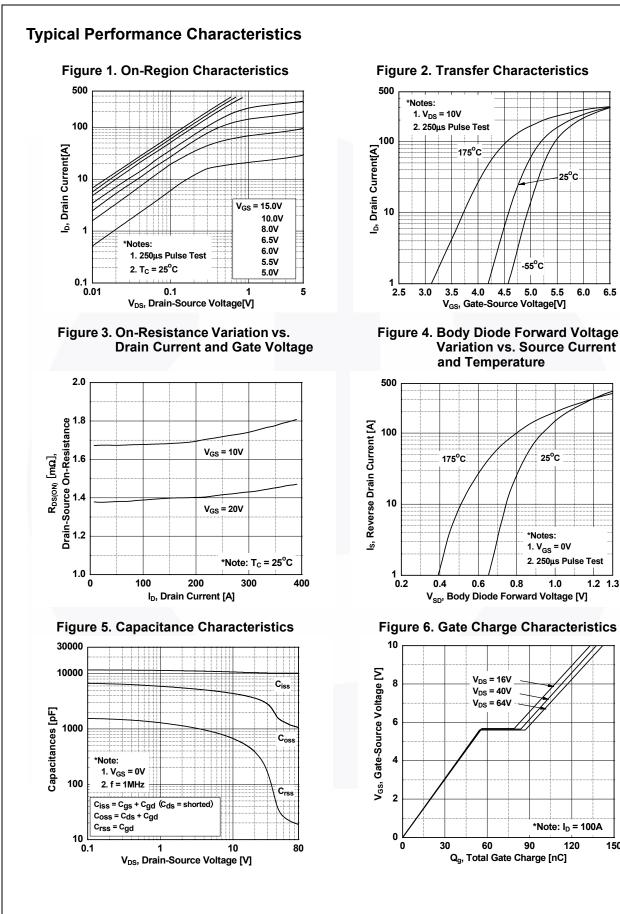
FDB024N08BL7 N-Channel PowerTrench[®] MOSFET

Part Nu	nber	Top Mark	Package	Packing Method	Reel Size	Тар	e Width	Qua	ntity
•		D2PAK-7L	K-7L Tape and Reel 330 mm		24 mm		800 units		
Electrica	l Chara	acteristics T _C = 2	5°C unless of	therwise noted					
Symbol		Parameter		Test Condit	ions	Min.	Тур.	Max.	Unit
Off Charac	teristics	5							
BV _{DSS}	Drain to Source Breakdown Voltage		age	I _D = 250 μA, V _{GS} = 0 V			-	_	V
ΔBV _{DSS}		Breakdown Voltage Temperature				80			
ΔT_J	Coefficient			$I_D = 250 \ \mu$ A, Referenced to 25° C			0.05	-	V/°C
	7			V _{DS} = 64 V, V _{GS} = 0 V		-	-	1	
DSS	Zero Gate Voltage Drain Current		t v	$V_{DS} = 64 \text{ V}, \text{ T}_{C} = 150^{\circ}\text{C}$			-	500	μA
GSS	Gate to Body Leakage Current			$V_{GS} = \pm 20 \text{ V}, V_{DS} = 0 \text{ V}$			-	±100	nA
On Charac	teristics								
V _{GS(th)}	Gate Th	reshold Voltage	,	V _{GS} = V _{DS} , I _D = 250 μ	A	2.5	-	4.5	V
R _{DS(on)}	Static Dr	ain to Source On Resis		$V_{GS} = 10 \text{ V}, \text{ I}_{D} = 100 \text{ A}$		-	1.7	2.4	mΩ
9 _{FS}	Forward	Transconductance		$V_{\rm DS} = 10 \text{ V}, \text{ I}_{\rm D} = 100 \text{ A}$		-	227	-	S
Dynamic C	haracte	ristics					1		1
C _{iss}	- I	pacitance				-	10170	13530	pF
C _{oss}		Capacitance		V _{DS} = 40 V, V _{GS} = 0 V, f = 1 MHz		-	1670	2220	pF
C _{rss}		Transfer Capacitance				-	35	-	pF
C _{oss} (er)		elated Output Capacitar	ce	V _{DS} = 40 V, V _{GS} = 0 V	/	-	3025	_	pF
$Q_{g(tot)}$		te Charge at 10V					137	178	nC
Q _{gs}	-	Source Gate Charge	,	V _{DS} = 40 V, V _{GS} = 10	V,	-	56	-	nC
Q _{gs2}		arge Threshold to Plate		I _D = 100 A (Note 4)			25	-	nC
Q _{gd}		Drain "Miller" Charge				-	28	-	nC
ESR		nt Series Resistance (G	i-S)	f = 1MHz	. ,	-	2.4	-	Ω
Switching	Charact	oristics			L. L.				
t _{d(on)}		Delay Time				-	47	104	ns
t _r		Rise Time		$V_{DD} = 40 \text{ V}, \text{ I}_{D} = 100 \text{ A},$ $V_{GS} = 10 \text{ V}, \text{ R}_{G} = 4.7 \Omega$ (Note 4)			66	142	ns
t _{d(off)}		Delay Time				-	87	184	ns
t _f		Fall Time				_	41	92	ns
	1				(1010-1)	7			
Jrain-Soui		e Characteristics					1		
s	Maximum Continuous Drain to Source Dioc					-	-	229*	A
SM	Maximum Pulsed Drain to Source Diode F						-	916	A
V _{SD}	Drain to Source Diode Forward Voltage			V _{GS} = 0 V, I _{SD} = 100 A			-	1.3	V
t _{rr}		Recovery Time		$V_{GS} = 0 V, V_{DD} = 40 V, I_{SD} = 100 A,$ $dI_F/dt = 100 A/\mu s$		-	80	-	ns
Q _{rr}	Reverse	Recovery Charge	(-	112	-	nC

3. $I_{SD} \le 100$ A, di/dt ≤ 200 A/µs, $V_{DD} \le BV_{DSS}$, starting $T_J = 25^{\circ}C$. 4. Essentially independent of operating temperature typical characteristics.

25°C

6.0 6.5



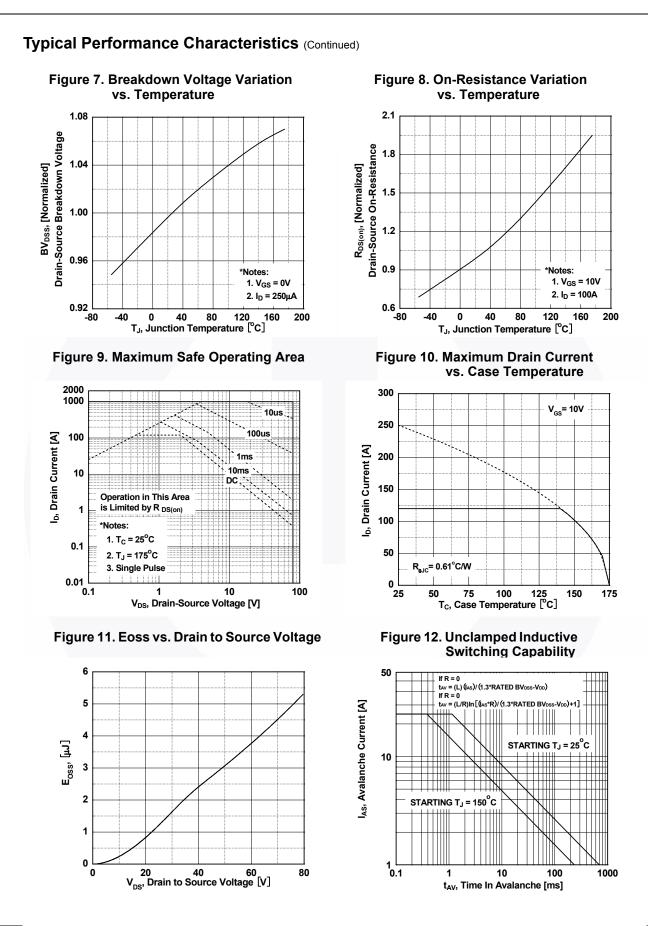
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120

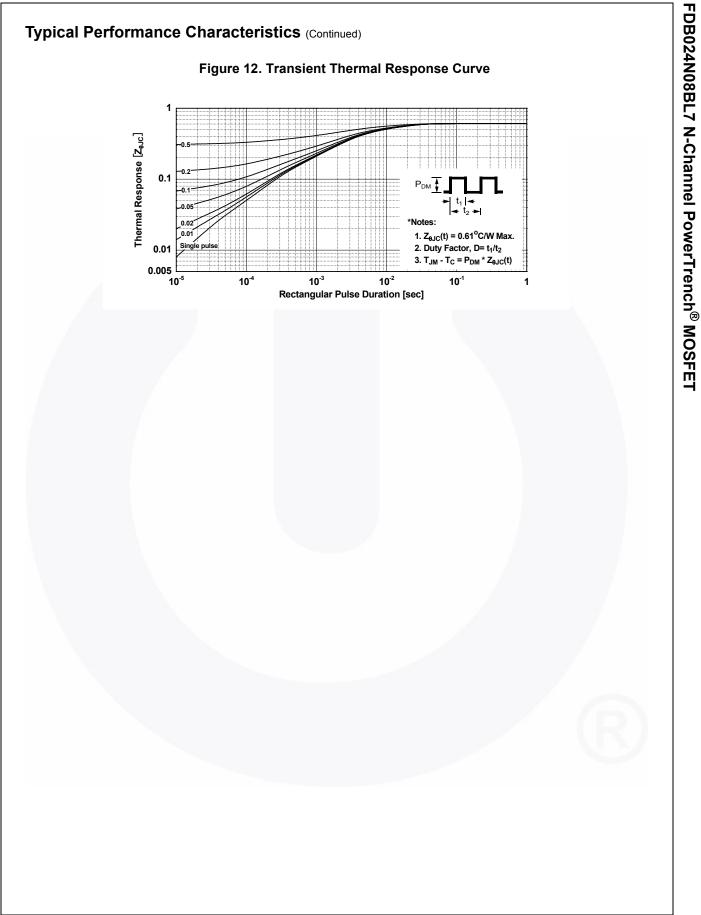
1.2 1.3

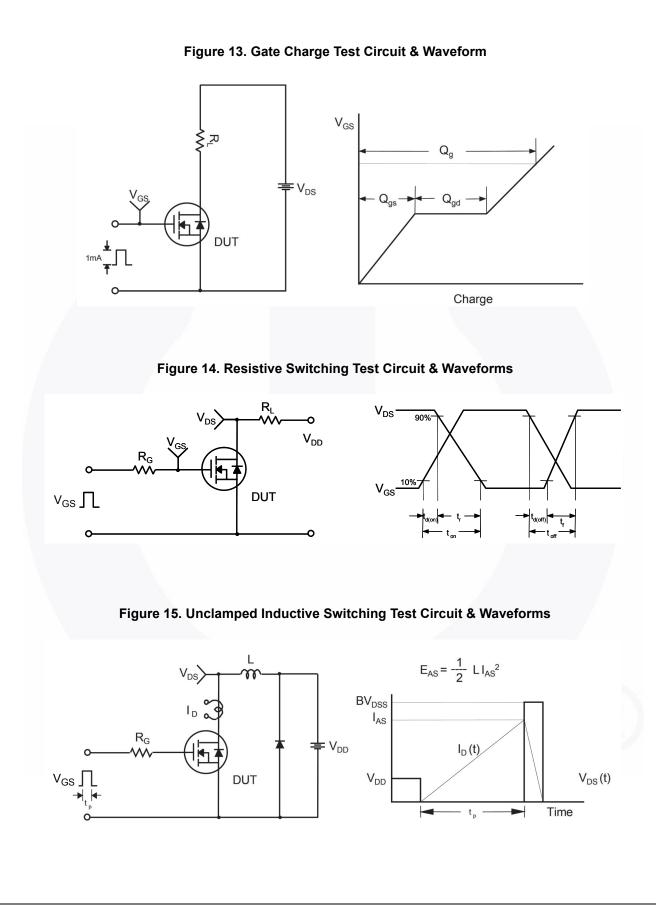
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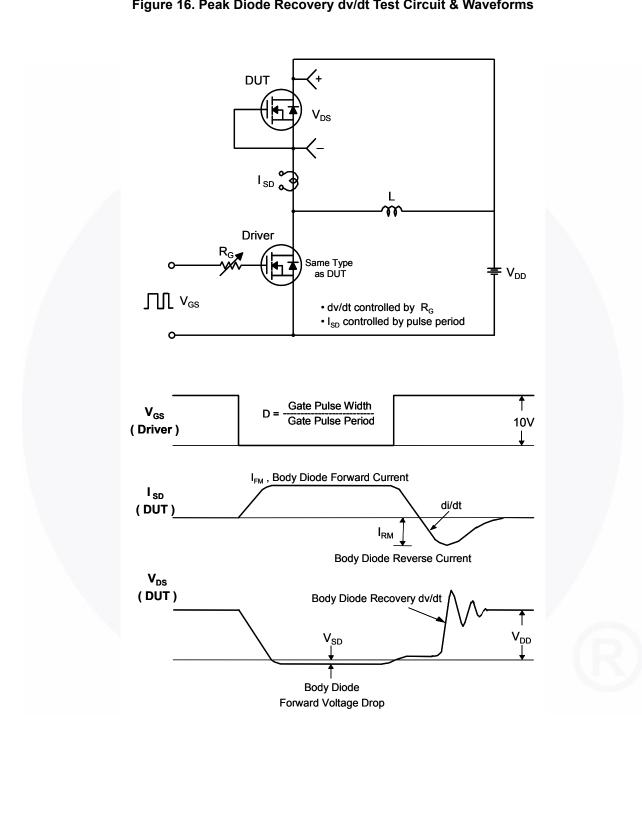


Figure 16. Peak Diode Recovery dv/dt Test Circuit & Waveforms

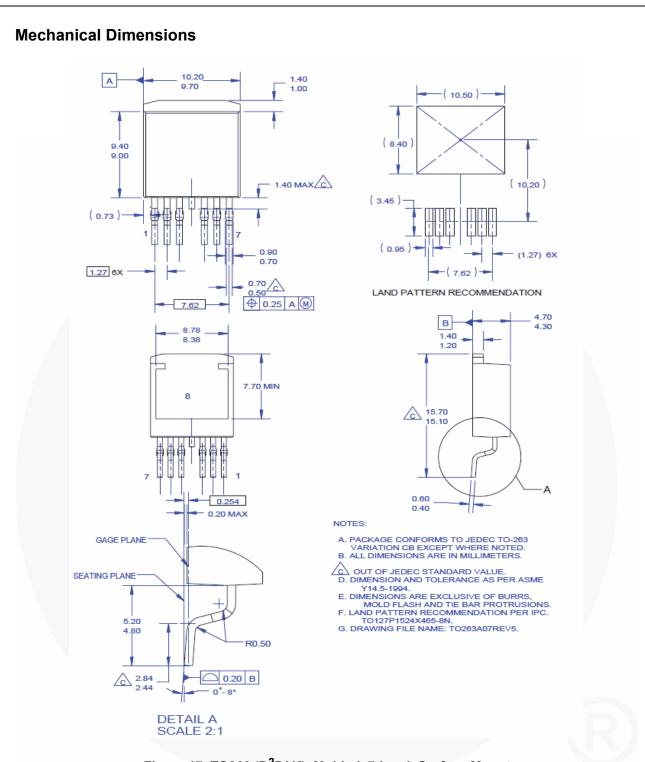


Figure 17. TO263 (D²PAK), Molded, 7-Lead, Surface Mount

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