

STD11NM50N STF11NM50N, STP11NM50N

N-channel 500 V, 0.4 Ω, 8.5 A MDmesh™ II Power MOSFET in DPAK, TO-220FP and TO-220

Features

Order codes	V _{DSS} @T _{Jmax}	R _{DS(on)} max	I _D
STD11NM50N			
STF11NM50N	550 V	< 0.47 Ω	8.5 A
STP11NM50N			

- 100% avalanche tested
- Low input capacitance and gate charge
- Low gate input resistance

Application

Switching applications

Description

These devices are made using the second generation of MDmesh™ technology. This revolutionary Power MOSFET associates a new vertical structure to the company's strip layout to yield one of the world's lowest on-resistance and gate charge. It is therefore suitable for the most demanding high efficiency converters.

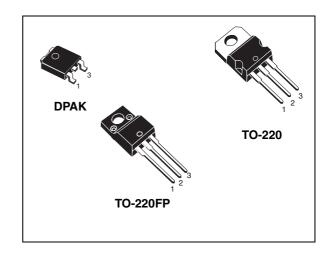


Figure 1. Internal schematic diagram

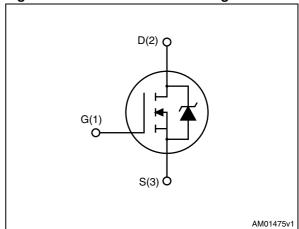


Table 1. Device summary

Order codes	Marking	Package	Packaging
STD11NM50N	11NM50N	DPAK	Tape and reel
STF11NM50N	11NM50N	TO-220FP	Tube
STP11NM50N	11NM50N	TO-220	Tube

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1 Electrical ratings

Table 2. Absolute maximum ratings

Cymbol	Parameter		Unit		
Symbol	Farameter	TO-220	DPAK	TO-220FP	Ollit
V_{DS}	Drain-source voltage (V _{GS} = 0)		500		V
V _{GS}	Gate-source voltage		± 25		٧
I _D	Drain current (continuous) at T _C = 25 °C	8	.5	8.5 ⁽¹⁾	Α
I _D	Drain current (continuous) at T _C = 100 °C	6 6 (1)		6 ⁽¹⁾	Α
I _{DM} ⁽²⁾	Drain current (pulsed)	34 34 ⁽¹⁾		34 ⁽¹⁾	Α
P _{TOT}	Total dissipation at T _C = 25 °C	70	70	25	W
dv/dt (3)	Peak diode recovery voltage slope		15		V/ns
V _{ISO}	Insulation withstand voltage (RMS) from all three leads to external heat sink (t = 1 s; Tc = 25 °C)	ternal heat sink 2500		V	
T _{stg}	Storage temperature	- 55 to 150		°C	
T _j	Max. operating junction temperature		150		°C

- 1. Limited only by maximum temperature allowed
- 2. Pulse width limited by safe operating area
- 3. $I_{SD} \leq 8.5 \text{ A, di/dt} \leq 400 \text{ A/µs, V}_{Peak} < V_{(BR)DSS}, V_{DD} = 80\% V_{(BR)DSS}$

Table 3. Thermal data

Symbol	Parameter		Value		Unit
Symbol	raiailletei	TO-220	DPAK	TO-220FP	Oilit
R _{thj-case}	Thermal resistance junction-case max	1.	79	5	°C/W
R _{thj-amb}	Thermal resistance junction-ambient max	62.5		62.5	°C/W
R _{thj-pcb}	Thermal resistance junction-pcb max ⁽¹⁾		50		°C/W
T _I	Maximum lead temperature for soldering purpose	300		300	°C

^{1.} When mounted on 1inch² FR-4 board, 2 oz Cu

Table 4. Thermal data

Symbol	Parameter	Value	Unit
I _{AR}	Avalanche current, repetetive or not repetetive ⁽¹⁾	3	Α
E _{AS}	Single pulse avalanche energy (2)	150	mJ

- 1. Pulse width limited by T_{JMAX} .
- 2. Starting $T_j = 25$ °C, $I_D = I_{AR}$, $V_{DD} = 50$ V.



2 Electrical characteristics

 $(T_C = 25 \, ^{\circ}C \text{ unless otherwise specified})$

Table 5. On /off states

Symbol	Parameter	Test conditions	Min.	Тур.	Max.	Unit
V _{(BR)DSS}	Drain-source breakdown voltage	I _D = 1 mA, V _{GS} = 0	500			V
I _{DSS}	Zero gate voltage drain current (V _{GS} = 0)	V _{DS} = Max rating V _{DS} = Max rating, T _C =125 °C			1 100	μ Α μ Α
I _{GSS}	Gate-body leakage current (V _{DS} = 0)	V _{GS} = ± 25 V			100	nA
V _{GS(th)}	Gate threshold voltage	$V_{DS} = V_{GS}, I_{D} = 250 \mu A$	2	3	4	V
R _{DS(on)}	Static drain-source on resistance	$V_{GS} = 10 \text{ V}, I_D = 4.5 \text{ A}$		0.4	0.47	Ω

Table 6. Dynamic

Symbol	Parameter	Test conditions	Min.	Тур.	Max.	Unit
C _{iss} C _{oss} C _{rss}	Input capacitance Output capacitance Reverse transfer capacitance	$V_{DS} = 50 \text{ V, f} = 1 \text{ MHz,}$ $V_{GS} = 0$	-	547 42 2	-	pF pF pF
Coss eq. (1)	Output equivalent capacitance	V _{DS} = 0 to 400 V, V _{GS} = 0	-	210	-	pF
R _G	Intrinsic gate resistance	f = 1 MHz open drain	-	5.8	-	Ω
Q _g Q _{gs} Q _{gd}	Total gate charge Gate-source charge Gate-drain charge	$V_{DD} = 400 \text{ V}, I_{D} = 8.5 \text{ A},$ $V_{GS} = 10 \text{ V}$ (see <i>Figure 18</i>)	-	19 3.7 10	-	nC nC nC

^{1.} $C_{oss\ eq.}$ is defined as a constant equivalent capacitance giving the same charging time as C_{oss} when V_{DS} increases from 0 to 80% V_{DS} .

Table 7. Switching times

Symbol	Parameter	Test conditions	Min.	Тур.	Max	Unit
t _{d(on)} t _r t _{d(off)} t _f	Turn-on delay time Rise time Turn-off delay time Fall time	$V_{DD} = 250 \text{ V}, I_D = 4.25 \text{ A},$ $R_G = 4.7 \Omega, V_{GS} = 10 \text{ V}$ (see <i>Figure 19</i>)	-	8 10 33 10	-	ns ns ns ns

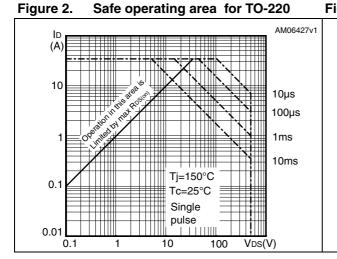
Table 8. Source drain diode

Symbol	Parameter	Test conditions	Min.	Тур.	Max.	Unit
I _{SD}	Source-drain current Source-drain current (pulsed)		-		8.5 34	A A
V _{SD} ⁽²⁾	Forward on voltage	I _{SD} = 8.5 A, V _{GS} = 0	-		1.5	V
t _{rr} Q _{rr} I _{RRM}	Reverse recovery time Reverse recovery charge Reverse recovery current	I _{SD} = 8.5 A, di/dt = 100 A/μs V _{DD} = 60 V (see <i>Figure 22</i>)	-	230 2.1 18		ns μC A
t _{rr} Q _{rr} I _{RRM}	Reverse recovery time Reverse recovery charge Reverse recovery current	$I_{SD} = 8.5 \text{ A, di/dt} = 100 \text{ A/µs}$ $V_{DD} = 60 \text{ V, T}_j = 150 \text{ °C}$ (see <i>Figure 22</i>)	-	275 2.5 18		ns μC A

^{1.} Pulse width limited by safe operating area

^{2.} Pulsed: pulse duration = 300 μ s, duty cycle 1.5%

Electrical characteristics (curves) 2.1



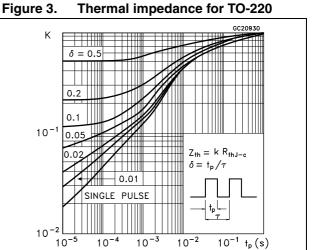
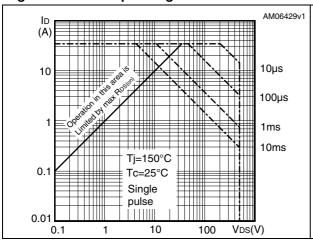


Figure 4. Safe operating area for TO-220FP

Figure 5. Thermal impedance for TO-220FP



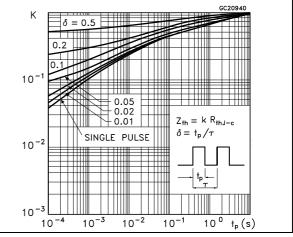
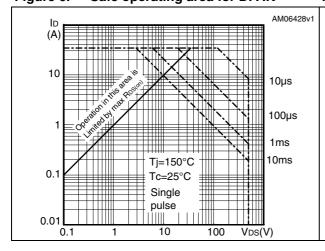
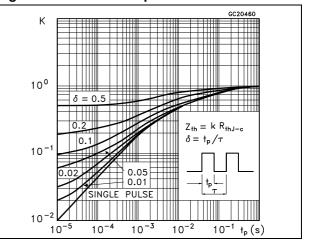


Figure 6. Safe operating area for DPAK

Figure 7. Thermal impedance for DPAK





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Figure 8. Output characteristics

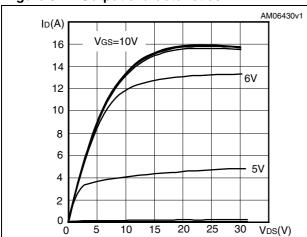


Figure 9. Transfer characteristics

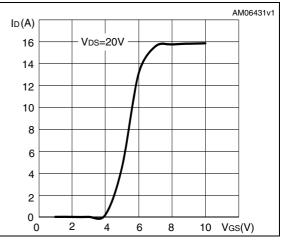
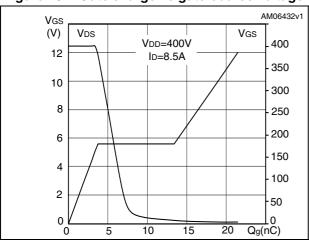


Figure 10. Gate charge vs gate-source voltage Figure 11. Static drain-source on resistance



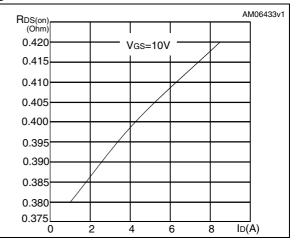
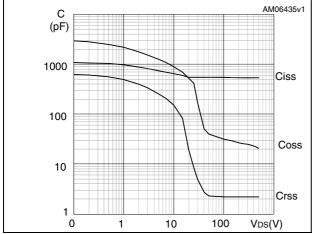
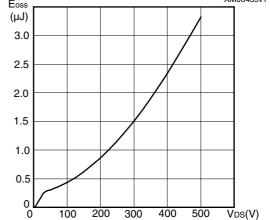


Figure 12. Capacitance variations

Figure 13. Output capacitance stored energy

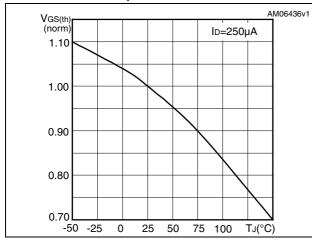
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Figure 14. Normalized gate threshold voltage Figure 15. Normalized on resistance vs vs temperature temperature



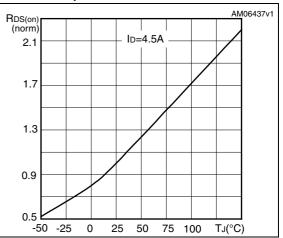
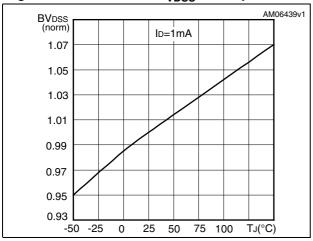


Figure 16. Normalized B_{VDSS} vs temperature



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3 Test circuits

Figure 17. Switching times test circuit for resistive load

Figure 18. Gate charge test circuit

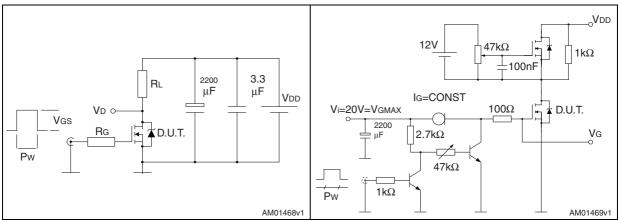


Figure 19. Test circuit for inductive load switching and diode recovery times

Figure 20. Unclamped inductive load test circuit

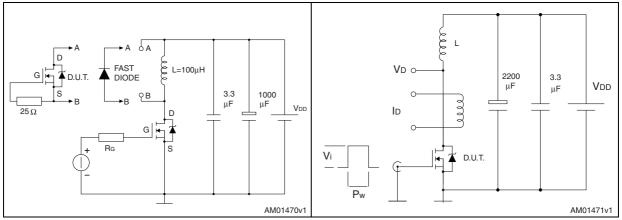
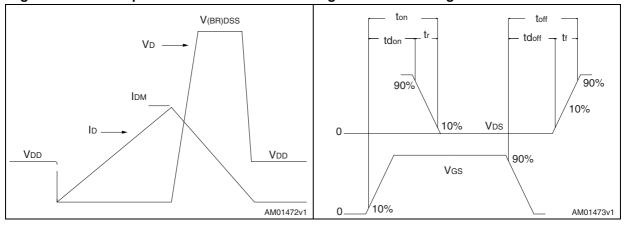


Figure 21. Unclamped inductive waveform

Figure 22. Switching time waveform



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4 Package mechanical data

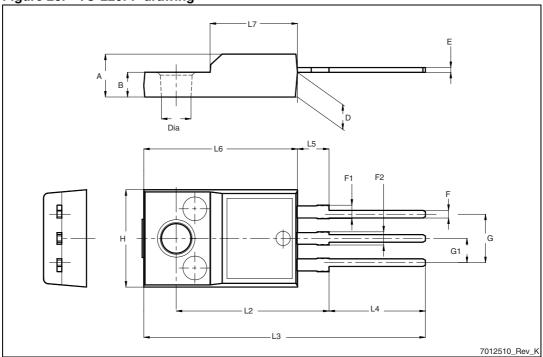
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Table 9. TO-220FP mechanical data

Dim		mm	
Dim.	Min.	Тур.	Max.
А	4.4		4.6
В	2.5		2.7
D	2.5		2.75
E	0.45		0.7
F	0.75		1
F1	1.15		1.70
F2	1.15		1.70
G	4.95		5.2
G1	2.4		2.7
Н	10		10.4
L2		16	
L3	28.6		30.6
L4	9.8		10.6
L5	2.9		3.6
L6	15.9		16.4
L7	9		9.3
Dia	3		3.2

Figure 23. TO-220FP drawing



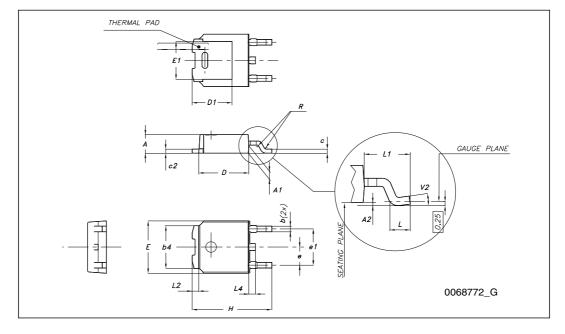
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TO-252 (DPAK) mechanical data

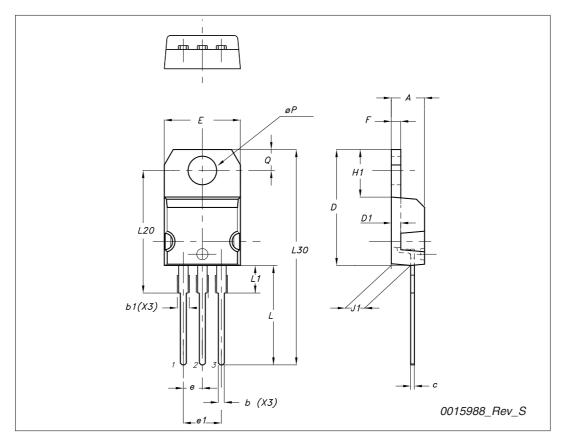
DIM.	mm.			
	min.	typ	max.	
Α	2.20		2.40	
A1	0.90		1.10	
A2	0.03		0.23	
b	0.64		0.90	
b4	5.20		5.40	
С	0.45		0.60	
c2	0.48		0.60	
D	6.00		6.20	
D1		5.10		
E	6.40		6.60	
E1		4.70		
е		2.28		
e1	4.40		4.60	
Н	9.35		10.10	
L	1			
L1		2.80		
L2		0.80		
L4	0.60		1	
R		0.20		
V2	0 °		8 °	



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TO-220 type A mechanical data

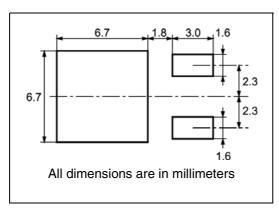
Dim	mm		
	Min	Тур	Max
A	4.40		4.60
b	0.61		0.88
b1	1.14		1.70
С	0.48		0.70
D	15.25		15.75
D1		1.27	
E	10		10.40
е	2.40		2.70
e1	4.95		5.15
F	1.23		1.32
H1	6.20		6.60
J1	2.40		2.72
L	13		14
L1	3.50		3.93
L20		16.40	
L30		28.90	
ØP	3.75		3.85
Q	2.65		2.95



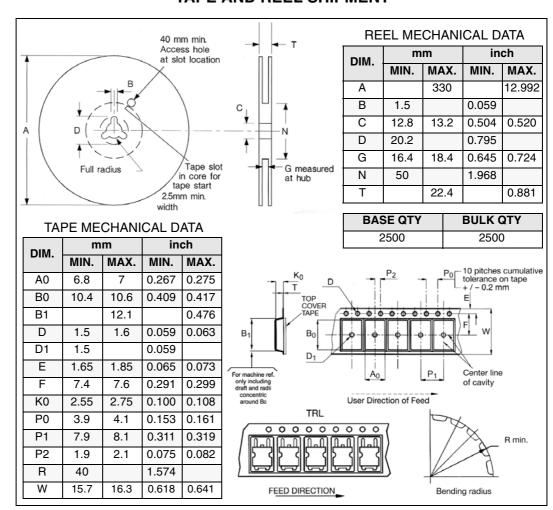


5 Packaging mechanical data

DPAK FOOTPRINT



TAPE AND REEL SHIPMENT



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6 Revision history

Table 10. Document revision history

Date	Revision	Changes	
22-Feb-2010	1	First release.	
26-Apr-2010	2	Updated Table 8: Source drain diode.	
24-Nov-2010	3	New value inserted in <i>Table 6: Dynamic</i> .	

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