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Please note: As part of the Fairchild Semiconductor integration, some of the Fairchild orderable part numbers will need to change in order to meet ON Semiconductor's system requirements. Since the ON Semiconductor product management systems do not have the ability to manage part nomenclature that utilizes an underscore (\_), the underscore (\_) in the Fairchild part numbers will be changed to a dash (-). This document may contain device numbers with an underscore (\_). Please check the ON Semiconductor website to verify the updated device numbers. The most current and up-to-date ordering information can be found at <a href="https://www.onsemi.com">www.onsemi.com</a>. Please email any questions regarding the system integration to <a href="https://www.onsemi.com">Fairchild\_questions@onsemi.com</a>.

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## Dual 1-of-4 Decoder / Demultiplexer

## **General Description**

The AC/ACT139 is a high-speed, dual 1-of-4 decoder/demultiplexer. The device has two independent decoders, each accepting two inputs and providing four mutually-exclusive active-LOW outputs. Each decoder has an active-LOW Enable input which can be used as a data input for a 4-output demultiplexer. Each half of the AC/ACT139 can be used as a function generator providing all four minterms of two variables.

### Features

- I<sub>CC</sub> Reduced by 50%
- Multifunction Capability
- Two Completely Independent 1-of-4 Decoders
- Active LOW Mutually Exclusive Outputs
- Outputs Source/Sink 24 mA
- ACT139 has TTL-compatible Inputs

## **ORDERING CODE:**

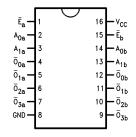


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OKDERING COL	)L.				
Order Number	Case Number	Package Description			
74AC139SC	751BG	16-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-012, 0.150" Narrow Body			
74AC139SJ	565BF	16-Lead Small Outline Package (SOIC), EIAJ Type II, 5.3 mm Wide			
74AC139MTC	948AH	16-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 4.4 mm Wide			
74AC139PC	648	16-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300" Wide			
74ACT139SC	751BG	16-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-012, 0.150" Narrow Body			
74ACT139SJ	565BF	16-Lead Small Outline Package (SOIC), EIAJ Type II, 5.3 mm Wide			
74ACT139MTC	948AH	16-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 4.4 mm Wide			
74ACT139PC	648	16-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300" Wide			

NOTE: Device also available in Tape and Reel. Specify by appending suffix letter "X" to the ordering code.

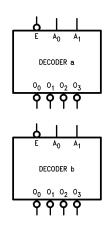
## **CONNECTION DIAGRAM**



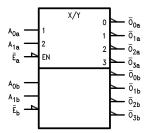
### **PIN DESCRIPTIONS**

Pin Names	Description		
A <sub>0</sub> , A <sub>1</sub>	Address Inputs		
Ē	Enable Inputs		
$\overline{O}_0 - \overline{O}_3$	Outputs		

### Logic Symbol/s







#### **TRUTH TABLE/S**

	Inputs			Outputs				
Ē	A <sub>0</sub>	A <sub>1</sub>	$\overline{O}_0$	<u>0</u> 1	$\overline{O}_2$	$\overline{O}_3$		
Н	Х	Х	Н	Н	Н	Н		
L	L	L	L	Н	Н	Н		
L	Н	L	Н	L	Н	Н		
L	L	Н	Н	Н	L	Н		
L	Н	Н	Н	Н	Н	L		

H = HIGH Voltage Level

L = LOW Voltage Level

X = Immaterial

## **Functional Description**

The AC/ACT139 is a high–speed dual 1–of–4 decoder/ demultiplexer. The device has two independent decoders, each of which accepts two binary weighted inputs  $(A_0-A_1)$ and provides four mutually exclusive active–LOW outputs  $(O_0-O_3)$ . Each decoder has an active–LOW enable (E). When E is HIGH all outputs are forced HIGH. The enable can be used as the data input for a 4–output demultiplexer application. Each half of the AC/ACT139 generates all four minterms of two variables. These four minterms are useful in some applications, replacing multiple gate functions as shown in Figure 1, and thereby reducing the number of packages required in a logic network.

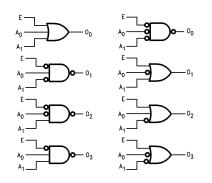
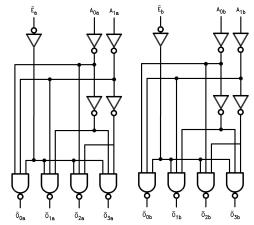


Figure 1. Gate Functions (Each Half)

### Logic Diagram/s



Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

## ABSOLUTE MAXIMUM RATINGS

Supply Voltage (V <sub>CC</sub> )	–0.5 V to +7.0 V
DC Input Diode Current (I <sub>IK</sub> ) $V_I = -0.5 V$ $V_I = V_{CC} + 0.5 V$	–20 mA +20 mA
DC Input Voltage (VI)	-0.5 V to V <sub>CC</sub> + 0.5 V
DC Output Diode Current ( $I_{OK}$ ) $V_O = -0.5 V$ $V_O = V_{CC} + 0.5 V$	–20 mA +20 mA
DC Output Voltage (V <sub>O</sub> )	-0.5 V to V <sub>CC</sub> + 0.5 V
DC Output Source or Sink Current (I <sub>O</sub> )	±50 mA
DC $V_{CC}$ or Ground Current per Output Pin (I <sub>CC</sub> or I <sub>GND</sub> )	±50 mA
Storage Temperature (T <sub>STG</sub> )	–65°C to +150°C
Junction Temperature (T <sub>J</sub> ) PDIP	140°C

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

#### **RECOMMENDED OPERATING CONDITIONS**

Supply Voltage (V <sub>CC</sub> ) AC ACT	2.0 V to 6.0 V 4.5 V to 5.5 V
Input Voltage (VI)	0 V to $V_{CC}$
Output Voltage (V <sub>O</sub> )	0 V to V <sub>CC</sub>
Operating Temperature (T <sub>A</sub> )	−40°C to +85°C
$\begin{array}{l} \mbox{Minimum Input Edge Rate } (\Delta V / \Delta t) \\ \mbox{AC Devices} \\ \mbox{V_{IN} from 30\% to 70\% of V_{CC}} \\ \mbox{V_{CC}} @ 3.3 \ V, 4.5 \ V, 5.5 \ V \end{array}$	125 mV/ns
$\begin{array}{l} \mbox{Minimum Input Edge Rate } (\Delta V / \Delta t) \\ \mbox{ACT Devices} \\ \mbox{V}_{IN} \mbox{ from } 0.8 \ V \ to \ 2.0 \ V \\ \ \ \ \ \ \ \ \ \ \ \ \ \ \ \ \ \$	125 mV/ns

Functional operation above the stresses listed in the Recommended Operating Ranges is not implied. Extended exposure to stresses beyond the Recommended Operating Ranges limits may affect device reliability.

		v <sub>cc</sub>	T <sub>A</sub> = -	+25°C	$T_A = -40^{\circ}C$ to $+85^{\circ}C$		
Symbol	Parameter	(V)	Typ Guaranteed Limits		Units	Conditions	
V <sub>IH</sub>	Minimum HIGH Level	3.0	1.5	2.1	2.1	V	V <sub>OUT</sub> = 0.1 V
	Input Voltage	4.5	2.25	3.15	3.15		or V <sub>CC</sub> – 0.1 V
		5.5	2.75	3.85	3.85		
V <sub>IL</sub>	Maximum LOW Level	3.0	1.5	0.9	0.9	V	V <sub>OUT</sub> = 0.1 V
	Input Voltage	4.5	2.25	1.35	1.35		or V <sub>CC</sub> – 0.1 V
		5.5	2.75	1.65	1.65		
V <sub>OH</sub>	Minimum HIGH Level	3.0	2.99	2.9	2.9	V	I <sub>OUT</sub> = -50 μA
	Output Voltage	4.5	4.49	4.4	4.4		
		5.5	5.49	5.4	5.4		
		3.0		2.56	2.46	V	$V_{IN} = V_{IL} \text{ or } V_{IH}$ $I_{OH} = -12 \text{ mA}$ $I_{OH} = -24 \text{ mA}$ $I_{OH} = -24 \text{ mA} \text{ (Note 1)}$
		4.5		3.86	3.76		
		5.5		4.86	4.76		
V <sub>OL</sub>	Maximum LOW Level	3.0	0.002	0.1	0.1	V	I <sub>OUT</sub> = 50 μA
	Output Voltage	4.5	0.001	0.1	0.1		
		5.5	0.001	0.1	0.1		
		3.0		0.36	0.44	V	$V_{IN} = V_{IL} \text{ or } V_{IH}$
		4.5		0.36	0.44		l <sub>OL</sub> = 12 mA l <sub>OL</sub> = 24 mA
		5.5		0.36	0.44		$I_{OL} = 24 \text{ mA} (\text{Note 1})$
I <sub>IN</sub> (Note 3)	Maximum Input Leakage Current	5.5		±0.1	±1.0	μΑ	$V_I = V_{CC}, GND$
I <sub>OLD</sub>	Minimum Dynamic	5.5			75	mA	V <sub>OLD</sub> = 1.65 V Max
I <sub>OHD</sub>	Output Current (Note 2)	5.5			-75	mA	V <sub>OHD</sub> = 3.85 V Min
<sub>CC</sub> (Note 3)	Maximum Quiescent Supply Current	5.5		4.0	40.0	μΑ	$V_{IN} = V_{CC}$ or GND

## DC ELECTRICAL CHARACTERISTICS FOR AC

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions. 1. All outputs loaded; thresholds on input associated with output under test.

2. Maximum test duration 2.0 ms, one output loaded at a time. 3.  $I_{IN}$  and  $I_{CC}$  @ 3.0 V are guaranteed to be less than or equal to the respective limit @ 5.5 V V<sub>CC</sub>.

		v <sub>cc</sub>	T <sub>A</sub> = -	⊦25°C	$T_A = -40^{\circ}C$ to +85°C			
Symbol	Parameter	(V)	Тур С		Suaranteed Limits	Units	Conditions	
VIH	Minimum HIGH Level	4.5	1.5	2.0	2.0	V	V <sub>OUT</sub> = 0.1 V	
	Input Voltage	5.5	1.5	2.0	2.0		or V <sub>CC</sub> – 0.1 V	
VIL	Maximum LOW Level	4.5	1.5	0.8	0.8	V	V <sub>OUT</sub> = 0.1 V	
	Input Voltage	5.5	1.5	0.8	0.8		or V <sub>CC</sub> – 0.1 V	
V <sub>OH</sub>	Minimum HIGH Level	4.5	4.49	4.4	4.4	V	I <sub>OUT</sub> = –50 μA	
	Output Voltage	5.5	5.49	5.4	5.4			
		4.5		3.86	3.76	V	$V_{IN} = V_{IL} \text{ or } V_{IH}$	
		5.5		4.86	4.76		I <sub>OH</sub> = -24 mA I <sub>OH</sub> = -24 mA (Note 4)	
V <sub>OL</sub>	Maximum LOW Level	4.5	0.001	0.1	0.1	V	I <sub>OUT</sub> = 50 μA	
	Output Voltage	5.5	0.001	0.1	0.1			
		4.5		0.36	0.44	V	$V_{IN} = V_{IL} \text{ or } V_{IH}$ $I_{OL} = 24 \text{ mA}$	
		5.5		0.36	0.44		$I_{OL} = 24 \text{ mA} \text{ (Note 4)}$	
I <sub>IN</sub>	Maximum Input Leakage Current	5.5		±0.1	±1.0	μΑ	$V_I = V_{CC}, GND$	
ICCT	Maximum I <sub>CC</sub> /Input	5.5	0.6		1.5	mA	$V_{I} = V_{CC} - 2.1 V$	
I <sub>OLD</sub>	Minimum Dynamic	5.5			75	mA	V <sub>OLD</sub> = 1.65 V Max	
I <sub>OHD</sub>	Output Current (Note 5)	5.5			-75	mA	V <sub>OHD</sub> = 3.85 V Min	
I <sub>CC</sub>	Maximum Quiescent Supply Current	5.5		4.0	40.0	μΑ	$V_{IN} = V_{CC}$ or GND	

## DC ELECTRICAL CHARACTERISTICS FOR ACT

All outputs loaded; thresholds on input associated with output under test.
 Maximum test duration 2.0 ms, one output loaded at a time.

## AC ELECTRICAL CHARACTERISTICS FOR AC

		V <sub>cc</sub>	-	Γ <sub>A</sub> = +25°	C	T <sub>A</sub> = -40°	C to +85°C	
		(V)		C <sub>L</sub> = 50 pl	F	C <sub>L</sub> = 50 pF		
Symbol	Parameter	(Note 6)	Min	Тур	Max	Min	Max	Units
t <sub>PLH</sub>	Propagation Delay	3.3	4.0	8.0	11.5	3.5	13.0	ns
	$A_n$ to $\overline{O}_n$	5.0	3.0	6.5	8.5	2.5	9.5	
t <sub>PHL</sub>	Propagation Delay	3.3	3.0	7.0	10.0	2.5	11.0	ns
	$A_n$ to $\overline{O}_n$	5.0	2.5	5.5	7.5	2.0	8.5	1
t <sub>PLH</sub>	Propagation Delay	3.3	4.5	9.5	12.0	3.5	13.0	ns
	$\overline{E}_n$ to $\overline{O}_n$	5.0	3.5	7.0	8.5	3.0	10.0	1
t <sub>PHL</sub>	Propagation Delay	3.3	4.0	8.0	10.0	3.0	11.0	ns
	$\overline{E}_n$ to $\overline{O}_n$	5.0	2.5	6.0	7.5	2.5	8.5	1

6. Voltage Range 3.3 is 3.3 V  $\pm$  0.3 V. Voltage Range 5.0 is 5.0 V  $\pm$  0.5 V.

## AC ELECTRICAL CHARACTERISTICS FOR ACT

		V <sub>cc</sub>	٦	Γ <sub>A</sub> = +25°0	C	T <sub>A</sub> = −40°0		
		(V)	(	C <sub>L</sub> = 50 pl	F	C <sub>L</sub> =	50 pF	
Symbol	Parameter	(Note 7)	Min	Тур	Max	Min	Max	Units
t <sub>PLH</sub>	Propagation Delay $A_n$ to $\overline{O}_n$	5.0	1.5	6.0	8.5	1.5	9.5	ns
t <sub>PHL</sub>	Propagation Delay $A_n$ to $\overline{O}_n$	5.0	1.5	6.0	9.5	1.5	10.5	ns
t <sub>PLH</sub>	$ \begin{array}{c} Propagation \ Delay \\ \overline{E}_n \ to \ \overline{O}_n \end{array} $	5.0	2.5	7.0	10.0	2.0	11.0	ns
t <sub>PHL</sub>	$\frac{Propagation}{\overline{E}_n} to  \overline{O}_n$	5.0	2.0	7.0	9.5	1.5	10.5	ns

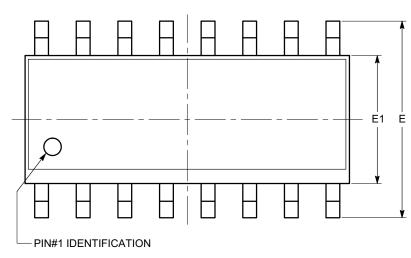
7. Voltage Range 5.0 is 5.0 V  $\pm$  0.5 V

## CAPACITANCE

Symbol	pol Parameter		Units	Conditions
C <sub>IN</sub>	C <sub>IN</sub> Input Capacitance		pF	V <sub>CC</sub> = OPEN
C <sub>PD</sub>	C <sub>PD</sub> Power Dissipation Capacitance		pF	$V_{CC} = 5.0V$

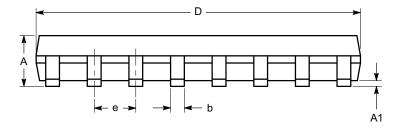
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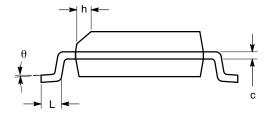
SOIC-16, 150 mils CASE 751BG-01 ISSUE O



SYMBOL	MIN	NOM	MAX
А	1.35		1.75
A1	0.10		0.25
b	0.33		0.51
с	0.19		0.25
D	9.80	9.90	10.00
E	5.80	6.00	6.20
E1	3.80	3.90	4.00
е		1.27 BSC	
h	0.25		0.50
L	0.40		1.27
θ	0°		8°

TOP VIEW





SIDE VIEW

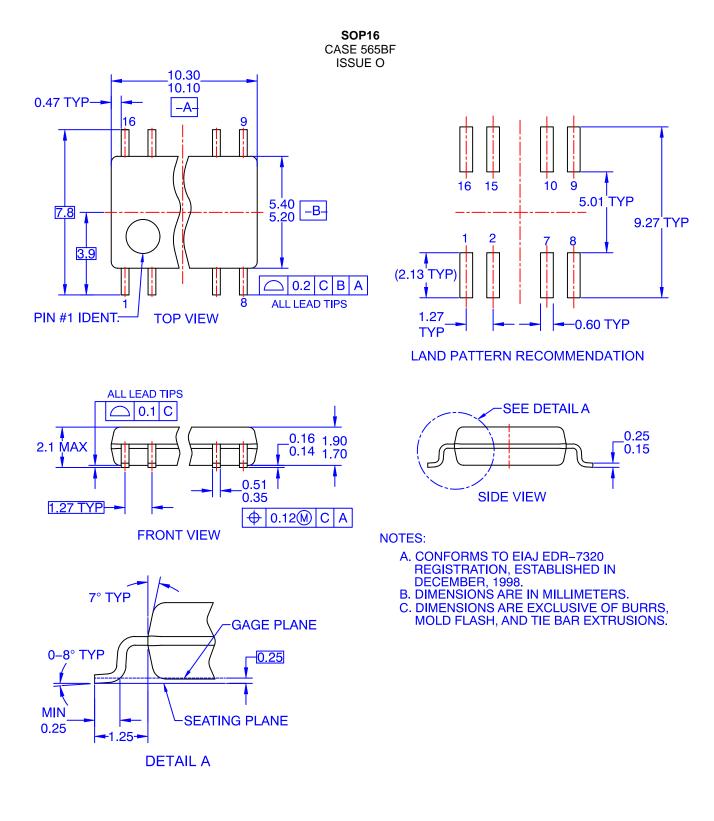
END VIEW

Notes:

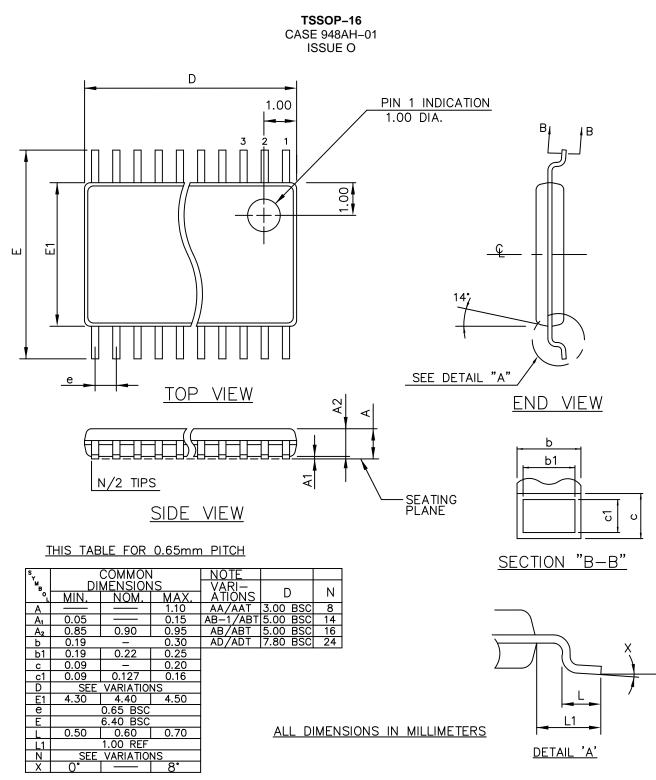
(1) All dimensions are in millimeters. Angles in degrees.

(2) Complies with JEDEC MS-012.

## PACKAGE DIMENSIONS



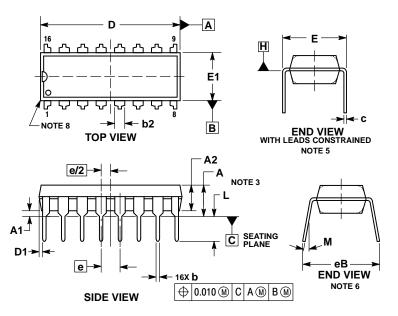
## PACKAGE DIMENSIONS



MOLD FLASH OR PROTRUSIONS SHALL NOT EXCEED 0.15mm ON D PER SIDE

#### PACKAGE DIMENSIONS

#### PDIP-16 CASE 648-018 **ISSUE V**



NOTES:

- 3
- DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994. DIMENSIONING DIMENSION: INCHES. DIMENSIONS A, A1 AND L ARE MEASURED WITH THE PACK-AGE SEATED IN JEDEC SEATING PLANE GAUGE GS-3. DIMENSIONS D, D1 AND E1 DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS. MOLD FLASH OR PROTRUSIONS ARE 4
- NOT TO EXCEED 0.10 INCH. DIMENSION E IS MEASURED AT A POINT 0.015 BELOW DATUM 5. PLANE H WITH THE LEADS CONSTRAINED PERPENDICULAR TO DATUM C.
- DIMENSION 6 IS MEASURED AT THE LEAD TIPS WITH THE LEADS UNCONSTRAINED. 6
- DATUM PLANE H IS COINCIDENT WITH THE BOTTOM OF THE LEADS, WHERE THE LEADS EXIT THE BODY. PACKAGE CONTOUR IS OPTIONAL (ROUNDED OR SQUARE
- 8 CORNERS)

			·		
	INC	HES	MILLIM	ETERS	
DIM	MIN	MIN MAX		MAX	
Α		0.210		5.33	
A1	0.015		0.38		
A2	0.115	0.195	2.92	4.95	
b	0.014	0.022	0.35	0.56	
b2	0.060	) TYP	1.52 TYP		
С	0.008	0.014	0.20	0.36	
D	0.735	0.775	18.67	19.69	
D1	0.005		0.13		
Е	0.300	0.325	7.62	8.26	
E1	0.240	0.280	6.10	7.11	
е	0.100	BSC	2.54	BSC	
eB		0.430		10.92	
L	0.115	0.150	2.92	3.81	
М		10°		10°	

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