NOVOSENSE
纳芯微电子

NCA9555

16-bit I2C-bus I/O port with interrupt

Datasheet (EN) 1.3

Product Overview

The NCA9555 is a 24-pin CMOS device that provides 16 bits of general-purpose parallel Input/Output (GPIO) expansion for I2C-bus applications. It provides a simple solution when additional I/O is needed for ACPI power switches, sensors, push buttons, LEDs, fans, etc.

The NCA9555 consists of two 8-bit Configuration (Input or Output selection); Input, Output and Polarity Inversion (active HIGH or active LOW operation) registers. The system master can enable the I/Os as either inputs or outputs by writing to the I/O configuration bits. The data for each Input or Output is kept in the corresponding Input or Output register. The polarity of the read register can be inverted with the Polarity Inversion register. All registers can be read by the system master.

The NCA9555 open-drain interrupt output is activated when any input state differs from its corresponding input port register state and is used to indicate to the system master that an input state has changed. The power-on reset sets the registers to their default values and initializes the device state machine.

Three hardware pins (A0, A1, A2) vary the fixed I2C-bus address and allow up to eight devices to share the same I2C-bus.

Key Features

- Operating power supply voltage range of 2.3 V to 5.5 V
- 5 V tolerant I/Os
- I2C to Parallel Port Expander
- Polarity Inversion register
- Active LOW interrupt output
- Compatible With Most Microcontrollers
- Address by Three Hardware Address Pins for Use of up to Eight Devices
- Latched Outputs With High-Current Drive Capability for Directly Driving LEDs
- Low standby current
- Noise filter on SCL/SDA inputs
- No glitch on power-up
- Internal power-on reset
- 16 I/O pins which default to 16 inputs
- 0 Hz to 400 kHz clock frequency
- ESD protection exceeds 2000 V HBM, 200 V MM, and 1000 V CDM
- Latch-up testing exceeds 100 mA

Applications

- GPIO expansion for I2C-bus applications
- Servers
- Routers (Telecom Switching Equipment)
- Personal Computers
- Personal Electronics
- Products with GPIO-Limited Processors

Device Information

Part Number	*Package*	*Body Size*
NCA9555	TSSOP24	7.80mm*4.40mm

Functional Block Diagrams

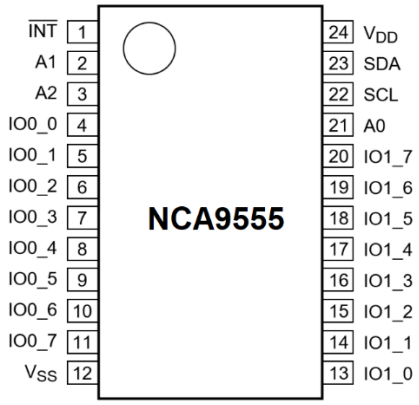

Figure 1. NCA9555 Block Diagram

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1. Pin Configuration and Functions

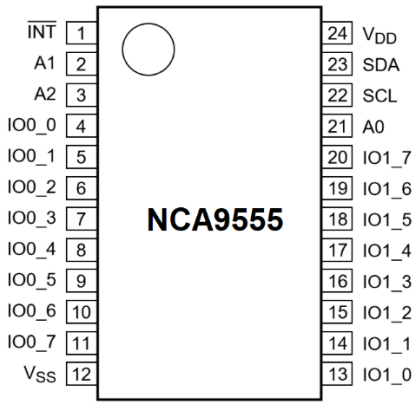


Figure 1.1. NCA9555 Package

Table 1.1. Pin Description

Symbol	*Pin*	*Description*
/INT	1	interrupt output (open-drain)
A1	2	address input 1
A2	3	address input 2
IO0_0	4	port 0 input/output
IO0_1	5	
IO0_2	6	
IO0_3	7	
IO0_4	8	
IO0_5	9	
IO0_6	10	
IO0_7	11	
VSS	12	supply ground
IO1_0	13	port 1 input/output
IO1_1	14	
IO1_2	15	
IO1_3	16	
IO1_4	17	
IO1_5	18	
IO1_6	19	
IO1_7	20	
A0	21	address input 0
SCL	22	serial clock line
SDA	23	serial data line
VDD	24	supply voltage

2. Absolute Maximum Ratings

Parameters	*Symbol*	*Min*	*Max*	*Unit*	*Conditions*
Supply voltage	V_{DD}	-0.5	+6.0	V	
Voltage on an input/output pin	$V_{I/O}$	VSS-0.5	6.0	V	
Output current	I_O	-	±50	mA	On an I/O pin
Input current	I_I	-	±20	mA	
Supply current	I_{DD}	-	160	mA	
Ground supply current	I_{SS}	-	200	mA	
Total power dissipation	P_{tot}	-	200	mW	
Maximum junction temperature	$T_{j(max)}$	-	125	℃	
Storage temperature	T_{stg}	-65	+150	℃	
Ambient temperature	T_{amb}	-40	+85	℃	Operating

3. Recommended Operating Conditions

Parameters	*Symbol*	*Min*	*Max*	*Unit*	*Conditions*
Supply voltage	V_{CCA}	2.3		5.5	V
High-level input voltage	V_{IH}	0.7*VCC		5.5	V
Low-level input voltage	V_{IL}	-0.5		0.3*VCC	V
High-level output current	I_{OH}			-10	mA
Low-level output current(P00-P07,P10-P17)	I_{OL}			10	mA
Low-level output current(/INT,SDA)	I_{OL}			3.5	mA
Operating free-air temperature	T_A	-40		85	℃

4. Thermal Information

Parameters	*Symbol*	*SOW-16*	*Unit*
Junction-to-ambient thermal resistance	θ_{JA}	108.8	℃/W
Junction-to-case(top) thermal resistance	$\theta_{JC(top)}$	54	
Junction-to-board thermal resistance	θ_{JB}	62.8	

5. SPECIFICATIONS

5.1. Electrical characteristics

V_{CC} = 2.3V to 5.5V;T_{amb} = -40℃ to +85℃; unless otherwise noted.

Parameters	*Symbol*	*Min*	*Typ*	*Max*	*Unit*	*Conditions*
Supplies						
Supply voltage Range	V_{DD}	2.3	-	5.5	V	
Power On Reset [1]	V_{POR}	-	0.94	1.5	V	no load; VI = VDD or VSS
Supply current	I_{DD}	-	5.74	90	µA	Operating mode; V_{DD} = 5.5 V; no load; f_{SCL} = 100 kHz
Standby current	I_{stb}	-	0.9	1.5	mA	Standby mode; V_{DD} = 5.5 V; no load; V_I = V_{SS}; f_{SCL} = 0 kHz; I/O = inputs
		-	0.25	1	µA	Standby mode; VDD = 5.5 V; no load; V_I = V_{DD}; f_{SCL} = 0 kHz; I/O = inputs
Input SCL; Input and Output SDA						
LOW-level input voltage	V_{IL}	-0.5	-	0.3*V_{DD}	V	
HIGH-level input voltage	V_{IH}	0.7*V_{DD}	-	5.5	V	
LOW-level output current	I_{OL}	3	-	-	mA	V_{DD} = 2.3 V to 5.5 V; V_{OL} = 0.4 V
Input leakage current	I_L	-1	-	+1	µA	V_{DD} = 2.3 V to 5.5 V; V_I = V_{DD} or V_{SS}
Input capacitance	C_i	-	6	10	pF	V_I = V_{SS}
I/Os						
LOW-level input voltage	V_{IL}	-0.5	-	0.3*V_{DD}	V	
HIGH-level input voltage	V_{IH}	0.7*V_{DD}	-	5.5	V	
LOW-level output current	I_{OL}	8	13 to 23	-	mA	VDD = 2.3 V to 5.5 V; VOL = 0.5 V[2]
		10	16 to 32	-	mA	VDD = 2.3 V to 5.5 V; VOL = 0.7 V[2]
	V_{OH}	1.8	-	-	V	IOH = -8 mA; VDD = 2.3 V[3]

HIGH-level output voltage		1.7	-	-	V	IOH = -10 mA; VDD = 2.3 V[3]
		2.6	-	-	V	IOH = -8 mA; VDD = 3.0 V[3]
		2.5	-	-	V	IOH = -10 mA; VDD = 3.0 V[3]
		4.3	-	-	V	IOH = -8 mA; VDD = 4.75V[3]
		4.0	-	-	V	IOH = -10 mA; VDD = 4.75V[3]
HIGH-level input leakage current	I_{LIH}	-	-	1	μA	VDD = 5.5 V; VI = VDD
LOW-level input leakage current	I_{LIL}	-	-	-100	μA	VDD = 5.5 V; VI = VSS
Input capacitance	C_i	-	3.7	5	pF	
Output capacitance	Co	-	3.7	5	pF	
Interrupt $\overline{INT}$						
LOW-level output current	I_{OL}	3	-	-	mA	VDD = 2.3 V to 5.5 V; VOL=0.4V
Select Inputs A0, A1, A2						
LOW-level input voltage	V_{IL}	-0.5	-	$0.3*V_{DD}$	V	
HIGH-level input voltage	V_{IH}	$0.7*V_{DD}$	-	5.5	V	
Input leakage current	I_{LI}	-1	-	+1	μA	VDD = 2.3 V to 5.5 V; VI = VDD or VSS

1.VDD must be lowered to 0.2V for at least 50μs in order to reset part.

2.Each I/O must be externally limited to a maximum of 25 mA and each octal (IO0_0 to IO0_7 and IO1_0 to IO1_7) must be limited to a maximum current of 100 mA for a device total of 200 mA.

3.The total current sourced by all I/Os must be limited to 160 mA.

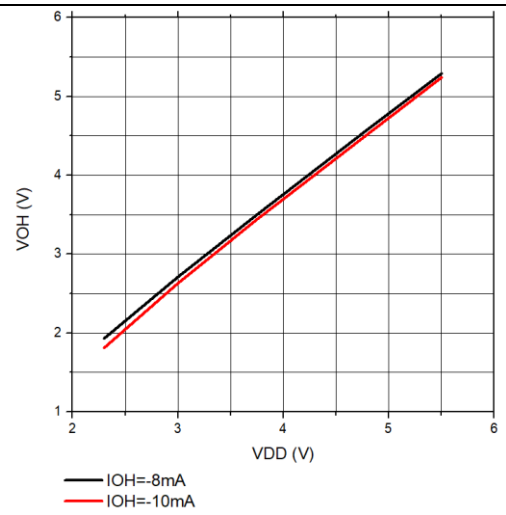


Fig 1. V_{OH} versus Supply Voltage

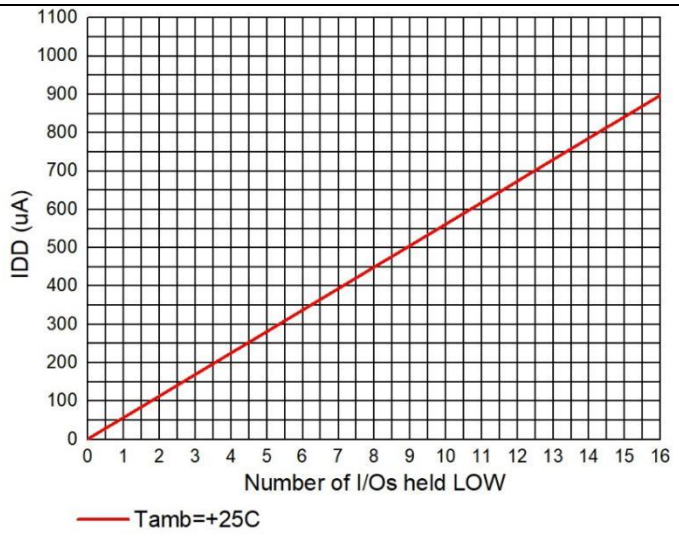


Fig 2. I_{DD} versus number of I/Os held LOW

5.2. Dynamic Characteristics

Parameters	*Symbol*	*Standard-mode I2C-bus*		*Fast-mode I2C-bus*		*Unit*
		Min	*Max*	*Min*	*Max*	
SCL clock frequency	f_{SCL}	0	100	0	400	kHz
bus free time between a STOP and START condition	t_{BUF}	4.7	-	1.3	-	μs
hold time (repeated) START condition	$t_{HD;STA}$	4.0	-	0.6	-	μs
set-up time for a repeated START condition	$t_{SU;STA}$	4.7	-	0.6	-	μs
set-up time for STOP condition	$t_{SU;STO}$	4.0	-	0.6	-	μs
data valid acknowledge time	$t_{VD;ACK}$[1]	0.3	3.45	0.1	0.9	μs
data hold time	$t_{HD;DAT}$	0	-	0	-	ns
data valid time	$t_{VD;DAT}$[2]	300	-	50	-	ns
data set-up time	$t_{SU;DAT}$	250	-	100	-	ns
LOW period of the SCL clock	t_{LOW}	4.7	-	1.3	-	μs
HIGH period of the SCL clock	t_{HIGH}	4.0	-	0.6	-	μs
fall time of both SDA and SCL signals	t_f	-	300	$20 + 0.1C_b$[3]	300	ns
rise time of both SDA and SCL signals	tr	-	1000	$20 + 0.1C_b$[3]	300	ns

pulse width of spikes that must be suppressed by the input filter	t_{SP}	-	50	-	50	ns
data output valid time	$t_{v(Q)}$	-	200	-	200	ns
data input set-up time	$t_{su(D)}$	150	-	150	-	ns
data input hold time	$t_{h(D)}$	1	-	1	-	µs
valid time on pin /INT	$t_{v(INT\_N)}$ [4]	-	4	-	4	µs
reset time on pin /INT	$t_{rst(INT\_N)}$ [5]	-	4	-	4	µs

1.$t_{VD;ACK}$ = time for acknowledgement signal from SCL LOW to SDA (out) LOW, see Figure 22.

2.$t_{VD;DAT}$ = minimum time for SDA data out to be valid following SCL LOW, see Figure 22.

3.C_b = total capacitance of one bus line in pF.

4.$t_{V(INT\_N)}$ is measured from 50% IO input to 0.3VDD on /INT

5.$t_{rst(INT\_N)}$ is measured from 0.3VDD on SCL to 0.7VDD on /INT.

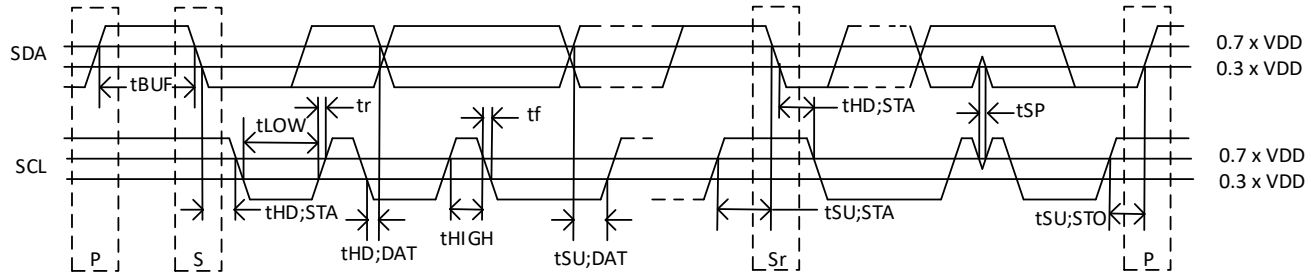


Fig 3. Definition of timing on I²C-bus

6. Register Description

The register map of the NCA9555 includes input port registers, output port registers, polarity inversion port registers and configuration registers.

6.1. Device address

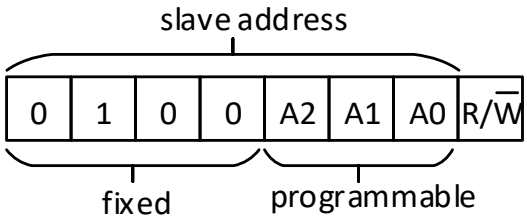


Fig 4. NCA9555 device address

6.2. command byte

The command byte is the first byte to follow the address byte during a write transmission. It is used as a pointer to determine which

of the following registers will be written or read.

Table 4. Command byte

Command	Register
0	Input port 0
1	Input port 1
2	Output port 0
3	Output port 1
4	Polarity Inversion port 0
5	Polarity Inversion port 1
6	Configuration port 0
7	Configuration port 1

6.3. registers 0 and 1 : input port registers

This register is an input-only port. It reflects the incoming logic levels of the pins, regardless of whether the pin is defined as an input or an output by Register 3. Writes to this register have no effect.
The default value 'X' is determined by the externally applied logic level.

Table 5. Input Port 0 Register

Bit	7	6	5	4	3	2	1	0
Symbol	I0.7	I0.6	I0.5	I0.4	I0.3	I0.2	I0.1	I0.0
Default	X	X	X	X	X	X	X	X

Table 6. Input Port 1 Register

Bit	7	6	5	4	3	2	1	0
Symbol	I1.7	I1.6	I1.5	I1.4	I1.3	I1.2	I1.1	I1.0
Default	X	X	X	X	X	X	X	X

6.4. registers 2 and 3 : output port registers

This register is an output-only port. It reflects the outgoing logic levels of the pins defined as outputs by Registers 6 and 7. Bit values in this register have no effect on pins defined as inputs. In turn, reads from this register reflect the value that is in the flip-flop controlling the output selection, not the actual pin value.

Table 7. Output Port 0 Register

Bit	7	6	5	4	3	2	1	0

Symbol	O0.7	O0.6	O0.5	O0.4	O0.3	O0.2	O0.1	O0.0
Default	1	1	1	1	1	1	1	1

Table 8. Output Port 1 Register

Bit	7	6	5	4	3	2	1	0
Symbol	O1.7	O1.6	O1.5	O1.4	O1.3	O1.2	O1.1	O1.0
Default	1	1	1	1	1	1	1	1

6.5. registers 4 and 5 : polarity inversion registers

This register allows the user to invert the polarity of the Input port register data. If a bit in this register is set (written with '1'), the Input port data polarity is inverted. If a bit in this register is cleared (written with a '0'), the Input port data polarity is retained.

Table 9. Polarity Inversion Port 0 Register

Bit	7	6	5	4	3	2	1	0
Symbol	N0.7	N0.6	N0.5	N0.4	N0.3	N0.2	N0.1	N0.0
Default	0	0	0	0	0	0	0	0

Table 10. Polarity Inversion Port 1 Register

Bit	7	6	5	4	3	2	1	0
Symbol	N1.7	N1.6	N1.5	N1.4	N1.3	N1.2	N1.1	N1.0
Default	0	0	0	0	0	0	0	0

6.6. Registers 6 and 7 : CONFIGURATION registers

This register configures the directions of the I/O pins. If a bit in this register is set (written with '1'), the corresponding port pin is enabled as an input with high-impedance output driver. If a bit in this register is cleared (written with '0'), the corresponding port pin is enabled as an output. Note that there is a high value resistor tied to VDD at each pin. At reset, the device's ports are inputs with a pull-up to VDD.

Table 11. Configuration Port 0 Register

Bit	7	6	5	4	3	2	1	0
Symbol	C0.7	C0.6	C0.5	C0.4	C0.3	C0.2	C0.1	C0.0
Default	1	1	1	1	1	1	1	1

Table 12. Configuration Port 1 Register

Bit	7	6	5	4	3	2	1	0
Symbol	C1.7	C1.6	C1.5	C1.4	C1.3	C1.2	C1.1	C1.0
Default	1	1	1	1	1	1	1	1

6.7. POWER-ON RESET

When power is applied to VDD, an internal power-on reset holds the NCA9555 in a reset condition until VDD has reached VPOR. At that point, the reset condition is released and the NCA9555 registers and I2C state machine will initialize to their default states. The power-on reset typically completes the reset and enables the part by the time the power supply is above VPOR. However, when it is required to reset the part by lowering the power supply, it is necessary to lower it below 0.2 V for at least 50μs.

6.8. I/O PORT

When an I/O is configured as an input, FETs Q1 and Q2 are off, creating a high-impedance input with a weak pull-up to VDD. The input voltage may be raised above VDD to a maximum of 5.5 V.
If the I/O is configured as an output, then either Q1 or Q2 is on, depending on the state of the Output Port register. Care should be exercised if an external voltage is applied to an I/O configured as an output because of the low-impedance path that exists between the pin and either VDD or VSS.

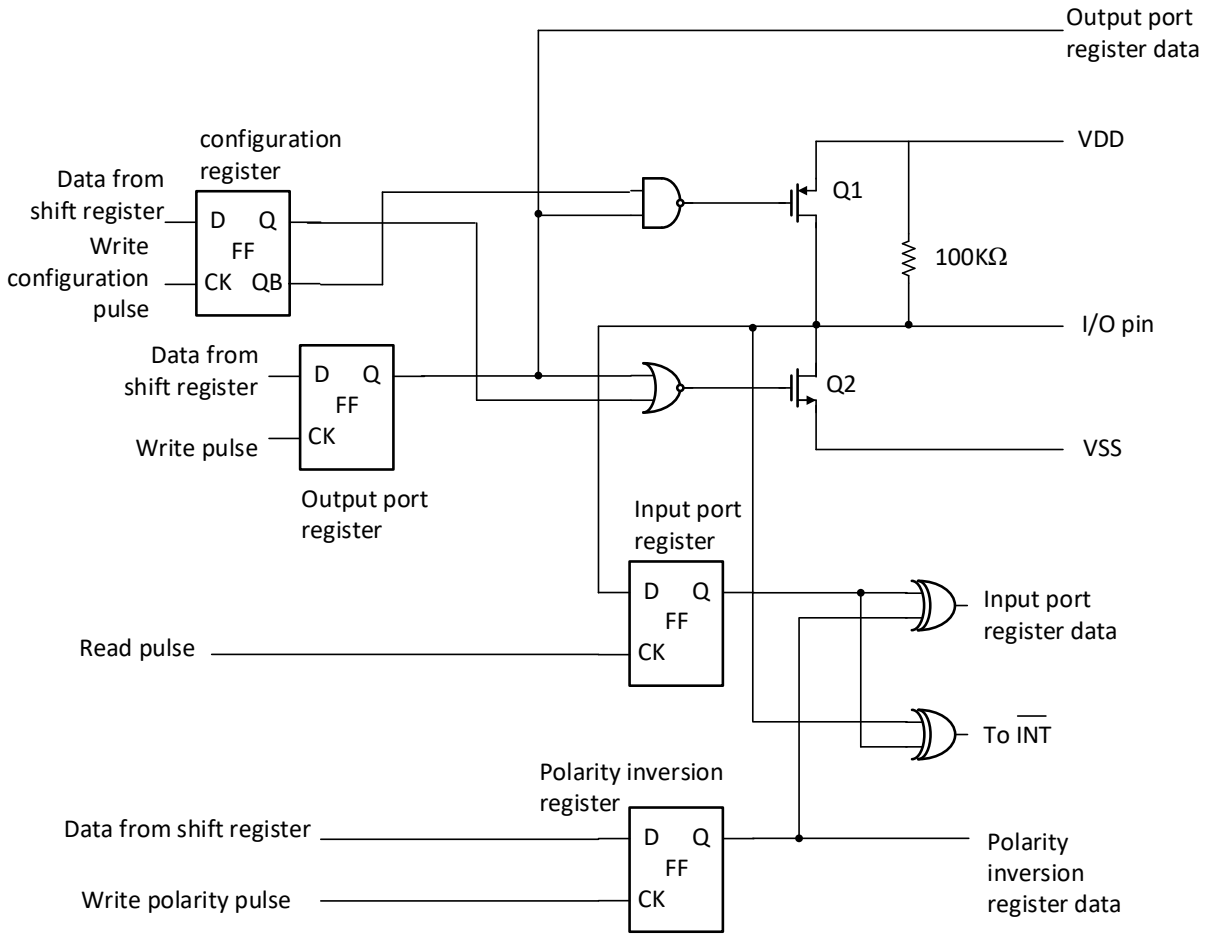


Fig 5. Simplified schematic of I/Os

7. BUS TRANSACTIONS

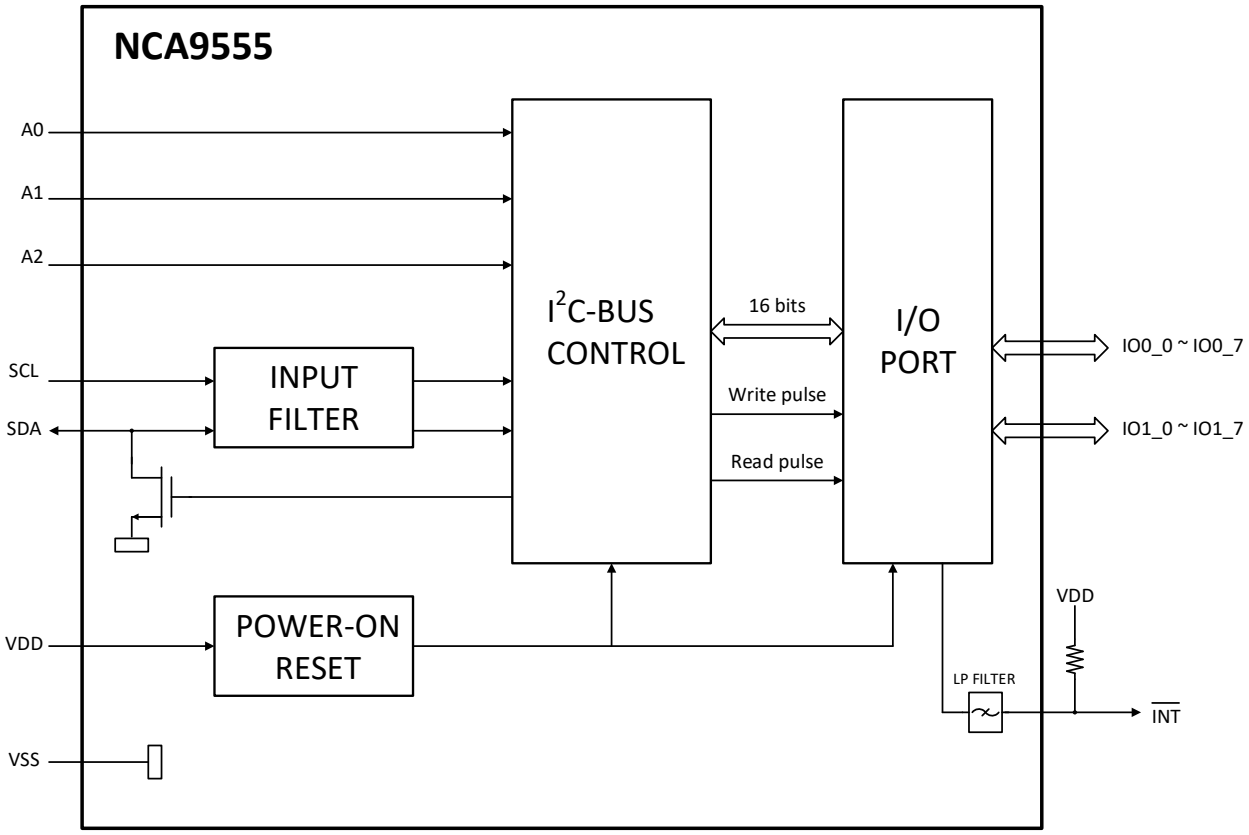


Fig 6. Block Diagram of NCA9555

7.1. WRITING TO THE PORT REGISTERS

Data is transmitted to the NCA9555 by sending the device address and setting the least significant bit to a logic 0 (see Figure 4 “NCA9555 device address”). The command byte is sent after the address and determines which register will receive the data following the command byte.

The eight registers within the NCA9555 are configured to operate as four register pairs. The four pairs are Input Ports, Output Ports, Polarity Inversion Ports, and Configuration Ports. After sending data to one register, the next data byte will be sent to the other register in the pair (see Figure 7 and Figure 8). For example, if the first byte is sent to Output Port 1 (register 3), then the next byte will be stored in Output Port 0 (register 2). There is no limitation on the number of data bytes sent in one write transmission. In this way, each 8-bit register may be updated independently of the other registers.

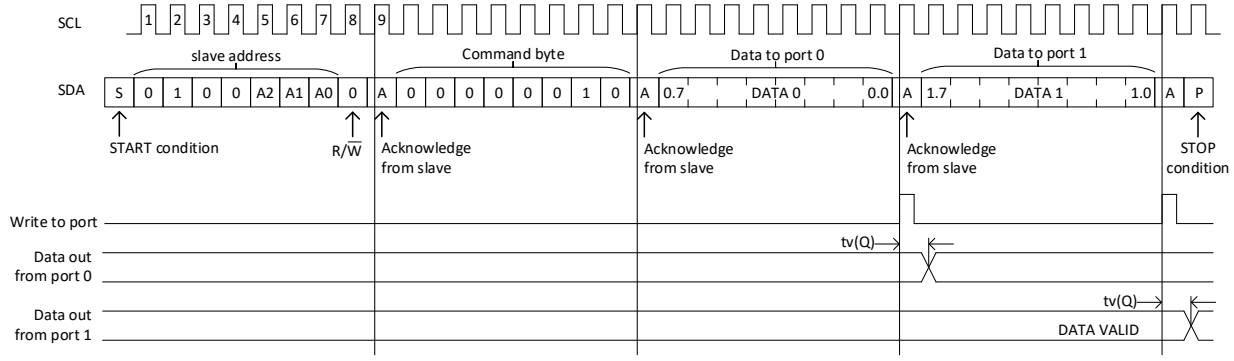


Fig 7. Write to output port registers

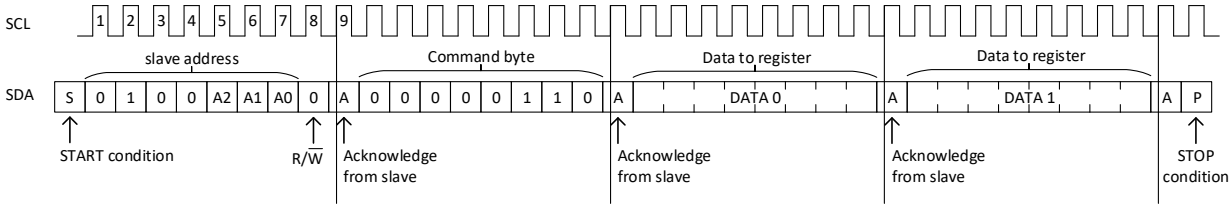
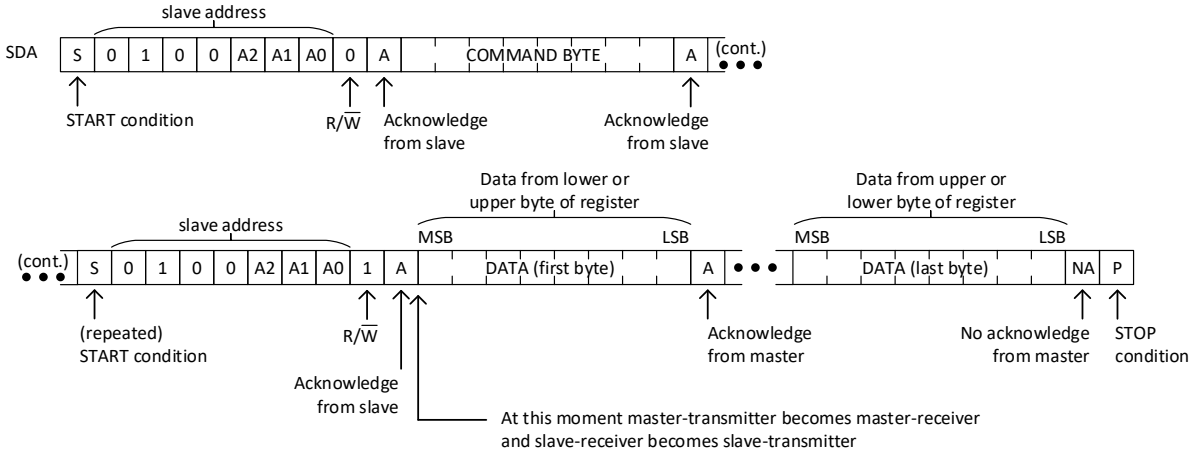


Fig 8. Write to config registers

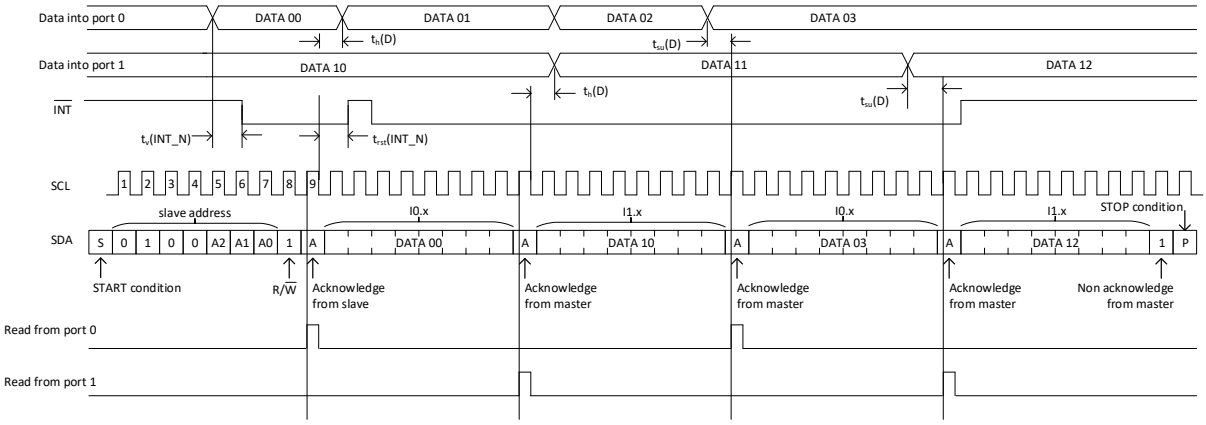
7.2. READING THE PORT REGISTERS

In order to read data from the NCA9555, the bus master must first send the NCA9555 address with the least significant bit set to a logic 0 (see Figure 4 “NCA9555 device address”). The command byte is sent after the address and determines which register will be accessed. After a restart, the device address is sent again, but this time the least significant bit is set to a logic 1. Data from the register defined by the command byte will then be sent by the NCA9555 (see Figure 9, Figure 10 and Figure 11). Data is clocked into the register on the rising edge of the acknowledge clock pulse. After the first byte is read, additional bytes may be read but the data will now reflect the information in the other register in the pair. For example, if you read Input Port 1, then the next byte read would be Input Port 0. There is no limitation on the number of data bytes received in one read transmission but the final byte received, the bus master must not acknowledge the data.



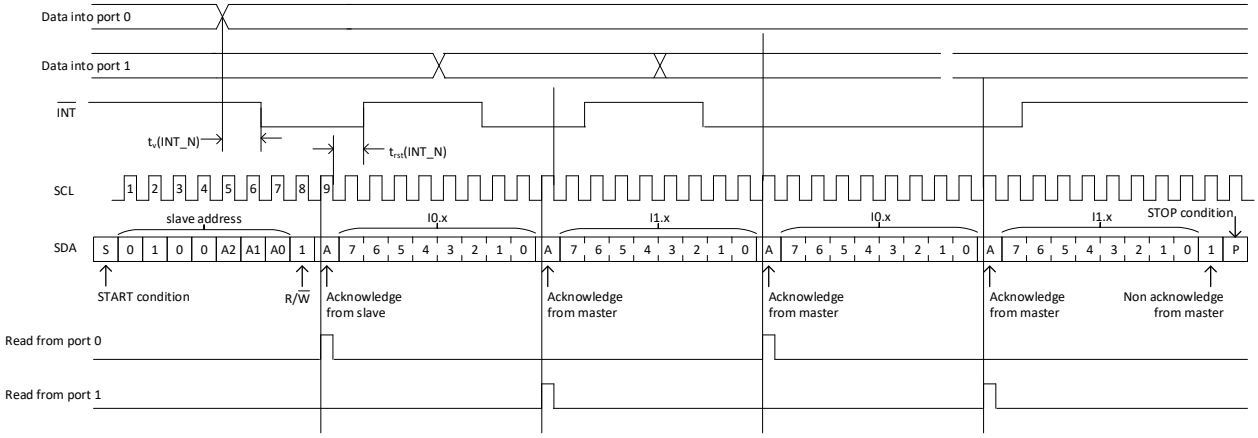
Remark: Transfer of data can be stopped at any moment by a STOP condition.

Fig 9. Read from registers



Remark: Transfer of data can be stopped at any moment by a STOP condition. When this occurs, data present at the latest acknowledge phase is valid(output mode). It is assumed that the command byte has previously been set to '00' (read Input Port register).

Fig 10. Read input port registers, scenario 1



Remark: Transfer of data can be stopped at any moment by a STOP condition. When this occurs, data present at the latest acknowledge phase is valid(output mode). It is assumed that the command byte has previously been set to '00' (read Input Port register).

Fig 11. Read input port registers, scenario 2

7.3. interrupt output

The open-drain interrupt output is activated when one of the port pins changes state and the pin is configured as an input. The interrupt is deactivated when the input returns to its previous state or the Input Port register is read (see Figure 10). A pin configured as an output cannot cause an interrupt. Since each 8-bit port is read independently, the interrupt caused by Port 0 will not be cleared by a read of Port 1 or the other way around.

Remark: Changing an I/O from an output to an input may cause a false interrupt to occur if the state of the pin does not match the contents of the Input Port register.

8. characteristics of the I²C-BUS

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The I2C-bus is for 2-way, 2-line communication between different ICs or modules. The two lines are a serial data line (SDA) and a serial

clock line (SCL). Both lines must be connected to a positive supply via a pull-up resistor when connected to the output stages of a device. Data transfer may be initiated only when the bus is not busy.

8.1. bit transfer

One data bit is transferred during each clock pulse. The data on the SDA line must remain stable during the HIGH period of the clock pulse as changes in the data line at this time will be interpreted as control signals (see Figure 12).

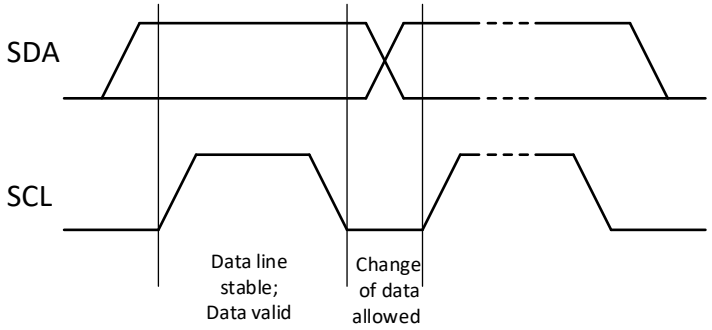


Fig 12. Bit transfer

8.2. start and stop conditions

Both data and clock lines remain HIGH when the bus is not busy. A HIGH-to-LOW transition of the data line while the clock is HIGH is defined as the START condition (S). A LOW-to-HIGH transition of the data line while the clock is HIGH is defined as the STOP condition (P) (see Figure 13).

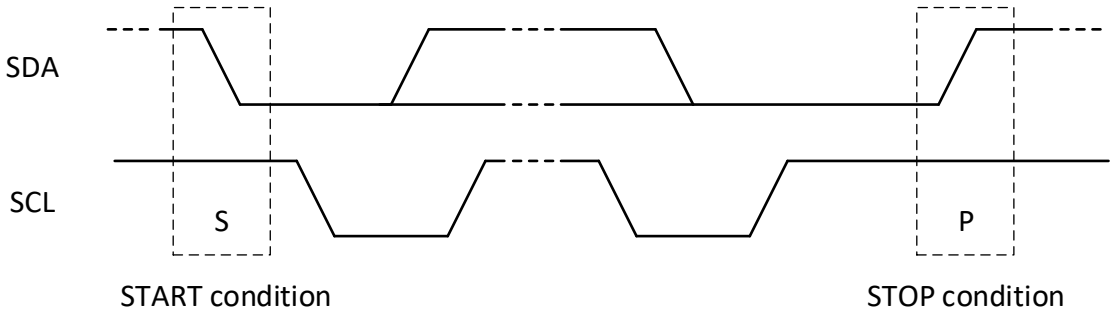


Fig 13. Definition of START and STOP conditions

8.3. system configuration

A device generating a message is a ‘transmitter’; a device receiving is the ‘receiver’. The device that controls the message is the ‘master’ and the devices which are controlled by the master are the ‘slaves’ (see Figure 14).

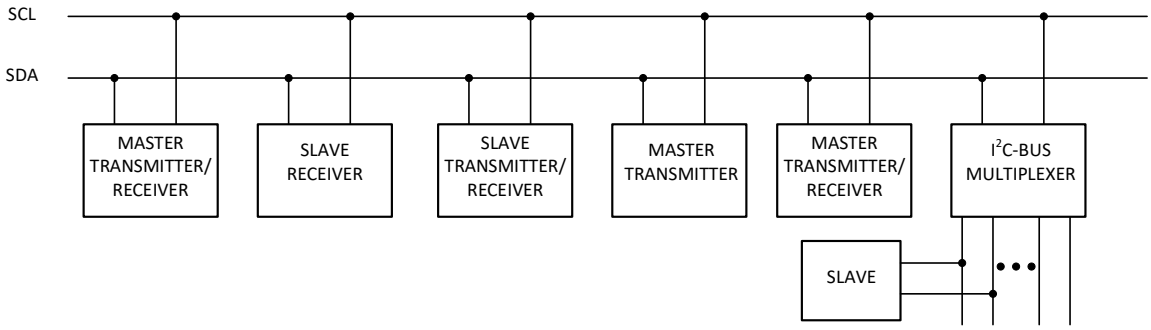


Fig 14. System configuration

8.4. Acknowledge

The number of data bytes transferred between the START and the STOP conditions from transmitter to receiver is not limited. Each byte of eight bits is followed by one acknowledge bit. The acknowledge bit is a HIGH level put on the bus by the transmitter, whereas the master generates an extra acknowledge related clock pulse.

A slave receiver which is addressed must generate an acknowledge after the reception of each byte. Also a master must generate an acknowledge after the reception of each byte that has been clocked out of the slave transmitter. The device that acknowledges has to pull down the SDA line during the acknowledge clock pulse, so that the SDA line is stable LOW during the HIGH period of the acknowledge related clock pulse; set-up time and hold time must be taken into account.

A master receiver must signal an end of data to the transmitter by not generating an acknowledge on the last byte that has been clocked out of the slave. In this event, the transmitter must leave the data line HIGH to enable the master to generate a STOP condition.

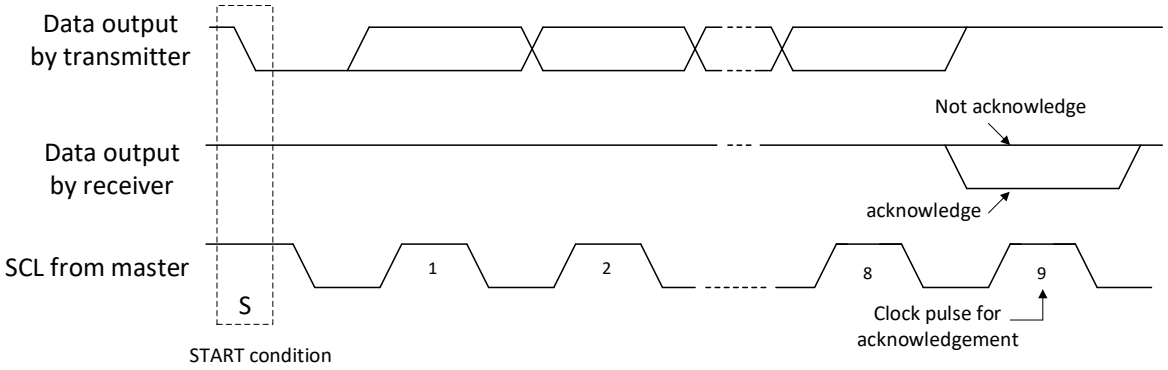


Fig 15. Acknowledgement on I²C-bus

9. APPLICATION DESIGN-IN INFORMATION

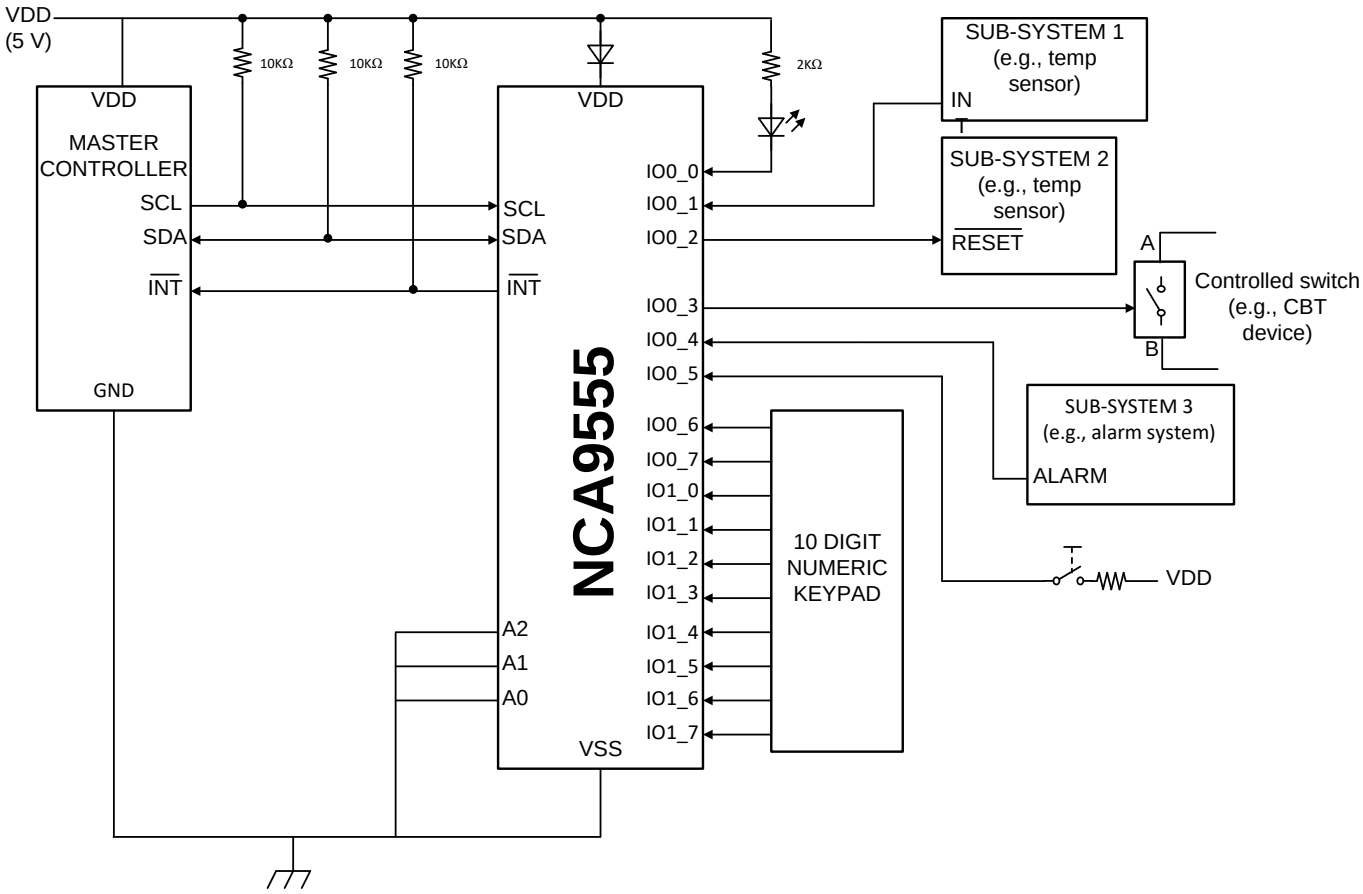
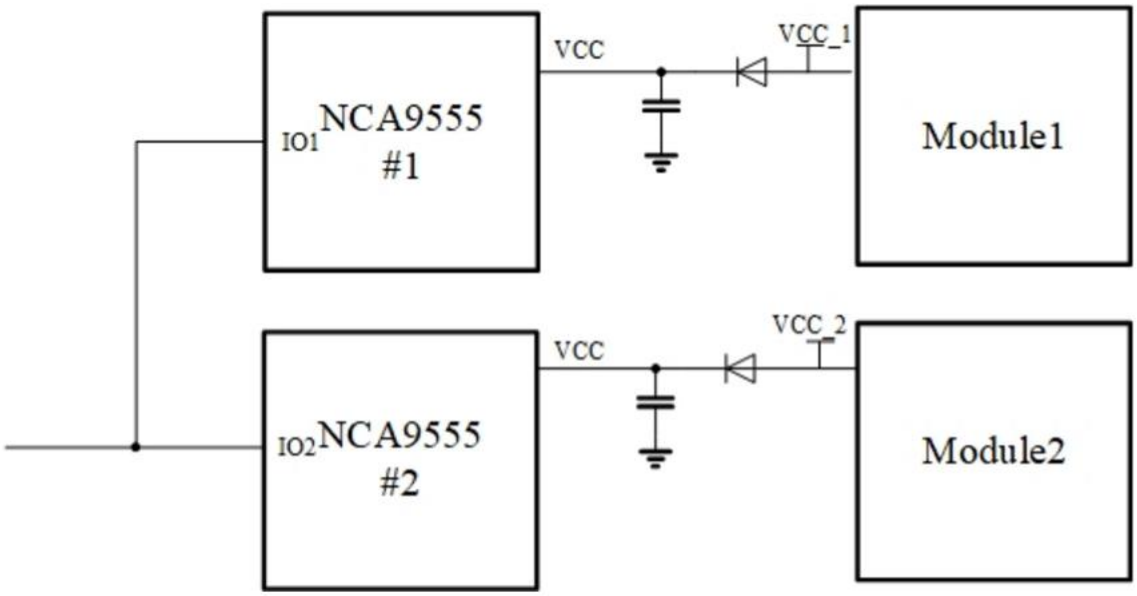
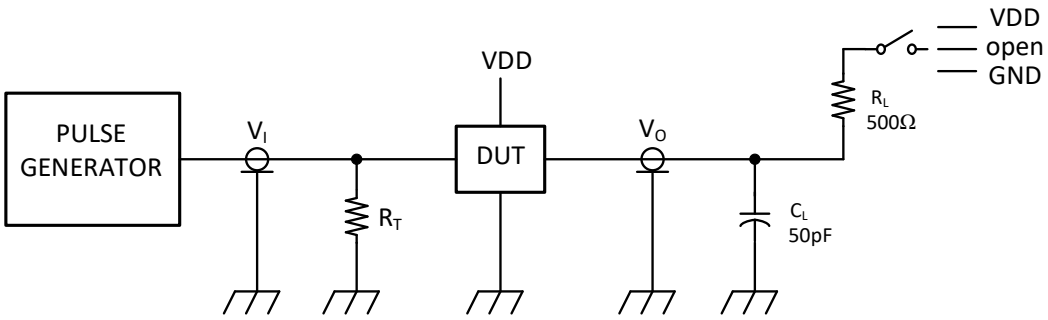


Fig 16. Typical application

When the IO level of the NCA9555 is higher than the power supply voltage, the diode inside the chip to prevent backflow will be turned on. In the case of power down and data input, the IO signal will be fed back to the VDD module (eg.master controller), which will cause the data to be pulled low. In order to realize IO still has high resistance characteristics when power down,it is recommended to connect a forward schottky diode to the power supply pin of NCA9555.



10. Test information



R_L = load resistor.
C_L = load capacitance includes jig and probe capacitance.
R_T = termination resistance should be equal to the output impedance of Z_o of the pulse generators.

Fig 17. Test circuitry for switching times

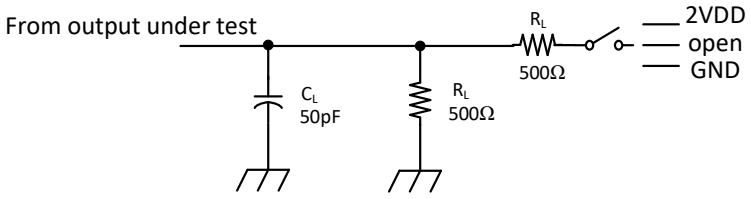


Fig 18. Load circuit

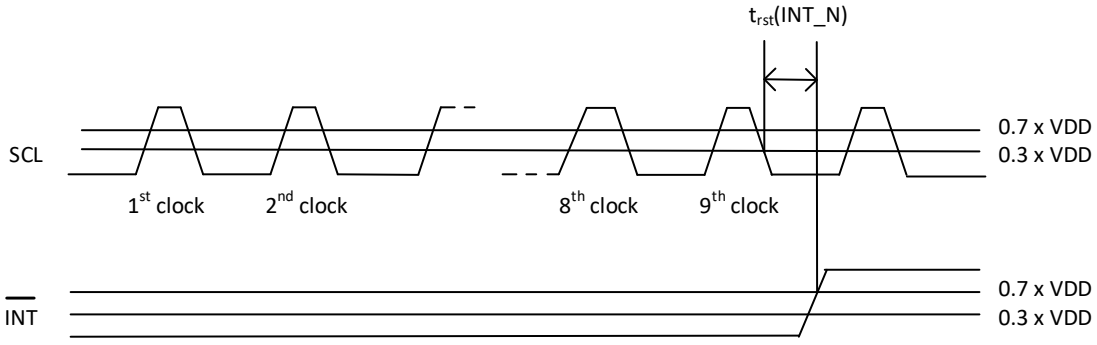


Fig 19. Parameter Measurement Waveform: $t_{rst(INT\_N)}$

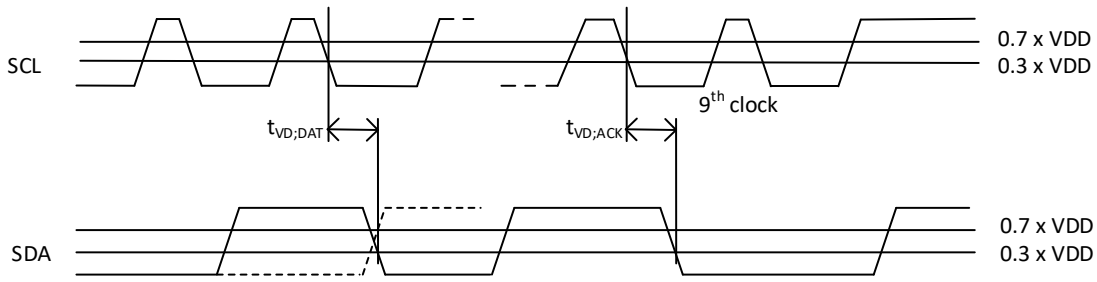
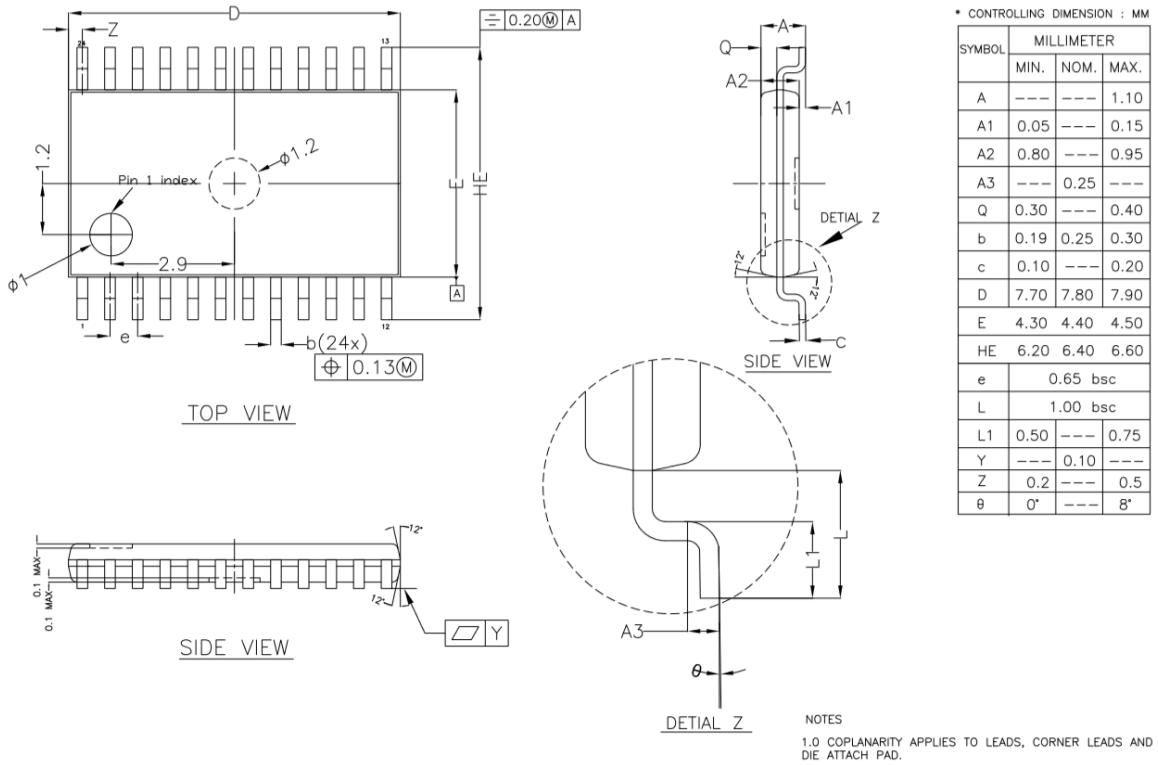


Fig 20. Parameter Measurement Waveform: tVD; DAT & tVD;ACK

11. Package information

11.1. package outline

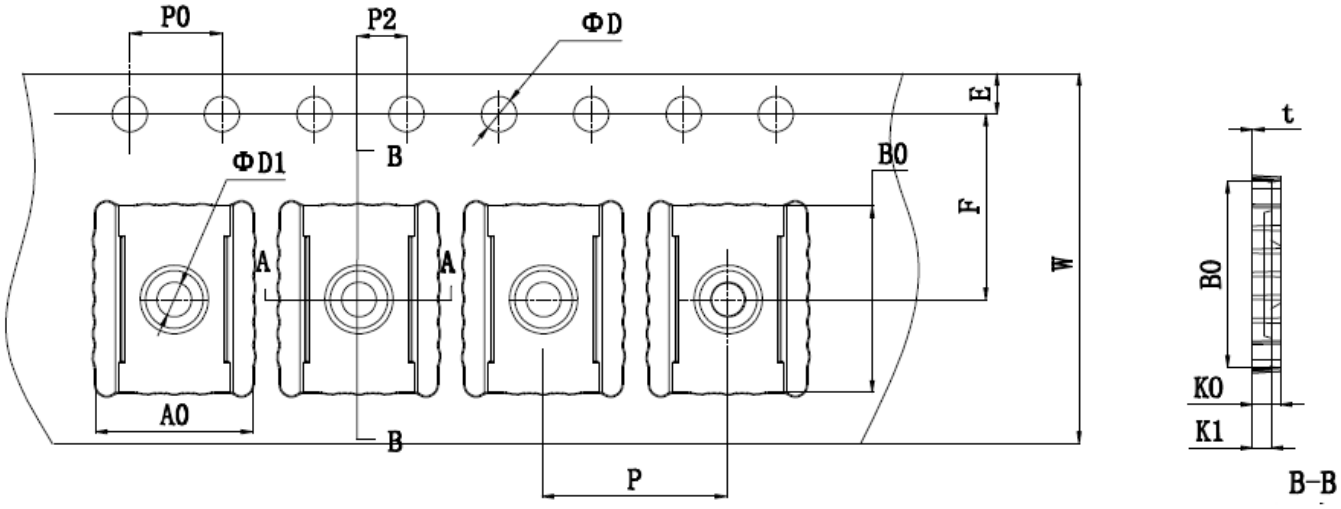


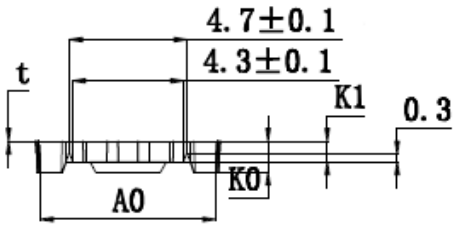
* CONTROLLING DIMENSION : MM

SYMBOL	MILLIMETER		
	MIN.	NOM.	MAX.
A	---	---	1.10
A1	0.05	---	0.15
A2	0.80	---	0.95
A3	---	0.25	---
Q	0.30	---	0.40
b	0.19	0.25	0.30
c	0.10	---	0.20
D	7.70	7.80	7.90
E	4.30	4.40	4.50
HE	6.20	6.40	6.60
e	0.65 bsc		
L	1.00 bsc		
L1	0.50	---	0.75
Y	---	0.10	---
Z	0.2	---	0.5
θ	0°	---	8°

Fig 21. Package outline for TSSOP24

12. TAPE AND REEL INFORMATION

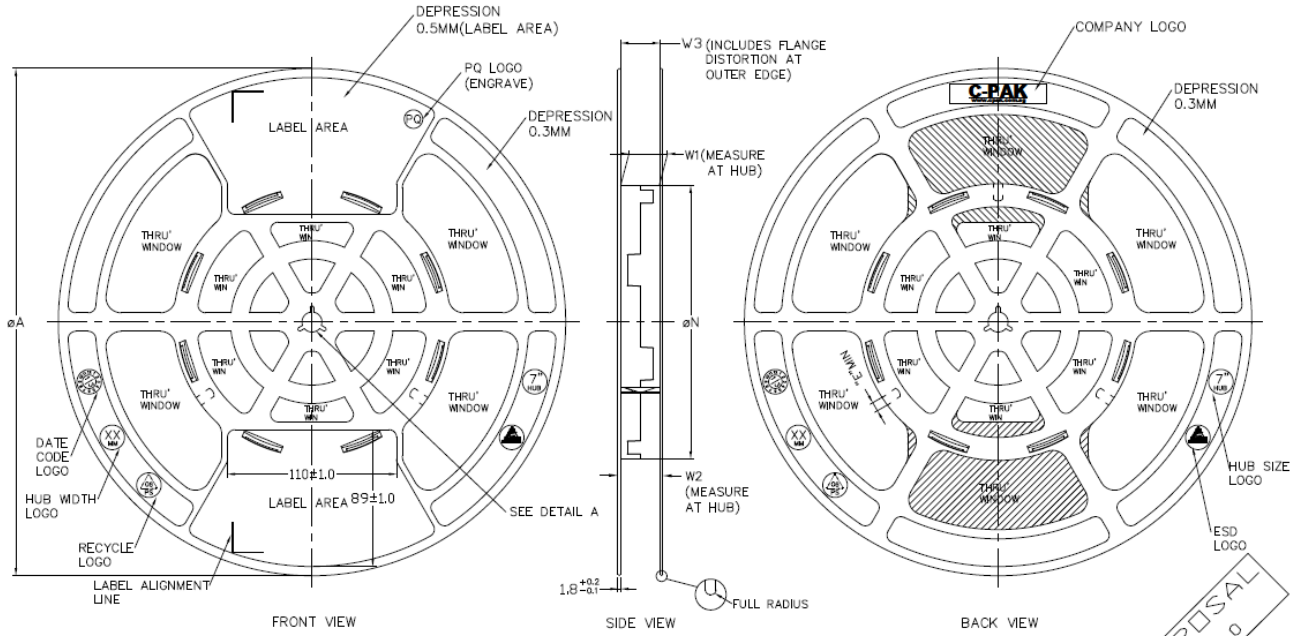


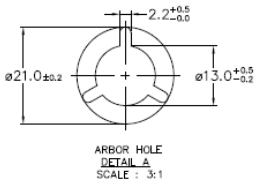


E	1.75±0.10
F	7.5±0.10
P2	2.00±0.10
D	1.55±0.10
D1	1.55±0.10
P0	4.00±0.10
10P0	40.00±0.20

W	16.00±0.30
P	8.00±0.10
A0	6.80±0.10
B0	8.04±0.10
K0	1.25±0.10
K1	1.1±0.10
t	0.30±0.05
θ	5° TYP

ALL DIMENSIONSIN MILLIMETERS UNLESS OTHERWISE STATED





PRODUCT SPECIFICATION

TAPE WIDTH	øA ±2.0	øN ±2.0	W1	W2 (MAX)	W3	E (MIN)
08MM	330	178	8.4	14.4	SHALL ACCOMMODATE TAPE WIDTH WITHOUT INTERFERENCE	5.5
12MM	330	178	12.4	18.4		5.5
16MM	330	178	16.4	22.4		5.5
24MM	330	178	24.4	30.4		5.5
32MM	330	178	32.4	38.4		5.5

SURFACE RESISTIMTY

LEGEND	SR RANGE	TYPE	COLOUR
A	BELOW 10^{12}	ANTISTATIC	ALL TYPES
B	10^{9} TO 10^{11}	STATIC DISSIPATIVE	BLACK ONLY
C	10^{5} & BELOW 10^{9}	CONDUCTIVE (GENERIC)	BLACK ONLY
E	10^{6} TO 10^{9}	ANTISTATIC (COATED)	ALL TYPES

Fig 22. tape and reel information for TSSOP24

13. Order information

Part No.	*Package Type*	*Pins*	*MSL Level*	*Package Qty*	*Temperature*
NCA9555	TSSOP	24	Level 1	2500	-40 to 85℃

14. Documentation Support

Part Number	*Product Folder*	*Datasheet*	*Technical Documents*	*Isolator selection guide*
NCA9555	Click here	Click here	Click here	Click here

15. Revision history

Revision	*Description*	*Date*
1.0	Initial version	2019/2/27
1.1	Added thermal information& order information	2020/2/10
1.2	Changed 3.0 supply current,VPOR and IOL	2020/5/31
1.3	Added application design-in information	2020/10/30