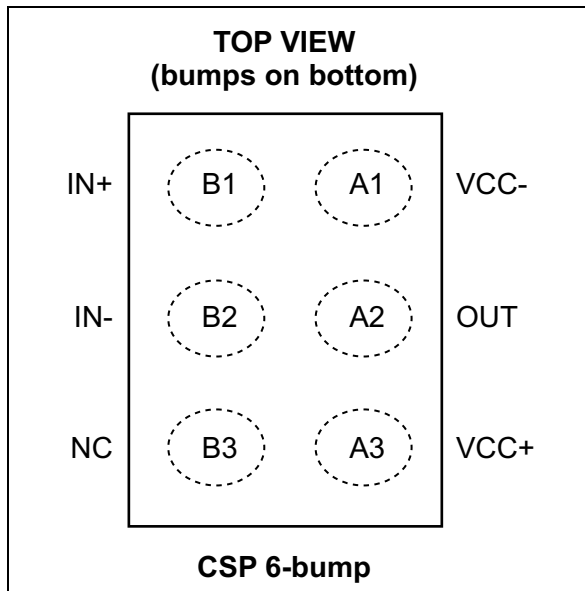


## Micropower low-voltage, 1.2 x 0.8 mm CSP comparator

Datasheet - production data



### Features

- Supply operation from 1.8 to 5 V
- Low current consumption: 14  $\mu\text{A}$
- Rail to rail inputs, push-pull outputs
- Low propagation delay: 300 ns
- 60  $\mu\text{A}$  supply current at 1 MHz switching frequency
- Low output saturation voltage
- Internal hysteresis
- Wide temperature range:  $-40^\circ$  to  $85^\circ\text{C}$
- ESD tolerance: 2 kV HBM
- 6-bump CSP, 1.2 x 0.8 mm, 400  $\mu\text{m}$  pitch

### Applications

- Mobiles phones
- Battery supplied electronics
- General purpose portable devices
- General purpose low voltage applications

### Description

The TS985 is a single micropower and low voltage comparator. It can operate with a supply voltage ranging from 1.8 V to 5 V with a typical current consumption as low as 14  $\mu\text{A}$  while achieving a 300 ns propagation delay. In addition, rail-to-rail inputs make it a perfect choice for low voltage applications.

The 6-bump chip scale package (CSP) is a real advantage for overcoming space constraints.

TS985 is specified for temperature between  $-40^\circ\text{C}$  to  $85^\circ\text{C}$ , making it ideal for a wide range of applications.

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# 1 Absolute maximum ratings

**Table 1. Absolute maximum ratings (AMR)**

Symbol	Parameter	Value	Unit
$V_{CC}$	Supply voltage <sup>(1)</sup>	5.5	V
$V_{id}$	Differential input voltage <sup>(2)</sup>	±5.5	
$V_{in}$	Input voltage <sup>(3)</sup>	$(V_{CC}^-) - 0.3$ to $(V_{CC}^+) + 0.3$	
$V_{out}$	Output voltage	5.5	
$I_F$	Forward current in ESD protection diodes on inputs <sup>(4)</sup>	10	mA
$T_j$	Maximum junction temperature	150	°C
$T_{stg}$	Storage temperature range	-65 to 150	
$R_{thja}$	Thermal resistance junction to ambient <sup>(5)</sup>	TBA	°C/W
ESD	HBM: human body model <sup>(6)</sup>	2000	V
	CDM: charged device model <sup>(7)</sup>	1500	
	Latch-up immunity	200	mA

1. All voltage values, except differential voltage, are with respect to network ground terminal.
2. Differential voltages are the non-inverting input terminal with respect to the inverting input terminal.
3. Excursions of input voltages may exceed the power supply level. As long as the common mode voltage  $[V_{icm}=(V_{in}^+ + V_{in}^-)/2]$  remains within the specified range, the comparator will provide a stable output state. However, the maximum current through the ESD diodes ( $I_F$ ) of the input stage must strictly be observed.
4. Guaranteed by design.
5. Short-circuits can cause excessive heating and destructive dissipation. Values are typical
6. According to JEDEC standard JESD22-A114F.
7. According to ANSI/ESD STM5.3.1.

**Table 2. Operating conditions**

Symbol	Parameter	Value	Unit
$V_{CC}^+$	Supply voltage	1.8 to 5.0	V
$V_{icm}$	Common mode input voltage range, $T_{amb} = 25\text{ °C}$	$(V_{CC}^-) - 0.25$ to $(V_{CC}^+) + 0.25$	
	Common mode input voltage range, $T_{min} \leq T_{amb} \leq T_{max}$	$(V_{CC}^-)$ to $(V_{CC}^+)$	
$T_{oper}$	Operating free-air temperature range	-40 to 85	°C

## 2 Electrical characteristics

**Table 3.  $V_{CC}^+ = 1.8\text{ V}$ ,  $V_{CC}^- = 0\text{ V}$ ,  $T_{amb} = 25\text{ °C}$  (unless otherwise specified)**

Symbol	Parameter	Min.	Typ.	Max.	Unit
$V_{io}$	Input offset voltage, full $V_{icm}$ range		0.5	8	mV
	Input offset voltage, $T_{min} \leq T_{amb} \leq T_{max}$			9	
$\Delta V_{io}/\Delta T$	Input offset voltage drift vs. temperature		4.5		$\mu\text{V}/\text{°C}$
$V_{Hyst}$	Input hysteresis voltage		3		mV
$I_{ib}$	Input bias current <sup>(1)</sup> , full $V_{icm}$ range		14	40	nA
	Input bias current <sup>(1)</sup> , $T_{min} \leq T_{amb} \leq T_{max}$			100	
$I_{io}$	Input offset current, full $V_{icm}$ range		1	10	
	Input offset current, $T_{min} \leq T_{amb} \leq T_{max}$			100	
CMR	Common-mode rejection ratio, $V_{icm} = 0$ to $1.8\text{ V}$	43			dB
$I_{CC}$	Supply current per comparator, no load - $V_{icm} = 0\text{ V}$		13	19	$\mu\text{A}$
	Supply current per comparator, $T_{min} \leq T_{amb} \leq T_{max}$			20	
$V_{OH}$	High-level output voltage, $I_{Source} = 1\text{ mA}$	1.69	1.71		V
	High-level output voltage, $T_{min} \leq T_{amb} \leq T_{max}$	1.67			
$V_{OL}$	Low-level output voltage, $I_{Sink} = 1\text{ mA}$		65	80	mV
	Low-level output voltage, $T_{min} \leq T_{amb} \leq T_{max}$			95	
$I_{Sink}$	$V_{OUT} = 0\text{ V}$	6	8		mA
	$T_{min} \leq T_{amb} \leq T_{max}$	5			
$I_{Source}$	$V_{OUT} = V_{CC}$	4.5	7.3		
	$T_{min} \leq T_{amb} \leq T_{max}$	3.5			
$t_{PHL}$	Response time high to low <sup>(2)</sup> , $V_{icm} = 0\text{ V}$ , $C_L = 15\text{ pF}$ , overdrive = $10\text{ mV}$		730		ns
	Response time high to low <sup>(2)</sup> , $V_{icm} = 0\text{ V}$ , $C_L = 15\text{ pF}$ , overdrive = $100\text{ mV}$		300		
$t_{PLH}$	Response time low to high <sup>(3)</sup> , $V_{icm} = 0\text{ V}$ , $C_L = 15\text{ pF}$ , overdrive = $10\text{ mV}$		730		
	Response time low to high <sup>(3)</sup> , $V_{icm} = 0\text{ V}$ , $C_L = 15\text{ pF}$ , overdrive = $100\text{ mV}$		300		

1. Maximum values include unavoidable inaccuracies of the industrial tests.
2.  $t_{PHL}$  is measured when the output signal crosses a voltage level at 50% of  $V_{CC}$  with the following conditions: inverting input voltage (IN-) =  $V_{ICM}$  and non-inverting input (IN+), moving from  $V_{ICM} + 100\text{ mV}$  to  $V_{ICM} - \text{overdrive}$ .
3.  $t_{PLH}$  is measured when the output signal crosses a voltage level at 50% of  $V_{CC}$  with the following conditions: inverting input voltage (IN-) =  $V_{ICM}$  and non-inverting input (IN+), moving from  $V_{ICM} - 100\text{ mV}$  to  $V_{ICM} + \text{overdrive}$ .

Table 4.  $V_{CC}^+ = 2.7\text{ V}$ ,  $V_{CC}^- = 0\text{ V}$ ,  $T_{amb} = 25\text{ }^\circ\text{C}$  (unless otherwise specified)

Symbol	Parameter	Min.	Typ.	Max.	Unit
$V_{io}$	Input offset voltage, full $V_{icm}$ range		0.5	8	mV
	Input offset voltage, $T_{min} \leq T_{amb} \leq T_{max}$			9	
$\Delta V_{io}/\Delta T$	Input offset voltage drift vs. temperature		4.5		$\mu\text{V}/^\circ\text{C}$
$V_{Hyst}$	Input hysteresis voltage		3		mV
$I_{ib}$	Input bias current <sup>(1)</sup> , full $V_{icm}$ range		15	40	nA
	Input bias current <sup>(1)</sup> , $T_{min} \leq T_{amb} \leq T_{max}$			100	
$I_{io}$	Input offset current, full $V_{icm}$ range		1	10	nA
	Input offset current, $T_{min} \leq T_{amb} \leq T_{max}$			100	
CMR	Common-mode rejection ratio, $V_{icm} = 0$ to $2.7\text{ V}$	48			dB
$I_{CC}$	Supply current per comparator, no load - $V_{icm} = 0\text{ V}$		14	20	$\mu\text{A}$
	Supply current per comparator, $T_{min} \leq T_{amb} \leq T_{max}$			22	
$V_{OH}$	High-level output voltage, $I_{Source} = 1\text{ mA}$	2.6	2.64		V
	High-level output voltage, $T_{min} \leq T_{amb} \leq T_{max}$	2.5			
$V_{OL}$	Low-level output voltage, $I_{Sink} = 1\text{ mA}$		43	55	mV
	Low-level output voltage, $T_{min} \leq T_{amb} \leq T_{max}$			65	
$I_{Sink}$	$V_{OUT} = 0\text{ V}$	14	18		mA
	$T_{min} \leq T_{amb} \leq T_{max}$	12			
$I_{Source}$	$V_{OUT} = V_{CC}$	14	18		mA
	$T_{min} \leq T_{amb} \leq T_{max}$	12			
$t_{PHL}$	Response time high to low <sup>(2)</sup> , $V_{icm} = 0\text{ V}$ , $C_L = 15\text{ pF}$ , overdrive = $10\text{ mV}$		860		ns
	Response time high to low <sup>(2)</sup> , $V_{icm} = 0\text{ V}$ , $C_L = 15\text{ pF}$ , overdrive = $100\text{ mV}$		330		
$t_{PLH}$	Response time low to high <sup>(3)</sup> , $V_{icm} = 0\text{ V}$ , $C_L = 15\text{ pF}$ , overdrive = $10\text{ mV}$		860		ns
	Response time low to high <sup>(3)</sup> , $V_{icm} = 0\text{ V}$ , $C_L = 15\text{ pF}$ , overdrive = $100\text{ mV}$		330		

1. Maximum values include unavoidable inaccuracies of the industrial tests.
2.  $t_{PHL}$  is measured when the output signal crosses a voltage level at 50% of  $V_{CC}$  with the following conditions: inverting input voltage (IN-) =  $V_{ICM}$  and non-inverting input (IN+), moving from  $V_{ICM} + 100\text{ mV}$  to  $V_{ICM} - \text{overdrive}$ .
3.  $t_{PLH}$  is measured when the output signal crosses a voltage level at 50% of  $V_{CC}$  with the following conditions: inverting input voltage (IN-) =  $V_{ICM}$  and non-inverting input (IN+), moving from  $V_{ICM} - 100\text{ mV}$  to  $V_{ICM} + \text{overdrive}$ .

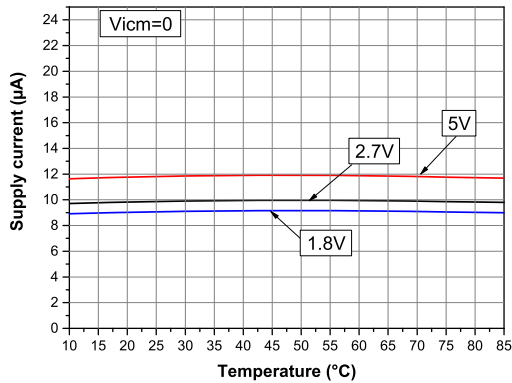
Table 5.  $V_{CC}^+ = 5\text{ V}$ ,  $V_{CC}^- = 0\text{ V}$ ,  $T_{amb} = 25\text{ °C}$  (unless otherwise specified)

Symbol	Parameter	Min.	Typ.	Max.	Unit
$V_{io}$	Input offset voltage, full $V_{icm}$ range		0.5	8	mV
	Input offset voltage, $T_{min} \leq T_{amb} \leq T_{max}$			9	
$\Delta V_{io}/\Delta T$	Input offset voltage drift vs. temperature		4.5		$\mu\text{V}/\text{°C}$
$V_{Hyst}$	Input hysteresis voltage		3		mV
$I_{ib}$	Input bias current <sup>(1)</sup> , full $V_{icm}$ range		17	50	nA
	Input bias current <sup>(1)</sup> , $T_{min} \leq T_{amb} \leq T_{max}$			100	
$I_{io}$	Input offset current, full $V_{icm}$ range		1	10	nA
	Input offset current, $T_{min} \leq T_{amb} \leq T_{max}$			100	
CMR	Common-mode rejection ratio, $V_{icm} = 0$ to $5\text{ V}$	56			dB
$I_{CC}$	Supply current per comparator, no load - $V_{icm} = 0\text{ V}$		16	24	$\mu\text{A}$
	Supply current per comparator, $T_{min} \leq T_{amb} \leq T_{max}$			25	
$V_{OH}$	High-level output voltage, $I_{Source} = 1\text{ mA}$	4.85	4.9		V
	High-level output voltage, $T_{min} \leq T_{amb} \leq T_{max}$	4.8			
$V_{OL}$	Low-level output voltage, $I_{Sink} = 1\text{ mA}$		31	45	mV
	Low-level output voltage, $T_{min} \leq T_{amb} \leq T_{max}$			55	
$I_{Sink}$	$V_{OUT} = 0\text{ V}$	35	42		mA
	$T_{min} \leq T_{amb} \leq T_{max}$	30			
$I_{Source}$	$V_{OUT} = V_{CC}$	45	52		mA
	$T_{min} \leq T_{amb} \leq T_{max}$	40			
$t_{PHL}$	Response time high to low <sup>(2)</sup> , $V_{icm} = 0\text{ V}$ , $C_L = 15\text{ pF}$ , overdrive = $10\text{ mV}$		1100		ns
	Response time high to low <sup>(2)</sup> , $V_{icm} = 0\text{ V}$ , $C_L = 15\text{ pF}$ , overdrive = $100\text{ mV}$		420		
$t_{PLH}$	Response time low to high <sup>(3)</sup> , $V_{icm} = 0\text{ V}$ , $C_L = 15\text{ pF}$ , overdrive = $10\text{ mV}$		1100		ns
	Response time low to high <sup>(3)</sup> , $V_{icm} = 0\text{ V}$ , $C_L = 15\text{ pF}$ , overdrive = $100\text{ mV}$		420		

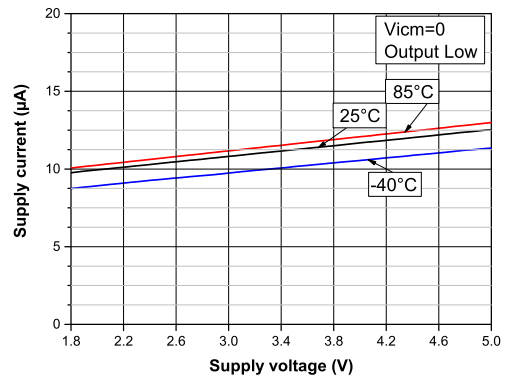
1. Maximum values include unavoidable inaccuracies of the industrial tests.
2.  $t_{PHL}$  is measured when the output signal crosses a voltage level at 50% of  $V_{CC}$  with the following conditions: inverting input voltage (IN-) =  $V_{ICM}$  and non-inverting input (IN+), moving from  $V_{ICM} + 100\text{ mV}$  to  $V_{ICM} - \text{overdrive}$ .
3.  $t_{PLH}$  is measured when the output signal crosses a voltage level at 50% of  $V_{CC}$  with the following conditions: inverting input voltage (IN-) =  $V_{ICM}$  and non-inverting input (IN+), moving from  $V_{ICM} - 100\text{ mV}$  to  $V_{ICM} + \text{overdrive}$ .

### 3 Electrical characteristic curves

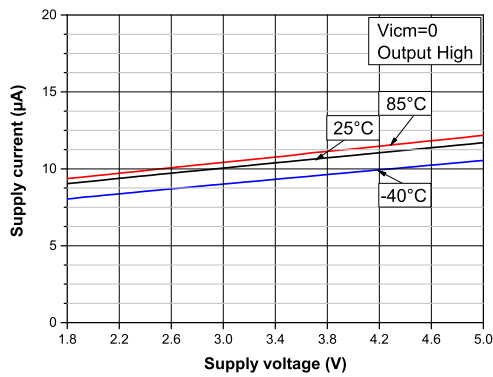
**Figure 1. Supply current vs temperature and supply voltage**



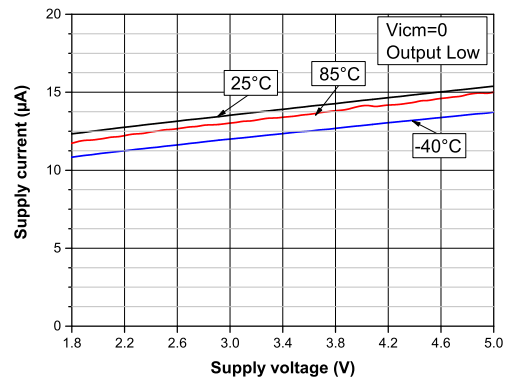
**Figure 2. Supply current vs supply voltage,  $V_{icm} = 0\text{ V}$ , output low**



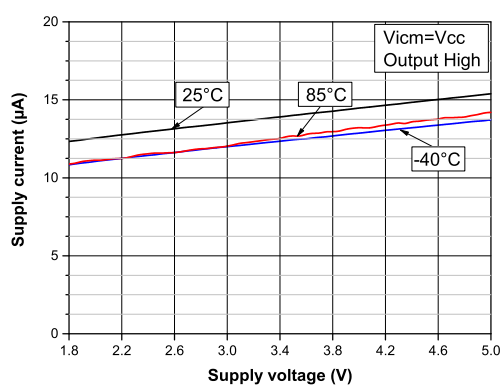
**Figure 3. Supply current vs supply voltage,  $V_{icm} = 0\text{ V}$ , output high**



**Figure 4. Supply current vs supply voltage,  $V_{icm} = V_{CC}$ , output low**



**Figure 5. Supply current vs supply voltage,  $V_{icm} = V_{CC}$ , output high**



**Figure 6. Input bias current vs. input common mode voltage  $V_{CC} = 1.8\text{ V}$**

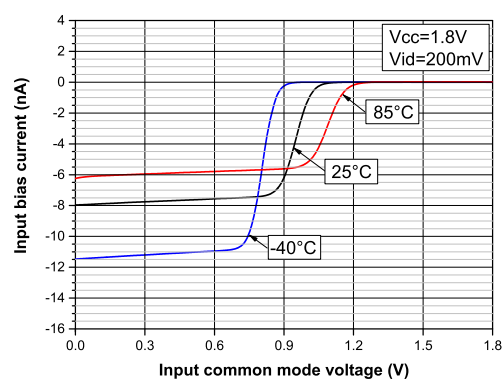


Figure 7. Input bias current vs. input common mode voltage  $V_{CC} = 2.7\text{ V}$

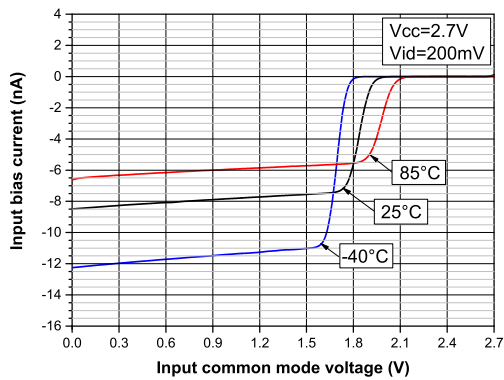


Figure 8. Input bias current vs. input common mode voltage  $V_{CC} = 5\text{ V}$

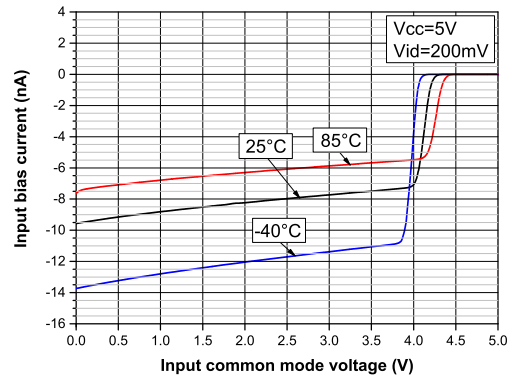


Figure 9. Input offset voltage vs. input common mode voltage  $V_{CC} = 1.8\text{ V}$

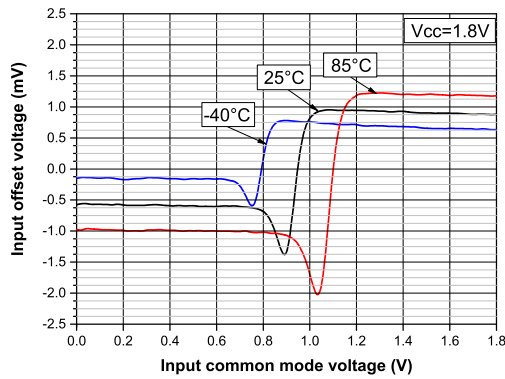


Figure 10. Input offset voltage vs. input common mode voltage  $V_{CC} = 2.7\text{ V}$

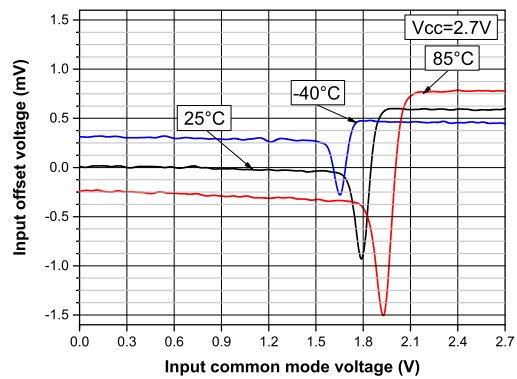


Figure 11. Input offset voltage vs. input common mode voltage  $V_{CC} = 5\text{ V}$

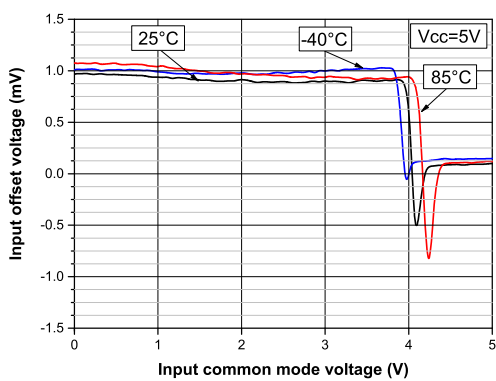
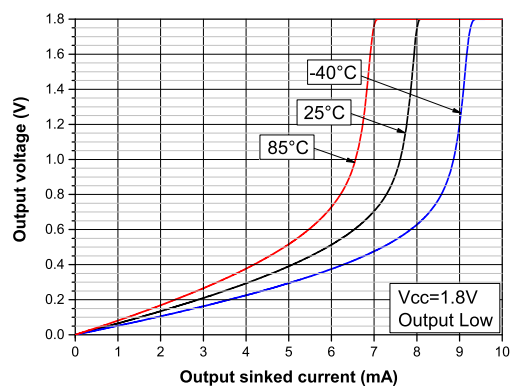
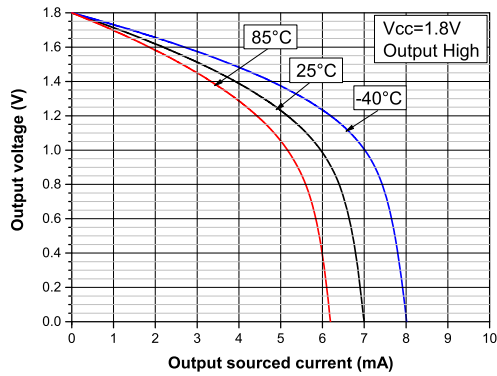


Figure 12. Output voltage vs. output sink current  $V_{CC} = 1.8\text{ V}$

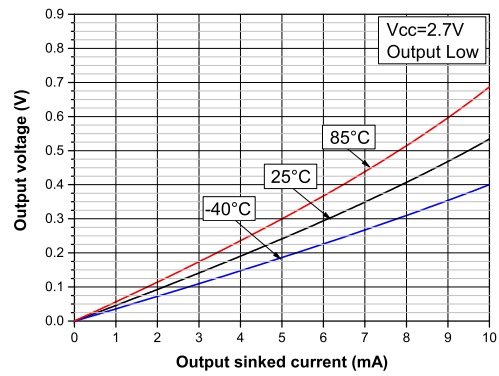




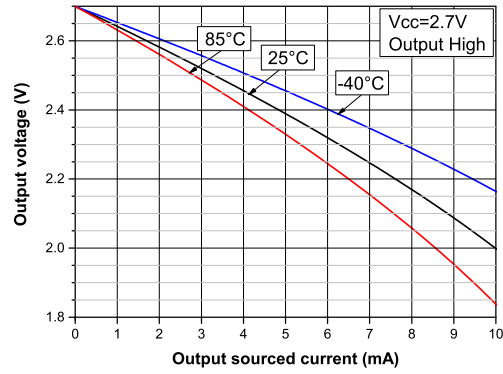
**Figure 13. Output voltage vs. output source current  $V_{CC} = 1.8\text{ V}$**



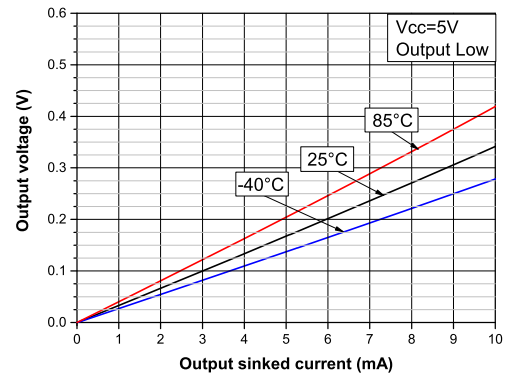
**Figure 14. Output voltage vs. output sink current  $V_{CC} = 2.7\text{ V}$**



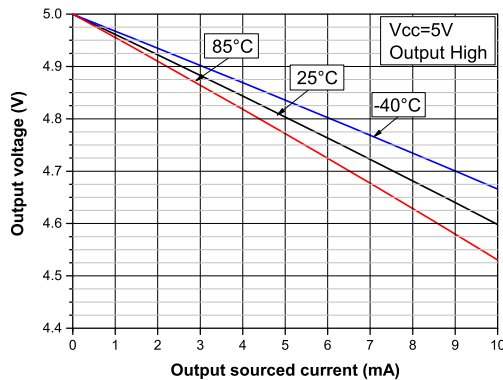
**Figure 15. Output voltage vs. output source current  $V_{CC} = 2.7\text{ V}$**



**Figure 16. Output voltage vs. output sink current  $V_{CC} = 5\text{ V}$**



**Figure 17. Output voltage vs. output source current  $V_{CC} = 5\text{ V}$**



**Figure 18. Propagation delay low to high vs temperature with 50 mV input overdrive**

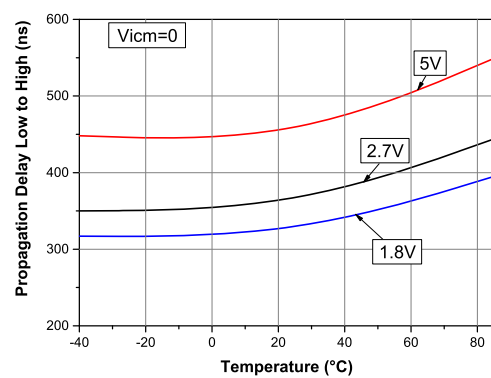


Figure 19. Propagation delay high to low vs temperature with 50 mV input overdrive

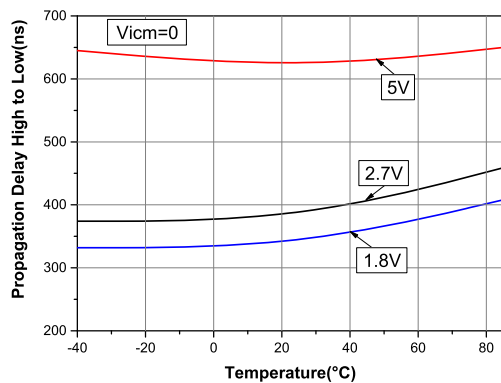


Figure 20. Propagation delay vs input common mode voltage  $V_{CC} = 1.8\text{ V}$  negative transition

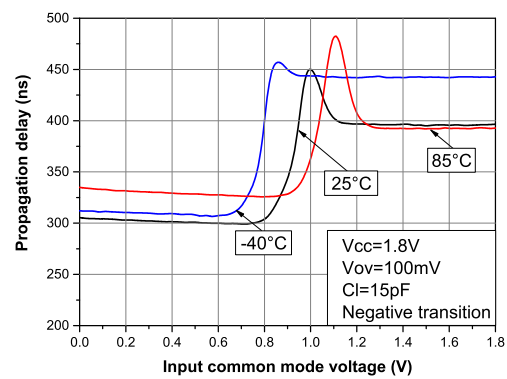


Figure 21. Propagation delay vs input common mode voltage  $V_{CC} = 1.8\text{ V}$  positive transition

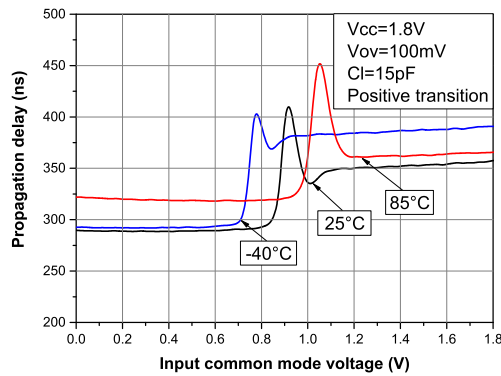


Figure 22. Propagation delay vs input common mode voltage  $V_{CC} = 2.7\text{ V}$  negative transition

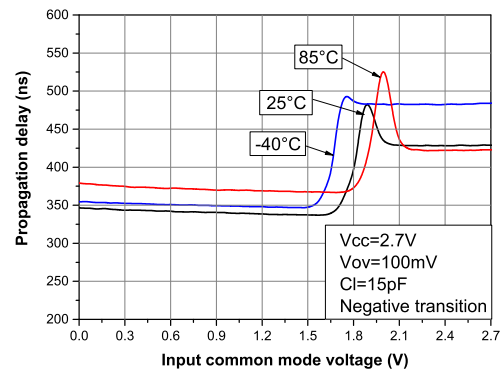


Figure 23. Propagation delay vs input common mode voltage  $V_{CC} = 2.7\text{ V}$  positive transition

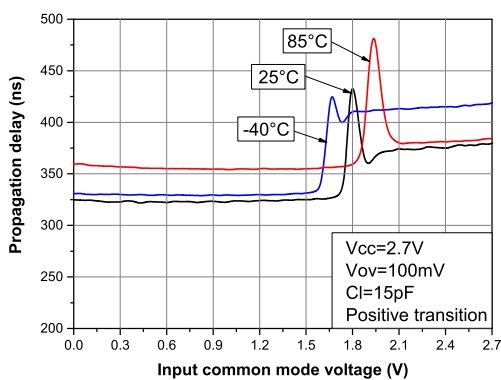
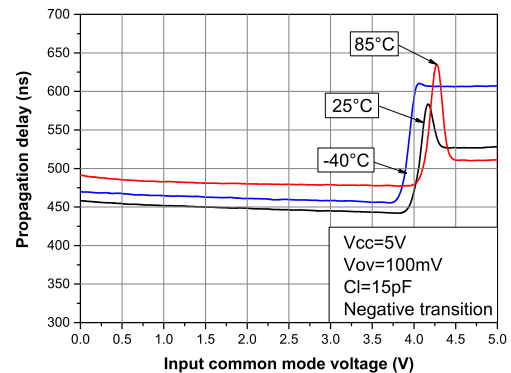
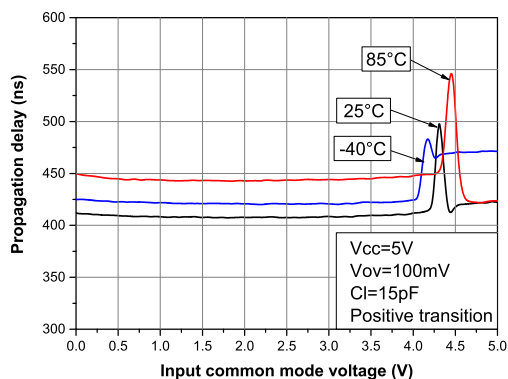


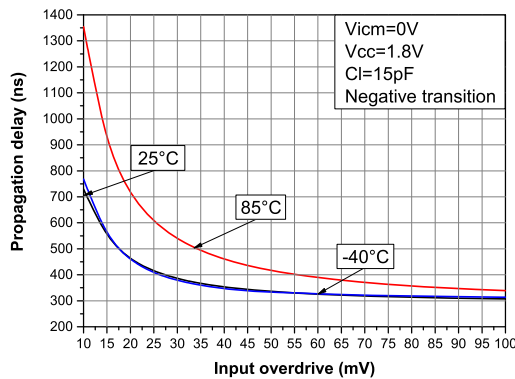
Figure 24. Propagation delay vs input common mode voltage  $V_{CC} = 5\text{ V}$  negative transition



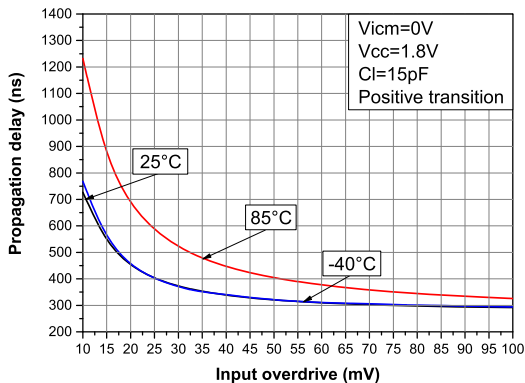
**Figure 25. Propagation delay vs input common mode voltage  $V_{CC} = 5\text{ V}$  positive transition**



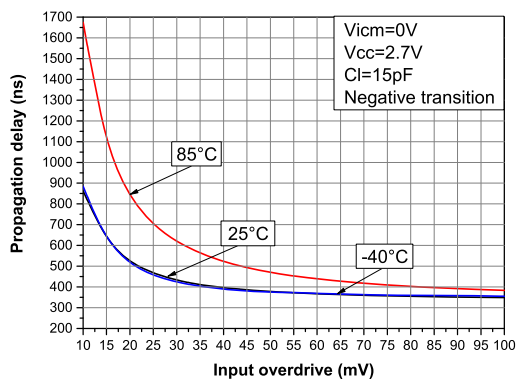
**Figure 26. Propagation delay vs input overdrive voltage  $V_{CC} = 1.8\text{ V}$  negative transition**



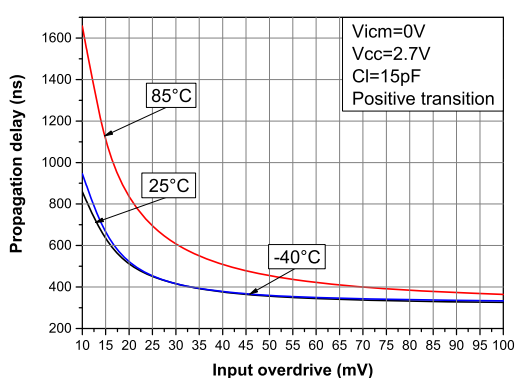
**Figure 27. Propagation delay vs input overdrive voltage  $V_{CC} = 1.8\text{ V}$  positive transition**



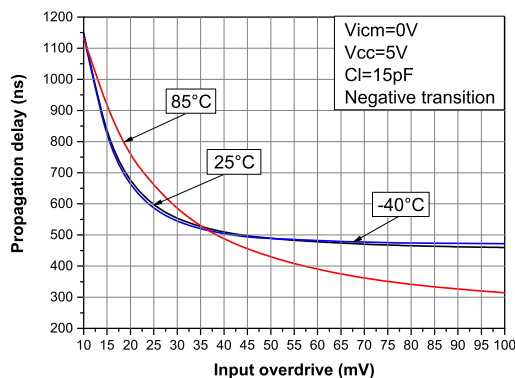
**Figure 28. Propagation delay vs input overdrive voltage  $V_{CC} = 2.7\text{ V}$  negative transition**



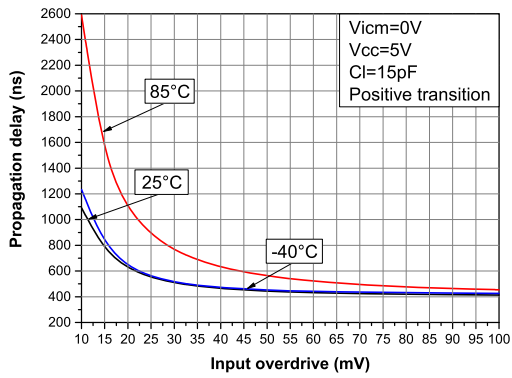
**Figure 29. Propagation delay vs input overdrive voltage  $V_{CC} = 2.7\text{ V}$  positive transition**



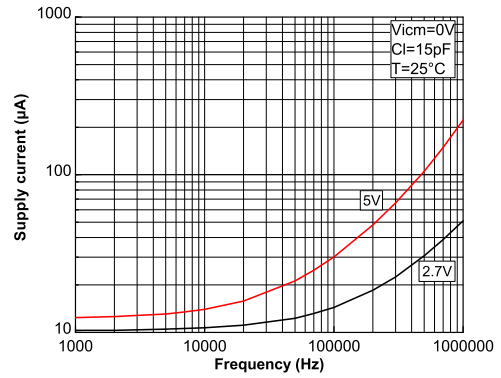
**Figure 30. Propagation delay vs input overdrive voltage  $V_{CC} = 5\text{ V}$  negative transition**



**Figure 31. Propagation delay vs input overdrive voltage  $V_{CC} = 5\text{ V}$  positive transition**



**Figure 32. Supply current vs output transition frequency and supply voltage**



## 4 Package information

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK<sup>®</sup> packages, depending on their level of environmental compliance. ECOPACK<sup>®</sup> specifications, grade definitions and product status are available at: [www.st.com](http://www.st.com). ECOPACK<sup>®</sup> is an ST trademark.

### 4.1 CSP 6-bump package information

Figure 33. CSP 6-bump package outline

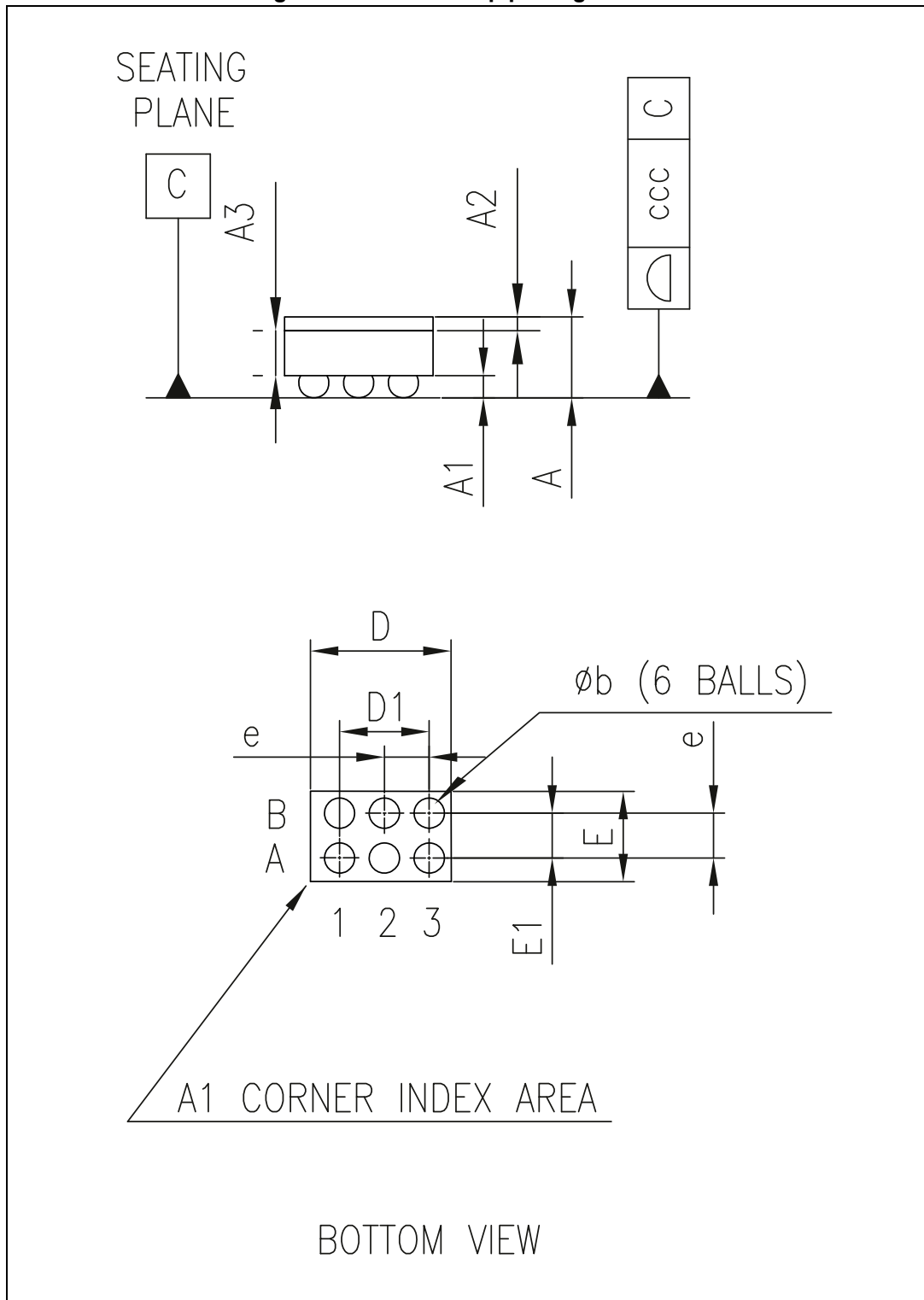


Table 6. CSP 6-bump mechanical data

Ref.	Dimensions					
	Millimeters			Inches		
	Min.	Typ.	Max.	Min.	Typ.	Max.
A	0.485	0.525	0.57	0.019	0.021	0.022
A1	0.17		0.23	0.007		0.009
A2		0.025	0.03		0.001	0.001
A3	0.275	0.3	0.325	0.011	0.012	0.013
b	0.23	0.26	0.29	0.009	0.01	0.011
D	1.18	1.2	1.22	0.046	0.047	0.048
D1		0.8			0.031	
E	0.78	0.8	0.82	0.031	0.031	0.032
E1		0.4			0.016	
e		0.4			0.016	
ccc			0.075			0.003

## 5 Ordering information

**Table 7. Order codes**

Order code	Temperature range	Package	Packing	Marking
TS985IJT	-40 °C to 85 °C	CSP 6-bump	Tape and reel	TBA



## 6 Revision history

Table 8. Document revision history

Date	Revision	Changes
23-Jun-2016	1	Initial release

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