Quad-Channel, HD Image Signal Processor with *Precision Timing* Core

ADI Confidential

ADDI7004

FEATURES

Support for CCD and CMOS image sensors
4 AFE channels
1.8 V analog and digital core supply voltage
Serial data output with reduced range LVDS outputs
Differential analog inputs
CDS or SHA configuration (CDS bypass) with
−3 dB, 0 dB, +3 dB, and +6 dB gain
6 dB to 42 dB, 10-bit variable gain amplifier (VGA)
14-bit, 72 MHz analog-to-digital converter (ADC)
Black level clamp with variable level control
***Precision Timing* core with 220 ps resolution at 72 MHz**

APPLICATIONS

Digital video cameras
Digital still cameras
Medical Imaging
High speed industrial cameras

GENERAL DESCRIPTION

The ADDI7004 is a highly integrated, quad-channel, HD image signal processor for high speed imaging applications. Each channel is specified at pixel rates of up to 72 MHz and consists of a complete analog front end (AFE) with ADC conversion. The *Precision Timing*™ core allows adjustment of the correlated double sampler (CDS) and sample-and-hold amplifier (SHA) clocks with 220 ps resolution at 72 MHz operation. The ADDI7004 also contains a reduced range low voltage differential signaling (LVDS) interface for the dual-channel data outputs.

Each analog front end includes black level clamping, a CDS/SHA, a VGA, and a 72 MHz, 14-bit analog-to-digital converter (ADC). Operation is programmed using a 3-wire serial interface.

Packaged in a space-saving, 6 mm × 6 mm, 76-ball BGA, the ADDI7004 is specified over an operating temperature range of −40°C to +85°C.

FUNCTIONAL BLOCK DIAGRAM

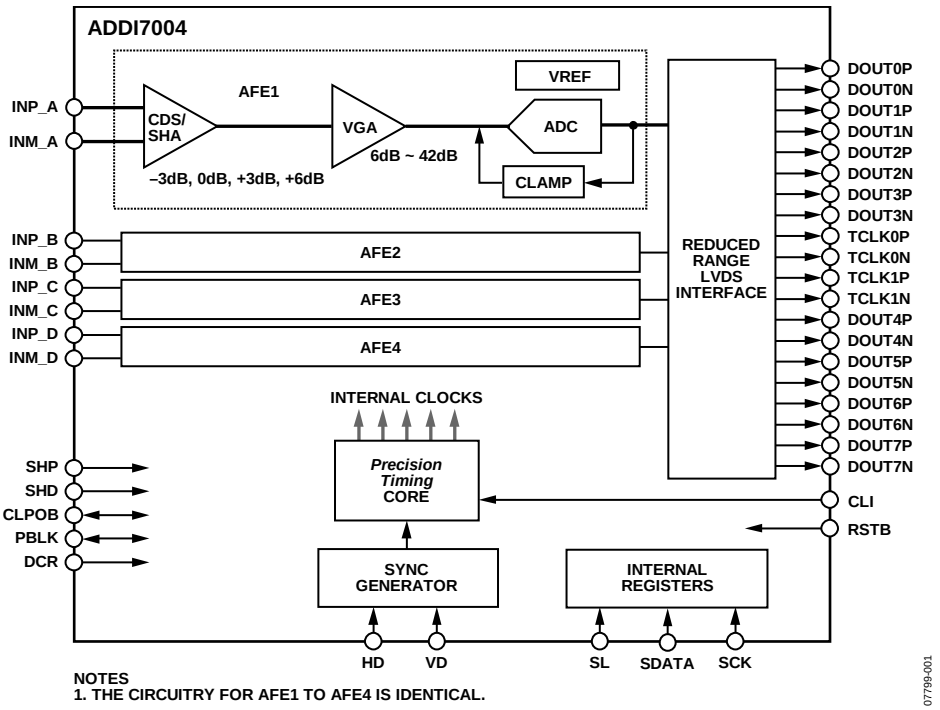

Figure 1.

Rev. SpE **Document Feedback**

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11/08—Revision Sp0: Initial Version

SPECIFICATIONS

Table 1.

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
TEMPERATURE RANGE					
Operating	−40		+85	°C	
Storage	−65		+150	°C	
POWER SUPPLY VOLTAGE[1]					
INVDD	2.7	3.0	3.6	V	AFE and CLI input supply
AVDD	1.65	1.8	2.0	V	AFE and timing core supply
DVDD	AVDD	1.8	AVDD + 0.2 (or 2.0 V)	V	Internal digital supply
LVDD	1.65	1.8	2.0	V	LVDS driver supply
IOVDD	1.65	3.0	3.6	V	I/O supply for HD, VD, SCK, SL, SDATA
POWER SUPPLY CURRENTS					
72 MHz Operation					
INVDD (CDS Mode)		0.1		mA	3.0 V
INVDD (SHA Mode)		9.1		mA	3.0 V
AVDD		203		mA	1.8 V
DVDD		44.5		mA	1.8 V
LVDD		31		mA	1.8 V
IOVDD		0.1		mA	3.0 V
Standby Mode Operation					
Standby 1 AVDD		13.5		mA	
Standby 2/Standby 3 AVDD		0.1		mA	
CLOCK RATE (CLI)	10		72	MHz	

[1] AVDD, DVDD, and LVDD must all originate from the same 1.8 V supply.

DIGITAL SPECIFICATIONS

IOVDD = 1.6 V to 3.6 V, C_L = 20 pF, T_{MIN} to T_{MAX}, unless otherwise noted.

Table 2.

Parameter	Symbol	Min	Typ	Max	Unit
LOGIC INPUTS					
High Level Input Voltage	V_{IH}	IOVDD − 0.6			V
Low Level Input Voltage	V_{IL}			0.6	V
High Level Input Current	I_{IH}		10		µA
Low Level Input Current	I_{IL}		10		µA
Input Capacitance	C_{IN}		10		pF
LOGIC OUTPUTS					
High Level Output Voltage, I_{OH} = 2 mA	V_{OH}	IOVDD − 0.5			V
Low Level Output Voltage, I_{OL} = 2 mA	V_{OL}			0.5	V
CLI INPUT (CLI_BIAS = 0)					
High Level Input Voltage	V_{IHCLI}	INVDD/2 + 0.5			V
Low Level Input Voltage	V_{ILCLI}			INVDD/2 − 0.5	V

ANALOG SPECIFICATIONS

AVDD = 1.8 V, f_{CLI} = 72 MHz, typical timing specifications, T_{MIN} to T_{MAX}, unless otherwise noted.

Table 3.

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
CDS[1]					
Input Capacitance		8		pF	
DC Restore Voltage	1.0	1.3	1.5	V	AVDD − 0.5 V
Allowable CCD Reset Transient		0.5	1.5	V	
CDS Gain Accuracy					VGA gain = 6 dB (Code 15, default value)
−3.0 dB CDS Gain	−3.4	−2.9	−2.4	dB	
0 dB CDS Gain (Default)	−0.7	−0.2	+0.3	dB	
+3 dB CDS Gain	2.2	2.7	3.2	dB	
+6 dB CDS Gain	4.8	5.3	5.8	dB	
Input Voltage Limits	AVSS − 0.3 V		INVDD + 0.3 V	V	Voltage at INP_x or INM_x
Maximum Signal Voltage					Differential signal in CDS or SHA mode
−3 dB CDS Gain		1.4		V p-p	
0 dB CDS Gain (Default)		1.0		V p-p	
+3 dB CDS Gain		0.7		V p-p	
+6 dB CDS Gain		0.5		V p-p	
Allowable Optical Black (OB) Pixel Amplitude[1]					
0 dB CDS Gain (Default)	−100		+200	mV	
+6 dB CDS Gain	−50		+100	mV	
VARIABLE GAIN AMPLIFIER (VGA)					
Gain Control Resolution		1024		Steps	
Gain Monotonicity		Guaranteed			
Low Gain Setting (VGA Code 15, Default)		6.3		dB	
Maximum Gain Setting (VGA Code 1023)		42.5		dB	
BLACK LEVEL CLAMP					
Clamp Level Resolution		1024		Steps	
Minimum Clamp Level (Code 0)		0		LSB	Measured at ADC output
Maximum Clamp Level (Code 1023)		1023		LSB	Measured at ADC output
ADC					
Resolution	14			Bits	
Differential Nonlinearity (DNL)	−1.0	±0.5		LSB	
No Missing Codes		Guaranteed			
Integral Nonlinearity (INL)		5	20	LSB	
Full-Scale Input Voltage		2.0		V	
SYSTEM PERFORMANCE					Specifications include entire signal chain
VGA Gain Accuracy					0 dB CDS gain (default)
Low Gain (Code 15)	5.8	6.3	6.8	dB	Gain = (0.0359 × code) + 5.76 dB
Maximum Gain (Code 1023)	4.1	42.5	43	dB	
Peak Nonlinearity, 500 mV Input Signal		0.3	0.3	%	12 dB total gain applied
Total Output Noise		2.2		LSB rms	AC-grounded input, 3 dB total gain applied
Power Supply Rejection (PSR)		45		dB	Measured with step change on supply

[1] Input signal characteristics are defined as shown in Figure 2.

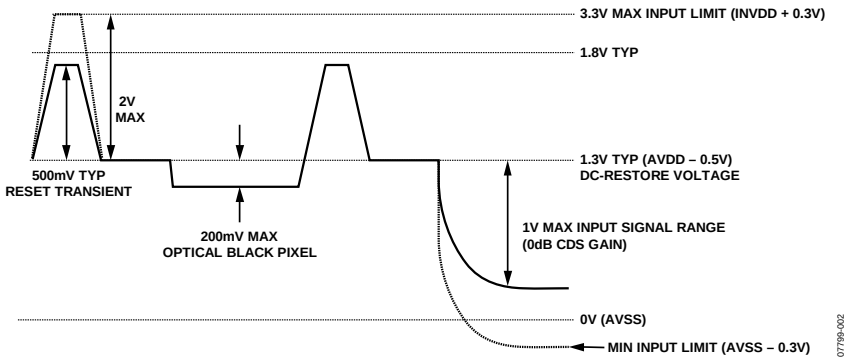


Figure 2. Input Signal Characteristics

CHANNEL-TO-CHANNEL SPECIFICATIONS

T_{MIN} to T_{MAX}, AVDD = DVDD = 1.8 V, INVDD = 3.0 V, f_{CLI} = 72 MHz, typical timing specifications

Table 4.

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
LINEARITY MISMATCH[1]		<0.5	1.0	%	Absolute value above 1/16 of maximum output code
CROSSTALK ERROR					CDS = 0 dB
Any Two Channels		80		dB	Full-scale step applied to one channel while measuring response on any other channel.

[1] Refer to linearity mismatch definition in the Terminology section for further measurement explanation.

LVDS SPECIFICATIONS

R_L = 100 Ω, LVDD = 1.8 V, f_{CLI} = 72 MHz, f_{TCLK} = 288 MHz, unless otherwise noted.

Table 5. Reduced Range LVDS Driver Specifications

Parameter	Conditions	Symbol	Min	Typ	Max	Unit
Output Voltage High, V_{OA} or V_{OB}	R_{LOAD} = 100 Ω ± 1%	V_{OH}			1400	mV
Output Voltage Low, V_{OA} or V_{OB}	R_{LOAD} = 100 Ω ± 1%	V_{OL}	1000			mV
Output Differential Voltage	R_{LOAD} = 100 Ω ± 1%	$\|V_{OD}\|$	120		290	mV
Output Offset Voltage	R_{LOAD} = 100 Ω ± 1%	V_{OS}	1075		1350	mV
Change in $\|V_{OD}\|$ Between 0 and 1	R_{LOAD} = 100 Ω ± 1%	$\|V_{OD}\|$			25	mV
Change in V_{OS} Between 0 and 1	R_{LOAD} = 100 Ω ± 1%	V_{OS}			25	mV

Table 6. LVDS Driver AC Specifications

Parameter	Conditions	Symbol	Min	Typ	Max	Unit
Clock Signal Duty Cycle		t_{CYCLE}	40		60	%
TCLK Frequency		f_{TCLK}			288	MHz
V_{OD} Fall Time, 20% to 80%	R_{LOAD} = 100 Ω ± 1%	t_{FALL}		140		ps
V_{OD} Rise Time, 20% to 80%	R_{LOAD} = 100 Ω ± 1%	t_{RISE}		140		ps
Differential Skew	Any differential pair	t_{SKEW1}		25		ps
Channel-to-Channel Skew	Any two signals	t_{SKEW2}		30		ps

LVDS TIMING DIAGRAMS

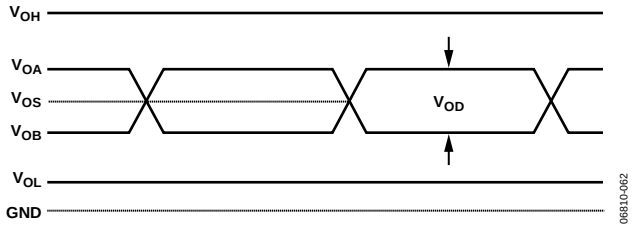


Figure 3. LVDS Driver Waveform

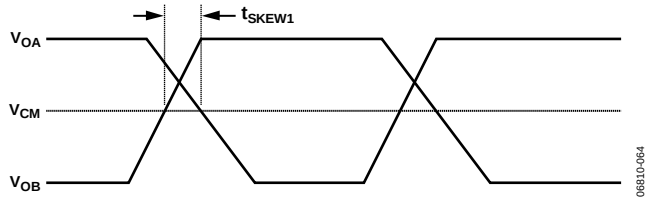


Figure 5. Definition of t_{SKEW1}

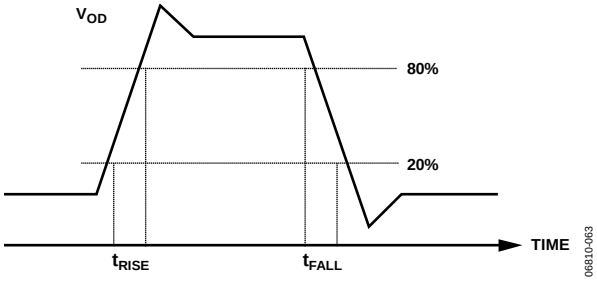


Figure 4. Driver Rise and Fall Times

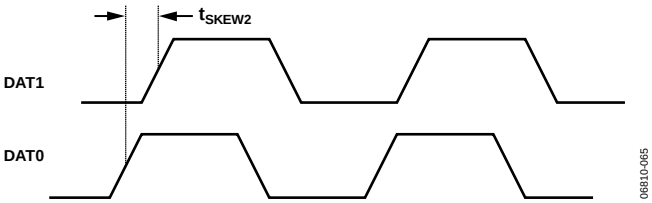


Figure 6. Definition of t_{SKEW2}

TIMING SPECIFICATIONS

C_L = 20 pF, AVDD = DVDD = 1.8 V, f_{CLI} = 72 MHz, unless otherwise noted.

Table 7.

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions/ Comments
MASTER CLOCK (CLI)						
CLI Clock Period	t_{CONV}	13.3			ns	
CLI High/Low Pulse Width	t_{ADC}	0.8 (t_{CONV}/2)	t_{CONV}/2	1.2 × t_{CONV}/2	ns	
Delay from CLI Rising Edge to Internal Pixel Position 0	t_{CLIDLY}		12.5		ns	
AFE						
SHPLOC Sample Edge to SHDLOC Sample Edge	t_{S1}	0.8 (t_{CONV}/2)	t_{CONV}/2	t_{CONV} − t_{S2}	ns	
SHDLOC Sample Edge to SHPLOC Sample Edge	t_{S2}	0.8 (t_{CONV}/2)	t_{CONV}/2	t_{CONV} − t_{S1}	ns	
AFE Pipeline Delay			23		Cycles	
CLPOB Pulse Width[1]		2	20		Pixels	
SERIAL INTERFACE						
Maximum SCK Frequency (Must Not Exceed CLI Frequency)	f_{SCLK}	72			MHz	
SL-to-SCK Setup Time	t_{LS}	10			ns	
SCK-to-SL Hold Time	t_{LH}	10			ns	
SDATA Valid-to-SCK Rising Edge Setup	t_{DS}	10			ns	
SCK Falling Edge-to-SDATA Valid Hold	t_{DH}	10			ns	

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions/ Comments
H-COUNTER RESET SPECIFICATIONS						
HD Pulse Width		t_{CLI}				
VD Pulse Width		t_{CLI}				
VD Falling Edge to HD Falling Edge	t_{VDHD}	0		VD period − t_{CONV}	ns	
HD Falling Edge to CLI Rising Edge (CLI_BIAS = 0)	t_{HDCLI}	3		t_{CONV} − 2	ns	
HD Falling Edge to CLI Rising Edge (CLI_BIAS = 1)	t_{HDCLI}	t_{CONV} − 1.5		t_{CONV} − 6.5	ns	
TIMING CORE SETTING RESTRICTIONS						
Inhibited Region for SHP Edge Location	t_{SHPINH}	44		63		Edge location
Inhibited Region for DOUTPHASEP Edge Location	$t_{DOUTINH}$	SHDLOC + 0		SHDLOC + 24		Edge location
Inhibited Region for External Active Edge Location:(CLI Rising Edge to External SHP Active Edge)	t_{SHPINH_EXT}	0.28 × t_{CONV}		0.51 × t_{CONV}		
Inhibited Region for DOUTPHASE with Respect to External SHD	$t_{DOUTINH\_EXT}$	SHD − (0.03 × t_{CONV})		SHD + (0.11 × t_{CONV})		

[1] Minimum CLPOB pulse width is for functional operation only. Wider typical pulses are recommended to achieve good clamp performance.

ABSOLUTE MAXIMUM RATINGS

Table 8.

Parameter	Rating
AVDD to AVSS	−0.3 V to +2.2 V
DVDD to DVSS	−0.3 V to +2.2 V
LVDD to LVSS	−0.3 V to +2.2 V
INVDD to INVSS	−0.3 V to +3.9 V
IOVDD to IOVSS	−0.3 V to +3.9 V
Any VSS to Any VSS	−0.3 V to +0.3 V
Digital Outputs to IOVSS	−0.3 V to IOVDD + 0.3 V
Digital Inputs to IOVSS	−0.3 V to IOVDD + 0.3 V
SCK, SL, SDATA to IOVSS	−0.3 V to IOVDD + 0.3 V
INP_x to INVSS	−0.3 V to INVDD + 0.3 V
Junction Temperature	150°C
Lead Temperature (Soldering, 10 sec)	350°C

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

THERMAL RESISTANCE

θ_{JA} is measured using a 4-layer PCB.

Table 9. Thermal Resistance

Package Type	θ_{JA}	Unit
76-Ball CSP_BGA	48.3	°C/W

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

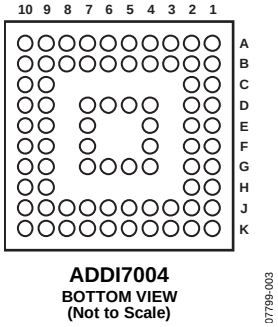


Figure 7. Pin Configuration

Table 10. Pin Function Descriptions

Pin No.	Mnemonic	Type	Description
A1	AVDD	Power	Analog Supply (1.8 V)
D1	SL	Digital input	3-Wire Serial Load
C2	SDATA	Digital input	3-Wire Serial Data
D2	SCK	Digital input	3-Wire Serial Clock
E1	IOVDD	Power	I/O Supply (1.8 V or 3.3 V)
F1	IOVDD	Power	I/O Supply (1.8 V or 3.3 V)
D4	IOVSS	Power	I/O Supply Ground
E4	IOVSS	Power	I/O Supply Ground
F4	IOVSS	Power	I/O Supply Ground
F2	VD	Digital input	Vertical Sync Pulse
G2	HD	Digital input	Horizontal Sync Pulse
G1	DVDD	Power	Digital Logic Supply (1.8 V)
G10	DVDD	Power	Digital Logic Supply (1.8 V)
D5	DVSS	Power	Digital Logic Ground
D6	DVSS	Power	Digital Logic Ground
D7	DVSS	Power	Digital Logic Ground
E7	DVSS	Power	Digital Logic Ground
F7	DVSS	Power	Digital Logic Ground
G7	DVSS	Power	Digital Logic Ground
G6	DVSS	Power	Digital Logic Ground
G5	DVSS	Power	Digital Logic Ground
G4	DVSS	Power	Digital Logic Ground
J1	DOUT0P	Digital output	Data Output 0, Positive Output
K1	DOUT0N	Digital output	Data Output 0, Negative Output
J2	DOUT1P	Digital output	Data Output 1, Positive Output
K2	DOUT1N	Digital output	Data Output 1, Negative Output
J3	DOUT2P	Digital output	Data Output 2, Positive Output
K3	DOUT2N	Digital output	Data Output 2, Negative Output
J4	DOUT3P	Digital output	Data Output 3, Positive Output
K4	DOUT3N	Digital output	Data Output 3, Negative Output
J5	TCLK0P	Digital output	Transmit Clock 0, Positive Output
K5	TCLK0N	Digital output	Transmit Clock 0, Negative Output
J6	TCLK1P	Digital output	Transmit Clock 1, Positive Output
K6	TCLK1N	Digital output	Transmit Clock 1, Negative Output
J7	DOUT4P	Digital output	Data Output 4, Positive Output
K7	DOUT4N	Digital output	Data Output 4, Negative Output
J8	DOUT5P	Digital output	Data Output 5, Positive Output
K8	DOUT5N	Digital output	Data Output 5, Negative Output

Pin No.	Mnemonic	Type	Description
J9	DOUT6P	Digital output	Data Output 6, Positive Output
K9	DOUT6N	Digital output	Data Output 6, Negative Output
J10	DOUT7P	Digital output	Data Output 7, Positive Output
K10	DOUT7N	Digital output	Data Output 7, Negative Output
H1	LVDD	Power	LVDS Driver Supply (1.8 V)
H2	LVSS	Power	LVDS Driver Ground
H10	LVDD	Power	LVDS Driver Supply (1.8 V)
H9	LVSS	Power	LVDS Driver Ground
E2	RSTB	Digital input	External Reset Input (Active Low)
D10	CLI	Digital input	Master Clock Input
A5	INVDD	Power	Input Supply (3.3 V)
B5	INVSS	Power	Input Ground
B1	AVDD	Power	Analog Supply (1.8 V)
C1	AVSS	Power	Analog Ground
A10	AVDD	Power	Analog Supply (1.8 V)
C10	AVSS	Power	Analog Ground
A2	INP_A	Analog input	Analog Input, Positive, Channel A
B2	INM_A	Analog input	Analog Input, Negative, Channel A
A4	INP_B	Analog input	Analog Input, Positive, Channel B
B4	INM_B	Analog input	Analog Input, Negative, Channel B
A6	INVDD	Power	Input Supply (3.3 V)
B6	INVSS	Power	Input Ground
A7	INP_C	Analog input	Analog Input, Positive, Channel C
B7	INM_C	Analog input	Analog Input, Negative, Channel C
A9	INP_D	Analog input	Analog Input, Positive, Channel D
B9	INM_D	Analog input	Analog Input, Negative, Channel D
A3	AVSS	Power	Analog Ground
B10	AVDD	Power	Analog Supply (1.8 V)
B3	AVSS	Power	Analog Ground
A8	AVSS	Power	Analog Ground
B8	AVSS	Power	Analog Ground
C9	PBLK	Digital input/output	External PBLK Input/Internal PBLK Output
D9	CLPOB	Digital input/output	External CLPOB Input/Internal CLPOB Output
E9	DCR	Digital input	External DCR Input
F9	TEST1	Digital input/output	Test Input/Output (Float)
G9	TEST2	Digital input/output	Test Input/Output (Float)
E10	SHD	Digital input	External SHD Input
F10	SHP	Digital input	External SHP Input

TYPICAL PERFORMANCE CHARACTERISTICS

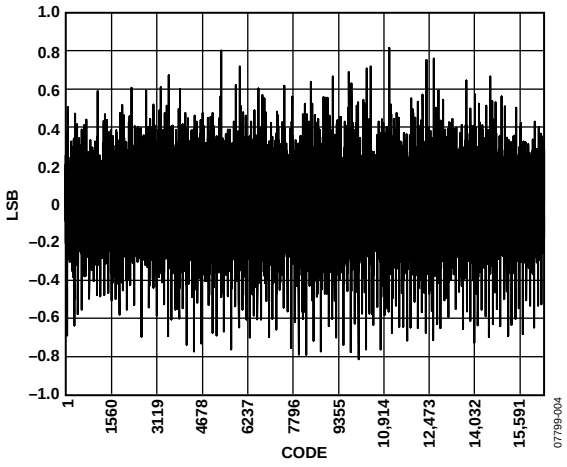


Figure 8. Differential Nonlinearity (DNL)

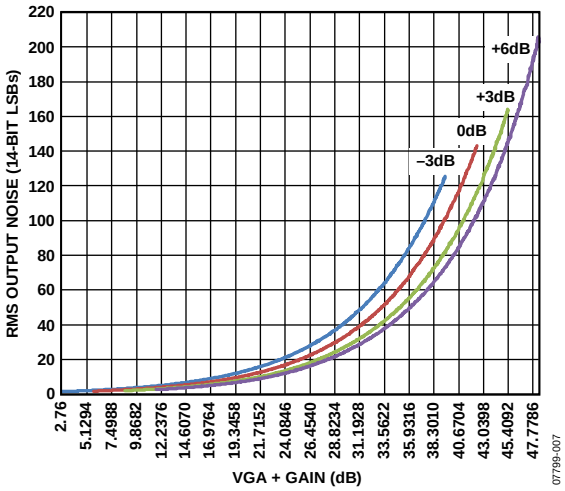


Figure 11. Noise vs. VGA + CDS Gain

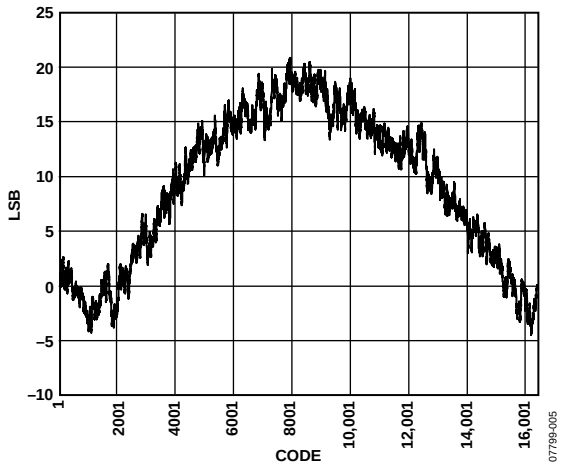


Figure 9. System Integral Nonlinearity (INL)

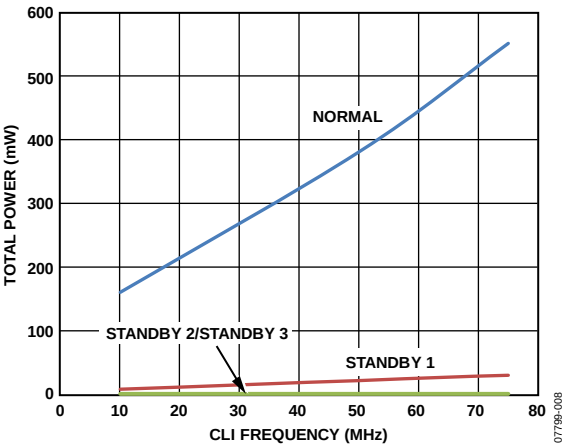


Figure 12. Power vs. Sample Rate

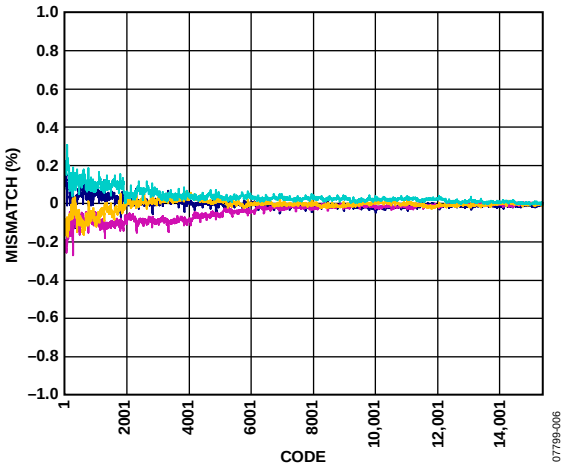


Figure 10. Linearity Mismatch vs. ADC Output Code

INPUT/OUTPUT CIRCUITS

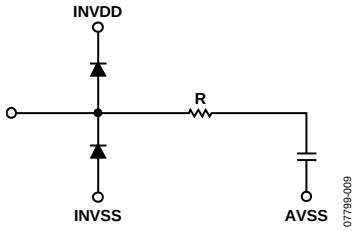


Figure 13. INP_x Input

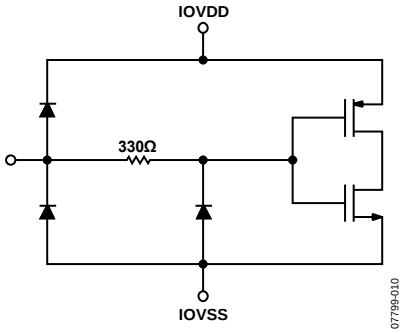


Figure 14. Digital Inputs

TERMINOLOGY

Differential Nonlinearity (DNL)
An ideal ADC exhibits code transitions that are exactly 1 LSB apart. DNL is the deviation from this ideal value. Therefore, every code must have a finite width. No missing codes guaranteed to 14-bit resolution indicates that all 16,384 codes, each for its respective input, must be present over all operating conditions.

Peak Nonlinearity
Peak nonlinearity, a full signal chain specification, refers to the peak deviation of the output of the ADDI7004 from a true straight line. The point used as zero scale occurs 0.5 LSB before the first code transition. Positive full scale is defined as a Level 1 LSB and 0.5 LSB beyond the last code transition. The deviation is measured from the middle of each particular output code to the true straight line. The error is then expressed as a percentage of the 2 V ADC full-scale signal. The input signal is always gained appropriately to fill the ADC full-scale range.

Total Output Noise
The total output noise is measured using histogram techniques. The standard deviation of the ADC output codes is calculated in LSBs and represents the rms noise level of the total signal chain at the specified gain setting. The output noise can be converted to an equivalent voltage using the relationship

$$1\ \text{LSB} = (\textit{ADC Full-Scale}/2^{n}\ \textit{Codes})$$

where n is the bit resolution of the ADC.

For the ADDI7004, 1 LSB is approximately 122.0 μV.

Linearity Mismatch
The linearity mismatch is calculated by taking the difference in INL of the two channels at an Input X, and then expressing the difference as a percentage of the output code at X. The values given in Table 4 are obtained over the range of 1/16 of maximum output code. The general trend is for the linearity mismatch to decrease as the output approaches the maximum code.

$$\textit{Linearity Mismatch}\,(\%) = \frac{\left|\textit{INL}\,A(X) - \textit{INL}\,B(X)\right|}{\textit{Output Code}(X)}$$

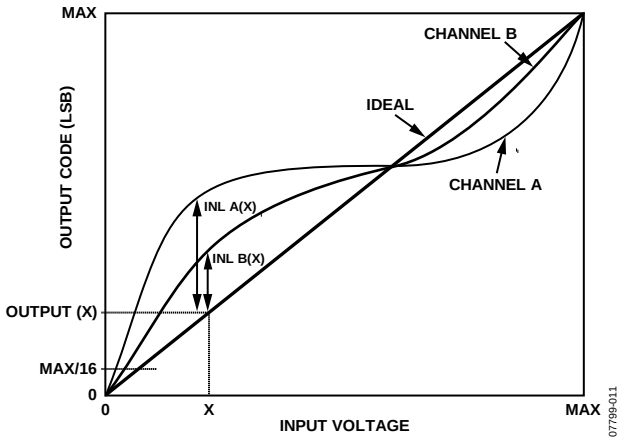


Figure 15. Linearity Mismatch Definition

Power Supply Rejection (PSR)
The PSR is measured with a step change applied to the supply pins. The PSR specification is calculated from the change in the data outputs for a given step change in the supply voltage.

Crosstalk
The crosstalk is measured while applying a full-scale step to one channel and measuring the interference on the opposite channel.

$$\textit{Crosstalk}\,(\text{dB}) = 20\log\left(\frac{\textit{Interference}\,(\text{LSB})}{16{,}384}\right)$$

THEORY OF OPERATION

Figure 16 shows the typical system block diagram for the ADDI7004. The CCD output is processed by the AFE circuitry of the ADDI7004, consisting of a CDS, VGA, black level clamp, and ADC converter. The digitized pixel information is sent to the digital image processor chip that performs the postprocessing and compression.

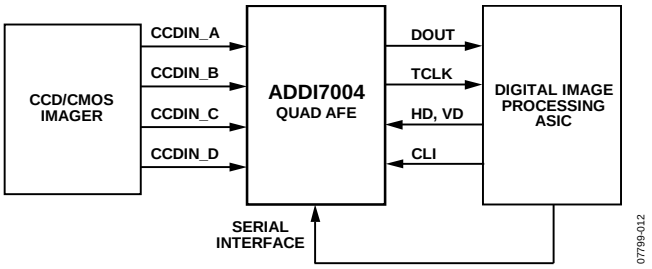


Figure 16. Typical Application

All ADDI7004 clocks are synchronized with VD and HD inputs. The pulse from the ADDI7004 black level clamp clock input (CLPOB) is programmed and generated internally.

Figure 17 and Figure 18 show the maximum vertical and horizontal counter dimensions for the ADDI7004. To specify line and pixel locations, these counters control all internal vertical and horizontal clocking. Maximum VD length is 8192 lines per field, and maximum HD length is 65,536 pixels per line.

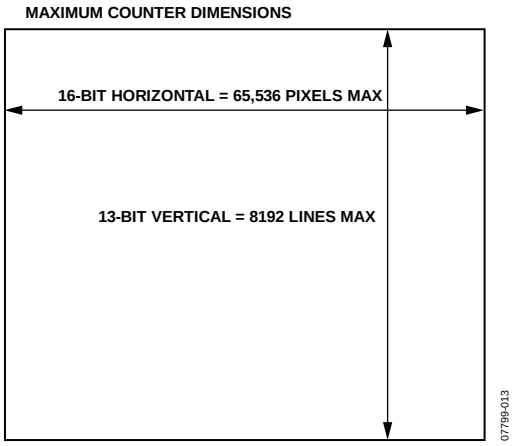


Figure 17. Vertical and Horizontal Counters

H-COUNTER BEHAVIOR IN SLAVE MODE

In the ADDI7004, the internal H-counter holds at its maximum count of 65,536 instead of rolling over. This feature allows the ADDI7004 to be used in applications containing a line length greater than 65,536 pixels. Although no programming values for the vertical and horizontal signals are available beyond 65,536 pixels, the horizontal driver (H), reset gate (RG), and analog front-end (AFE) clocking continues to operate, sampling the remaining pixels on the line.

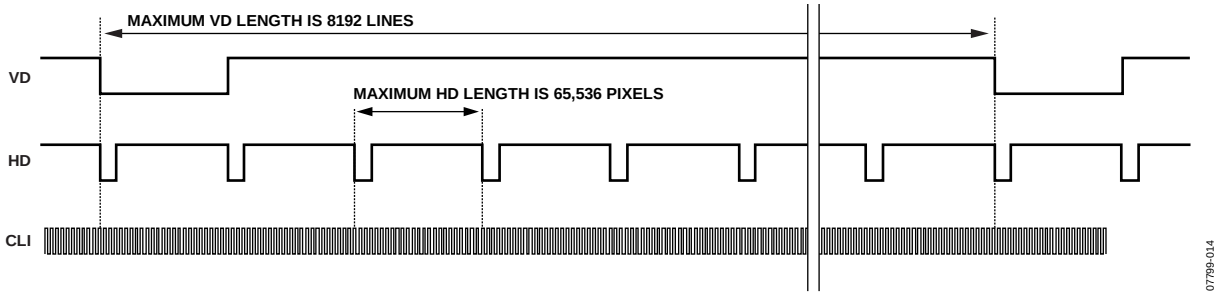


Figure 18. Maximum VD/HD Dimensions

PROGRAMMABLE TIMING GENERATION

Precision Timing HIGH SPEED TIMING CORE

The ADDI7004 generates flexible high speed timing signals using the *Precision Timing* core. This core is the foundation for generating the timing for both the AFE and SHP/SHD sample clocks. A unique architecture makes it routine for the system designer to optimize image quality by providing precise control over the AFE correlated double sampling.

Timing Resolution

The *Precision Timing* core uses a master clock input (CLI) as a reference. This clock should have the same frequency as the CCD pixel clock. Figure 19 illustrates how the internal timing core divides the master clock period into 64 steps, or edge positions. Therefore, the edge resolution of the *Precision Timing* core is (t_{CLI}/64). For more information on using CLI, refer to the Applications Information section.

Using a 72 MHz CLI frequency, the edge resolution of the *Precision Timing* core is approximately 220 ps. If a 1× system clock is not available, it is also possible to use a 2× reference clock by programming the CLI_DIVIDE register (Address 0x1B, Bits[1:0]). Then, the ADDI7004 internally divides the CLI frequency by 2.

High Speed Clock Programmability

Figure 20 shows how the high speed sample clocks SHP and SHD are generated.

The edge location registers are each six bits wide, allowing the selection of all 64 edge locations. Figure 20 shows the default timing locations for SHP and SHD.

Digital Data Outputs

For maximum system flexibility, the ADDI7004 uses the DOUTPHASEx register (Address 0x9A) to select the location for the start of each new pixel data value. Any edge location from 0 to 63 can be programmed. This register determines the start location of the data output and TCLK rising edge with respect to the master clock input (CLI). For more information, see the Programmable Data Delay section.

The pipeline delay through the ADDI7004 is shown in Figure 21. After the CCD input is sampled by SHD, there is a 23-cycle delay until the data is available.

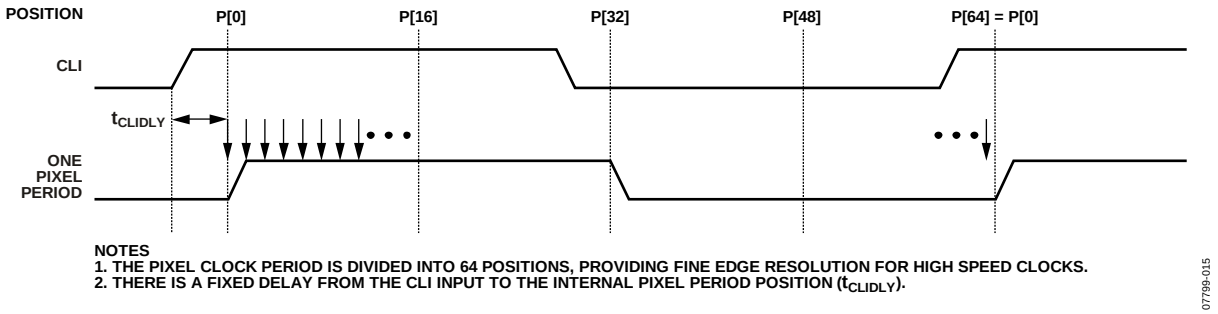
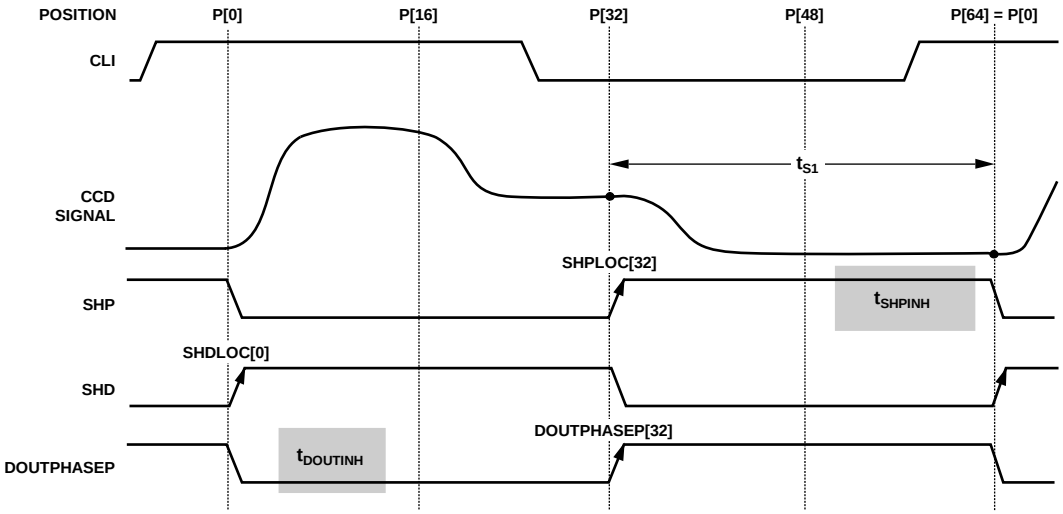


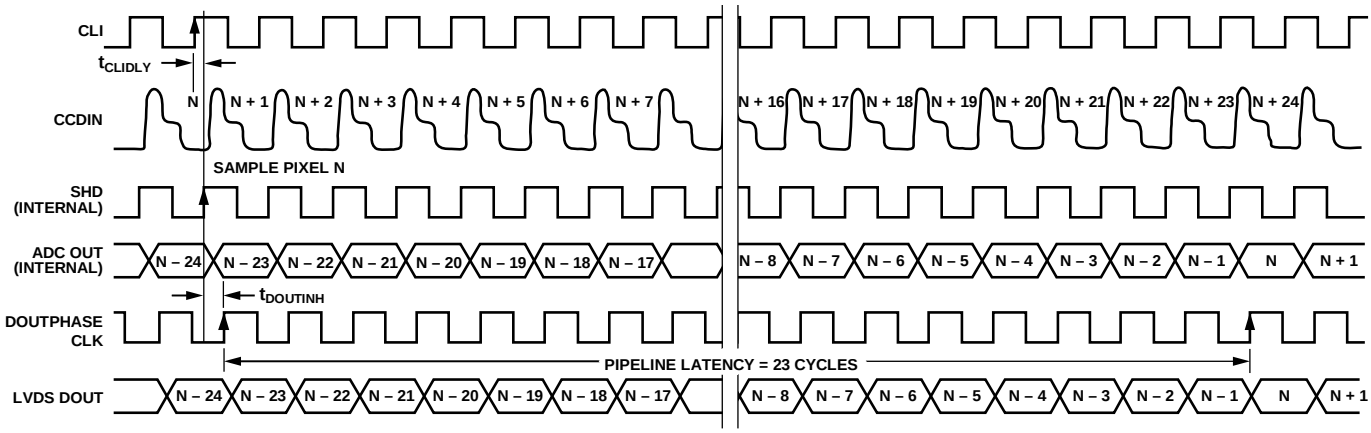
Figure 19. High Speed Clock Resolution from the Master Clock Input (CLI)



NOTES
1. SHP/SHD/DOUTx PHASE EDGES ARE FULLY PROGRAMMABLE TO ANY OF THE 64 POSITIONS WITHIN ONE PIXEL PERIOD. TYPICAL POSITIONS FOR EACH SIGNAL ARE SHOWN.
2. CERTAIN POSITIONS SHOULD BE AVOIDED FOR EACH SIGNAL AND ARE SHOWN ABOVE AS INHIBIT REGIONS.
3. IF A SETTING IN THE INHIBIT REGION IS USED, AN UNSTABLE PIXEL SHIFT MAY OCCUR IN THE CLPOB LOCATIONS OF THE AFE PIPELINE.

07799-016

Figure 20. High Speed Timing Typical Locations



NOTES
1. TIMING VALUES SHOWN ARE WITH SHDLOC = 0.
2. HIGHER VALUES OF SHD AND/OR DOUTPHASEx SHIFT DOUT TRANSITION TO THE RIGHT WITH RESPECT TO CLI LOCATION.
3. LVDS DOUT IS SHOWN AS A PARALLEL REPRESENTATION. SEE THE LVDS SERIAL DATA INTERFACE SECTION FOR MORE INFORMATION ON DOUT, TCLK, AND SERIAL DATA OUTPUT.

07799-017

Figure 21. Pipeline Delay of AFE Data Outputs

HORIZONTAL CLAMPING AND BLANKING

The horizontal clamping and blanking pulses of the ADDI7004 are fully programmable to suit a variety of applications. Individual control is provided for CLPOB during different regions of each field, specified by the region charge positions (RCPs), as shown in Figure 22. This allows the dark pixel clamping patterns to be changed at each stage of the readout to accommodate different image transfer timing and high speed line shifts.

Individual CLPOB and PBLK Patterns

The AFE horizontal timing consists of CLPOB and preblanking clock input (PBLK), as shown in Figure 23. These two signals are independently programmed using the registers listed in Table 11. POL is the start polarity for the signal, and TOG1 and TOG2 are the first and second toggle positions of the pulse, respectively. Note that only CLPOB has a POL setting. Both signals are active low and need to be programmed accordingly.

Two separate patterns for PBLK can be programmed, PBLK0 and PBLK1. The PBLKPAT register selects which of the two patterns is used in each field.

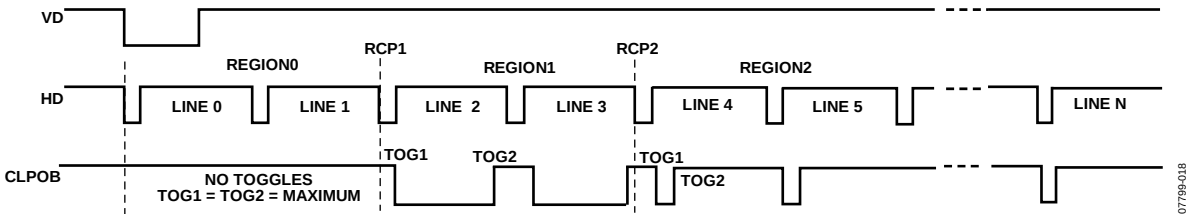


Figure 22. CLPOB Regions

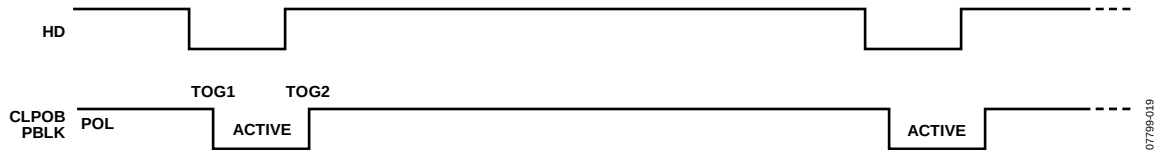


Figure 23. Clamp and Preblank Pulse Placement

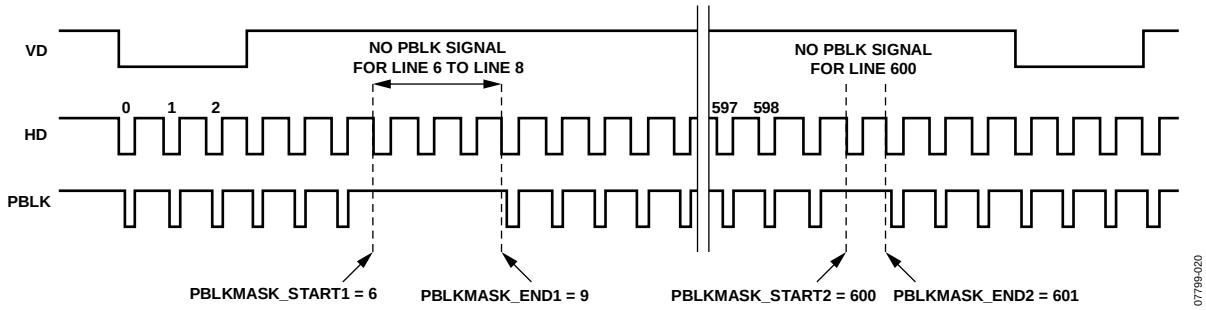


Figure 24. PBLK Masking Example

Table 11. CLPOB/PBLK Parameters

Parameter	Length	Range	Description
PBLK0_TOG1	16 bits	0 to 65,535 pixel location	First PBLK0 toggle position within the line.
PBLK0_TOG2	16 bits	0 to 65,535 pixel location	Second PBLK0 toggle position within the line.
PBLK1_TOG1	16 bits	0 to 65,535 pixel location	First PBLK1 toggle position within the line.
PBLK1_TOG2	16 bits	0 to 65,535 pixel location	Second PBLK1 toggle position within the line.
INT_PBLK_POL	1 bit	High/low	Starting polarity of the internal PBLK signal.
PBLKMASK_POL_REGx	1 bit	High/low	Starting polarity of PBLKMASK Region 1 to Region 3.
PBLKPAT	1 bit	0 to 1 settings	PBLK pattern selection.
PBLKMASK_STARTx	13 bits	0 to 8191 line location	PBLK mask start position. Three values are available.
PBLKMASK_ENDx	13 bits	0 to 8191 line location	PBLK mask end position. Three values are available.
RCPx	13 bits	0 to 8191 line location	Region change position for Region 0 to Region 6.
CLPOB_TOG1_REGx	16 bits	0 to 65,535 pixel location	First CLPOB toggle position for Region 0 to Region 7.
CLPOB_TOG2_REGx	16 bits	0 to 65,535 pixel location	Second CLPOB toggle position for Region 0 to Region 7.

PBLK and CLPOB Toggle Positions

The ADDI7004 uses an internal horizontal pixel counter to position PBLK and CLPOB toggle positions. Ideally, this counter resets to 0 on the falling edge of HD. The actual operation contains an internal pipeline delay associated with the counter. The horizontal counter does not reset to 0 until six CLI periods after the falling edge of HD. This six-cycle pipeline delay must be considered when determining the register toggle positions. For example, if CLPOB_TOG1_REGx = 100 and the pipeline delay is not considered, the final toggle position is applied at 112.

To obtain the correct toggle positions, the toggle position registers must be set to the desired toggle position minus 6. For example, if the desired toggle position is 100, CLPOB_TOGx_REGx should be set to 100 − 6 = 94 (see Figure 25).

Figure 26 and Figure 62 show the six-cycle pipeline delay referenced to the falling edge of HD. Figure 25 compares the toggle position values for desired and actual toggle positions. The CLPOB toggle settings must be set to greater than 0 for proper operation.

Disabling the PBLK and CLPOB Toggle Positions

If no toggles are desired for CLPOB or PBLK, one of the following settings should be used:

- CLPOB_TOG1_REGx = CLPOB_TOG2_REGx = 0x000
- CLPOB_TOG1_REGx = CLPOB_TOG2_REGx = 0xFFF

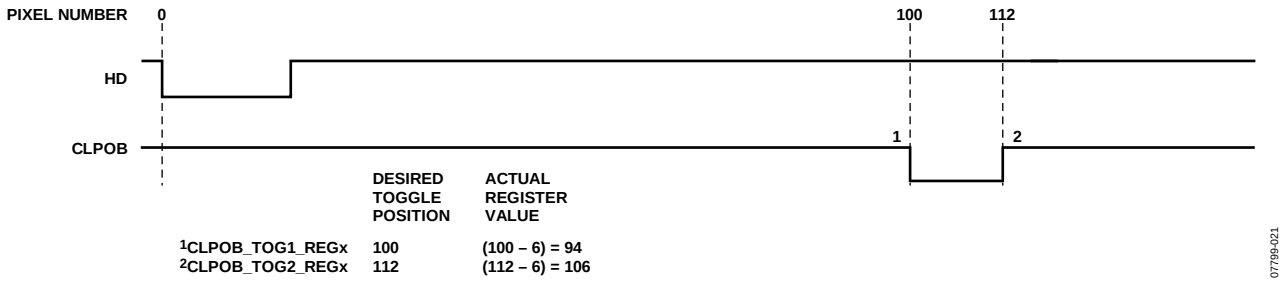


Figure 25. Example of Actual Register Settings to Obtain Desired Toggle Positions

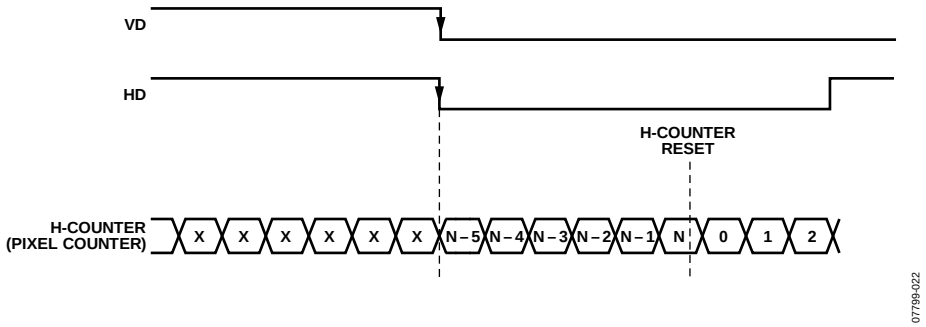


Figure 26. Restriction for H-Counter Reset Position Placement

HORIZONTAL TIMING SEQUENCE EXAMPLE

Figure 27 shows an example of a CCD layout. The horizontal CCD register contains 28 dummy pixels that occur on each line clocked from the CCD. In the vertical direction, there are 10 optical black (OB) lines at the front of the readout and two at the back of the readout. The horizontal direction has four OB pixels in the front and 48 in the back.

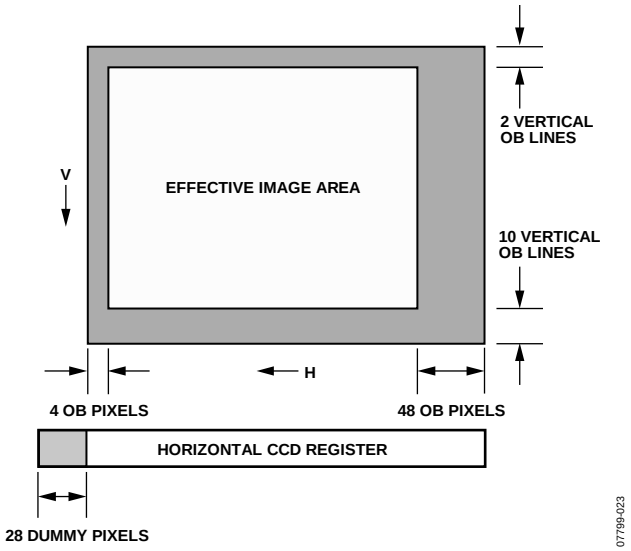


Figure 27. CCD Configuration Example

Figure 28 shows the basic sequence layout to use during the effective pixel readout. The 48 OB pixels at the end of each line are used for the CLPOB signals. PBLK is optional and is often used to blank the digital outputs during the vertical shift time.

Because PBLK is used to isolate the CDS input, do not use the PBLK signal during CLPOB operation. The change in the offset behavior that occurs during PBLK affects the accuracy of the CLPOB circuitry.

More elaborate clamping schemes can be used, such as adding a separate sequence to clamp in all shielded OB lines. This requires configuring a separate shielded region for clocking out the OB lines.

The PBLKMASK registers are also useful for disabling the PBLK on a few lines without affecting the setup of the PBLK toggle positions. It is important to use CLPOB only during valid OB pixels. During other portions on the frame timing, such as vertical blanking or sensor gate (SG) line timing, the CCD does not output valid OB pixels. Any CLPOB pulses that occur during this time cause errors in the clamping operation and therefore cause changes in the black level of the image.

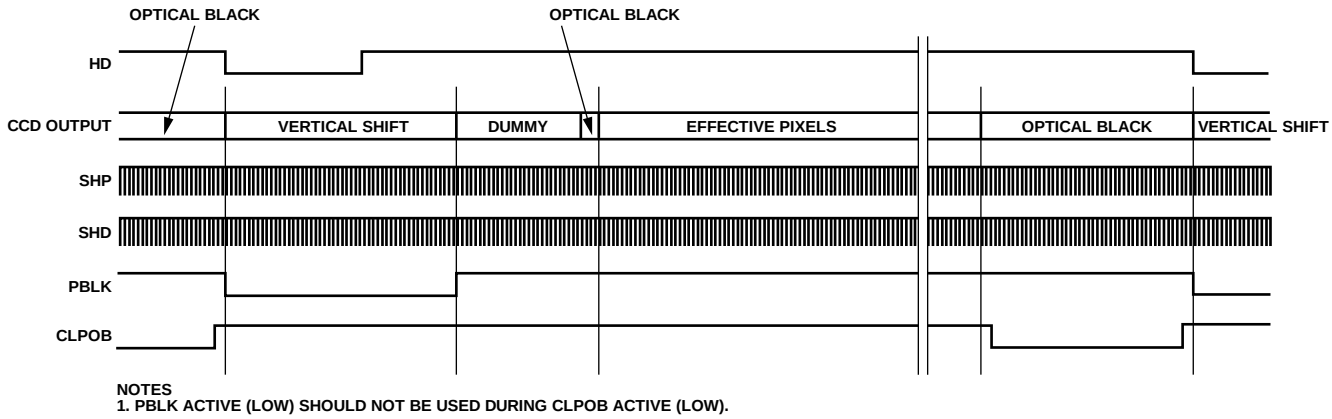


Figure 28. Horizontal Sequence Example

ANALOG FRONT-END DESCRIPTION/OPERATION

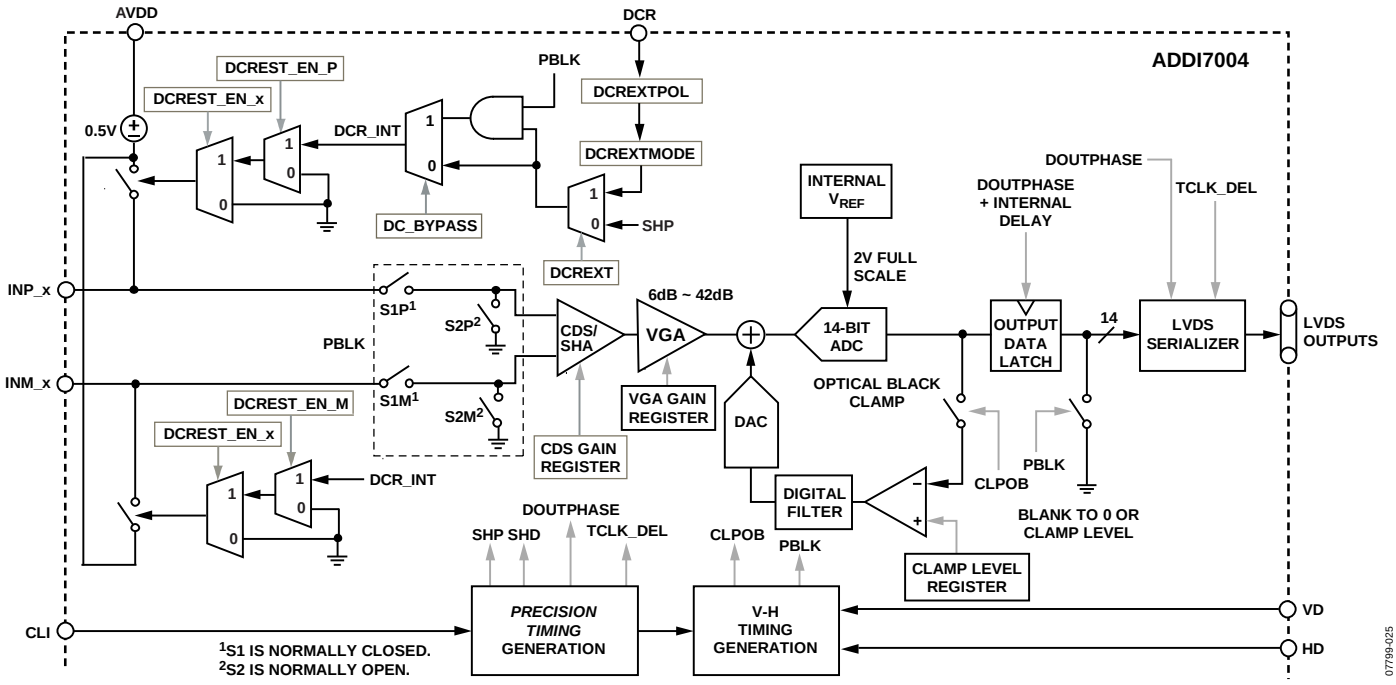


Figure 29. Analog Front-End Functional Block Diagram (One Channel Shown)

CORRELATED DOUBLE SAMPLER (CDS)

DC Restore

To reduce the large dc offset of the CCD output signal, a dc-restore circuit is used with an external 0.1 µF series coupling capacitor. This restores the dc level of the CCD signal to approximately 1.3 V (AVDD − 0.5 V) to be compatible with the 1.8 V core supply voltage of the ADDI7004. The dc-restore switch is active during the SHP sample pulse time.

The dc-restore circuit can be disabled when the optional PBLK signal is used to isolate large-signal swings from the CCD input. Bit 5 of Address 0x41 (hidden) controls whether the dc restore is active during the PBLK interval.

CDS Gain

By using AFE Address 0x07, the CDS gain is variable in four steps: −3 dB, 0 dB (default), +3 dB, and +6 dB. Improved noise performance results from using the +3 dB and +6 dB settings, but the input range is reduced (see Table 3).

Input Configurations

The CDS circuit samples each CCD pixel twice to extract the video information and to reject low frequency noise (see Figure 30). There are three possible configurations for the CDS.

- CDS mode
- SHA mode

The SAMP_MODE register (Address 0x06) selects which configuration is used. The differential inputs provide additional flexibility, as illustrated in the following sections.

Inverting CDS Mode

For this configuration, the signal from the CCD is applied to the positive input of the CDS system (INP_x) with the minus side (INM_x) grounded (see Figure 31). The SAMP_MODE register setting for this configuration is 0x00. Traditional CCD applications use this configuration with the reset level established below the AVDD supply level, at approximately 1.3 V, by the ADDI7004 dc-restore circuit. The maximum saturation level is 1.0 V below the reset level, as shown in Figure 32 and Table 12. A maximum saturation voltage of 1.4 V is also possible when using the minimum CDS gain setting.

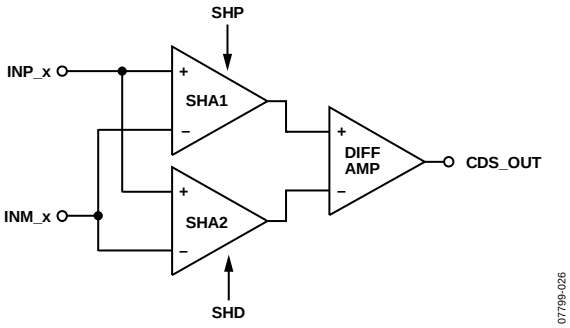


Figure 30. CDS Block Diagram (Conceptual)

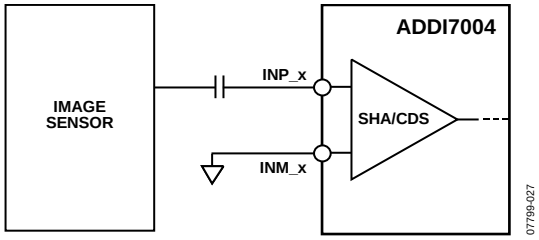


Figure 31. Single-Input CDS Configuration

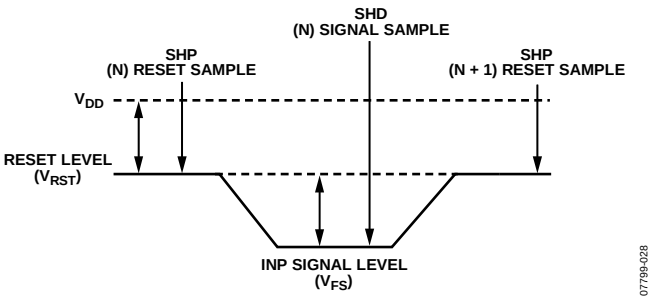


Figure 32. Traditional Inverting CDS Signal

Table 12. Inverting Voltage Levels

Level	Symbol	Min (mV)	Typ (mV)	Max (mV)
Saturation	V_{FS}		1000	1400
Reset	V_{RST}		1300	

Noninverting CDS Mode

A noninverting configuration is also available, with the reset (or black) level signal established at or above ground potential. In this configuration, the positive-going signal is applied to INM_x instead of INP_x. Generally, the dc-restore circuit is disabled in this mode because INP_x and INM_x are within the input limits of the ADDI7004. Saturation (or white) level is approximately 1 V above the reset level. Samples are taken at each signal level (see Figure 33, Figure 34, and Table 13).

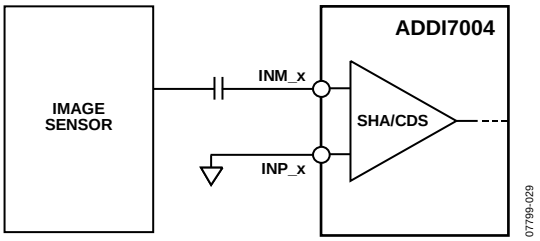


Figure 33. Single-Input CDS Configuration with Inputs Reversed

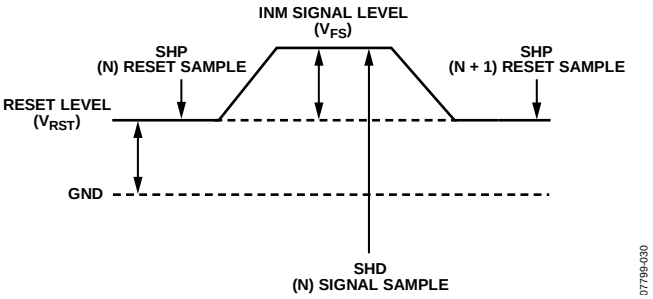


Figure 34. Noninverting CDS Signal

Table 13. Noninverting Voltage Levels

Level	Symbol	Min (mV)	Typ (mV)	Max (mV)
Saturation	V_{FS}		1000	1400
Reset	V_{RST}	0	250	500

Differential CDS Mode Input Configuration

This configuration uses a differential input signal, as shown in Figure 35 and Figure 36. In Figure 36, the dc restore circuit is enabled on both INP_x and INM_x, and dc-blocking capacitors are used on both inputs.

In this configuration, the CCD signal is applied differentially to the INP_x and INM_x inputs. Sampling occurs on both signals simultaneously at the two different sampling locations, SHP and SHD (see Figure 37). Note that the differential voltage sampled at the SHP sampling location ($V_{DIFF}[P]$) must be equal to or greater than the differential voltage sampled at the SHD sampling location ($V_{DIFF}[D]$), just as with the single-ended CDS Mode configurations. Table 14 summarizes the acceptable voltage levels for this mode.

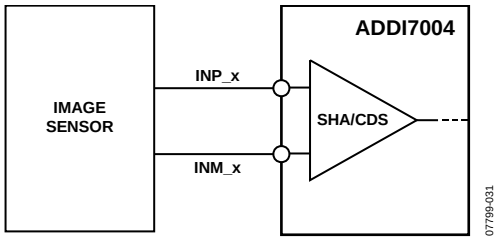


Figure 35. Differential Input Configuration (DC-Coupled)

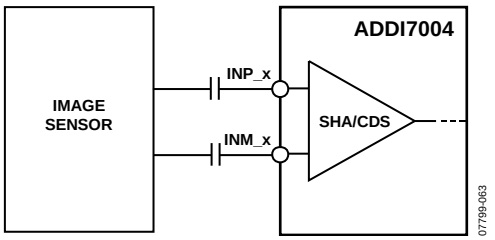


Figure 36. Differential Input Configuration (AC-Coupled)

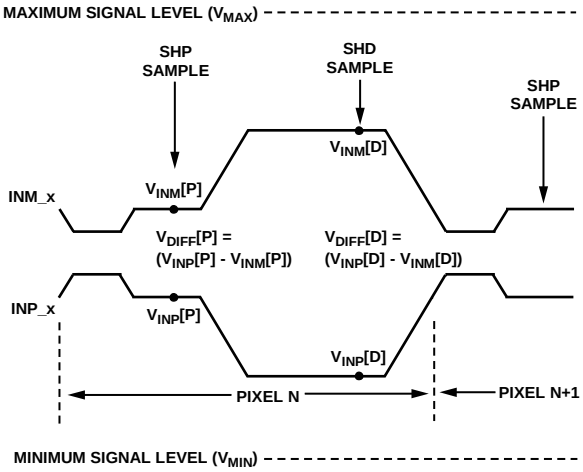


Figure 37. CDS Mode Differential Input Signal

Table 14. Differential CDS Mode Voltage Levels

Level	Symbol	Min (mV)	Typ(mV)	Max (mV)
Saturation Signal, $V_{DIFF}[P] - V_{DIFF}[D]$	V_{FS}	0	1000	1400
Maximum Voltage at INP_x or INM_x Pins	V_{MAX}	N/A	N/A	INVDD
Minimum Voltage at INP_x or INP_x Pins	V_{MIN}	0	N/A	N/A

SHA Mode Differential Input Configuration

This configuration uses a differential input sample-and-hold amplifier (SHA). In this configuration, a signal is applied to the INP_x input while an inverse signal is applied to the INM_x input. Sampling occurs simultaneously on both signals at the location specified by SHPLOC. This creates the differential output for amplification and the ADC (see Figure 38 and Table 15).

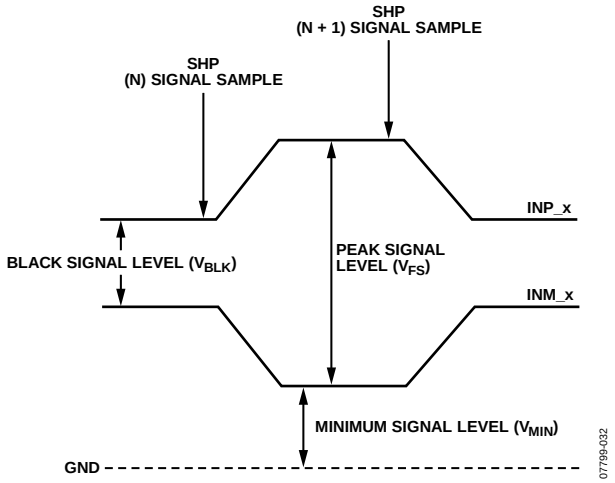


Figure 38. Differential Input Signal

Table 15. Differential Voltage Levels

Level	Symbol	Min (mV)	Typ (mV)	Max (mV)
Black Signal	V_{BLK}		0	
Saturation Signal	V_{FS}		1000	1400
Minimum Signal	V_{MIN}	0		

DC-Coupled, Single-Ended Input Configuration

The SHA mode can also be used in a single-ended fashion with the signal from the image sensor applied to the CDS/SHA using a single input, INP_x. This configuration is similar to the differential configuration except that, in this case, the INM_x line is held at a constant dc voltage. This establishes a reference level that matches the image sensor reference voltage (see Figure 39).

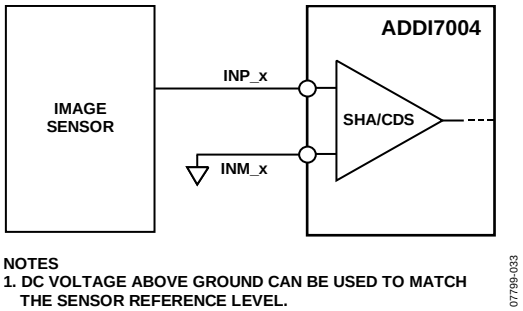


Figure 39. Single-Ended Input Configuration (DC-Coupled)

In Figure 40 and Table 16, the INM_x signal is a constant dc voltage set at a level above the ground potential. The sensor signal is applied to the other input, and samples are taken at the signal minimum and signal maximum. The resulting differential signal is the difference between the signal and the reference voltage.

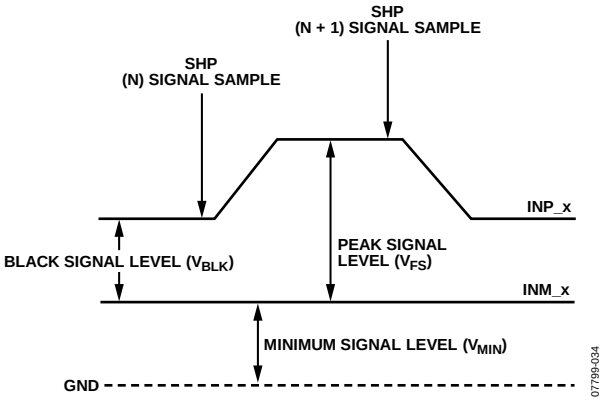


Figure 40. Single-Ended Input Signal (DC-Coupled)

Table 16. Single-Ended Input Voltages

Level	Symbol	Min (mV)	Typ (mV)	Max (mV)
Black Signal	V_{BLK}		0	
Saturation Signal	V_{FS}		1000	1400
Minimum Signal	V_{MIN}	0		

CDS Timing Control

The timing shown in Figure 20 illustrates how the two internally generated SHA clocks, SHP and SHD, are used to sample the voltage of the imager signal. The placement of the SHP and SHD sampling edges is determined by the setting of the SHPLOC register (Address 0x91, Bits[13:8]) and the SHDLOC register (Address 0x91, Bits[5:0]). Placement of these clock signals is critical for achieving the best performance from the CCD.

Note that, when SHA mode is selected, only the SHPLOC setting is used to sample the input signal. However, the SHDLOC signal should still be programmed to an edge setting of SHPLOC + 32.

VARIABLE GAIN AMPLIFIER

The VGA stage provides a gain range of approximately 6 dB to 42 dB, programmable with a 10-bit resolution through the serial digital interface. A gain of 6 dB is needed to match a 1 V input signal with the ADC full-scale range of 2 V. When compared with 1 V full-scale systems, the equivalent gain range is 0 dB to 36 dB.

The VGA gain curve follows a linear-in-dB characteristic. The exact VGA gain is calculated for any gain register value by

$$Gain\ (\text{dB}) = (0.0359 \times Code) + 5.76\ \text{dB}$$

where *Code* is the range of 0 to 1023.

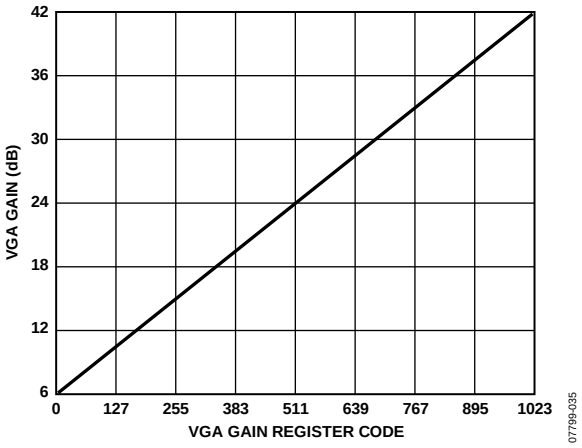


Figure 41. VGA Gain Curve

ADC ARCHITECTURE

The ADDI7004 uses a high performance ADC architecture optimized for high speed and low power. Differential non-linearity (DNL) performance is typically better than 0.5 LSB. The ADC uses a 2 V input range.

OPTICAL BLACK CLAMP

The optical black clamp loop removes residual offsets in the signal chain and tracks low frequency variations in the CCD black level. During the optical black (shielded) pixel interval on each line, the ADC output is compared with a fixed black level reference, selected by the user in the CLAMPLEVEL_x register (Address 0x10 through Address 0x13). The value can be programmed between 0 LSB and 1023 LSB in 1023 steps. The resulting error signal is filtered to reduce noise, and the correction value is applied to the ADC input through a DAC.

Normally, the optical black clamp loop is turned on once per horizontal line, but this loop can be updated more slowly to suit a particular application. If external digital clamping is used during postprocessing, the ADDI7004 optical black clamping can be disabled by using the CLAMPENABLE register (Address 0x02, Bit 0). When the loop is disabled, the CLAMPLEVEL_x register can still be used to provide fixed offset adjustment.

Note that, if the CLPOB loop is disabled, higher VGA gain settings reduce the dynamic range because the uncorrected offset in the signal path is gained up.

Align the CLPOB pulse with the optical black pixels of the CCD. It is recommended that the CLPOB pulse duration be at least 20 pixels wide. Shorter pulse widths can be used, but the ability of the loop to track low frequency variations in the black level is reduced.

DIGITAL DATA OUTPUTS

The ADDI7004 ADC digital output data is latched based on the SHDLOC register value as shown in Figure 20. The pipeline delay through the ADDI7004 is shown in Figure 21. After the CCD input is sampled by SHD, there is a 23-cycle delay until the data is available.

For maximum system flexibility, the ADDI7004 uses the DOUTPHASEx register (Address 0x9A) to select the location for the start of each new pixel data value. Any edge location from 0 to 63 can be programmed. This register determines the start location of the data output and TCLK rising edge with respect to CLI.

LVDS SERIAL DATA INTERFACE

As digital imaging products such as digital still cameras, camcorders, and scanners have become more prevalent in the market, designers of these systems have driven the demand for both higher speed and higher resolution analog front ends (AFEs) in the ongoing pursuit of better image quality.

The AFE (which includes the ADC) needs to be able to drive receiving logic and the accompanying PCB trace capacitance. The combination of the increase in data lines and higher speed signals presents the system designer with issues in EMI emissions, larger board area (due to the increase in data lines), higher power, and more current transients. This last issue can create kickback noise, a phenomenon in which transients created by driving the load are coupled back to the ADC analog front end, manifesting in the image as noise or distortion. All of these issues present a challenge to users attempting to develop a high performance imaging application.

A configurable low voltage differential signaling (LVDS) serial data interface offers another approach to providing high speed data outputs while minimizing performance limitations in AFE applications. LVDS is a differential signaling scheme that uses a low voltage swing.

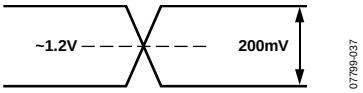


Figure 42. LVDS Output Levels

The LVDS offers the following advantages over the conventional parallel interface:

- Reduced kickback noise. LVDS outputs are current output stages that require a 100 Ω terminating resistor at the receiver (see Figure 43). This differs from CMOS outputs, which generally do not require termination

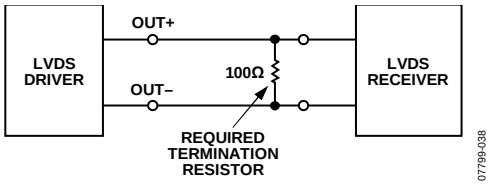


Figure 43. LVDS Requires Far-End Termination

  To avoid current spikes on the supply that can couple into the sensitive analog front end (resulting in kickback noise), the current output results in a fixed dc load current on the output supplies.

- Fewer data lines. With a serial data output, the number of data lines is reduced significantly. This is important in applications that require multiple channels, such as higher speed imaging applications needing a small form factor. LVDS serial data outputs dramatically reduce kickback noise due to the limited number of data output switching compared with a 14- or 16-bit parallel output bus switching simultaneously.
- Reduced EMI emissions. Because two balanced signals of the same magnitude transmit through the line in opposite directions, the electromagnetic field from each signal is radiated in the opposite direction, effectively canceling each other's EMI emissions. This reduces shielding, which lowers overall system cost. It also reduces RF interference, which is critical in wireless enabled systems.

In addition to the inherent benefits of LVDS, a configurable transmitter enables the AFE to support a wide variety of LSI receivers, allowing the system designer to implement a receiver that optimizes system performance. The configurable LVDS transmitter enables the user to adjust the following parameters:

- Number of output ports to accommodate higher speed outputs. This allows the designer to use the same device to upgrade the system for higher speed applications.
- Configurable current values to adjust for varying capacitive loads.
- Generation of test pattern for simpler verification of functionality.
- Phase delay and trigger adjustment for better synchronization.
- Control word configuration to accommodate various system protocols for data synchronization.
- Configurable data formatting with single and double data port options.

LVDS SERIAL DATA LINK OPERATION

The LVDS registers for serial register programming are described in Table 17. The configuration of these registers determines the LVDS configuration and operation mode. The serial data link output consists of three pairs of differential output signals, as shown in Figure 44. The DOUTx outputs are each 8- or 16-bit data outputs that can be configured to operate in different modes by using the TX_CTRL register. The TCLK is the data transmit clock corresponding to valid output data on both rising and falling edges.

Note that, although the DOUTx data outputs can be 16 bits in length for single data port mode, the ADC output data is only 14 bits. The two LSBs of the 16-bit output are always set to 0.

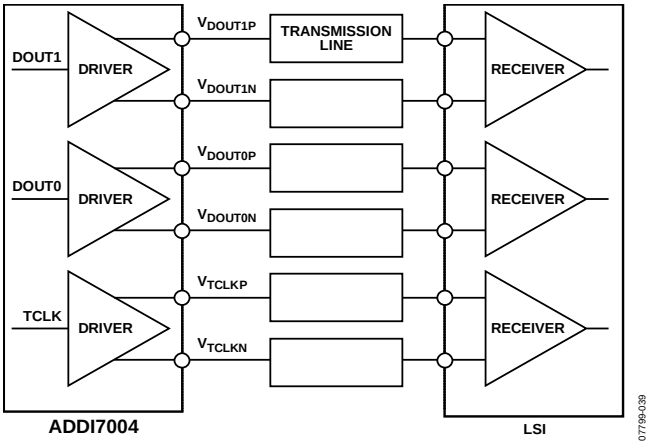


Figure 44. LVDS Serial Data Output

Table 17. LVDS Registers

Register	Length (Bits)	Description	Settings
TCLKx_PDN	1	TCLK output enable	0 = normal operation. 1 = power-down.
DOUTx_PDN	1	DOUTx output enable	0 = normal operation. 1 = power-down.
TX_CTRL	2	Serial data transmit control	0 = single port mode, data output DOUT0/DOUT2/ DOUT4/DOUT6. 1 = double port mode, data LSB output DOUT0/DOUT2/ DOUT4/DOUT6. 2 = single port mode, data output DOUT1/DOUT3/ DOUT5/DOUT7. 3 = double port mode, data LSB output, DOUT1/ DOUT3/DOUT5/DOUT7.
TCLK_DEL	3	TCLK rising edge delay	0 = default with no delay. 1 LSB = 1/16 cycle of internal TCLK when operating in double port mode. 1 LSB = 1/8 cycle of internal TCLK when operating in single port mode.
LSB_ALIGN	1	LVDS LSB align control	0 = MSB first. 1 = LSB first.
CLIP_ZS	1	Data clip operation for ADC zero-scale output data	0 = clip function disabled, ADC zero scale = 0x0000. 1 = clip function enabled, ADC zero scale = 0x0001.
CLIP_FS	1	Data clip operation for ADC full-scale output data	0 = clip function disabled, ADC full scale = 0x3FFF. 1 = clip function enabled, ADC full scale = 0x3FFE.
LVDS_TEST_EN_x	2	LVDS data input test enable	0 = disable LVDS test pattern for Channel x. 1 = enable LVDS test pattern for Channel x.
TCLK_PATTERN	16	Pattern of the TCLK signal when TCLK pattern mode is enabled	TCLK_PATTERN[15:0] used in single port mode. TCLK_PATTERN[15:8] used in double port mode.
TCLK_MODE	1	TCLK pattern mode enable	0 = disable TCLK pattern mode. 1 = enable TCLK pattern mode.

CONFIGURABLE DATA FORMATTING

The serial data outputs can be configured to operate in single data port mode or double data port mode to support different LSI receiver capabilities. In both single and double data port modes, double data rate is used with respect to TCLK rising and falling timing.

Note that, although the DOUTx data outputs can be 16 bits in length for single data port mode, the ADC output data is only 14 bits. The two LSBs of the 16-bit output are always set to 0.

Single Data Port Mode

Single data port operation outputs the entire 16-bit word on only one data port. The DOUT0 or DOUT1 data port is selected to output the data by using the TX_CTRL register.

During single data port operation, the TCLK runs at the maximum allowable data rate of 288 MHz, resulting in the TCLK frequency being eight times the CLI input pixel clock (see Figure 47). This implies that a maximum CLI clock frequency of 36 MHz can be supported while operating in this mode.

288 MHz/8 = 36 MHz

Double Data Port Mode

Double data port operation uses both DOUT0 and DOUT1 to output the 16-bit word at double the single port data rate. Apply the upper and lower bytes to either port using the TX_CTRL register. During double port operation, the TCLK runs at only four times the CLI input pixel clock, as shown in Figure 48. Because the maximum allowable data rate is 288 MHz, the double port operation allows for faster AFE operation of up to 72 MHz (288 MHz/4).

PROGRAMMABLE DATA DELAY

The ADDI7004 also provides programmable delay for the serial data outputs, allowing fine adjustment with the LVDS receiver. Two levels of programmability are provided, one at the pixel clock rate (DOUTPHASE) and one at the serial data clock rate (TCLK).

TCLK Delay Adjustment

Additional features provide the ability to delay the TCLK phase relative to the starting location of each data bit by using the TCLK_DEL register (Address 0xA2, Bits[4:2]). This feature optimally positions the rising edge of TCLK at the center of the data bit at the receiver input, as shown in Figure 51. The TCLK adjustment range differs between the single data port mode and the double data port mode as illustrated in Figure 45 and Figure 46, respectively. Figure 45 shows that there are four adjustment range positions for the single port mode, and Figure 46 shows that there are eight adjustment range positions during operation in the double port mode.

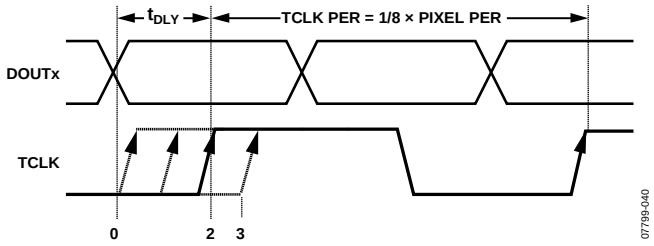


Figure 45. TCLK Delay for Single Data Port Mode

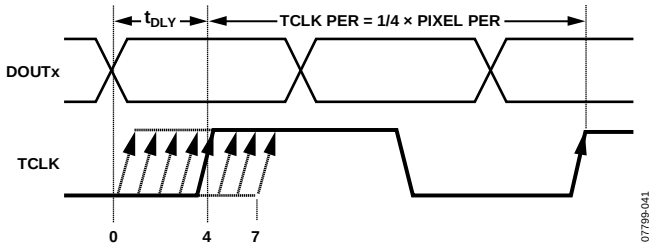


Figure 46. TCLK Delay for Double Data Port Mode

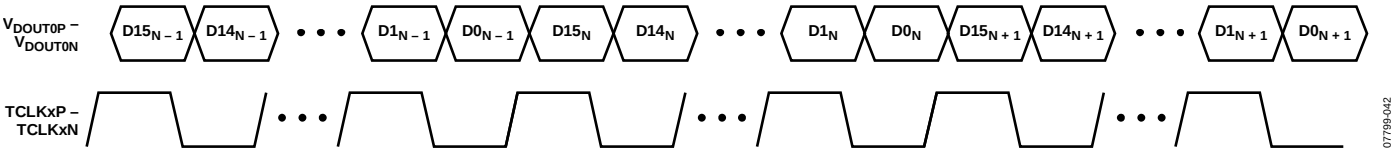


Figure 47. Data and Clock Format for Single Data Port Operation (Using DOUT0, MSB First)

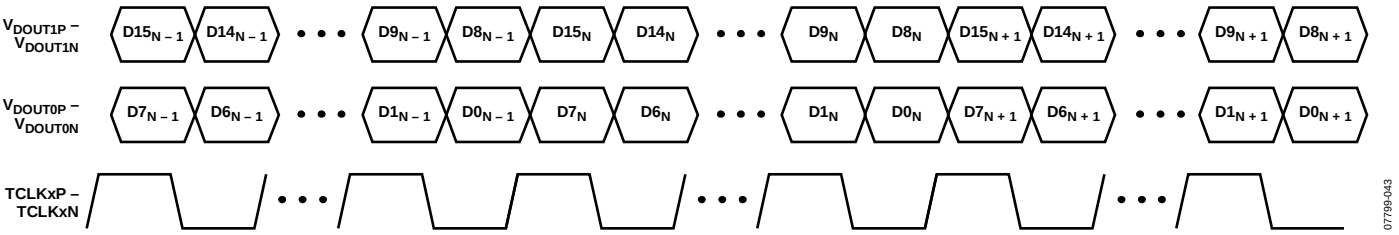


Figure 48. Data and Clock Format for Double Data Port Operation (Using Upper Byte on DOUT1, MSB First)

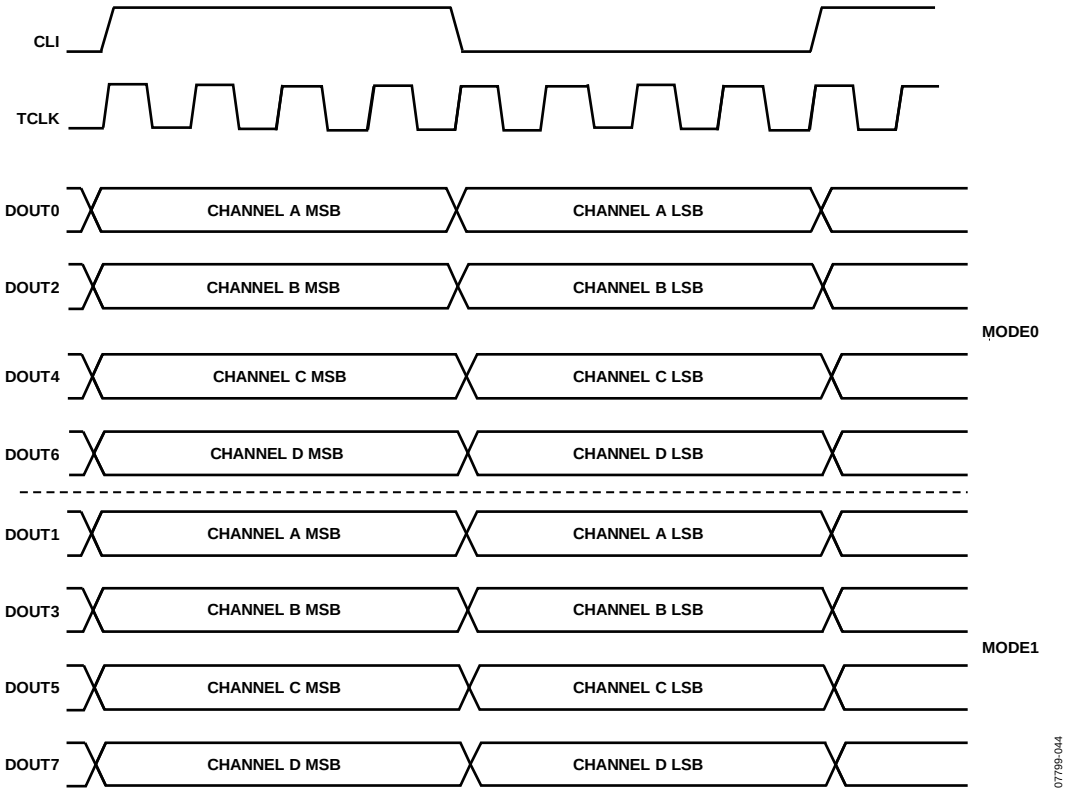


Figure 49. LVDS Data Format Settings, Single Port Mode

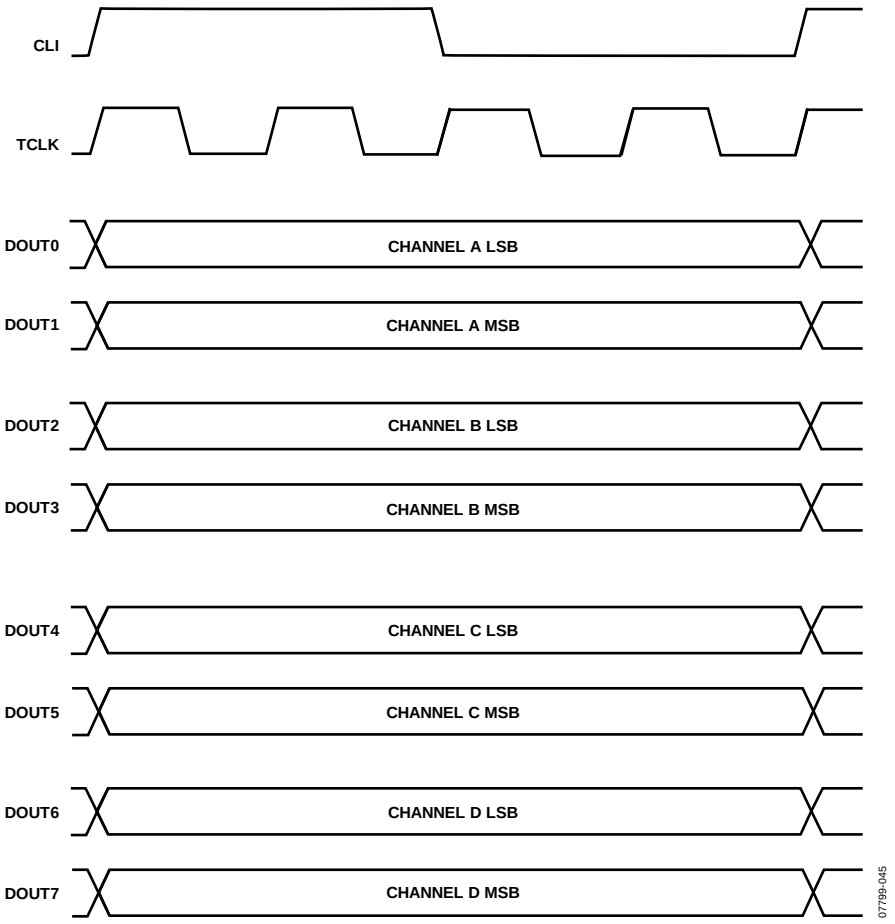


Figure 50. LVDS Data Format, Double Port Mode

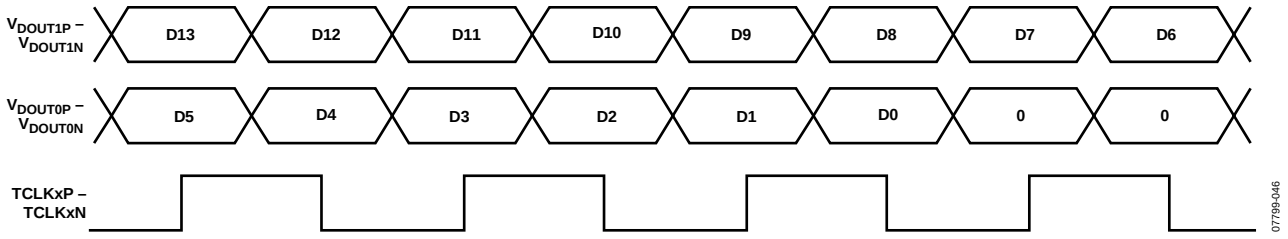


Figure 51. Ideal TCLK Phase Location Centered

DOUTPHASE Control

Use the DOUTPHASEP register to skew the TCLK and DOUT phases with respect to the rising edge of the CLI master clock. The value of the DOUTPHASEN register is dependent on the DOUTPHASEP value. DOUTPHASEN must always be set as follows: DOUTPHASEN = DOUTPHASEP + 0x20. This maintains a 50% internal DOUTPHASE clock. Figure 52 shows the internal DOUTPHASE clock with respect to CLI and the DOUTPHASEP register setting.

TCLK Pattern

By enabling the TCLK_MODE register, it is possible to generate a unique TCLK pattern. When the TCLK_MODE register is enabled, TCLK_PATTERN Bits[15:0] determine the polarity of 1/16 of one CLI period, respectively, with MSB first.

For example, to generate a TCLK pattern with the same period as the CLI, TCLK_PATTERN Bits[15:8] are set to 0xFF00, as shown in Figure 54. In the double data port mode, only the TCLK_PATTERN[15:8] register is used to output a desired TCLK pattern, as shown in Figure 53. The eight LSBs from TCLK_PATTERN are ignored.

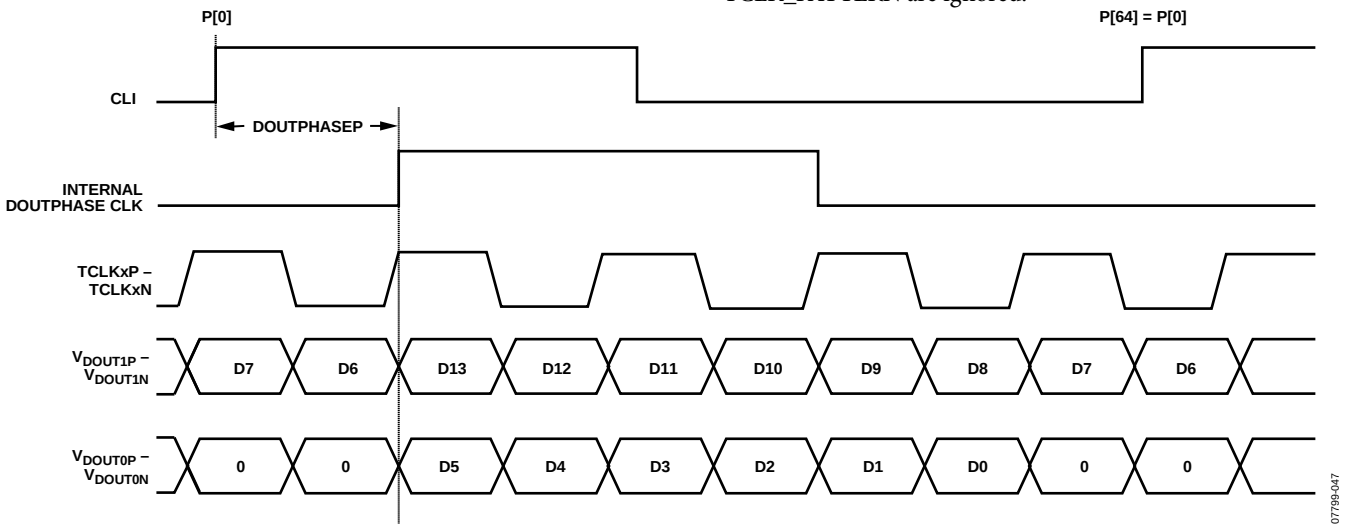


Figure 52. DOUTPHASEP Operation

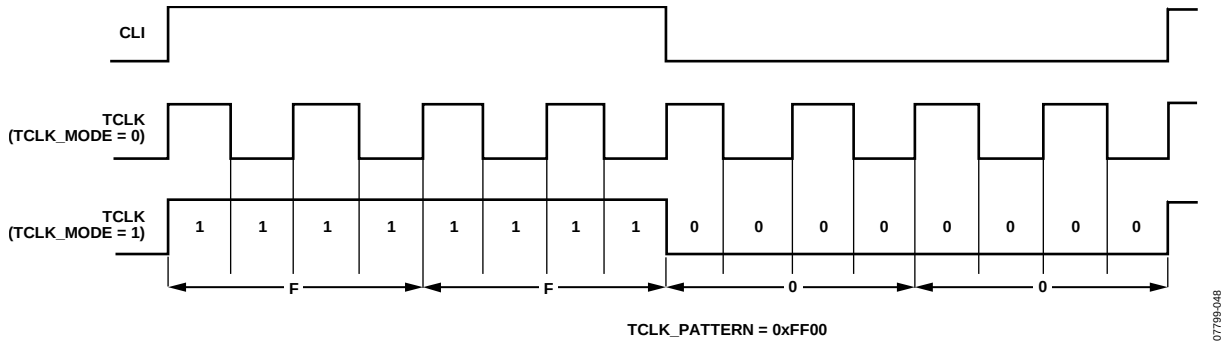
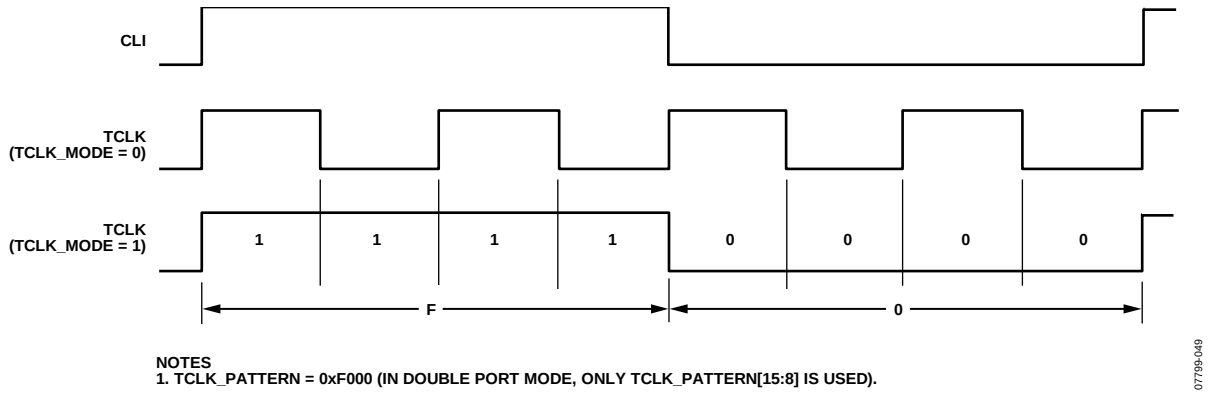


Figure 53. Using the TCLK Pattern Function to Create a Frame Clock Signal in Single Data Port Mode



NOTES
1. TCLK_PATTERN = 0xF000 (IN DOUBLE PORT MODE, ONLY TCLK_PATTERN[15:8] IS USED).

Figure 54. Using the TCLK Pattern Function to Create a Frame Clock Signal in Double Data Port Mode

LVDS Test Pattern Insertion

A special test pattern insertion feature can be enabled to output a 16-bit data-word programmed in the TEST_PATTERN_x registers for the A, B, C, and D channels. The 16-bit pattern programmed in these registers is output by setting the LVDS_TEST_EN_x registers to 1. Use this feature to assist with the initial LVDS serial interface system development. Figure 55 shows the mux operation that enables the test pattern mode.

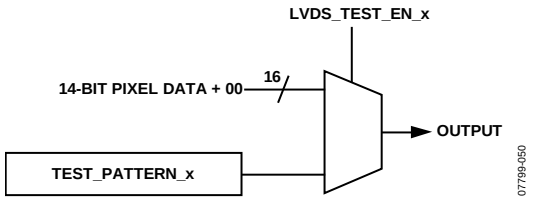


Figure 55. LVDS Test Pattern Mux Control

CONFIGURABLE SERIAL DATA SYNCHRONIZATION PROTOCOLS

Configurable synchronization programmability is provided while operating in single data port and double data port modes. The host processor uses these synchronization features to automatically track pixel data with respect to the start of each field and line position. Table 18 describes the synchronization registers.

Up to seven configurable synchronization words followed by one configurable control word are supported, as shown in Figure 56. The multiple preprogrammed synchronization words are available to eliminate the risk of synchronization errors between the LVDS serializer and the receiver. The synchronization and control words always replace the preceding pixel data.

Table 18. Synchronization Registers

Register	Length	Range	Description
NUM_SYNC_WORD	3 bits	0 to 7 sync words	Total number of synchronization words.
CTRL_WORD_EN	1 bit	1/0	Control word enable.
SYNC_WORD0	16 bits	0 to 15 sync word bits	Synchronization Word 0 data bits.
SYNC_WORD1	16 bits	0 to 15 sync word bits	Synchronization Word 1 data bits.
SYNC_WORD2	16 bits	0 to 15 sync word bits	Synchronization Word 2 data bits.
SYNC_WORD3	16 bits	0 to 15 sync word bits	Synchronization Word 3 data bits.
SYNC_WORD4	16 bits	0 to 15 sync word bits	Synchronization Word 4 data bits.
SYNC_WORD5	16 bits	0 to 15 sync word bits	Synchronization Word 5 data bits.
SYNC_WORD6	16 bits	0 to 15 sync word bits	Synchronization Word 6 data bits.
SYNC_RISING_EN	8 bits	0 to 7 control word bits	Rising edge synchronization enable (triggered operation).
SYNC_FALLING_EN	8 bits	0 to 7 control word bits	Falling edge synchronization enable (triggered operation).
SYNC_START_LOC	16 bits	0 to 8192 count	Synchronization sequence starting pixel count location (automatic).
SYNC_ALIGN	1 bit	1/0	Synchronization word location (automatic).
SYNC_CW_EN	1 bit	1/0	Automatic synchronization and control word enable (automatic).

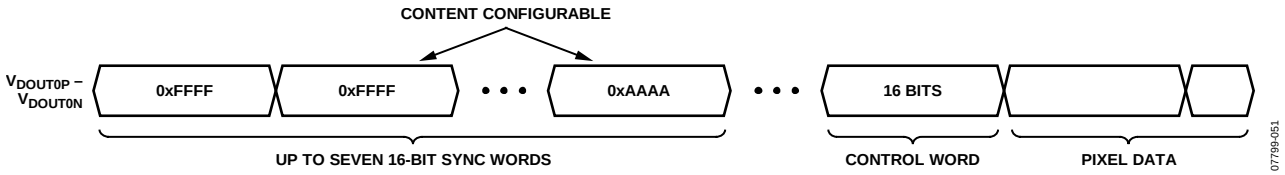


Figure 56. Synchronization and Control Word Output Format

Control Word

One control word is supported to provide VD/HD, CLPOB, and PBLK status information. Figure 58 and Figure 57 show the control word configuration for single and double data port operation, respectively. As shown, the upper byte of the control word is always the inverse of the lower byte.

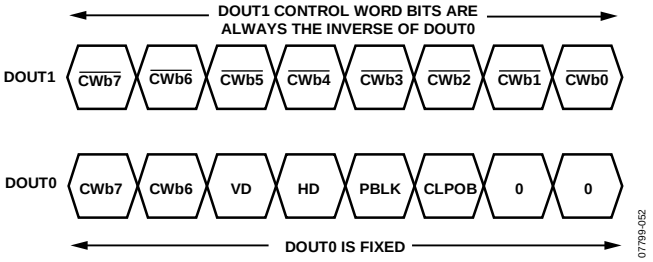


Figure 57. Control Word Configuration for Double Data Port Mode

Triggered Synchronization

A synchronization sequence can be initiated in two ways. A triggered synchronization event is initiated by an internal signal transition. The setting programmed for the control word determines the internal signals that trigger a sync sequence.

The synchronization is triggered on either the rising or falling edge of the control word setting by using the SYNC_RISING_EN or SYNC_FALLING_EN register. Figure 59 shows an example of triggering the synchronization sequence on two occasions. In this example, the sync sequence is triggered at the falling edge of VD and the rising edge of PBLK.

Automatic Synchronization

An automatic synchronization event is initiated at the start of each line. The synchronization sequence can be delayed by a certain number of pixels by using the SYNC_START_LOC register. Additionally, the SYNC_ALIGN register either starts or ends the synchronization sequence determined by the SYNC_START_LOC setting. Figure 60 show two examples of using these registers to delay the synchronization sequences after being enabled by the start of the line.

LVDS Synchronization

Figure 60 shows the complete pipeline delay of the H-counter reset plus the LVDS serializer delay, along with the AFE pipeline delay. The sync and control words are placed relative to the delayed position of Pixel 0, based on the register setting of SYNC_START_LOC and SYNC_ALIGN. The pipeline delay from the external HD falling edge to the LVDS output of Pixel 0 is 14 cycles, and the total AFE pipeline delay from the analog input to the LVDS output is 23 cycles.

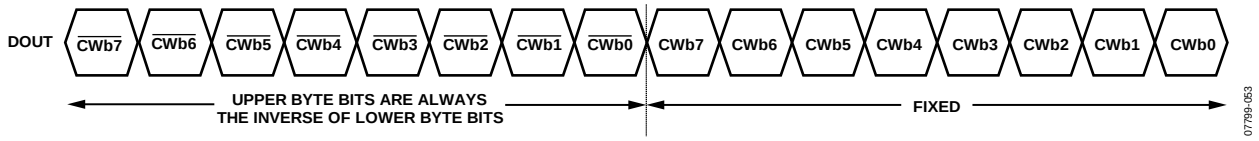


Figure 58. Control Word Configuration for Single Data Port Mode

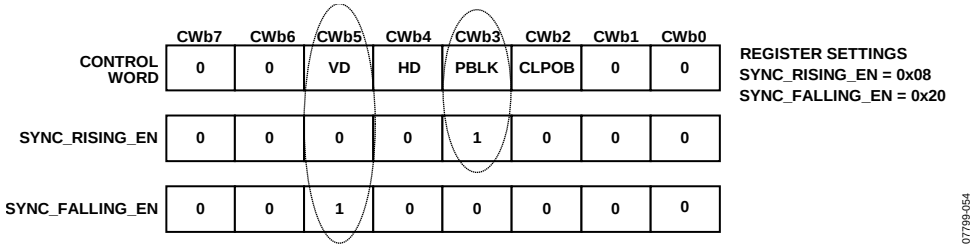


Figure 59. Example of Configuring the Synchronization Register

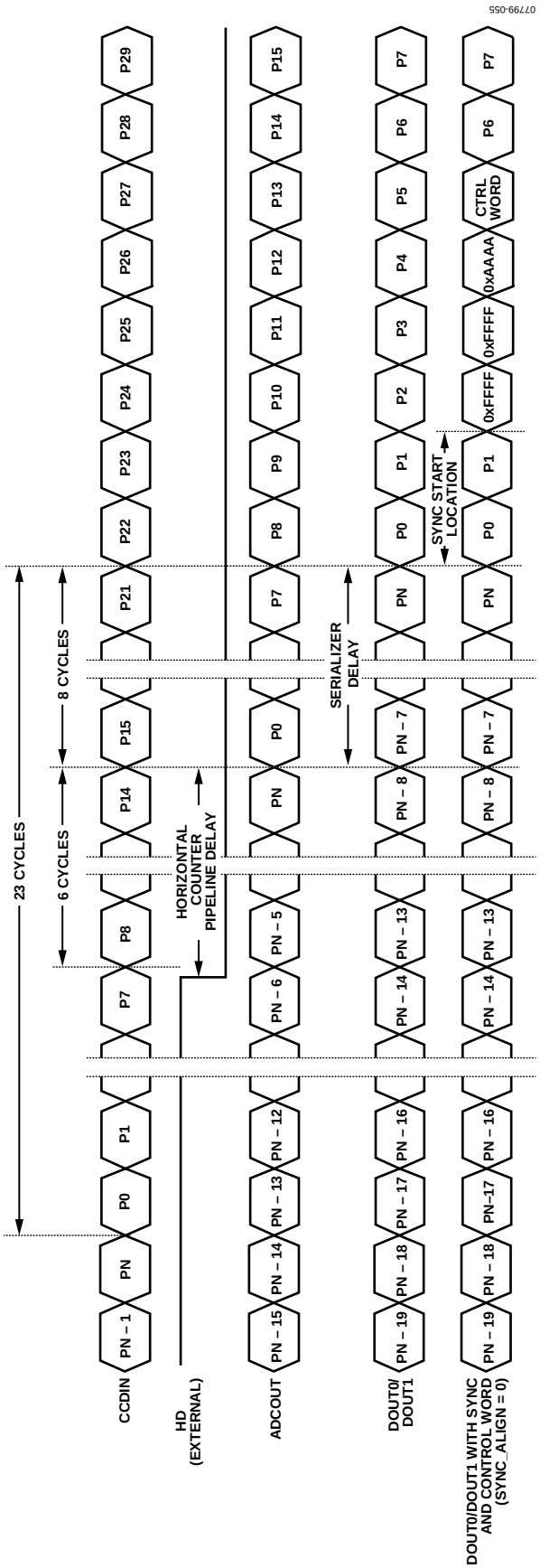


Figure 60. Pipeline Delays: Example of Automatic Synchronization with SYNC_START_LOC = 2 and SYNC_ALIGN = 0

APPLICATIONS INFORMATION

RECOMMENDED POWER-UP SEQUENCE

To power up the ADDI7004, use the following sequence (refer to Figure 61 for each step):

1. Turn on the power supplies for the ADDI7004 and apply the CLI clock. Note that the same 1.8 V supply must be used for all of the 1.8 V supply pins.
2. Write a 1 to the SW_RESET register (Address 0x30) to reset all the internal registers to their default values. This bit is self-clearing and automatically resets to 0.
3. Load register settings. If operating at greater than 65 MHz, the STARTUP1 and STARTUP2 registers must be programmed to the following values:
   Register 0xF3 = 0x000F
   Register 0xF9 = 0xC037
4. Place the part into normal power operation by writing a 0 to the STANDBY_x register (Address 0x00) and REFBUF_PDN_x register (Address 0x01). Wait at least 500 µs before completing Step 6.
5. Reset the *Precision Timing* core by writing a 1 to the TGCORE_RSTB register (Address 0x33). This starts the internal timing core operation. Wait at least 100 µs before completing Step 7.
6. Enable the LVDS output by writing a 0 to the TCLKx_PDN and DOUTx_PDN registers (Address 0xA0). The LVDS output becomes active.
7. Configure the ADDI7004 for double data port mode by writing 0x1 to the TX_CTRL register (Address 0xA2, Bits[1:0]), and set the desired TCLK delay setting to Address 0xA2, Bits[5:2].
8. Write a 0 to the PREVENTUPDATE register (Address 0x38).
9. Write a 1 to the OUT_CONTROL register (Address 0x31).

The next VD/HD falling edge allows register updates to occur, including OUT_CONTROL, which enables all clock outputs.

Additional Precautions

During operation, note the following precautions:

- Locate the HD falling edge in the same CLI clock cycle as the VD falling edge or later than the VD falling edge. The HD falling edge should not be located between one cycle and five cycles prior to the VD falling edge.
- Perform all start-up serial writes with VD and HD disabled, if possible. This prevents unknown behavior caused by partial updating of registers before all information is loaded.
- The following registers should not be written to except during power-up or reset: 0x1B, 0x30, 0x33, 0x34, 0xA1, 0xA2, and 0x9A.

The internal horizontal counter is reset six CLI cycles after the falling edge of HD. See Figure 62 for details on how the internal counter is reset.

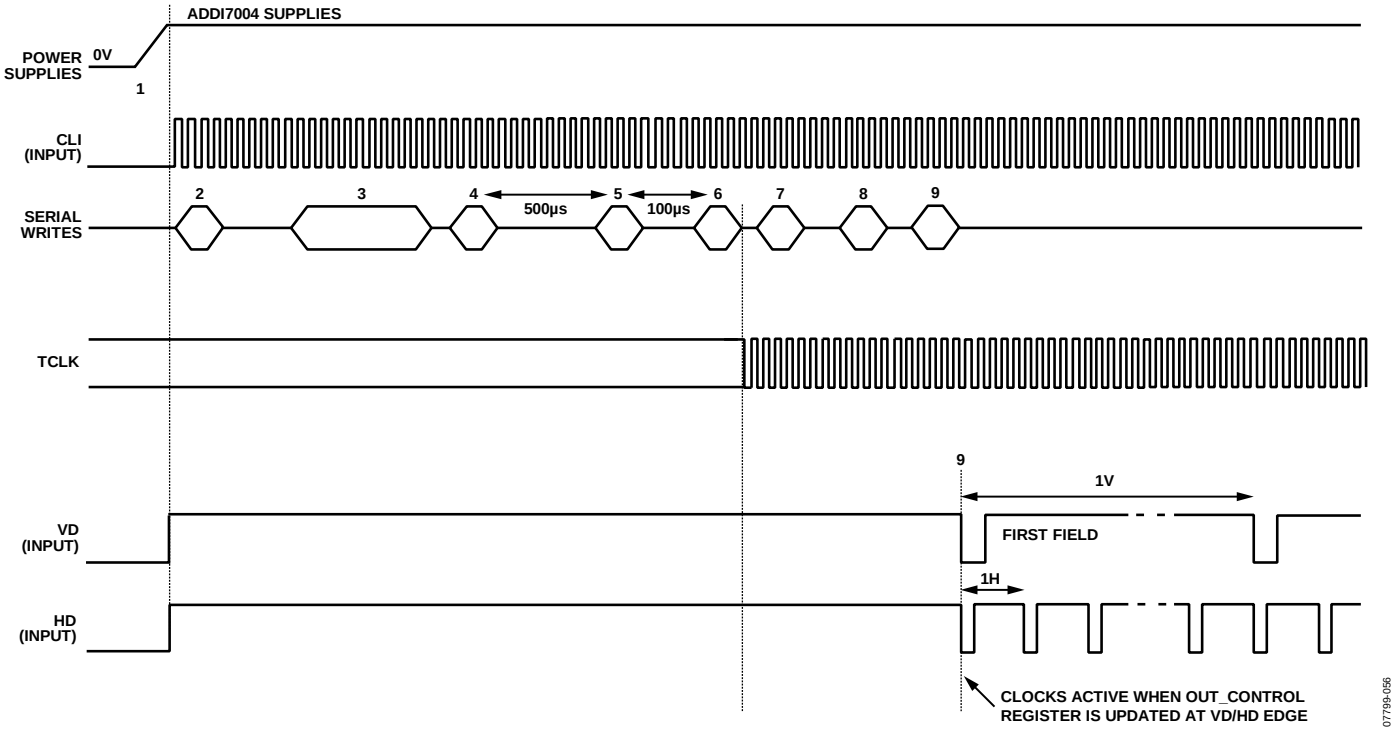
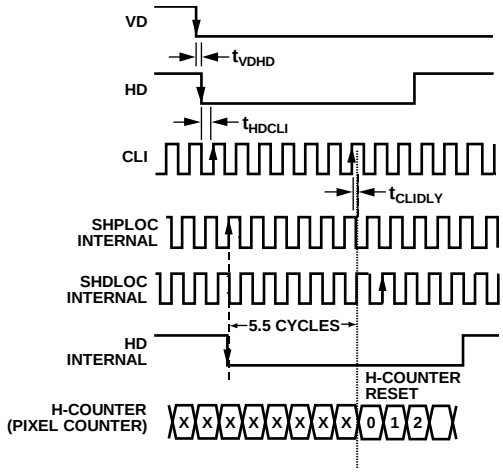


Figure 61. Recommended Power-Up Sequence



NOTES
1. THE EXTERNAL HD FALLING EDGE IS LATCHED BY THE CLI RISING EDGE, AND THEN LATCHED BY SHPLOC (INTERNAL SAMPLING EDGE).
2. THE INTERNAL H-COUNTER IS ALWAYS RESET 5½ CLOCK CYCLES AFTER THE INTERNAL HD FALLING EDGE AT SHDLOC (INTERNAL SAMPLING EDGE).
3. DEPENDING ON THE VALUE OF SHDLOC, H-COUNTER RESET CAN OCCUR SEVEN OR EIGHT CLI CLOCK EDGES AFTER THE EXTERNAL HD FALLING EDGE.
4. SHPLOC = 32, SHDLOC = 0. IN THIS CASE, THE H-COUNTER RESET OCCURS SEVEN CLI RISING EDGES AFTER HD FALLING EDGE.
5. THE HD FALLING EDGE SHOULD OCCUR SIMULTANEOUSLY WITH THE VD FALLING EDGE (WITHIN THE SAME CLI CYCLE) OR AFTER THE VD FALLING EDGE. THE HD FALLING EDGE SHOULD NOT OCCUR WITHIN ONE CLI CYCLE IMMEDIATELY BEFORE THE VD FALLING EDGE.

07799-057

Figure 62. Horizontal Counter Pipeline Delay

Table 19. Power-Down Mode Operation

I/O Block	Total Shutdown (Default)[1, 2]	OUT_CONTROL = Low	Reference Standby
AFE	Off	No change	Only internal VREF on
Timing Core	Off	No change	On
TCLK	Low	Running	Running
DOUT0, DOUT1	Low	Low	Low

[1] To exit total shutdown for Channel A, write 00 to the STANDBY_A register (Address 0x00, Bits[1:0]) and then reset the timing core after 500 µs to guarantee proper settling.
[2] Total shutdown mode takes priority over the OUT_CONTROL register (Address 0x31) for determining the output polarities.

STANDBY MODE OPERATION

The ADDI7004 contains two standby modes to optimize the overall power dissipation in a particular application. Bits[1:0] of the STANDBY_x register (Address 0x00) control the power-down state of Channel A, Bits[3:2] control Channel B, Bits[5:4] control Channel C, and Bits[7:6] control Channel D.

- STANDBY_x [1:0] = 0 = normal operation (full power)
- STANDBY_x [1:0] = 1 = reference standby mode
- STANDBY_x [1:0] = 2 or 3 = total shutdown mode (lowest power)

Table 19 summarizes the operation of each power-down mode. The OUT_CONTROL (Address 0x31) register takes priority over the reference standby mode in determining the digital output states, but total shutdown mode takes priority over OUT_CONTROL.

Total shutdown mode has the lowest power consumption. When returning from total shutdown mode to normal operation, the timing core must be reset at least 500 µs after the STANDBY_x register is written to.

There is an additional register, REFBUF_PDN_x (Address 0x01, Bit 0), to disable the internal voltage reference buffer independently. By default, the buffer is disabled, but the buffer must be enabled for normal operation.

CLI FREQUENCY CHANGE

If the input clock, CLI, is interrupted or changes to a different frequency, the timing core must be reset for proper operation. After the CLI clock has settled to the new frequency, or the previous frequency is resumed, write 0 and then 1 to the TGCORE_RSTB register (Address 0x33). Allow at least 100 µs settling time, and then write to Address 0xA2 to configure the desired TCLK delay setting. This guarantees proper timing core operation.

CIRCUIT CONFIGURATION

The ADDI7004 recommended circuit configuration is shown in Figure 63. Achieving good image quality from the ADDI7004 requires careful attention to the printed circuit board (PCB) layout. Route all signals to maintain low noise performance. To minimize interference with the INP_x and INM_x signals, carefully route the master clock, CLI to DIO (digital input/output).

To minimize crosstalk, carefully route the sensor signals away from one another to minimize stray capacitance between them.

GROUNDING AND DECOUPLING RECOMMENDATIONS

As shown in Figure 63, a single ground plane is recommended for the ADDI7004. This ground plane should be as continuous as possible, particularly around the analog pins.

This configuration ensures that all analog decoupling capacitors provide the lowest possible impedance path between the power and bypass pins and their respective ground pins. Locate all high frequency decoupling capacitors as close as possible to the package pins.

All the supply pins must be decoupled to ground with quality, high frequency chip capacitors. In addition, provide a 0.1 µF (or larger) bypass capacitor for each main supply (1.8 V for the AVDD, DVDD, and LVDD and 3.3 V for the IOVDD and INVDD), although this is not necessary for each individual pin.

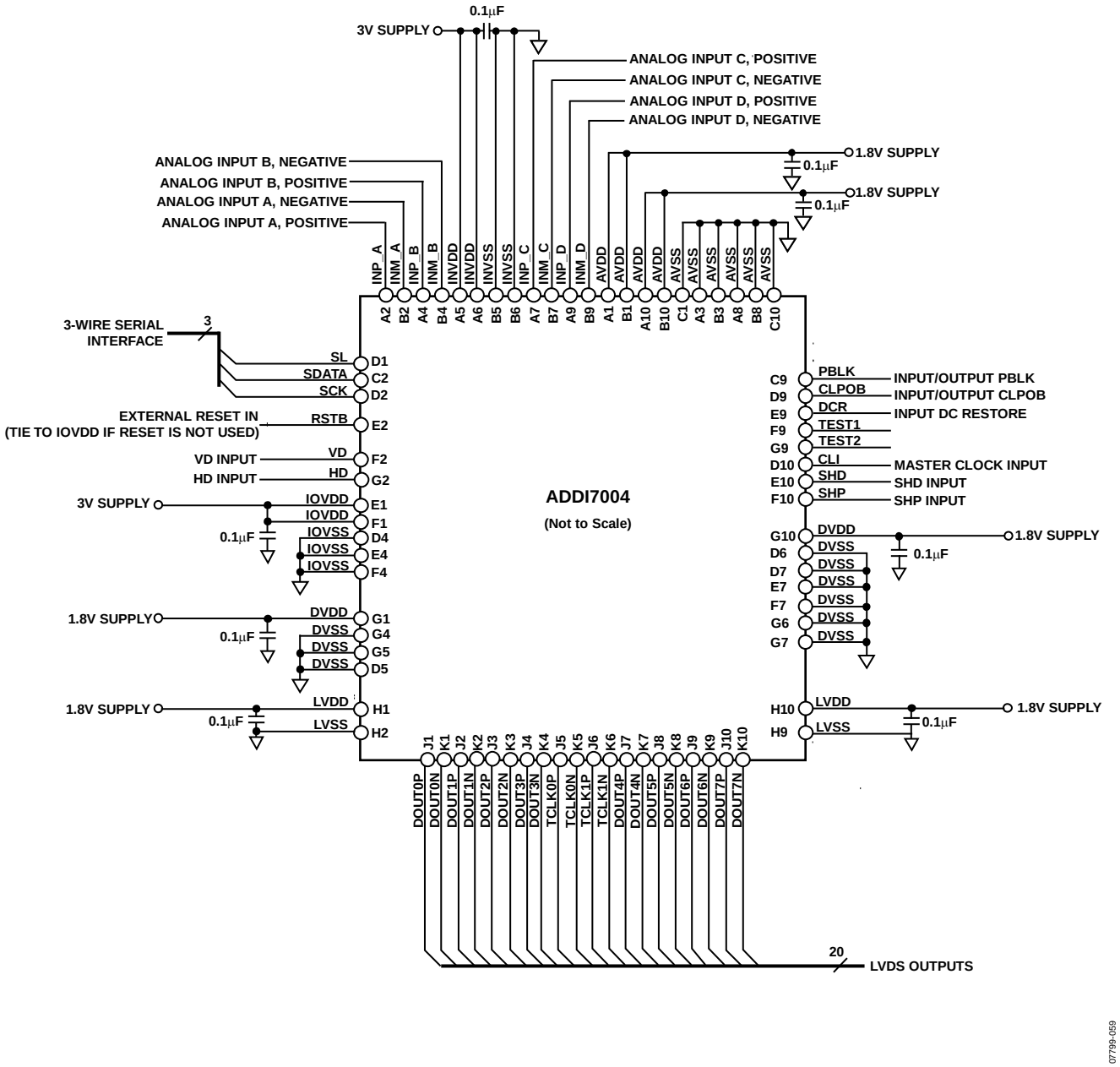


Figure 63. Recommended Circuit Configuration

SERIAL INTERFACE TIMING

All of the ADDI7004 internal registers are accessed through a 3-wire serial interface. Each register consists of a 16-bit address and a 16-bit data-word. Both the address and data-word are written by starting with the LSB. To write to each register, a 32-bit operation is required, as shown in Figure 64. Although many data-words are fewer than 16 bits wide, all 16 bits must be written for each register. For example, if the data-word is only eight bits wide, the upper eight bits are don't cares and must be filled with 0s during the serial write operation. If fewer than 16 data bits are written, the register is not updated with new data.

Figure 65 shows a more efficient way to write to the registers, using the ADDI7004 address autoincrement capability. Using this method, the lowest desired address is written first, followed by multiple 16-bit data-words. Each data-word is automatically written to the address of the next higher register. By eliminating the need to write each address, faster register loading is achieved. Continuous write operations can start with any register location.

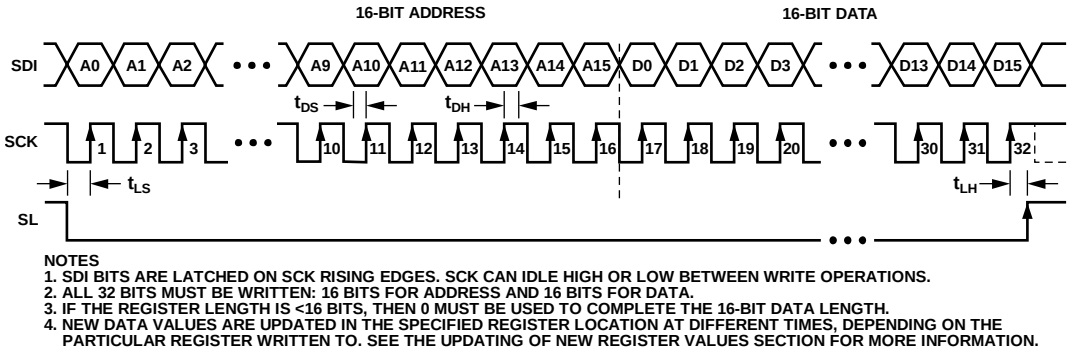


Figure 64. Serial Write Operation

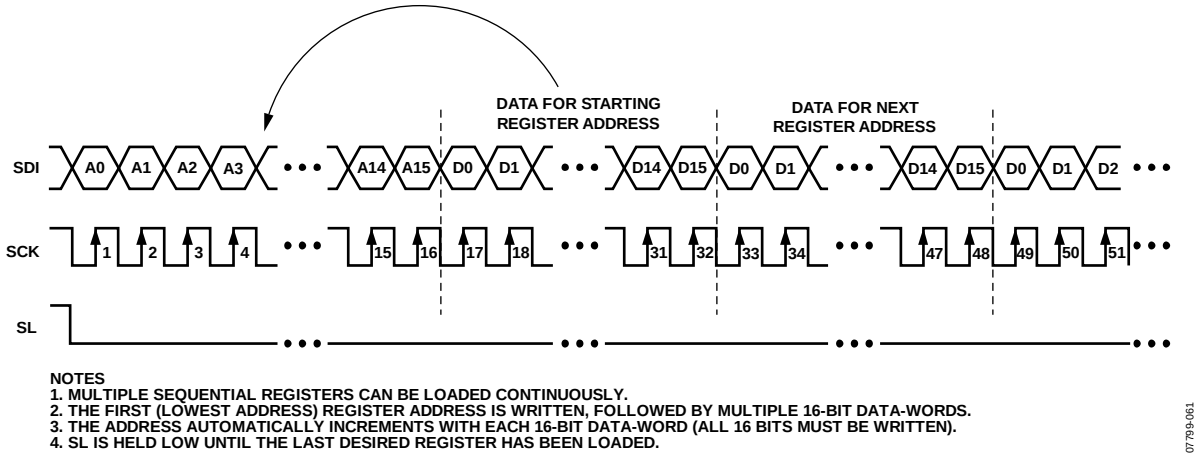


Figure 65. Continuous Serial Write Operation

The ADDI7004 address space is divided into several register areas as illustrated in Figure 66.

The ADDI7004 address space contains many unused addresses. Do not write to any undefined addresses between Address 0x40 and Address 0xFF; otherwise, the ADDI7004 may operate incorrectly. Carefully perform continuous register writes to avoid writing to undefined registers.

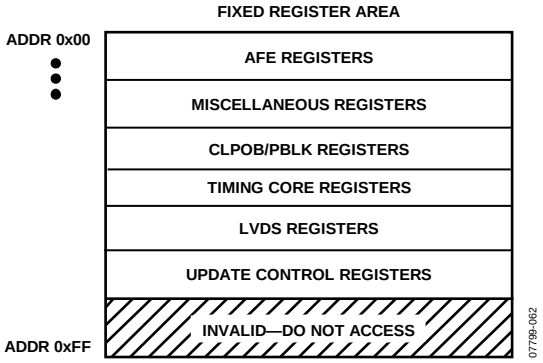


Figure 66. Layout of ADDI7004 Registers

UPDATING OF NEW REGISTER VALUES

The internal registers of the ADDI7004 are updated at different times, depending on the particular register. Table 20 summarizes the two types of register updates. The register listing tables in the Complete Register Listings section contain update type columns to identify when each register is updated.

- SCK update. Some registers are updated immediately when the 16th data bit is written to. These registers are used for functions that do not require gating with the next VD boundary, such as power-up and reset functions.
- VD update. Many registers are updated at the next VD falling edge. By updating these values at the next RCP edge, the current field is not corrupted, and the new register values are applied to the next field. The VD update can be further delayed past the VD falling edge by using the VDUPDATE[12:0] register (Address 0x37). This delays the VD updated register updates to any HD line in the field.

Table 20. Register Update Locations

Update Type	Description
SCK	The register is immediately updated when the 16th data bit (D15) is clocked in.
VD	The register is updated at the falling edge of VD.

COMPLETE REGISTER LISTINGS

All addresses and default values are expressed in hexadecimal. When an address contains fewer than 16 data bits, all remaining bits must be written as 0s. All test registers must be set to the specified values or not accessed.

AFE REGISTERS

Table 21.

Hex Address	Data Bit Content	Default Value	Update	Mnemonic	Description
0x00	[1:0]	0x03	SCK/VD	STANDBY_A	Channel_x standby control 0 = normal operation 1 = reference standby 2 = full power-down 3 = full power-down
	[3:2]	0x03		STANDBY_B	
	[5:4]	0x03		STANDBY_C	
	[7:6]	0x03		STANDBY_D	
0x01	[0]	0x01	SCK/VD	REFBUF_PDN_A	0 = reference buffer power-up 1 = reference buffer power-down
	[1]	0x01		REFBUF_PDN_B	
	[2]	0x01		REFBUF_PDN_C	
	[3]	0x01		REFBUF_PDN_D	
0x02	[0]	0x01	SCK/VD	CLAMPENABLE	0 = disable OB clamp 1 = enable OB clamp
	[1]	0x00		CLAMPSPEED	0 = select normal OB clamp settling 1 = select fast OB clamp settling
	[2]	0x00		FASTUPDATE	0 = ignore CDS gain 1 = very fast clamping when CDS gain is updated
	[3]	0x00		EXT_CLPOB	0 = internal CLPOB 1= external CLPOB
	[4]	0x00		Test	Test use only; set to 0
0x03	[0]	0x00	SCK/VD	PBLK_LVL	0 = blank to 0 during PBLK 1 = blank to clamp level during PBLK
	[1]	0x00		PBLKPAT	PBLK select Pattern 0 or Pattern 1
	[2]	0x00		DC_BYPASS	0 = dc restore enabled during PBLK 1 = dc restore disabled during PBLK
	[4:3]	0x00		Test	Test use only; set to 0
	[5]	0x00		EXT_PBLK	0 = internal PBLK 1= external PBLK
	[6]	0x00		Test	Test use only; set to 0
0x04	[0]	0x00	SCK/VD	EXT_SHPD	0 = internal SHP/SHD 1 = external SHP/SHD
	[1]	0x01		POL_SHP	External SHP active polarity 0 = rising edge active 1= falling edge active
	[2]	0x01		POL_SHD	External SHD active polarity 0 = rising edge active 1= falling edge active
	[3]	0x00		Test	Test use only; set to 0
	[4]	0x00		MONITOR_INT_CLK	0 = do not monitor internal clocks 1 = monitor internal clocks Pin D9: CLPOB Pin C9: PBLK Pin E9: SHP Pin F9: internal sampling clock Pin G9: invalid

Hex Address	Data Bit Content	Default Value	Update	Mnemonic	Description
0x05	[0]	0x00	SCK/VD	POL_VD	VD active polarity 0 = falling edge active 1 = rising edge active
	[1]	0x00		POL_HD	HD active polarity 0 = falling edge active 1 = rising edge active
	[2]	0x00		Test	Test use only; set to 0
0x06	[0]	0x00	SCK/VD	SAMP_MODE	0 = CDS mode 1 = SHA mode
0x07	[1:0]	0x01	SCK/VD	CDS_GAIN_A	0 = −3 dB 1 = 0 dB 2 = +3 dB 3 = +6 dB
	[3:2]	0x01		CDS_GAIN_B	
	[5:4]	0x01		CDS_GAIN_C	
	[7:6]	0x01		CDS_GAIN_D	
0x08	[9:0]	0x0F	SCK/VD	VGAGAIN_A	Channel A VGA gain; 6 dB to 42 dB (0.035 dB per step)
0x09	[9:0]	0x0F	SCK/VD	VGAGAIN_B	Channel B VGA gain; 6 dB to 42 dB (0.035 dB per step)
0x0A	[9:0]	0x0F	SCK/VD	VGAGAIN_C	Channel C VGA gain; 6 dB to 42 dB (0.035 dB per step)
0x0B	[9:0]	0x0F	SCK/VD	VGAGAIN_D	Channel D VGA gain; 6 dB to 42 dB (0.035 dB per step)
0x0C	[9:0]	0x0F	SCK/VD	Test	Test use only; set to 0x0F
0x0D	[9:0]	0x0F	SCK/VD	Test	Test use only; set to 0x0F
0x0E	[9:0]	0x0F	SCK/VD	Test	Test use only; set to 0x0F
0x0F	[9:0]	0x0F	SCK/VD	Test	Test use only; set to 0x0F
0x10	[9:0]	0x1EC	SCK/VD	CLAMPLEVEL_A	Channel A optical black clamp level; 0 LSB to 1023 LSB (1 LSB per step)
0x11	[9:0]	0x1EC	SCK/VD	CLAMPLEVEL_B	Channel B optical black clamp level; 0 LSB to 1023 LSB (1 LSB per step)
0x12	[9:0]	0x1EC	SCK/VD	CLAMPLEVEL_C	Channel C optical black clamp level; 0 LSB to 1023 LSB (1 LSB per step)
0x13	[9:0]	0x1EC	SCK/VD	CLAMPLEVEL_D	Channel D optical black clamp level; 0 LSB to 1023 LSB (1 LSB per step)
0x14	[9:0]	0x1EC	SCK/VD	Test	Test use only; set to 0x1EC
0x15	[9:0]	0x1EC	SCK/VD	Test	Test use only; set to 0x1EC
0x16	[9:0]	0x1EC	SCK/VD	Test	Test use only; set to 0x1EC
0x17	[9:0]	0x1EC	SCK/VD	Test	Test use only; set to 0x1EC
0x18	[0]	0x00	SCK/VD	Test	Test use only; set to 0
0x19	[11:0]	0xFFF	SCK/VD	Test	Test use only; set to 0xFFF
0x1A	[11:0]	0xFFF	SCK/VD	Test	Test use only; set to 0xFFF
0x1B	[1:0]	0x00	SCK/VD	CLI_DIVIDE	0 = CLK equals CLI 1 = CLK equals CLI/2 2 = CLK equals CLI/4 3 = CLK equals CLI/4
	[2]	0x00		Test	Test use only; must be set to 0
	[3]	0x00		Test	Test use only; must be set to 0
	[4]	0x00		Test	Test use only; must be set to 0
	[5]	0x01		Test	Test use only; must be set to 1
	[7:6]	0x00		Test	Test use only; must be set to 0
	[10:8]	0x02		Test	Test use only; must be set to 2

Hex Address	Data Bit Content	Default Value	Update	Mnemonic	Description
0x1C	[0]	0x00	SCK/VD	DCREST_EN_P	0 = disable dc restore on INP_x (all channels) 1 = enable dc restore on INP_x (all channels)
	[1]	0x00		DCREST_EN_N	0 = disable dc restore on INM_x (all channels) 1 = enable dc restore on INM_x (all channels)
	[2]	0x00		DCREST_EN_A	Channel A 0 = disable dc restore 1 = enable dc restore
	[3]	0x00		DCREST_EN_B	Channel B 0 = disable dc restore 1 = enable dc restore
	[4]	0x00		DCREST_EN_C	Channel C 0 = disable dc restore 1 = enable dc restore
	[5]	0x00		DCREST_EN_D	Channel D 0 = disable dc restore 1 = enable dc restore
	[6]	0x00		DCRSTR	DCR switch strength 0 = weak (approximately 20 kΩ), required for pixel rate DCR 1 = strong (approximately 500 Ω), can be used for line rate DCR
	[9:7]	0x00		Test	Test use only; set to 0
	[10]	0x00		DCREXT	DCR external control 0 = use internal pixel rate DCR control 1 = use external pin to control DCR
	[11]	0x01		DCREXTMODE	DCR mode 0 = external signal directly controls DCR switch 1 = gate external signal with internal SHPWIDTH/DCR signal
	[12]	0x00		DCREXTPOL	DCR pin polarity 0 = external DCR signal high active 1 = external DCR signal low active
	[15:13]	0x04		Test	Test use only; set to 4

MISCELLANEOUS REGISTERS

Table 22.

Hex Address	Data Bit Content	Default Value	Update	Mnemonic	Description
0x30	[0]	0x00	SCK/VD	SW_RESET	Software reset; self-resetting
0x31	[0]	0x00	SCK/VD	OUT_CONTROL	Output control 0 = disable outputs 1 = enable outputs
0x32	[0]	0x00	SCK/VD	Test	Test use only; set to 0
0x33	[0]	0x00	SCK/VD	TGCORE_RSTB	0 = TG core in power-down mode
0x34	[0]	0x00	SCK/VD	CLI_BIAS	Enable bias for CLI input 0 = disable bias (CLI is dc-coupled) 1 = enable bias (CLI is ac-coupled)
0x35	[0]	0x00	SCK/VD	Test	Test use only; set to 0
0x36	[0]	0x00	SCK/VD	READBACK	SPI readback mode
0x37	[12:0]	0x00	SCK/VD	VDUPDATE	Line control for VD updated SPI data
0x38	[0]	0x01	SCK/VD	PREVENTUPDATE	Prevents the update of the VD updated registers
0x39	[1:0]	0x02	SCK/VD	Test	Test use only; set to 2
0x3A	[2:0]	0x00	SCK/VD	Test	Test use only; set to 0
0x3B	[7:0]	0x00	SCK/VD	Test	Test use only; set to 0
0x3C	[5:0]	0x00	SCK/VD	Test	Test use only; set to 0

CLPOB/PBLK REGISTERS

Table 23.

Hex Address	Data Bit Content	Default Value	Update	Mnemonic	Description
0x50	[12:0]	0x1FFF	SCK/VD	RCP0	Region 0 end line
0x51	[12:0]	0x00	SCK/VD	RCP1	Region 1 end line
0x52	[12:0]	0x00	SCK/VD	RCP2	Region 2 end line
0x53	[12:0]	0x00	SCK/VD	RCP3	Region 3 end line
0x54	[12:0]	0x00	SCK/VD	RCP4	Region 4 end line
0x55	[12:0]	0x00	SCK/VD	RCP5	Region 5 end line
0x56	[12:0]	0x00	SCK/VD	RCP6	Region 6 end line
0x57	[15:0]	0x00	SCK/VD	CLPOB_TOG1_REG0	CLPOB Toggle Position 1 for Region 0. Toggle 0 cannot be used.
0x58	[15:0]	0xFFFF	SCK/VD	CLPOB_TOG2_REG0	CLPOB Toggle Position 2 for Region 0. Toggle 0 cannot be used.
0x59	[15:0]	0x00	SCK/VD	CLPOB_TOG1_REG1	CLPOB Toggle Position 1 for Region 1. Toggle 0 cannot be used.
0x5A	[15:0]	0x00	SCK/VD	CLPOB_TOG2_REG1	CLPOB Toggle Position 2 for Region 1. Toggle 0 cannot be used.
0x5B	[15:0]	0x00	SCK/VD	CLPOB_TOG1_REG2	CLPOB Toggle Position 1 for Region 2. Toggle 0 cannot be used.
0x5C	[15:0]	0x00	SCK/VD	CLPOB_TOG2_REG2	CLPOB Toggle Position 2 for Region 2. Toggle 0 cannot be used.
0x5D	[15:0]	0x00	SCK/VD	CLPOB_TOG1_REG3	CLPOB Toggle Position 1 for Region 3. Toggle 0 cannot be used.
0x5E	[15:0]	0x00	SCK/VD	CLPOB_TOG2_REG3	CLPOB Toggle Position 2 for Region 3. Toggle 0 cannot be used.
0x5F	[15:0]	0x00	SCK/VD	CLPOB_TOG1_REG4	CLPOB Toggle Position 1 for Region 4. Toggle 0 cannot be used.
0x60	[15:0]	0x00	SCK/VD	CLPOB_TOG2_REG4	CLPOB Toggle Position 2 for Region 4. Toggle 0 cannot be used.
0x61	[15:0]	0x00	SCK/VD	CLPOB_TOG1_REG5	CLPOB Toggle Position 1 for Region 5. Toggle 0 cannot be used.
0x62	[15:0]	0x00	SCK/VD	CLPOB_TOG2_REG5	CLPOB Toggle Position 2 for Region 5. Toggle 0 cannot be used.
0x63	[15:0]	0x00	SCK/VD	CLPOB_TOG1_REG6	CLPOB Toggle Position 1 for Region 6. Toggle 0 cannot be used.
0x64	[15:0]	0x00	SCK/VD	CLPOB_TOG2_REG6	CLPOB Toggle Position 2 for Region 6. Toggle 0 cannot be used.
0x65	[15:0]	0x00	SCK/VD	CLPOB_TOG1_REG7	CLPOB Toggle Position 1 for Region 7. Toggle 0 cannot be used.
0x66	[15:0]	0x00	SCK/VD	CLPOB_TOG2_REG7	CLPOB Toggle Position 2 for Region 7. Toggle 0 cannot be used.
0x67	[4:0]	0x09	SCK/VD	TC_REG0	TC_SEL for Region 0
0x68	[4:0]	0x00	SCK/VD	TC_REG1	TC_SEL for Region 1
0x69	[4:0]	0x00	SCK/VD	TC_REG2	TC_SEL for Region 2
0x6A	[4:0]	0x00	SCK/VD	TC_REG3	TC_SEL for Region 3
0x6B	[4:0]	0x00	SCK/VD	TC_REG4	TC_SEL for Region 4
0x6C	[4:0]	0x00	SCK/VD	TC_REG5	TC_SEL for Region 5
0x6D	[4:0]	0x00	SCK/VD	TC_REG6	TC_SEL for Region 6
0x6E	[4:0]	0x00	SCK/VD	TC_REG7	TC_SEL for Region 7
0x6F	[12:0]	0x00	SCK/VD	PBLKMASK_START1	PBLK Mask Region 1 start position
0x70	[12:0]	0x00	SCK/VD	PBLKMASK_END1	PBLK Mask Region 1 end position
0x71	[12:0]	0x00	SCK/VD	PBLKMASK_START2	PBLK Mask Region 2 start position
0x72	[12:0]	0x00	SCK/VD	PBLKMASK_END2	PBLK Mask Region 2 end position
0x73	[12:0]	0x00	SCK/VD	PBLKMASK_START3	PBLK Mask Region 3 start position
0x74	[12:0]	0x00	SCK/VD	PBLKMASK_END3	PBLK Mask Region 3 end position
0x75	[15:0]	0x00	SCK/VD	PBLK0_TOG1	PBLK Pattern 0, Toggle Position 1
0x76	[15:0]	0x00	SCK/VD	PBLK0_TOG2	PBLK Pattern 0, Toggle Position 2
0x77	[15:0]	0x00	SCK/VD	PBLK1_TOG1	PBLK Pattern 1, Toggle Position 1
0x78	[15:0]	0x00	SCK/VD	PBLK1_TOG2	PBLK Pattern 1, Toggle Position 2

Hex Address	Data Bit Content	Default Value	Update	Mnemonic	Description
0x79	[7:0]	0xFF	SCK/VD	INT_CLPOB_POL	[0] = INT_CLPOB_REG0_POL [1] = INT_CLPOB_REG1_POL [2] = INT_CLPOB_REG2_POL [3] = INT_CLPOB_REG3_POL [4] = INT_CLPOB_REG4_POL [5] = INT_CLPOB_REG5_POL [6] = INT_CLPOB_REG 6_POL [7] = INT_CLPOB_REG7_POL
0x7A	[3:0]	0x0F	SCK/VD	INT_PBLK_POL	[0] = INT_PBLK_POL [1] = PBLKMASK_POL_REG1 [2] = PBLKMASK_POL_REG2 [3] = PBLKMASK_POL_REG3

TIMING CORE REGISTERS

Table 24.

Hex Address	Data Bit Content	Default Value	Update	Mnemonic	Description
0x90	[2:0]	0x00	SCK/VD	Test	Test use only; set to 0
0x91	[5:0] [13:8]	0x00 0x20	SCK/VD	SHDLOC SHPLOC	SHD sampling location SHP sampling location
0x92	[15:0]	0x2000	SCK/VD	Test	Test use only; set to 0x2000
0x93	[15:0]	0x2000	SCK/VD	Test	Test use only; set to 0x2000
0x94	[15:0]	0x2000	SCK/VD	Test	Test use only; set to 0x2000
0x95	[15:0]	0x2000	SCK/VD	Test	Test use only; set to 0x2000
0x96	[15:0]	0x2000	SCK/VD	Test	Test use only; set to 0x2000
0x97	[15:0]	0x2000	SCK/VD	Test	Test use only; set to 0x2000
0x98	[15:0]	0x2000	SCK/VD	Test	Test use only; set to 0x2000
0x99	[5:0] [13:8]	0x00 0x20	SCK/VD	Test Test	Test use only; set to 0 Test use only; set to 0x20
0x9A	[5:0] [13:8]	0x00 0x20	SCK/VD	DOUTPHASEP DOUTPHASEN	DOUT phase control. DOUT phase control; should be set equal to DOUTPHASEP + 0x20
0x9B	[1:0]	0x00	SCK/VD	Test	Test use only; set to 0

LVDS REGISTERS

Table 25.

Hex Address	Data Bit Content	Default Value	Update	Mnemonic	Description
0xA0	[0]	0x01	SCK/VD	TCLK0_PDN	0 = normal operation, 1 = power-down (default)
	[1]	0x01		TCLK1_PDN	0 = normal operation, 1 = power-down (default)
	[2]	0x01		DOUT0_PDN	0 = normal operation, 1 = power-down (default)
	[3]	0x01		DOUT1_PDN	0 = normal operation, 1 = power-down (default)
	[4]	0x01		DOUT2_PDN	0 = normal operation, 1 = power-down (default)
	[5]	0x01		DOUT3_PDN	0 = normal operation, 1 = power-down (default)
	[6]	0x01		DOUT4_PDN	0 = normal operation, 1 = power-down (default)
	[7]	0x01		DOUT5_PDN	0 = normal operation, 1 = power-down (default)
	[8]	0x01		DOUT6_PDN	0 = normal operation, 1 = power-down (default)
	[9]	0x01		DOUT7_PDN	0 = normal operation, 1 = power-down (default)
0xA1	[1:0]	0x00	SCK/VD	Test	Test use only; set to 0
	[2]	0x00		LVDS_VDIFF_SEL_EN	0 = disable LVDS differential voltage selection 1 = enable LVDS differential voltage selection
	[6:3]	0x00		LVDS_VDIFF_SEL	LVDS bias selection 0 = test use only 1 = 150 mV (1.5 mA) 2 = 200 mV (2.0mA) 3 to 15 = test use only
	[7]	0x00		LVDS_VCM	0 = LVDS common-mode voltage = 1.2 V 1 = LVDS common-mode voltage = LVDD/2
0xA2	[1:0]	0x00	SCK/VD	TX_CTRL	Serial data transmit control 0 = single port mode, data output DOUT0/DOUT2/DOUT4/DOUT6 1 = double port mode, data LSB output DOUT0/DOUT2/DOUT4/DOUT6 2 = single port mode, data output DOUT1/DOUT3/DOUT5/DOUT7 3 = double port mode, data LSB output, DOUT1/DOUT3/DOUT5/DOUT7
	[4:2]	0x00		TCLK_DEL	TCLK rising edge delay 0 = default, no delay 1 LSB = 1/16 cycle of TCLK in double port mode. Allowable settings are 0 to 7. 1 LSB = 1/8 cycle of TCLK in single port mode. Allowable settings are 0 to 3 only.
	[6:5]	0x00		Test	Test use only; set to 0
	[8:7]	0x01		Test	Test use only; set to 1
	[15:9]	0x00		Test	Test use only; set to 0
0xA4	[0]	0x00	SCK/VD	CLIP_ZS	0 = clip function disabled, ADC zero scale = 0x0000 1 = clip function enabled, ADC zero scale = 0x0001
	[1]	0x00		CLIP_FS	0 = clip function disabled, ADC full scale = 0x3FFF 1 = clip function enabled, ADC full scale = 0x3FFE
	[2]	0x00		LSB_ALIGN	0 = MSB first (default), 1 = LSB first
	[3]	0x00		ZEROMSB	0 = put 0s on LSB, 1 = put 0s on MSB
00A5	[0]	0x00	SCK/VD	Test	Test use only; set to 0
0xA6	[6:0]	0x20	SCK/VD	Test	Test use only; set to 0x20
0xA7	[10:0]	0x4B0	SCK/VD	Test	Test use only; set to 0x4B0
0xA8	[2:0]	0x00	SCK/VD	NUM_SYNC_WORD	Number of sync words
	[3]	0x00		CTRL_WORD_EN	Enable control word
0xA9	[15:0]	0x00	SCK/VD	SYNC_WORD0	Synchronization Word 0 data bits
0xAA	[15:0]	0x00	SCK/VD	SYNC_WORD1	Synchronization Word 1 data bits
0xAB	[15:0]	0x00	SCK/VD	SYNC_WORD2	Synchronization Word 2 data bits
0xAC	[15:0]	0x00	SCK/VD	SYNC_WORD3	Synchronization Word 3 data bits

Hex Address	Data Bit Content	Default Value	Update	Mnemonic	Description
0xAD	[15:0]	0x00	SCK/VD	SYNC_WORD4	Synchronization Word 4 data bits
0xAE	[15:0]	0x00	SCK/VD	SYNC_WORD5	Synchronization Word 5 data bits
0xAF	[15:0]	0x00	SCK/VD	SYNC_WORD6	Synchronization Word 6 data bits
0xB0	[1:0]	0x00	SCK/VD	LVDS_TEST_EN_A	0 = disable LVDS test pattern for Channel A 1 = insert LVDS test pattern for Channel A 2, 3 = unused
	[5:2]	0x00	SCK/VD	LVDS_TEST_TYPE_A	Test data pattern selection for Channel A [0] = enable pseudorandom data generation [1] = enable test pattern shifting [2] = enable ramp data generation [3] = test use only
0xB1	[15:0]	0x0	SCK/VD	TEST_PATTERN_A	Channel A test pattern
0xB2	[1:0]	0x00	SCK/VD	LVDS_TEST_EN_B	0 = disable LVDS test pattern for Channel B 1 = insert LVDS test pattern for Channel B 2, 3 = unused
	[5:2]	0x00	SCK/VD	LVDS_TEST_TYPE_B	Test data pattern selection for Channel B [0] = enable pseudorandom data generation [1] = enable test pattern shifting [2] = enable ramp data generation [3] = test use only
0xB3	[15:0]	0x00	SCK/VD	TEST_PATTERN_B	Channel B test pattern
0xB4	[1:0]	0x00	SCK/VD	LVDS_TEST_EN_C	0 = disable LVDS test pattern for Channel C 1 = insert LVDS test pattern for Channel C 2, 3 = unused
	[5:2]	0x00		LVDS_TEST_TYPE_C	Test data pattern selection for Channel C [0] = enable pseudorandom data generation [1] = enable test pattern shifting [2] = enable ramp data generation [3] = test use only
0xB5	[15:0]	0x00	SCK/VD	TEST_PATTERN_C	Channel C test pattern
0xB6	[1:0]	0x00	SCK/VD	LVDS_TEST_EN_D	0 = disable LVDS test pattern for Channel D 1 = insert LVDS test pattern for Channel D 2, 3 = unused
	[5:2]	0x00		LVDS_TEST_TYPE_D	Test data pattern selection for Channel D [0] = enable pseudorandom data generation [1] = enable test pattern shifting [2] = enable ramp data generation [3] = test use only
0xB7	[15:0]	0x00	SCK/VD	TEST_PATTERN_D	Channel D test pattern
0xB8	[15:0]	0x00	SCK/VD	TCLK_PATTERN	Pattern for TCLK Single port uses Bits[15:0] Double port uses Bits[15:8]
0xB9	[0]	0x00	SCK/VD	TCLK_MODE	0 = disable TCLK pattern mode 1 = enable TCLK pattern mode
0xBA	[7:0]	0x00	SCK/VD	SYNC_RISING_EN	Rising sync enable for control word bits
0xBB	[7:0]	0x00	SCK/VD	SYNC_FALLING_EN	Falling sync enable for control word bits
0xBC	[15:0]	0x00	SCK/VD	SYNC_START_LOC	Sync sequence start location for automatic mode
0xBD	[0]	0x00	SCK/VD	SYNC_ALIGN	0 = sync word insert after SYNC_START_LOC (default) 1 = sync word insert before SYNC_START_LOC
	[1]	0x00		SYNC_CW_EN	1 = enable automatic sync and control word output
0xBE	[1:0]	0x00	SCK/VD	Test	Test use only; set to 0
0xBF	[7:0]	0x00	SCK/VD	Test	Test use only; set to 0
0xC0	[12:0]	0x00	SCK/VD	Test	Test use only; set to 0
0xC1	[12:0]	0x00	SCK/VD	Test	Test use only; set to 0

Hex Address	Data Bit Content	Default Value	Update	Mnemonic	Description
0xC2	[15:0]	0x00	SCK/VD	Test	Test use only; set to 0
0xC3	[15:0]	0x00	SCK/VD	Test	Test use only; set to 0
0xC4	[15:0]	0xE4	SCK/VD	Test	Test use only; set to 0xE4
0xC5	[1:0]	0x00	SCK/VD	Test	Test use only; set to 0

UPDATE CONTROL REGISTERS

Table 26.

Hex Address	Data Bit Content	Default Value	Update	Mnemonic	Description
0xD0	[15:0]	0xFFFF	SCK	AFE_UPDT_SCK[15:0]	Each bit corresponds to one address location in the range of 0x00 to 0x0F; 0 = VD edge, 1 = SCK rising edge. [0] = update timing for Register 0x00. [1] = update timing for Register 0x01. … … [15] = update timing for Register 0x0F.
0xD1	[15:0]	0xFFFF	SCK	AFE_UPDT_SCK[28:16]	Each bit corresponds to one address location in the range of 0x10 to 0x1C; 0 = VD edge, 1 = SCK rising edge. [0] = update timing for Register 0x10. [1] = update timing for Register 0x11. … [12] = update timing for Register 0x1C.
0xD2	[15:0]	0xFFFF	SCK	Test	Test use only; set to 0.
0xD3	[15:0]	0xFFFF	SCK	Test	Test use only; must be set to 0xFFFF.
0xD4	[15:0]	0xFFFF	SCK	Test	Test use only; must be set to 0xFFFF.
0xD5	[15:0]	0xFFFF	SCK	Test	Test use only; set to 0.
0xD6	[15:0]	0xFBFF	SCK	MISC_UPDT_SCK[15:0]	Each bit corresponds to one address location in the range of 0x30 to 0x3C; 0 = VD edge, 1 = SCK rising edge. [0] = update timing for Register 0x30. [1] = update timing for Register 0x31. … … [12] = update timing for Register 0x3C.
0xD7	[15:0]	0xFFFF	SCK	Test	Test use only; set to 0.
0xD8	[15:0]	0xFFFF	SCK	Test	Test use only; must be set to 0xFFFF.
0xD9	[15:0]	0xFFFF	SCK	Test	Test use only; set to 0.
0xDA	[0]	0x00	SCK	CLPOB_UPDT_SCK	Enable SCK update of all registers in the range of 0x50 to 0x8F.
0xDB	[0]	0x01	SCK	Test	Test use only; must be set to 0x1.
0xDC	[15:0]	0xFFFF	SCK	TGCORE_UPDT_SCK[11:0]	Each bit corresponds to one address location in the range of 0x90 to 0x9B; 0 = VD edge, 1 = SCK rising edge. [0] = update timing for Register 0x90. [1] = update timing for Register 0x91. … … [11] = update timing for Register 0x9B.
0xDD	[15:0]	0xFFFF	SCK	Test	Test use only; must be set to 0xFFFF.

Hex Address	Data Bit Content	Default Value	Update	Mnemonic	Description
0xDE	[15:0]	0xFFFF	SCK	LVDS_UPDT_SCK[15:0]	Each bit corresponds to one address location in the range of 0xA0 to 0xAF; 0 = VD edge, 1 = SCK rising edge. [0] = update timing for Register 0xA0. [1] = update timing for Register 0xA1. … … [15] = update timing for Register 0xAF.
0xDF	[15:0]	0xFFFF	SCK	LVDS_UPDT_SCK[31:16]	Each bit corresponds to one address location in the range of 0xB0 to 0xBF; 0 = VD edge, 1 = SCK rising edge. [0] = update timing for Register 0xB0. [1] = update timing for Register 0xB.1 … … [15] = update timing for Register 0xBF.
0xE0	[15:0]	0x20	SCK	LVDS_UPDT_SCK[37:32]	Each bit corresponds to one address location in the range of 0xC0 to 0xC5; 0 = VD edge, 1 = SCK rising edge. [0] = update timing for Register 0xC0. [1] = update timing for Register 0xC1. … … [5] = update timing for Register 0xC5.
0xE1	[15:0]	0xFFFF	SCK	Test	Test use only; must be set to 0xFFFF.
0xE2	[15:0]	0xFFFF	SCK	Test	Test use only; must be set to 0xFFFF.
0xE3	[15:0]	0xFFFF	SCK	Test	Test use only; must be set to 0xFFFF.

Table 27.

Hex Address	Data Bit Content	Default Value	Update	Mnemonic	Description
0xF3	[15:0]	0x0000	SCK	STARTUP1	Required startup register for >65 MHz operation must be set to 0x000F. For 65 MHz or lower, the default value of 0x0 is recommended.
0xF9	[15:0]	0xC007	SCK	STARTUP2	Required startup register for >65 MHz operation must be set to 0xC037. For 65 MHz or lower, the default value of 0xC007 is recommended.

OUTLINE DIMENSIONS

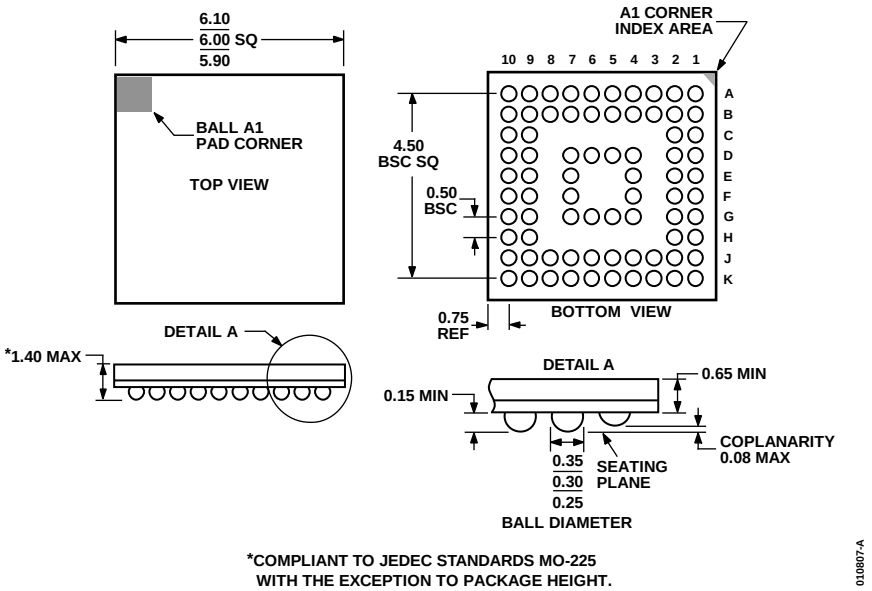


Figure 67. 76-Ball Chip Scale Package Ball Grid Array [CSP_BGA]
(BC-76-1)
Dimensions shown in millimeters

ORDERING GUIDE

Model[1]	Temperature Range	Package Description	Package Option
ADDI7004BBBCZ	−40°C to +85°C	76-Ball CSP_BGA	BC-76-1
ADDI7004BBBCZRL	−40°C to +85°C	76-Ball CSP_BGA	BC-76-1

[1] Z = RoHS Compliant Part.

NOTES