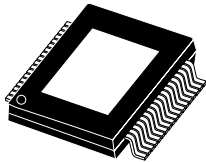


160-watt + 160-watt dual BTL class-D audio amplifier



PowerSSO-36
exposed pad up

Features

- 160-W + 160-W output power at THD = 10% with $R_L = 4 \Omega$ and $V_{CC} = 36 V$
- 1 x 220 W output power mono parallel BTL at THD = 10% with $R_L = 3 \Omega$ and $V_{CC} = 36 V$
- Wide-range single-supply operation (14 - 36 V)
- High efficiency ($\eta = 85\%$)
- Parallel BTL function using the MODE pin
- Four selectable, fixed gain settings of nominally 23.8 dB, 29.8 dB, 33.3 dB and 35.8 dB
- Differential inputs minimize common-mode noise
- Standby and mute features
- Smart protection
- Thermal overload protection
- Small offset less than 20 mV

Description

The TDA7498E is a dual BTL class-D audio amplifier with a single power supply designed for home systems and active speaker applications.

It comes in a 36-pin PowerSSO package with exposed pad up (EPU) to facilitate mounting a separate heatsink.

Maturity status link

[TDA7498E](#)

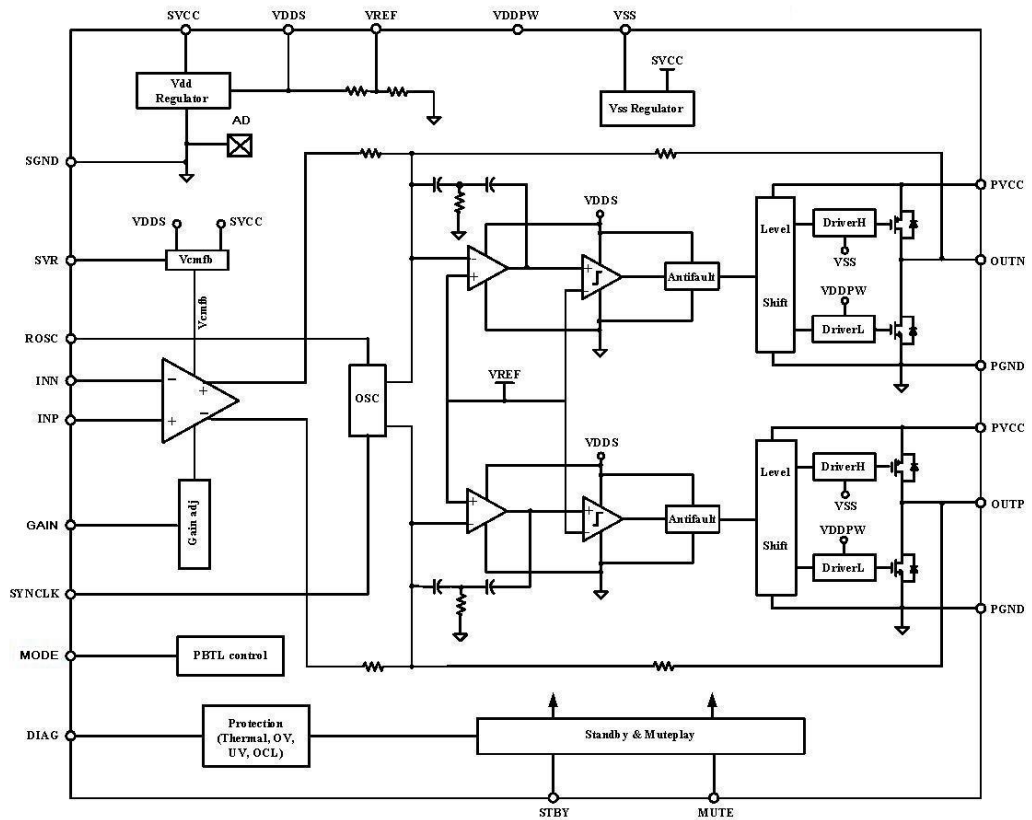
Device summary

| | |
|-----------------------------|------------------|
| Order code | TDA7498ETR |
| Operating temperature range | 0 to 70 °C |
| Package | PowerSSO36 (EPU) |
| Packing | Tape and reel |

1 Device block diagram

The figure below shows the block diagram of one of the two identical channels of the TDA7498E.

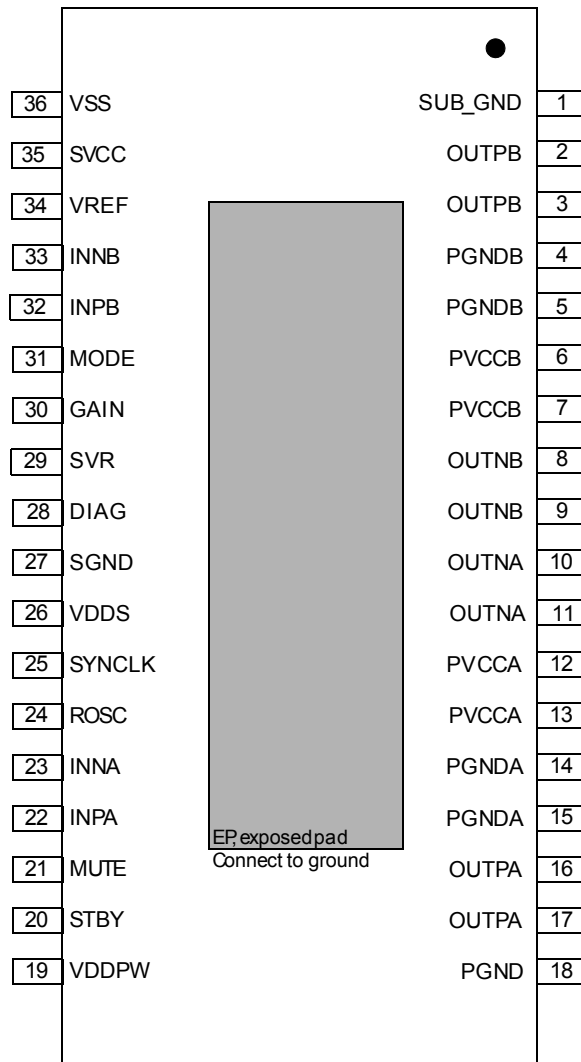
Figure 1. Internal block diagram (showing one channel only)



2 Pin description

2.1 Pinout

Figure 2. Pin connections (top view, PCB view)



2.2 Pin list

Table 1. Pin description list

| Number | Name | Type | Description |
|--------|---------|------|---|
| 1 | SUB_GND | PWR | Connect to the frame |
| 2,3 | OUTPB | O | Positive PWM for right channel |
| 4,5 | PGNDB | PWR | Power stage ground for right channel |
| 6,7 | PVCCB | PWR | Power supply for right channel |
| 8,9 | OUTNB | O | Negative PWM output for right channel |
| 10,11 | OUTNA | O | Negative PWM output for left channel |
| 12,13 | PVCCA | PWR | Power supply for left channel |
| 14,15 | PGNDA | PWR | Power stage ground for left channel |
| 16,17 | OUTPA | O | Positive PWM output for left channel |
| 18 | PGND | PWR | Power stage ground |
| 19 | VDDPW | O | 3.3-V (nominal) regulator output referred to ground for power stage |
| 20 | STBY | I | Standby mode control |
| 21 | MUTE | I | Mute mode control |
| 22 | INPA | I | Positive differential input of left channel |
| 23 | INNA | I | Negative differential input of left channel |
| 24 | ROSC | O | Master oscillator frequency-setting pin |
| 25 | SYNCLK | I/O | Clock in/out for external oscillator |
| 26 | VDDS | O | 3.3-V (nominal) regulator output referred to ground for signal blocks |
| 27 | SGND | PWR | Signal ground |
| 28 | DIAG | O | Open-drain diagnostic output |
| 29 | SVR | O | Supply voltage rejection |
| 30 | GAIN | I | Gain setting input |
| 31 | MODE | I | Enables stereo or mono BTL mode of operation |
| 32 | INPB | I | Positive differential input of right channel |
| 33 | INNB | I | Negative differential input of right channel |
| 34 | VREF | O | Half VDDS (nominal) referred to ground |
| 35 | SVCC | PWR | Signal power supply |
| 36 | VSS | O | 3.3-V (nominal) regulator output referred to power supply |
| - | EP | - | Exposed pad for heatsink, to be connected to ground |

3 Electrical specifications

3.1 Absolute maximum ratings

Table 2. Absolute maximum ratings

| Symbol | Parameter | Value | Unit |
|-----------|--|-------------|------|
| V_{CC} | DC supply voltage for pins PVCCA, PVCCB, SVCC | 45 | V |
| V_I | Voltage limits for input pins STBY, MUTE, INNA, INPA, INNB, INPB, GAIN, MODE | -0.3 to 4.0 | V |
| T_j | Operating junction temperature | 0 to 150 | °C |
| T_{op} | Operating ambient temperature | 0 to 70 | °C |
| T_{stg} | Storage temperature | -40 to 150 | °C |

3.2 Thermal data

Table 3. Thermal data

| Symbol | Parameter | Min. | Typ. | Max. | Unit |
|------------------|--------------------------------------|------|------|------|------|
| $R_{th\ j-case}$ | Thermal resistance, junction to case | - | 3.0 | | °C/W |

3.3 Recommended operating conditions

Table 4. Recommended operating conditions

| Symbol | Parameter | Min | Typ | Max | Unit |
|-----------|--|-----|-----|-----|------|
| V_{CC} | Supply voltage for pins PVCCA, PVCCB, SVCC | 14 | - | 39 | V |
| T_{amb} | Ambient operating temperature | 0 | - | 70 | °C |

3.4 Electrical specifications

Unless otherwise stated, the values in the table below are specified for the conditions: $V_{CC} = 36\text{ V}$, $R_L = 4\ \Omega$, $R_{OSC} = R_3 = 39\text{ k}\Omega$, $C_8 = 100\text{ nF}$, $f = 1\text{ kHz}$, $G_V = 23.6\text{ dB}$ $T_{amb} = 25\text{ °C}$.

Table 5. Electrical specifications

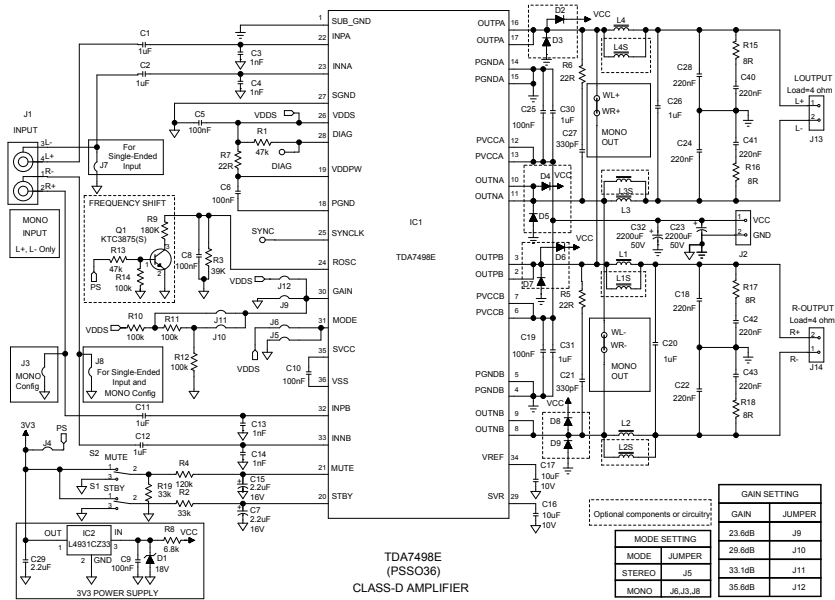
| Symbol | Parameter | Condition | Min. | Typ. | Max. | Unit |
|-------------|--|--|------|------|------|---------------|
| I_q | Total quiescent current | No LC filter, no load | - | 60 | | mA |
| I_{qSTBY} | Quiescent current in standby | - | - | 1 | | μA |
| V_{OS} | Output offset voltage | $V_i = 0$, $A_v = 23.6\text{ dB}$, no load | -20 | - | 20 | mV |
| I_{OCP} | Overcurrent protection threshold | $R_L = 0\ \Omega$ | 10 | 11 | 14 | A |
| T_j | Junction temperature at thermal shutdown | - | 140 | 150 | 160 | °C |
| R_i | Input resistance | Differential input | | 69 | - | k Ω |
| V_{UVP} | Undervoltage protection threshold | - | - | - | 8 | V |
| R_{dsON} | Power transistor on-resistance | High side | - | 0.15 | - | Ω |

| Symbol | Parameter | Condition | Min. | Typ. | Max. | Unit |
|----------------------------------|---|---|---------|------|------|------------------|
| (Continued) R _{dsON} | (Continued) Power transistor on-resistance | Low side | - | 0.15 | - | (Continued) Ω |
| P _o | Output power | THD = 10% | - | 160 | - | W |
| | | THD = 1% | - | 125 | - | |
| P _o | Parallel BTL (mono) output power, R _L = 3 ohm, V _{cc} = 36 V | THD = 10% | - | 220 | - | W |
| | | THD = 1% | - | 170 | - | |
| η | Efficiency | | - | 85 | - | % |
| THD | Total harmonic distortion | P _o = 1 W | - | 0.05 | - | % |
| G _V | Closed-loop gain | GAIN < 0.25*VDD | | 23.8 | | dB |
| | | 0.25*VDD < GAIN < 0.5*VDD | | 29.8 | | |
| | | 0.5*VDD < GAIN < 0.75*VDD | | 33.3 | | |
| | | GAIN > 0.75*VDD | | 35.8 | | |
| ΔG _V | Gain matching | - | -1 | - | 1 | dB |
| C _T | Crosstalk | f = 1 kHz, P _o = 1 W | 50 | 60 | - | dB |
| V _n | Total output noise | Inputs shorted and to ground, A Curve | | 231 | | μV |
| | | Inputs shorted and to ground, f = 20 Hz to 20 kHz | | 400 | | |
| SVRR | Supply voltage rejection ratio | fr = 100 Hz, Vr = 0.5 Vpp, C _{SVR} = 10 μF | - | 55 | - | dB |
| T _r , T _f | Rise and fall times | - | - | 35 | - | ns |
| f _{SW} | Switching frequency | Internal oscillator | 240 | 310 | 400 | kHz |
| f _{SWR} | Output switching frequency range | With internal oscillator by changing R _{OSC} ⁽¹⁾ | 240 | - | - | kHz |
| V _{inH} | Digital input high (H) | - | 2.0 | - | - | V |
| V _{inL} | Digital input low (L) | | - | - | 0.8 | |
| Function mode | Standby & mute & play | STBY < 0.5 V; MUTE = X | Standby | | | |
| | | STBY > 2.5 V; MUTE < L | Mute | | | |
| | | STBY > 2.5 V; MUTE > H | Play | | | |
| A _{MUTE} | Mute attenuation | V _{MUTE} < L, V _{STBY} = H | - | 75 | - | dB |

1. $f_{SW} = 10^6 / ((16 * R_{OSC} + 182) * 4)$ kHz, $f_{SYNCLK} = 2 * f_{SW}$ with R3 = 39 kΩ (see Figure 3. Test circuit stereo application and mono BTL mode).

3.5 Test circuit

Figure 3. Test circuit stereo application and mono BTL mode



4 Characterization curves

Unless otherwise stated the measurements were made under the following conditions:

$V_{CC} = 36\text{ V}$, $f = 1\text{ kHz}$, $G_V = 23.6\text{ dB}$, $R_{OSC} = 39\text{ k}\Omega$, $C_{OSC} = 100\text{ nF}$, $T_{amb} = 25\text{ }^\circ\text{C}$

4.1 For $R_L = 4\text{ }\Omega$, stereo configuration

Figure 4. Output power vs. supply voltage

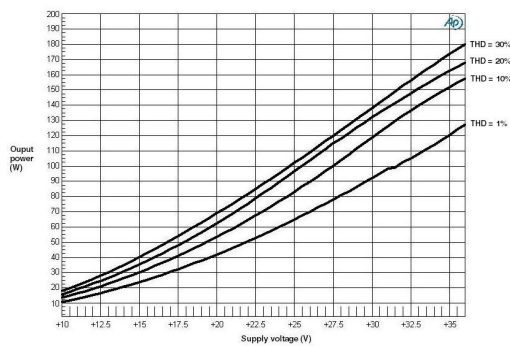


Figure 5. THD vs. output power

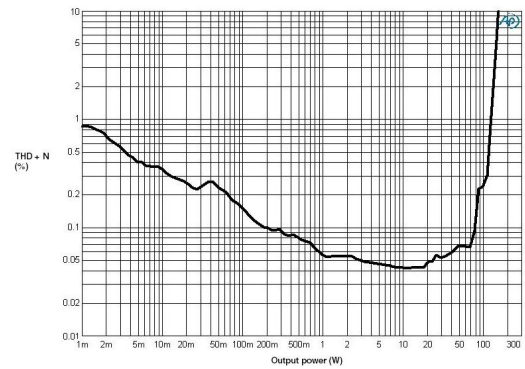


Figure 6. THD vs. frequency

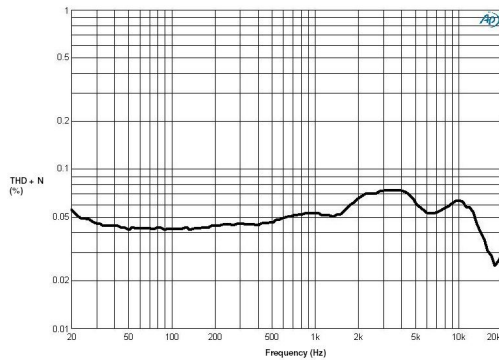


Figure 7. FFT performance

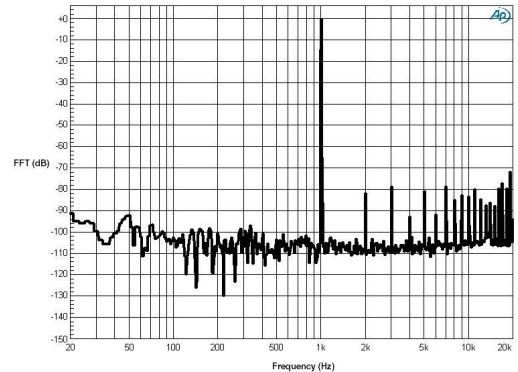
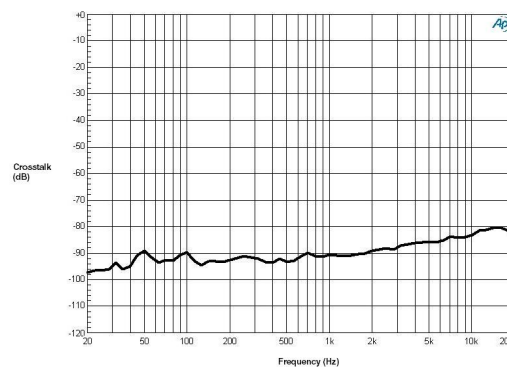


Figure 8. Crosstalk vs. frequency



4.2 For $R_L = 3 \Omega$, mono BTL configuration

Figure 9. Output power vs. supply voltage

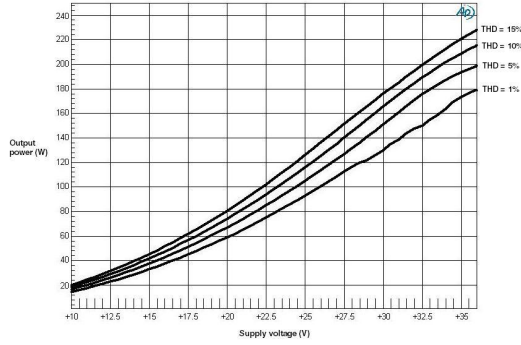


Figure 10. THD vs. output power

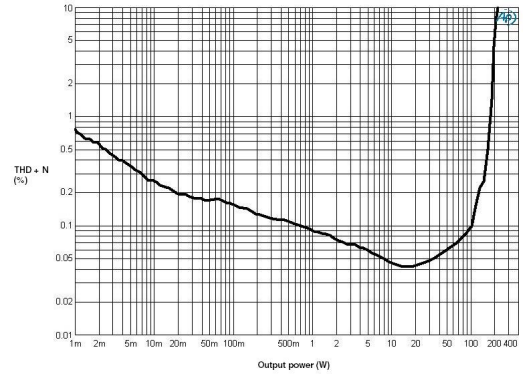
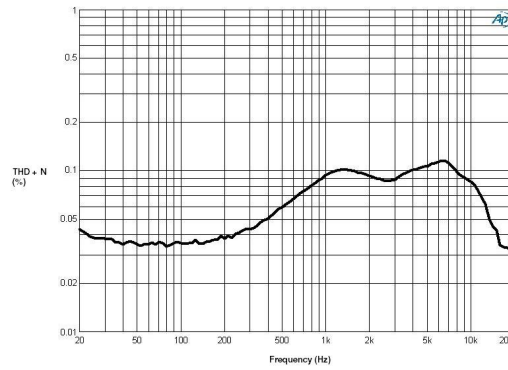


Figure 11. THD vs. frequency



5 Application information

5.1 Stereo and mono BTL operation selection using the MODE pin

The TDA7498E can be used in stereo applications or mono BTL applications. Connecting the MODE pin to the VDDS pin configures the device in mono BTL. The output of the two channels can be paralleled. When the MODE pin is connected to ground or floating (pulled down internally) the device works as a stereo amplifier.

5.2 Gain setting

The gain of the TDA7498E is set by GAIN (pin 30).

Table 6. Gain settings

| GAIN | Total gain | Application recommendation |
|--|------------|--------------------------------|
| $VGAIN < 0.25 \cdot VDDS$ | 23.6 dB | GAIN pin connected to SGND |
| $0.25 \cdot VDDS < VGAIN < 0.5 \cdot VDDS$ | 29.6 dB | Rc10 = Rc11 = Rc12 = 100 K max |
| $0.5 \cdot VDDS < VGAIN < 0.75 \cdot VDDS$ | 33.1 dB | Rc10 = Rc11 = Rc12 = 100 K max |
| $VGAIN > 0.75 \cdot VDDS$ | 35.6 dB | GAIN pin connected to VDDS |

5.3 Smart protection

The TDA7498E embeds an overcurrent protection circuitry to protect the device from unwanted current peaks. If the overcurrent protection threshold ([Table 5. Electrical specifications](#)) is exceeded, the power stage will be shut down immediately. The device will recover automatically once the fault is removed.

6 Package information

In order to meet environmental requirements, ST offers these devices in different grades of **ECOPACK** packages, depending on their level of environmental compliance. ECOPACK specifications, grade definitions and product status are available at: www.st.com. ECOPACK is an ST trademark.

6.1 PowerSSO-36 EPU package information

Figure 12. PowerSSO-36 EPU package outline

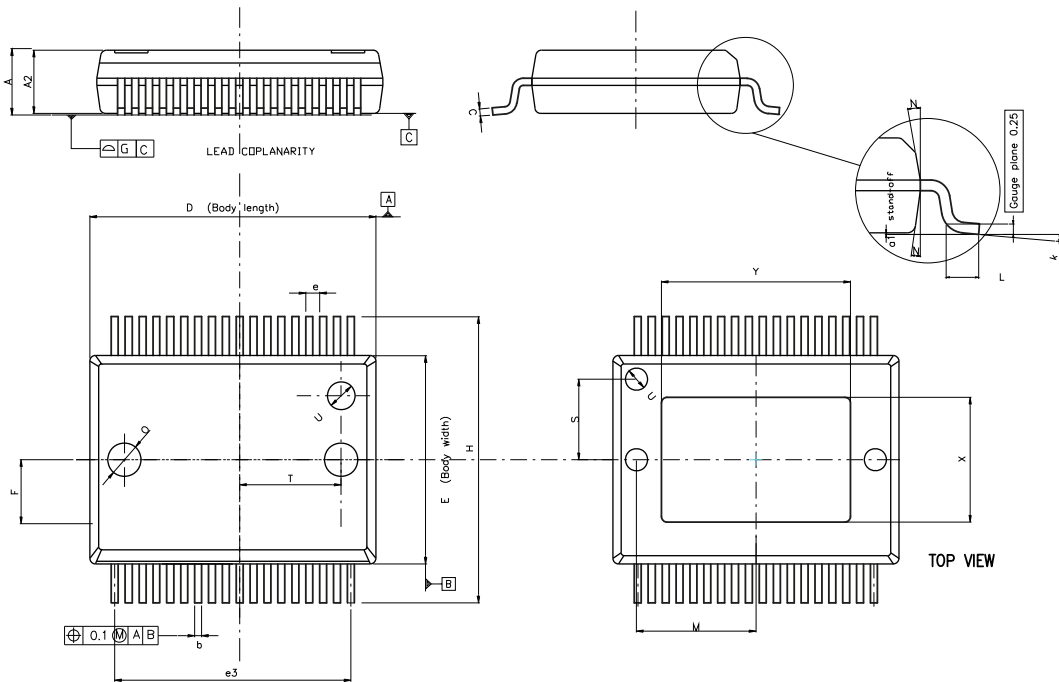


Table 7. PowerSSO-36 EPU package mechanical data

| Symbol | mm | | | inches | | |
|--------|-------|------|------------|--------|-------|------------|
| | Min. | Typ. | Max. | Min. | Typ. | Max. |
| A | 2.15 | - | 2.45 | 0.085 | - | 0.096 |
| A2 | 2.15 | - | 2.35 | 0.085 | - | 0.093 |
| a1 | 0 | - | 0.10 | 0 | - | 0.004 |
| b | 0.18 | - | 0.36 | 0.007 | - | 0.014 |
| c | 0.23 | - | 0.32 | 0.009 | - | 0.013 |
| D | 10.10 | - | 10.50 | 0.398 | - | 0.413 |
| E | 7.40 | - | 7.60 | 0.291 | - | 0.299 |
| e | - | 0.5 | - | - | 0.020 | - |
| e3 | - | 8.5 | - | - | 0.335 | - |
| F | - | 2.3 | - | - | 0.091 | - |
| G | - | - | 0.10 | - | - | 0.004 |
| H | 10.10 | - | 10.50 | 0.398 | - | 0.413 |
| h | - | - | 0.40 | - | - | 0.016 |
| k | 0 | - | 8 degrees | 0 | - | 8 degrees |
| L | 0.55 | - | 0.85 | 0.022 | - | 0.033 |
| M | - | 4.30 | - | - | 0.169 | - |
| N | - | - | 10 degrees | - | - | 10 degrees |
| O | - | 1.20 | - | - | 0.047 | - |
| Q | - | 0.80 | - | - | 0.031 | - |
| S | - | 2.90 | - | - | 0.114 | - |
| T | - | 3.65 | - | - | 0.144 | - |
| U | - | 1.00 | - | - | 0.039 | - |
| X | 4.10 | - | 4.70 | 0.161 | - | 0.185 |
| Y | 6.50 | - | 7.10 | 0.193 | - | 0.280 |

Revision history

Table 8. Document revision history

| Date | Revision | Changes |
|-------------|----------|---|
| 12-Dec-2011 | 1 | Initial release. |
| 16-Jun-2015 | 2 | Updated V_{CC} in Table 3: "Absolute maximum ratings" , updated Section 6.3: "Smart protection", and updated dimension L in Table 8: "PowerSSO-36 EPU package mechanical data". |
| 10-Dec-2018 | 3 | Updated device summary on the cover page. |
| 25-Jun-2020 | 4 | Updated Figure 12 and Y min. value in Table 7 |

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