TDA7440

TONE CONTROL
DIGITALLY CONTROLLED AUDIO PROCESSOR

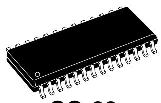
1 FEATURES

- INPUT MULTIPLEXER
  - 4 STEREO INPUTS
  - SELECTABLE INPUT GAIN FOR OPTIMAL ADAPTATION TO DIFFERENT SOURCES
- ONE STEREO OUTPUT
- TREBLE AND BASS CONTROL IN 2.0dB STEPS
- VOLUME CONTROL IN 1.0dB STEPS
- TWO SPEAKER ATTENUATORS:
  - TWO INDEPENDENT SPEAKER CONTROL IN 1.0dB STEPS FOR BALANCE FACILITY
  - INDEPENDENT MUTE FUNCTION
- ALL FUNCTION ARE PROGRAMMABLE VIA SERIAL BUS

2 DESCRIPTION

The TDA7440D is a volume tone (bass and treble) balance (Left/Right) processor for quality audio applications in Hi-Fi systems.

Figure 1. Package



SO-28

Table 1. Order Codes

Order code	Package
TDA7440D	SO-28
TDA7440D013TR	Tape & Reel

Selectable input gain is provided. Control of all the functions is accomplished by serial bus.

The AC signal setting is obtained by resistor networks and switches combined with operational amplifiers.

Thanks to the used BIPOLAR/CMOS Technology, Low Distortion, Low Noise and DC stepping are obtained

Figure 2. Block Diagram

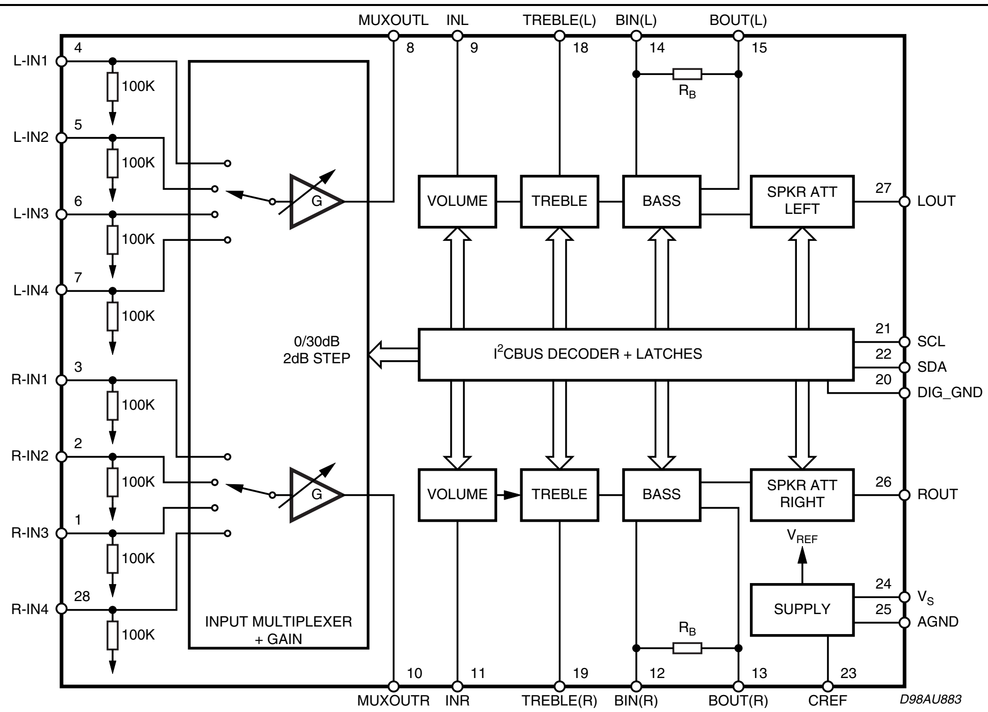


Figure 3. Pin Connection (Top view)

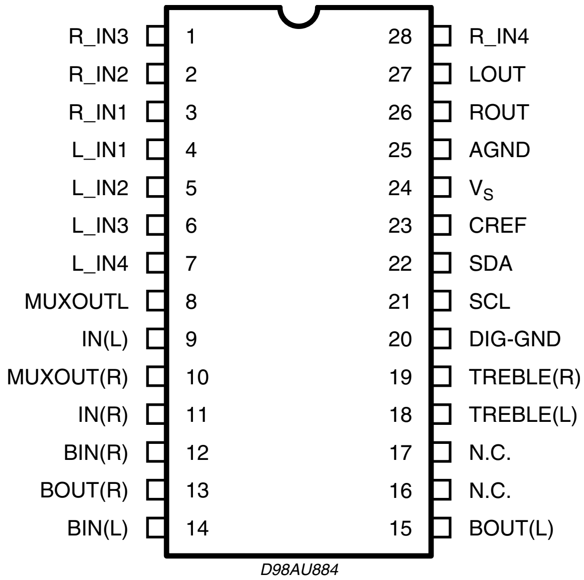


Table 2. Absolute Maximum Ratings

Symbol	Parameter	Value	Unit
V_S	Operating Supply Voltage	10.5	V
T_{amb}	Operating Ambient Temperature	0 to 70	°C
T_{stg}	Storage Temperature Range	-55 to 150	°C

Table 3. Thermal Data

Symbol	Parameter	Value	Unit
$R_{th\ j\text{-}pin}$	Thermal Resistance Junction-pins	85	°C/W

Table 4. Quick Reference Data

Symbol	Parameter	Min.	Typ.	Max.	Unit
V_S	Supply Voltage	6	9	10.2	V
V_{CL}	Max. input signal handling	2			Vrms
THD	Total Harmonic Distortion V = 1Vrms f = 1KHz	0.01	0.1	%	
S/N	Signal to Noise Ratio V_{out} = 1Vrms (mode = OFF)		106		dB
S_C	Channel Separation f = 1KHz		90		dB
	Input Gain in (2dB step)	0		30	dB
	Volume Control (1dB step)	-47		0	dB
	Treble Control (2dB step)	-14		+14	dB
	Bass Control (2dB step)	-14		+14	dB
	Balance Control 1dB step	-79		0	dB
	Mute Attenuation		100		dB

Table 5. Electrical Characteristcs

Refer to the test circuit T_{amb} = 25°C, V_S = 9V, R_L = 10KΩ, R_G = 600Ω, all controls flat (G = 0dB), unless otherwise specified.

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Unit
SUPPLY						
V_S	Supply Voltage		6	9	10.2	V
I_S	Supply Current		4	7	10	mA
SVR	Ripple Rejection		60	90		dB
INPUT STAGE						
R_{IN}	Input Resistance		70	100	130	KΩ
V_{CL}	Clipping Level	THD = 0.3%	2	2.5		Vrms
S_{IN}	Input Separation	The selected input is grounded through a 2.2μ capacitor	80	100		dB
G_{inmin}	Minimum Input Gain		-1	0	1	dB
G_{inman}	Maximum Input Gain		29	30	31	dB
G_{step}	Step Resolution		1.5	2	2.5	dB
VOLUME CONTROL						
R_i	Input Resistance		20	33	50	KΩ
C_{RANGE}	Control Range		45	47	49	dB
A_{VMAX}	Max. Attenuation		45	47	49	dB
A_{STEP}	Step Resolution		0.5	1	1.5	dB
E_A	Attenuation Set Error	A_V = 0 to -24dB	-1.0	0	1.0	dB
		A_V = -24 to -47dB	-1.5	0	1.5	dB
E_T	Tracking Error	A_V = 0 to -24dB		0	1	dB
		A_V = -24 to -47dB		0	2	dB
V_{DC}	DC Step	adjacent attenuation steps from 0dB to A_V max		0 0.5	3	mV mV
A_{mute}	Mute Attenuation		80	100		dB
BASS CONTROL (1)						
Gb	Control Range	Max. Boost/cut	+12.0	+14.0	+16.0	dB
B_{STEP}	Step Resolution		1	2	3	dB
R_B	Internal Feedback Resistance		33	44	55	KΩ
TREBLE CONTROL (1)						
Gt	Control Range	Max. Boost/cut	+13.0	+14.0	+15.0	dB
T_{STEP}	Step Resolution		1	2	3	dB
SPEAKER ATTENUATORS						
C_{RANGE}	Control Range		70	76	82	dB
S_{STEP}	Step Resolution		0.5	1	1.5	dB
E_A	Attenuation Set Error	A_V = 0 to -20dB	-1.5	0	1.5	dB
		A_V = -20 to -56dB	-2	0	2	dB
V_{DC}	DC Step	adjacent attenuation steps		0	3	mV
A_{mute}	Mute Attenuation		80	100		dB

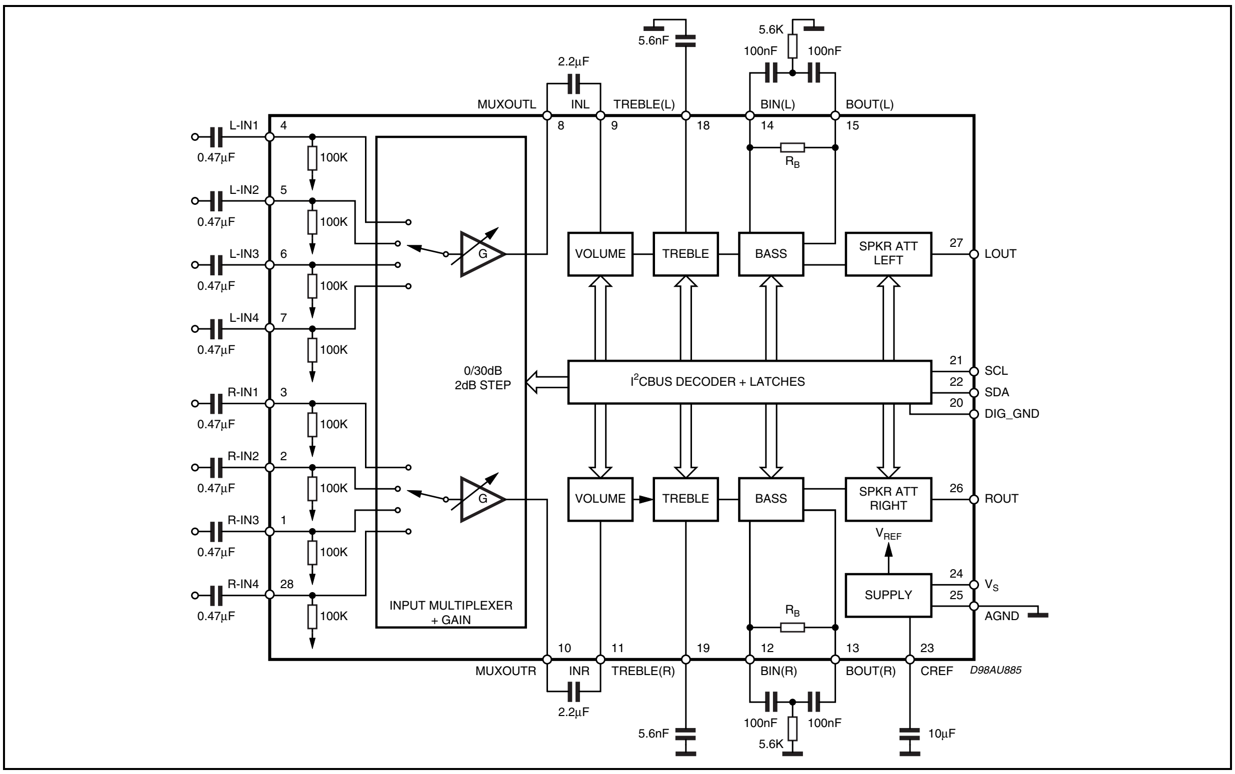
NOTE1:
1) The device is functionally good at Vs = 5V. a step down, on Vs, to 4V doesn't reset the device.
2) BASS and TREBLE response: The center frequency and the response quality can be chosen by the external circuitry.

Table 5. Electrical Characteristcs (continued)

Refer to the test circuit T_{amb} = 25°C, V_S = 9V, R_L = 10KΩ, R_G = 600Ω, all controls flat (G = 0dB), unless otherwise specified.

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Unit
AUDIO OUTPUTS						
V_{CLIP}	Clipping Level	d = 0.3%	2.1	2.6		Vrms
R_L	Output Load Resistance		2			KΩ
R_O	Output Impedance		10	30	50	Ω
V_{DC}	DC Voltage Level		3.5	3.8	4.1	V
GENERAL						
E_{NO}	Output Noise	All gains = 0dB;		5	15	µV
		BW = 20Hz to 20KHz flat				
E_t	Total Tracking Error	A_V = 0 to -24dB		0	1	dB
		A_V = -24 to -47dB		0	2	dB
S/N	Signal to Noise Ratio	All gains 0dB; V_O = 1Vrms	95	106		dB
S_C	Channel Separation Left/Right		80	100		dB
d	Distortion	A_V = 0; V_I = 1Vrms		0.01	0.08	%
BUS INPUT						
V_{IL}	Input Low Voltage				1	V
V_{IH}	Input High Voltage		3			V
I_{IN}	Input Current	V_{IN} = 0.4V	-5	0	5	µA
V_O	Output Voltage SDA Acknowledge	I_O = 1.6mA		0.4	0.8	V

Figure 4. Test Circuit



3 APPLICATION SUGGESTIONS

The first and the last stages are volume control blocks. The control range is 0 to -47dB (mute) for the first one, 0 to -79dB (mute) for the last one. Both of them have 1dB step resolution. The very high resolution allows the implementation of systems free from any noisy acoustical effect.

The TDA7440D audioprocessor provides 3 bands tones control.

3.1 Bass Stage

Several filter types can be implemented, connecting external components to the Bass IN and OUT pins.

The fig.5 refers to basic T Type Bandpass Filter starting from the filter component values (R1 internal and R2,C1,C2 external) the centre frequency Fc, the gain Av at max. boost and the filter Q factor are computed as follows:

$$F_C = \frac{1}{2 \cdot \pi \cdot \sqrt{R1 \cdot R2 \cdot C1 \cdot C2}}$$

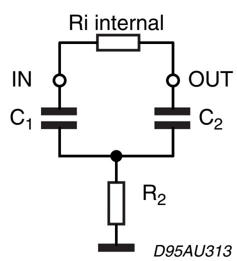
$$A_V = \frac{R2\ C2 + R2\ C1 + R_i\ C1}{R2\ C1 + R2\ C2}$$

$$Q = \frac{\sqrt{R1 \cdot R2 \cdot C1 \cdot C2}}{R2\ C1 + R2\ C2}$$

Viceversa, once Fc, Av, and Ri internal value are fixed, the external components values will be:

$$C1 = \frac{A_V - 1}{2 \cdot \pi \cdot F_C \cdot R_i \cdot Q} \qquad C2 = \frac{Q^2 \cdot C1}{A_V - 1 - Q^2} \qquad R2 = \frac{A_V - 1 - Q^2}{2 \cdot \pi \cdot C1 \cdot F_C \cdot (A_V - 1) \cdot Q}$$

Figure 5.



Treble Stage

The treble stage is a high pass filter whose time constant is fixed by an internal resistor (25KΩ typical) and an external capacitor connected between treble pins and ground.
Typical responses are reported in Figg. 14 to 17.

CREF

The suggested 10mF reference capacitor (CREF) value can be reduced to 4.7mF if the application requires faster power ON.

Figure 6. THD vs. frequency

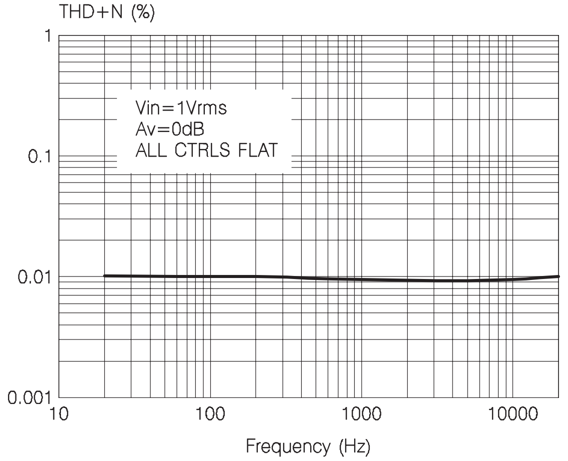


Figure 7. THD vs. R_{LOAD}

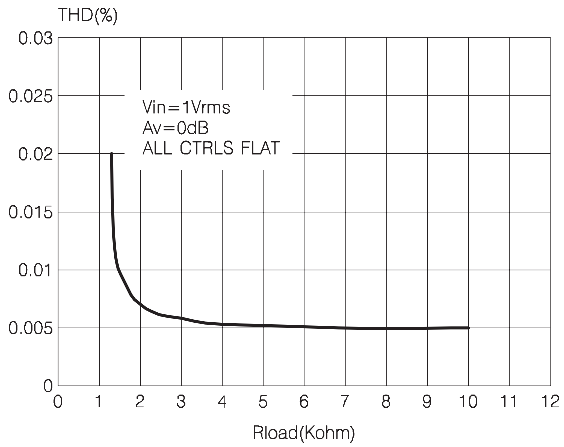


Figure 8. Channel separation vs. frequency

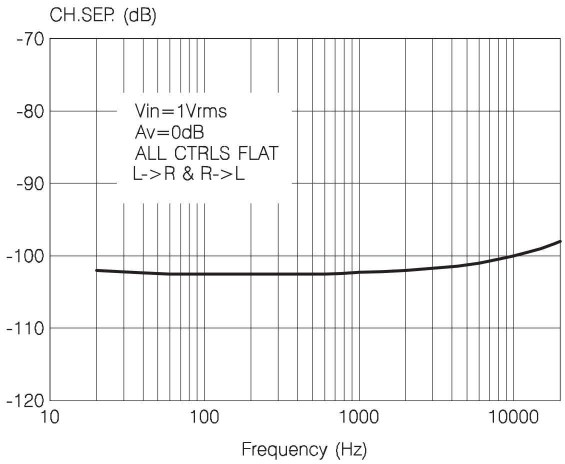


Figure 9. Bass response

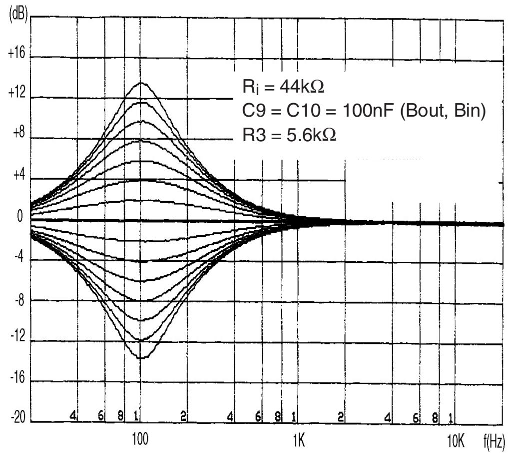
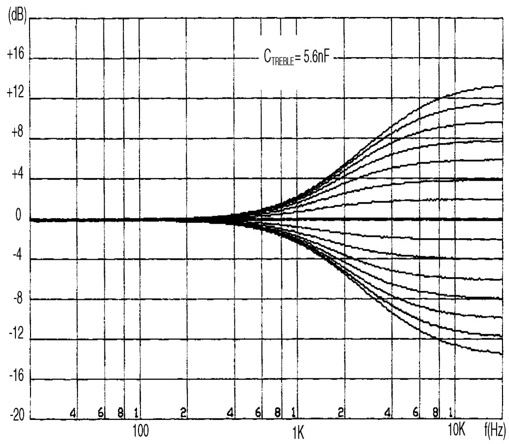


Figure 10. Treble responsey



4 I²C BUS INTERFACE

Data transmission from microprocessor to the TDA7440D and vice versa takes place through the 2 wires I²C BUS interface, consisting of the two lines SDA and SCL (pull-up resistors to positive supply voltage must be connected).

4.1 Data Validity

As shown in fig. 11, the data on the SDA line must be stable during the high period of the clock. The HIGH and LOW state of the data line can only change when the clock signal on the SCL line is LOW.

4.2 Start and Stop Conditions

As shown in fig. 12 a start condition is a HIGH to LOW transition of the SDA line while SCL is HIGH. The stop condition is a LOW to HIGH transition of the SDA line while SCL is HIGH.

4.3 Byte Format

Every byte transferred on the SDA line must contain 8 bits. Each byte must be followed by an acknowledge bit. The MSB is transferred first.

4.4 Acknowledge

The master (μP) puts a restive HIGH level on the SDA line during the acknowledge clock pulse (see fig. 13). The peripheral (audio processor) that acknowledges has to pull-down (LOW) the SDA line during this clock pulse.

The audio processor which has been addressed has to generate an acknowledge after the reception of each byte, otherwise the SDA line remains at the HIGH level during the ninth clock pulse time. In this case the master transmitter can generate the STOP information in order to abort the transfer.

4.5 Transmission without Acknowledge

Avoiding to detect the acknowledge of the audio processor, the μP can use a simpler transmission: simply it waits one clock without checking the slave acknowledging, and sends the new data.

This approach of course is less protected from misworking.

Figure 11. Data Validity on the I²CBUS

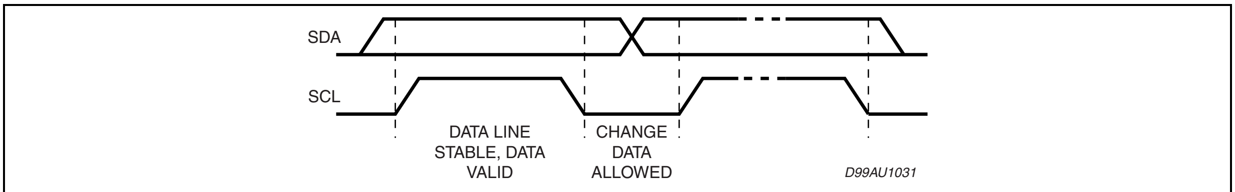


Figure 12. Timing Diagram of I²CBUS

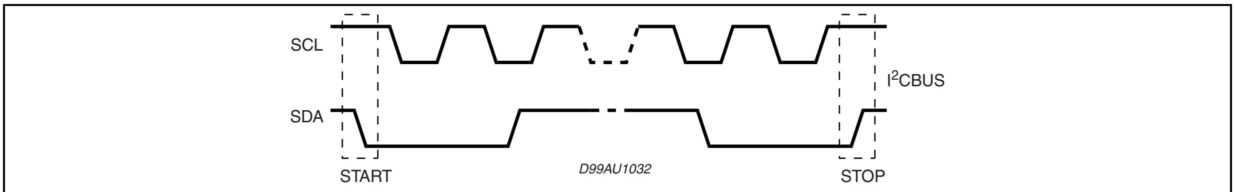
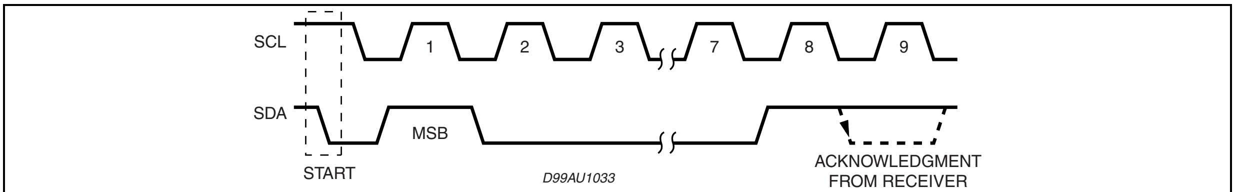


Figure 13. Acknowledge on the I²CBUS



5 SOFTWARE SPECIFICATION

Interface Protocol

The interface protocol comprises:

- A start condition (S)
- A chip address byte, containing the TDA7440D
- A subaddress bytes
- A sequence of data (N byte + acknowledge)
- A stop condition (P)

	CHIP ADDRESS									SUBADDRESS						DATA 1 to DATA n								
	MSB							LSB		MSB				LSB		MSB						LSB		
S	1	0	0	0	1	0	0	0	ACK	X	X	X	B	DATA	ACK				DATA				ACK	P

D96AU420

ACK = Acknowledge

S = Start

P = Stop

A = Address

B = Auto Increment

5.1 EXAMPLES

5.1.1 No Incremental Bus

The TDA7440D receives a start condition, the correct chip address, a subaddress with the B = 0 (no incremental bus), N-datas (all these data concern the subaddress selected), a stop condition.

	CHIP ADDRESS									SUBADDRESS									DATA								
	MSB							LSB		MSB							LSB		MSB						LSB		
S	1	0	0	0	1	0	0	0	ACK	X	X	X	0	D3	D2	D1	D0	ACK				DATA				ACK	P

D96AU421

5.1.2 Incremental Bus

The TDA7440D receive a start conditions, the correct chip address, a subaddress with the B = 1 (incremental bus): now it is in a loop condition with an autoincrease of the subaddress whereas SUBADDRESS from "XXX1000" to "XXX1111" of DATA are ignored.

The DATA 1 concern the subaddress sent, and the DATA 2 concerns the subaddress sent plus one sent in the loop etc, and at the end it receivers the stop condition.

	CHIP ADDRESS									SUBADDRESS									DATA 1 to DATA n								
	MSB							LSB		MSB							LSB		MSB						LSB		
S	1	0	0	0	1	0	0	0	ACK	X	X	X	1	D3	D2	D1	D0	ACK				DATA				ACK	P

D96AU422

5.2 POWER ON RESET CONDITION

Table 6.

INPUT SELECTION	IN2
INPUT GAIN	28dB
VOLUME	MUTE
BASS	0dB
TREBLE	2dB
SPEAKER	MUTE

5.3 DATA BYTES

Address = 88 HEX (ADDR:OPEN).

Table 7. FUNCTION SELECTION: First byte (subaddress)

MSB							LSB	SUBADDRESS
D7	D6	D5	D4	D3	D2	D1	D0	
X	X	X	B	0	0	0	0	INPUT SELECT
X	X	X	B	0	0	0	1	INPUT GAIN
X	X	X	B	0	0	1	0	VOLUME
X	X	X	B	0	0	1	1	BASS
X	X	X	B	0	1	0	0	NOT USED
X	X	X	B	0	1	0	1	TREBLE
X	X	X	B	0	1	1	0	SPEAKER ATTENUATE "R"
X	X	X	B	0	1	1	1	SPEAKER ATTENUATE "L"

B = 1: INCREMENTAL BUS ACTIVE
B = 0: NO INCREMENTAL BUS
X = DON'T CARE

In Incremental Bus Mode, the "not used" function must be addressed in any case. For example to refresh "Volume = 0dB" and Speaker_R = -40dB", the following bytes must be sent:

Table 8.

SUBADDRESS	XXX10010
VOLUME DATA	X0000000
BUS DATA	XXXX1111
NOT USED DATA	XXXX1111
TREBLE DATA	XXXX1111
SPEAKER_R DATA	X0000010

Table 9. INPUT SELECTION

MSB							LSB	INPUT MULTIPLEXER
D7	D6	D5	D4	D3	D2	D1	D0	
X	X	X	X	X	X	0	0	IN4
X	X	X	X	X	X	0	1	IN3
X	X	X	X	X	X	1	0	IN2
X	X	X	X	X	X	1	1	IN1

5.3 DATA BYTES (continued)

Table 10. INPUT GAIN SELECTION

MSB							LSB	INPUT GAIN
D7	D6	D5	D4	D3	D2	D1	D0	2dB STEPS
				0	0	0	0	0dB
				0	0	0	1	2dB
				0	0	1	0	4dB
				0	0	1	1	6dB
				0	1	0	0	8dB
				0	1	0	1	10dB
				0	1	1	0	12dB
				0	1	1	1	14dB
				1	0	0	0	16dB
				1	0	0	1	18dB
				1	0	1	0	20dB
				1	0	1	1	22dB
				1	1	0	0	24dB
				1	1	0	1	26dB
				1	1	1	0	28dB
				1	1	1	1	30dB

GAIN = 0 to 30dB

Table 11. VOLUME SELECTION

MSB							LSB	VOLUME
D7	D6	D5	D4	D3	D2	D1	D0	1dB STEPS
					0	0	0	0dB
					0	0	1	-1dB
					0	1	0	-2dB
					0	1	1	-3dB
					1	0	0	-4dB
					1	0	1	-5dB
					1	1	0	-6dB
					1	1	1	-7dB
	0	0	0	0				0dB
	0	0	0	1				-8dB
	0	0	1	0				-16dB
	0	0	1	1				-24dB
	0	1	0	0				-32dB
	0	1	0	1				-40dB
	X	1	1	1	X	X	X	MUTE

VOLUME = 0 to 47dB/MUTE

5.3 DATA BYTES (continued)

Table 12. BASS SELECTION

MSB							LSB	BASS
D7	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**	**2dB STEPS**
				0	0	0	0	-14dB
				0	0	0	1	-12dB
				0	0	1	0	-10dB
				0	0	1	1	-8dB
				0	1	0	0	-6dB
				0	1	0	1	-4dB
				0	1	1	0	-2dB
				0	1	1	1	0dB
				1	1	1	1	0dB
				1	1	1	0	2dB
				1	1	0	1	4dB
				1	1	0	0	6dB
				1	0	1	1	8dB
				1	0	1	0	10dB
				1	0	0	1	12dB
				1	0	0	0	14dB

Table 13. TREBLE SELECTION

MSB							LSB	TREBLE
D7	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**	**2dB STEPS**
				0	0	0	0	-14dB
				0	0	0	1	-12dB
				0	0	1	0	-10dB
				0	0	1	1	-8dB
				0	1	0	0	-6dB
				0	1	0	1	-4dB
				0	1	1	0	-2dB
				0	1	1	1	0dB
				1	1	1	1	0dB
				1	1	1	0	2dB
				1	1	0	1	4dB
				1	1	0	0	6dB
				1	0	1	1	8dB
				1	0	1	0	10dB
				1	0	0	1	12dB
				1	0	0	0	14dB

5.3 DATA BYTES (continued)

Table 14. SPEAKER ATTENUATE SELECTION

MSB						LSB	SPEAKER ATTENUATION
D7	D6	D5	D4	D3	D2	D1	D0	1dB
					0	0	0	0dB
					0	0	1	-1dB
					0	1	0	-2dB
					0	1	1	-3dB
					1	0	0	-4dB
					1	0	1	-5dB
					1	1	0	-6dB
					1	1	1	-7dB
	0	0	0	0				0dB
	0	0	0	1				-8dB
	0	0	1	0				-16dB
	0	0	1	1				-24dB
	0	1	0	0				-32dB
	0	1	0	1				-40dB
	0	1	1	0				-48dB
	0	1	1	1				-56dB
	1	0	0	0				-64dB
	1	0	0	1				-72dB
	1	1	1	1	X	X	X	MUTE

Figure 14. PINS: 23

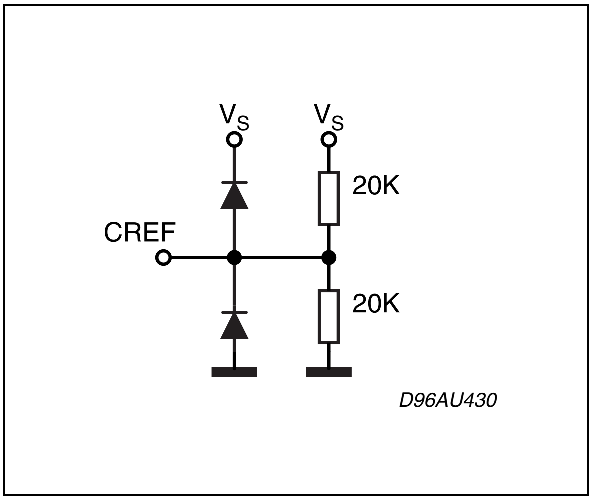


Figure 15. PINS: 26, 27

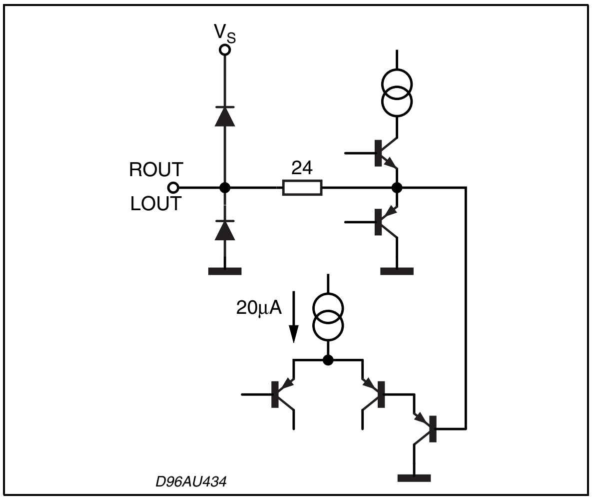


Figure 16. PINS: 1, 2, 3, 4, 5, 6, 7, 28

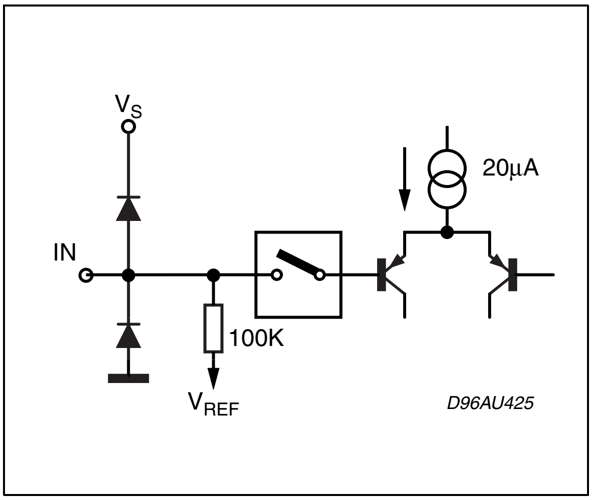


Figure 17. PINS: 8, 10

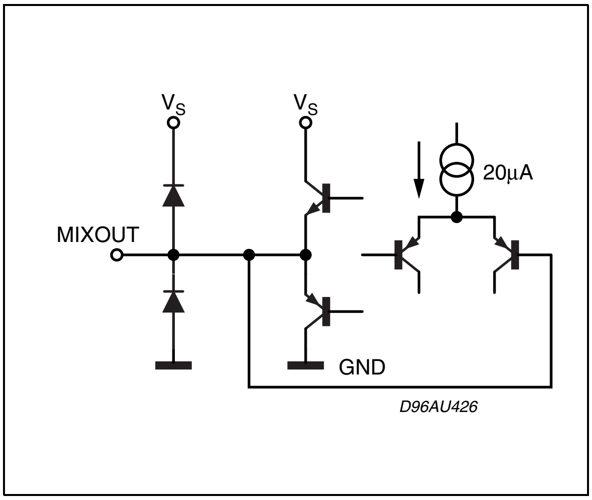


Figure 18. PINS: 19, 11

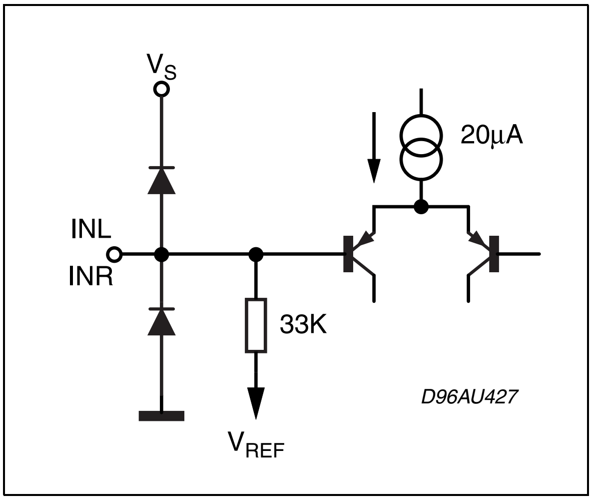


Figure 19. PINS: 12, 14

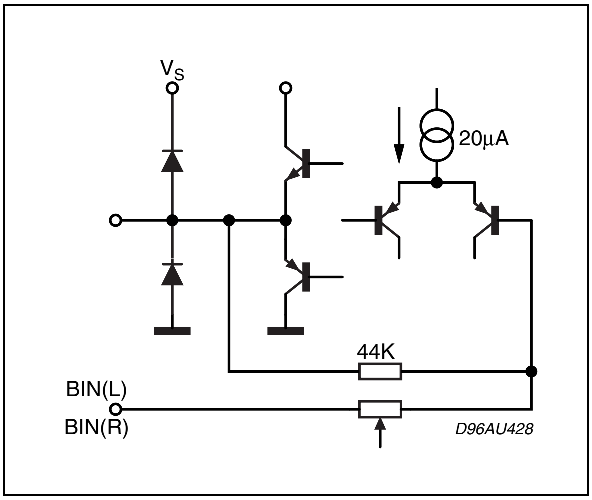


Figure 20. PINS: 13, 15

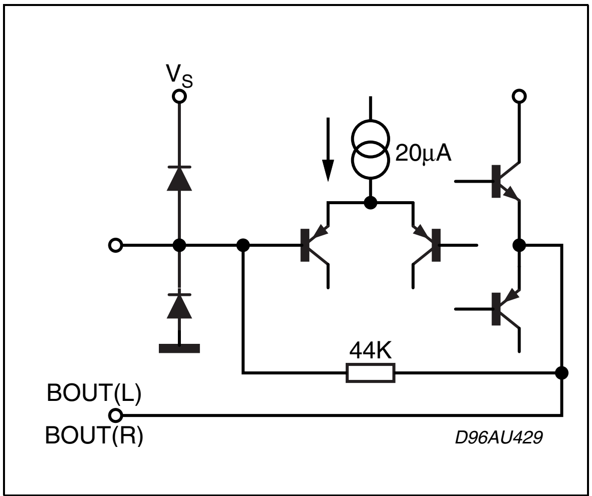


Figure 22. PIN: 20

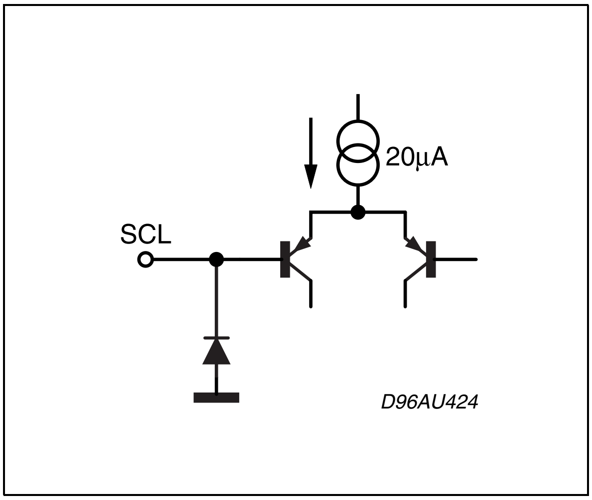


Figure 21. PINS: 18, 19

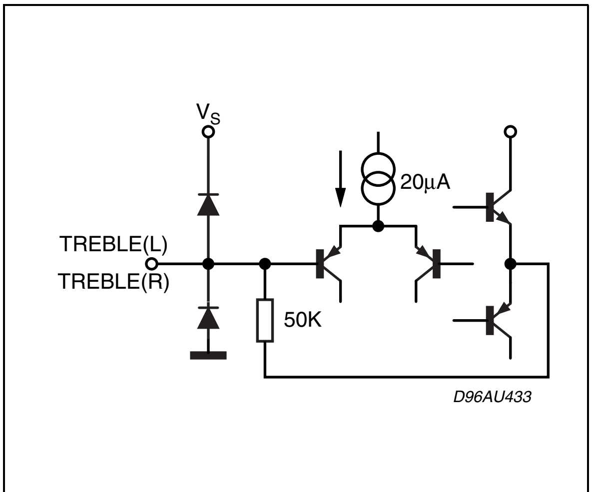
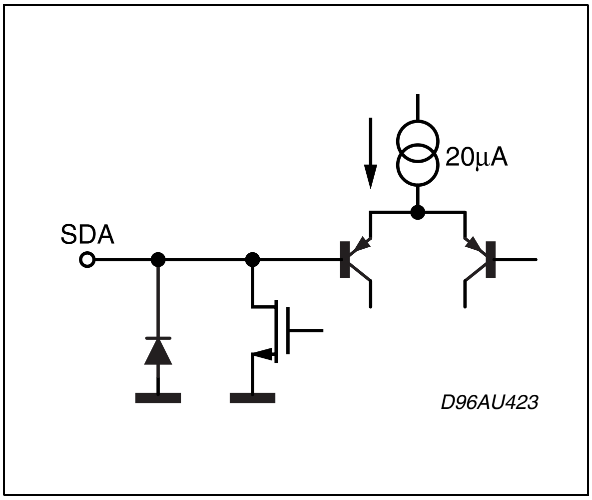


Figure 23. PIN 21



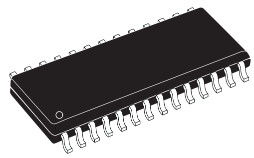
6 PACKAGE MECHANICAL DATA

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: www.st.com. ECOPACK® is an ST trademark.

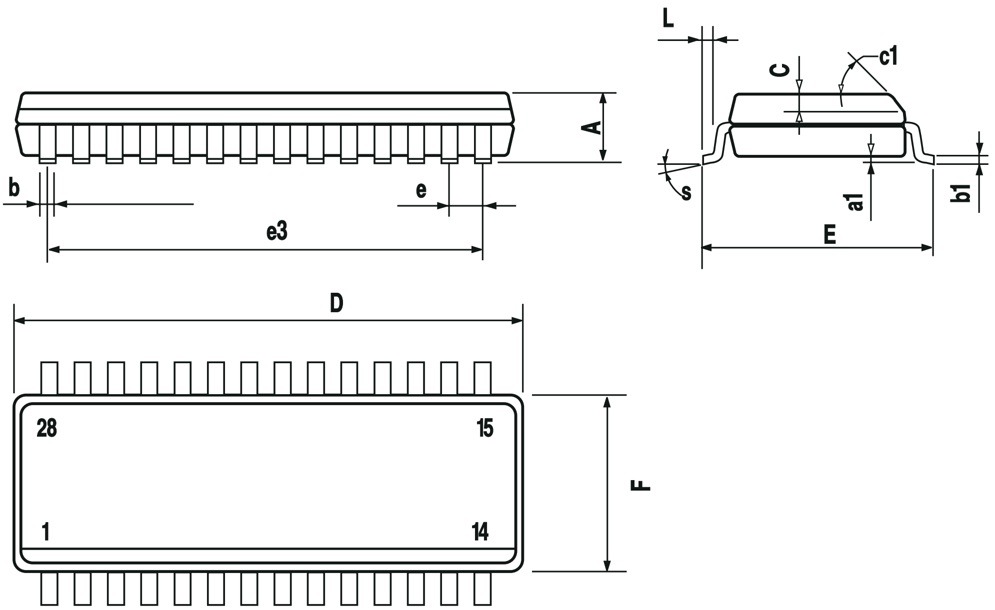
Figure 24. SO-28 Mechanical Data & Package Dimensions

DIM.	mm			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A			2.65			0.104
a1	0.1		0.3	0.004		0.012
b	0.35		0.49	0.014		0.019
b1	0.23		0.32	0.009		0.013
C		0.5			0.020	
c1	45° (typ.)					
D	17.7		18.1	0.697		0.713
E	10		10.65	0.394		0.419
e		1.27			0.050	
e3		16.51			0.65	
F	7.4		7.6	0.291		0.299
L	0.4		1.27	0.016		0.050
S	8 ° (max.)					

OUTLINE AND MECHANICAL DATA



SO-28



7 REVISION HISTORY

Table 15. Revision History

Date	Revision	Description of Changes
January 2004	2	First Issue
June 2004	3	Modified the style-sheet in compliance with the last revision of the “Corporate Technical Pubblications Design Guide”.
30-Apr-2010	4	Updated title and added environmental compliance statement for package