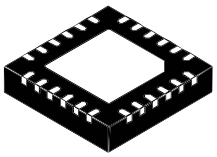
STUSB1702

Datasheet

USB Type-C™ source controller with TX/RX line driver and BMC



Maturity status link
STUSB1702

Device summary	
Order code	STUSB1702YQTR
AEC-Q100	Yes
Package	QFN24 EP 4x4 mm wettable flanks
Temp. range	- 40 °C up to 105 °C
Marking	1702Y

Features

- Type-C™ attach and cable orientation detection
- Power role support: source
- Integrated power switch for V_{CONN} supply:
  - programmable current limit up to 600 mA
  - overcurrent, overvoltage, and thermal protection
  - undervoltage lockout
- I²C interface and interrupt
- Integrated V_{BUS} voltage monitoring
- Integrated V_{BUS} and V_{CONN} discharge path
- Integrated BMC transceiver
- V_{BUS} switch gate driver
- Short-to-V_{BUS} protection on CC pins (22 V) and V_{BUS} pins (28 V)
- Accessory mode support
- Dual power supply (V_{SYS} and/or V_{DD}):
  - V_{SYS} = [3.0 V; 5.5 V]
  - V_{DD} = [4.1 V; 22 V]
- Temperature range: -40 °C up to 105 °C
- ESD: 4 kV HBM - 1.5 kV CDM
- AEC-Q100 qualified
- Compliant with:
  - USB Type-C™ rev 1.2
  - USB PD rev 2.0
- Compatible with:
  - USB PD rev 3.0

Applications

- Car charger, car infotainment
- Smart plugs, wall adapters, and chargers
- Power hubs and docking stations
- Any Type-C source device

Description

The STUSB1702 is a generic IC, in a 20 V technology it addresses a USB Type-C™ port management on the host side. It is designed for a broad range of applications and can handle the following USB Type-C functions: attach detection, plug orientation detection, host to device connection, V_{CONN} support, and V_{BUS} configuration.

It also provides a USB PD TX/RX line driver and BMC (bi-phase mark coding) transceiver which allow USB PD negotiation and an alternate mode through an external MCU.

1 Functional description

The STUSB1702 is a USB Type-C controller IC. It is designed to interface with the Type-C receptacle on host side. It is used to establish and manage the source-to-sink connection between two USB Type-C host and device ports.

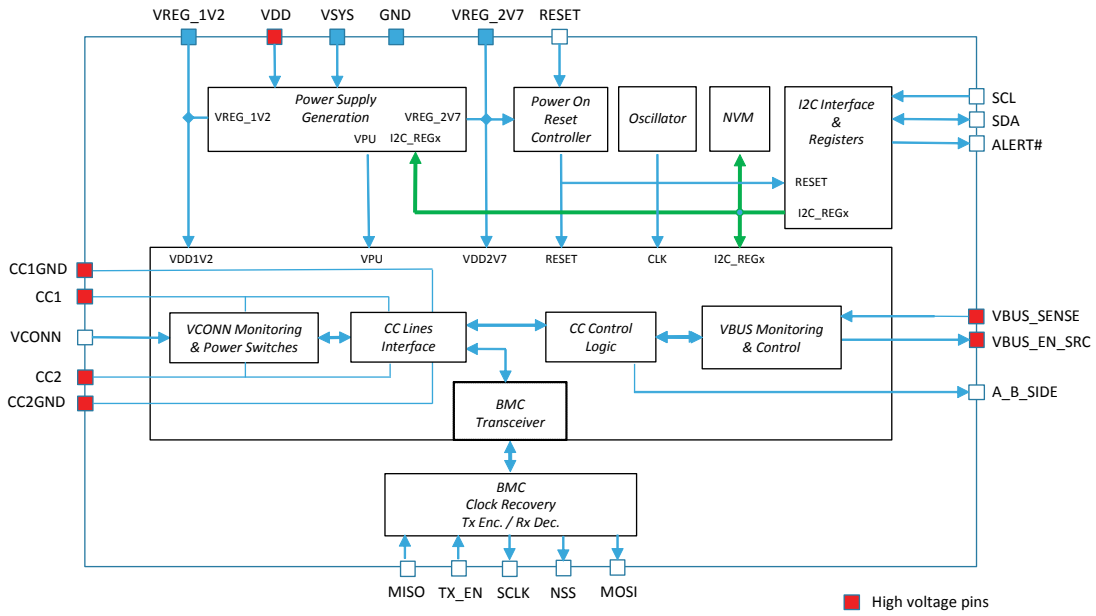
The STUSB1702 major role is to:

1. Detect the connection between two USB Type-C ports (attach detection)
2. Establish a valid source-to-sink connection
3. Determine the attached device mode
4. Resolve cable orientation and twist connections to establish USB data routing (MUX control)
5. Configure and monitor V_{BUS} power path
6. Manage V_{BUS} power capability: USB default, Type-C medium or Type-C high current mode
7. Configure V_{CONN} when required
8. Support USB PD negotiation

The STUSB1702 also provides:

- Low power standby mode
- I²C interface and interrupt
- Start-up configuration customization: static through NVM and/or dynamic through I²C
- High voltage protection
- Accessory mode detection

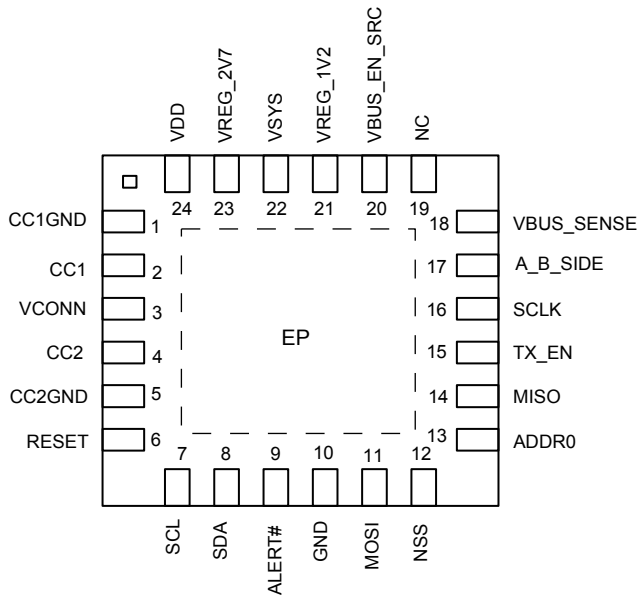
Figure 1. Functional block diagram



2 Inputs / outputs

2.1 Pinout

Figure 2. **STUSB1702 pin connections**



2.2 Pin list

Table 1. **Pin functions list**

Pin	Name	Type	Description	Typical connection
1	CC1GND	GND	Ground reference channel 1	Ground
2	CC1	HV AIO	Type-C configuration channel 1	Type-C receptacle A5
3	VCONN	PWR	Power input for active plug	5 V power source
4	CC2	HV AIO	Type-C configuration channel 2	Type-C receptacle B5
5	CC2GND	GND	Ground reference channel 2	Ground
6	RESET	DI	Reset input (active high)	
7	SCL	DI	I²C clock input	To I²C master, ext. pull-up
8	SDA	DI/OD	I²C data input/output, active low open drain	To I²C master, ext. pull-up
9	ALERT#	OD	I²C interrupt, active low open drain	To I²C master, ext. pull-up
10	GND	GND	Ground	Ground
11	MOSI	DO	Master out slave in: serial data from STUSB1702 to MCU, BMC decoded from connected CC line	To MCU, ext. pull-up referenced to MCU Vio
12	NSS	OD	Chip select, open drain active low to control MCU SPI/MSP interface	To MCU, ext. pull-up referenced to MCU Vio

Pin	Name	Type	Description	Typical connection
13	ADDR0	DI	I²C device address setting (see Section 5 I²C interface)	Static
14	MISO	DI	Master in slave out: serial data from MCU to STUSB1702 encoded in BMC to drive the CC line	From MCU, ext. pull-up referenced to MCU Vio
15	TX_EN	DI	TX enable, open drain active high to drive CC line from the embedded BMC interface	From MCU, needs to be maintained low by MCU or pulled down when receiving standby
16	SCLK	DO	Serial clock to clock data transfer between MCU and the STUSB1702. Open drain output pin, needs external pull-up referenced to MCU Vio	To MCU, ext. pull-up referenced to MCU Vio
17	A_B_SIDE	OD	Cable orientation, active low open drain	USB super speed MUX select, ext. pull-up
18	VBUS_SENSE	HV AI	V_{BUS} voltage monitoring and discharge path	From V_{BUS}
19	NC	HV AIO	Not connected	Open
20	VBUS_EN_SRC	HV AIO	V_{BUS} source power path enable, active low open drain	To switch or power system, ext. pull-up
21	VREG_1V2	PWR	1.2 V internal regulator output	1 µF typ. decoupling capacitor
22	VSYS	PWR	Power supply from system	From power system, connect to ground if not used
23	VREG_2V7	PWR	2.7 V internal regulator output	1 µF typ. decoupling capacitor
24	VDD	HV PWR	Main power supply from USB power line	From V_{BUS}
-	EP	GND	Exposed pad is connected to ground	To ground

Table 2. Pin function descriptions

Type	Description
D	Digital
A	Analog
O	Output pad
I	Input pad
IO	Bidirectional pad
OD	Open drain output
PD	Pull-down
PU	Pull-up
HV	High voltage
PWR	Power
GND	Ground

2.3 Pin description

2.3.1 CC1 / CC2

CC1 and CC2 are the configuration channel pins used for connection and attachment detection, plug orientation determination and system configuration management across USB Type-C cable.

2.3.2 CC1GND / CC2GND

CC1GND and CC2GND are used as a reference to ground and must be connected to ground.

2.3.3 VCONN

This power input is connected to a power source that can be a 5 V power supply. It is used to provide power to the local plug. It is internally connected to power switches that are protected against short-circuit and overvoltage. This does not require any protection on the input side. When a valid source-to-sink connection is determined and the V_{CONN} power switches are enabled, V_{CONN} is provided by the source to the unused CC pin (see Section 3.4 V_{CONN} supply).

2.3.4 RESET

Active high reset.

2.3.5 I²C interface pins

Table 3. I²C interface pins list

Name	Description
SCL	I²C clock – need external pull-up
SDA	I²C data – need external pull-up
ALERT#	I²C interrupt – need external pull-up
ADDR0	I²C device address bit (see Section 5 I²C interface)

2.3.6 GND

Ground.

2.3.7 MOSI

Master out slave in: data from the connected CC line are decoded using the BMC and then transmitted via the STUSB1702 to the MCU. Data are valid on the falling edge of the SCLK line and must be sampled by the MCU on this edge.

2.3.8 NSS

The chip select signal is driven by the STUSB1702 and is connected to the MCU. It activates the SPI/MSP interface transfer. The NSS signal drives the MCU so that:

- When TX_EN is asserted (TX mode), the STUSB1702 transmits data from the MCU over the CC line. Note, the MCU must provide data to be encoded on the MISO line which must be in synchrony with the SCLK
- When TX_EN is not asserted (RX mode, default), the CC line is activity detected, data are received, and the BMC is decoded by the STUSB1702. Decoded data are sent on the MOSI line in synchrony with the SCLK

2.3.9 MISO

Master in slave out: data from the MCU are encoded using the BMC and then transmitted via the STUSB1702 to the connected CC line driver. Data are sampled by the STUSB1702 on the rising edge of the SCLK line and must be stable on this edge.

2.3.10 TX_EN

TX_EN is a control signal from the MCU to the STUSB1702. It enables the BMC control logic that transfers data from the MCU serial interface, encodes it in BMC format, and drives the connected CC line.

Note: TX mode overrides RX mode.

2.3.11 SCLK

The serial clock signal from the STUSB1702 drives the SPI/MSP interface of the MCU and the clock data on the MISO and MOSI pins.

2.3.12 A_B_SIDE

This output pin provides cable orientation. It is used to establish USB SuperSpeed signal routing. The cable orientation is also provided by an internal I²C register. This signal is not required in the case of USB 2.0 support.

Table 4. USB data MUX select

Value	CC pin position
HiZ	CC1 pin is attached to CC line
0	CC2 pin is attached to CC line

2.3.13 VBUS_SENSE

This input pin is used to sense V_{BUS} presence, monitor V_{BUS} voltage and discharge V_{BUS} on USB Type-C receptacle side.

2.3.14 VBUS_EN_SRC

In source power role, this pin allows the outgoing V_{BUS} power to be enabled when the connection to a sink is established and V_{BUS} is in a valid operating range. The open drain output allows a PMOS transistor to be directly driven. The logic value of the pin is also advertised in a dedicated I²C register bit.

2.3.15 VREG_1V2

This pin is used only for external decoupling of 1.2 V internal regulator. The recommended decoupling capacitor is: 1 µF typ. (0.5 µF min.; 10 µF max.).

2.3.16 VSYS

This is the low power supply of the system, if there is any. It can be connected directly to a system power supply delivering 3.3 V or 5 V. It is recommended to connect this pin to ground when it is not used.

2.3.17 VREG_2V7

This pin is used for external decoupling of the 2.7 V internal regulator. The recommended decoupling capacitor is: 1 µF typ. (0.5 µF min., 10 µF max.).

2.3.18 VDD

This is the power supply from the USB power line for applications powered by V_{BUS}.

In source power role, this pin can be used to sense the voltage level of the main power supply providing the V_{BUS}. It allows UVLO and OVLO thresholds to be considered independently on the VDD pin as additional conditions to enable the V_{BUS} power path through the VBUS_EN_SRC pin (see Section 3.3.3 V_{BUS} power path assertion). When the UVLO threshold detection is enabled, the VDD pin must be connected to the main power supply to establish the connection and to assert the V_{BUS} power path.

3 General description

3.1 CC interface

The STUSB1702 controls the connection to the configuration channel (CC) pins, CC1 and CC2, through two main blocks: the CC line interface block and the CC control logic block.

The CC line interface block is used to:

- Configure termination mode on the CC pins relative to the power mode supported i.e. pull-up for source power role
- Monitor the CC pin voltage values relative to the attachment detection thresholds
- Configure V_{CONN} on the unconnected CC pin when required
- Protect the CC pins against overvoltage

The CC control logic block is used to:

- Execute the Type-C FSM relative to the Type-C power mode supported
- Determine the electrical state for each CC pin relative to the detected thresholds
- Evaluate the conditions relative to the CC pin states and the V_{BUS} voltage value to transition from one state to another in the Type-C FSM
- Detect and establish a valid source-to-sink connection
- Determine the attached device mode
- Determine cable orientation to allow external routing of the USB data
- Manage V_{BUS} power capability: USB default, Type-C medium or Type-C high current mode
- Handle hardware faults

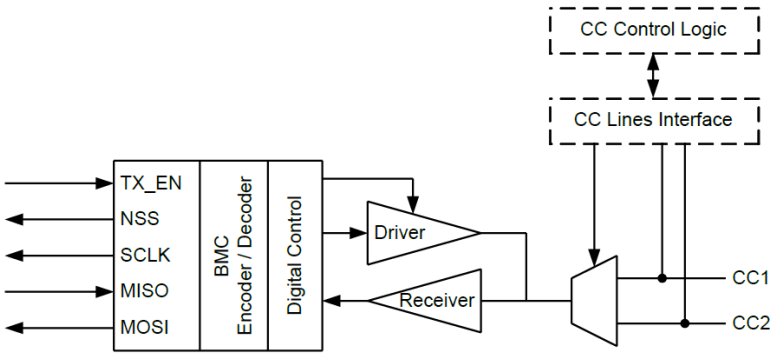
The CC control logic block implements the Type-C FSMs corresponding to the following Type-C power modes:

- Source power role with accessory support

The default Type-C power mode is selected through NVM programming (see Section 6 Start-up configuration) and can be changed by software during operation through the I²C interface.

3.2 BMC interface

Figure 3. BMC interface



3.2.1 BMC interface behavior

When a connection is established on the STUSB1702 (any attached state), the CC line used for connection is also internally connected to BMC block which allows the communication on this line.

The CC line is primary managed by CC control logic. BMC communication on the CC line must not interact with this control logic, as driving times of the line are short and are related to denounce times of the CC logic.

BMC block handles BMC encoding and decoding. It also handles CC line activity detection, discharging the external MCU of such operations.

The default state of the BMC block is to listen to the line (RX mode). TX mode is enabled only by assertion of the TX_EN signal via the external MCU.

3.2.2 TX mode

When the TX_EN signal is asserted via MCU, BMC block goes to the TX state:

- NSS signal is driven low, indicating to the SPI/MSP slave interface of the MCU that data are being transmitted on the CC line. MCU provides the data
- The STUSB1702 drives the NSS signal low, informing SPI/MSP slave interface of the MCU that data are requested on the MISO line
- The STUSB1702 clocks the SCLK signal
- MCU presents data to be transmitted on the MISO line and data are sampled on the rising edge of SCLK (data must be stable on this edge)
- Sampled data (from MISO line) are encoded by the BMC, and the resulting values drive the CC line according to USB PD standard

When all data are transmitted, MCU drives the TX_EN pin low, and lists the end of transmission. The STUSB1702 ends transmission with a corresponding trailing edge termination. It then goes back into to default state and releases the CC line from the BMC driver to the pull-up/pull-down CC line interfaces.

3.2.3 RX mode

RX mode is the default state of the BMC interface.

In this mode, the receiver listens to the connected CC line. It does not interface with the CC line interfaces or the CC control logic.

When all data are detected and received on the CC line, according to the activity described in the USB Power Delivery Standard, the BMC interface:

- Drives NSS signal low
- Outputs the clock on the SCLK signal which is recovered from the BMC signal
- Outputs recovered data (from the BMC signal) on the MOSI line to the connected MCU. Data are valid on the SCLK falling edge and are sampled on this edge by the SPI/MSP interface of MCU

When no more data are detected on the CC line, the NSS goes back to “high” which is its default state. This informs the MCU that no more activity is present on the bus.

3.3 VBUS power path control

3.3.1 VBUS monitoring

The V_{BUS} monitoring block supervises from the VBUS_SENSE pin the V_{BUS} voltage on the USB Type-C receptacle side.

It is used to check that the V_{BUS} is within a valid voltage range:

- To establish a valid source-to-sink connection according to USB Type-C standard specifications
- To safely enable the VBUS power path through the VBUS_EN_SRC pin

It allows detection of unexpected V_{BUS} voltage conditions such as undervoltage or overvoltage relative to the valid V_{BUS} voltage range. When such conditions occur, the STUSB1702 reacts as follows:

- At attachment, it prevents the source-to-sink connection and the V_{BUS} power path assertion
- After attachment, it deactivates the source-to-sink connection and disables the V_{BUS} power path. In source power role, the device goes into error recovery state.

The V_{BUS} voltage value is adjusted automatically at attachment (vSafe5V) and via MCU at each PDO transition. Monitoring is then disabled during T_PDO_transition (i.e. the default value of 300 ms is changed through NVM programming). Additionally, if a transition occurs to a lower voltage, the discharge path is activated during this time.

The valid V_{BUS} voltage range is defined from the V_{BUS} nominal voltage by a high threshold voltage and a low threshold voltage whose nominal values are respectively V_{BUS} +5% and V_{BUS} -5%. The nominal threshold limits can be shifted by a fraction of V_{BUS} from +1% to +15% for the high threshold voltage and from -1% to -15% for the low threshold voltage. This means the threshold limits can vary from V_{BUS} +5% to V_{BUS} +20% for the high limit and from V_{BUS}-5% to V_{BUS} -20% for the low limit.

The threshold limits are preset by default in NVM (see Section 8.3 Electrical and timing characteristics). The threshold limits can be changed independently through NVM programming (see Section 6 Start-up configuration) and also by software during attachment through the I²C interface.

3.3.2 VBUS discharge

The monitoring block also handles the internal V_{BUS} discharge path connected to the VBUS_SENSE pin. The discharge path is activated at detachment, or when the device goes into the error recovery state whatever the power role (see Section 3.6 Hardware fault management).

The V_{BUS} discharge path is enabled by default in NVM and can be disabled through NVM programming only (see Section 6 Start-up configuration). The discharge time duration is also preset by default in NVM (see Section 8.3 Electrical and timing characteristics). The discharge time duration can be changed through NVM programming (see Section 6 Start-up configuration) and also by software through the I²C interface.

3.3.3 VBUS power path assertion

The STUSB1702 can control the assertion of the V_{BUS} power path on the USB Type-C port, directly or indirectly, through the VBUS_EN_SRC pin.

The tables below summarize the configurations of the STUSB1702 and the operation conditions that determine the electrical value of the VBUS_EN_SRC pin during system operations.

Table 5. Conditions for V_{BUS} power path assertion in source power role

Pin	Electrical value	Operation conditions			Comment
		Type-C attached state	VDD pin monitoring	VBUS_SENSE pin monitoring	
VBUS_EN_SRC	0	Attached.SRC or UnorientedDebug Accessory.SRC or OrientedDebug Accessory.SRC	VDD > UVLO if VDD_UVLO enabled and/or VDD < OVLO if VDD_OVLO enabled	V_{BUS} is within valid voltage range if VBUS_VALID_RANGE enabled or V_{BUS} > UVLO if V_{BUS} _VALID_RANGE disabled	The signal is asserted only if all the valid operation conditions are met
	HiZ	Any other state	VDD < UVLO if VDD_UVLO enabled and/or VDD > OVLO if VDD_OVLO enabled	V_{BUS} is out ofvalid voltage range if VBUS_VALID_RANGE enabled or VBUS < UVLO if V_{BUS} _VALID_RANGE disabled	The signal is de-asserted when at least one non valid operation condition is met

As specified in the USB Type-C standard specification, the attached state “Attached.SRC” is reached only if the voltage on the V_{BUS} receptacle side is at vSafe0V condition when a connection is detected.

“Type-C attached state” refers to the Type-C FSM states as defined in the USB Type-C standard specification and as described in the I²C register CC_OPERATION_STATUS.

“VDD pin monitoring” is valid only in source power role. Activation of the UVLO and OVLO threshold detections can be done through NVM programming (see Section 6 Start-up configuration) and also by software through the I²C interface. When UVLO and/or OVLO threshold detection is activated, VBUS_EN_SRC pin is asserted only if the device is attached and the valid threshold conditions on VDD are met. Once the VBUS_EN_SRC pin is asserted, the V_{BUS} monitoring is done on VBUS_SENSE pin instead of the VDD pin.

"VBUS_SENSE pin monitoring" relies, by default, on a valid V_{BUS} voltage range. The voltage range condition can be disabled to consider UVLO threshold detection instead. The monitoring condition of the V_{BUS} voltage can be changed through NVM programming (see Section 6 Start-up configuration) and also by software through the I²C interface. VBUS_EN_SRC pin is maintained asserted as long as the device is attached and a valid voltage condition on the V_{BUS} is met.

3.4 V_{CONN} supply

3.4.1 V_{CONN} input voltage

V_{CONN} is a regulated supply used to power circuits in the plug of USB3.1 full-featured cables and other accessories. V_{CONN} nominal operating voltage is 5.0 V +/- 5%.

3.4.2 V_{CONN} application conditions

V_{CONN} pin of the STUSB1702 is connected to each CC pin (CC1 and CC2) across independent power switches.

The STUSB1702 applies V_{CONN} only to the CC pin not connected to the CC wire when all below conditions are met:

- The device is configured in source power role
- V_{CONN} power switches are enabled
- A valid connection to a sink is achieved
- R_a presence is detected on the unwired CC pin
- A valid power source is applied to the V_{CONN} pin with respect to a predefined UVLO threshold

3.4.3 V_{CONN} monitoring

The V_{CONN} monitoring block detects if V_{CONN} power supply is available on the V_{CONN} pin. It is used to check that V_{CONN} voltage is above a pre-defined undervoltage lockout (UVLO) threshold to allow the enabling of the V_{CONN} power switches.

The default value of the UVLO threshold is 4.65 V typical for powered cables operating at 5 V. This value can be changed by software to 2.65 V typical to support V_{CONN}-powered accessories that operate down to 2.7 V.

3.4.4 V_{CONN} discharge

The behavior of Type-C FSMs is extended to an internal V_{CONN} discharge path capability on the CC pins in source power mode only. The discharge path is activated during 250 ms from sink detachment detection. This feature is disabled by default. It can be activated through NVM programming (see Section 6 Start-up configuration) and also by software through the I²C interface.

3.4.5 V_{CONN} control and status

The supplying conditions of V_{CONN} across the STUSB1702 are managed through the I²C interface. Different I²C registers and bits are used specifically for this purpose.

3.4.6 V_{CONN} power switches

Features

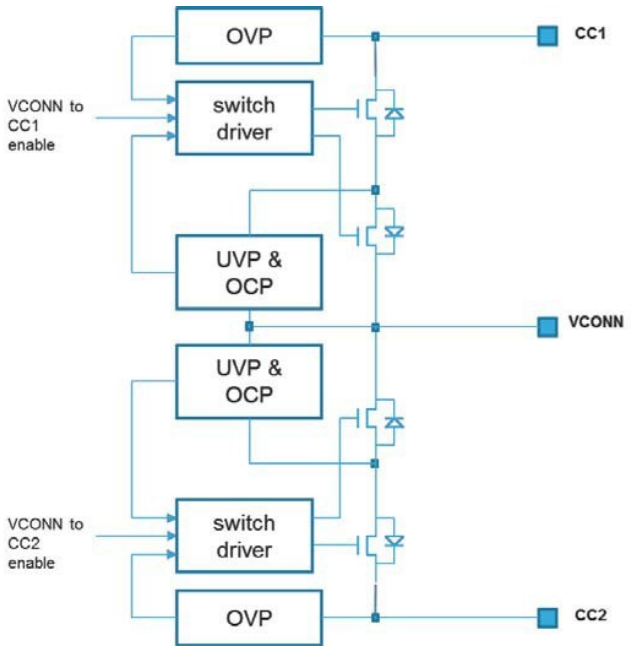
The STUSB1702 integrates two current limited high-side power switches with protection that tolerates high voltage up to 22 V on the CC pins.

Each V_{CONN} power switch is presents the following features:

- Soft-start to limit inrush current
- Constant current mode overcurrent protection
- Adjustable current limit
- Thermal protection

- Undervoltage and overvoltage protections
- Reverse current and reverse voltage protections

Figure 4. V_{CONN} to CC1 and CC2 power switch protections



Current limit programming

The current limit can be set within the range 100 mA to 600 mA by a step of 50 mA. The default current limit is programmed through NVM programming (see Section 6 Start-up configuration) and can be changed by software through the I²C interface. At power-on or after a reset, the current limit takes the default value preset in the NVM.

Fault management

The table below summarizes the different fault conditions that could occur during switch operation and the associated responses. An I²C alert is generated when a fault condition happens.

Table 6. Fault management conditions

Fault types	Fault conditions	Expected actions
Short-circuit	CC output pin shorted to ground via very low resistive path causing rapid current surge	Power switch limits the current and reduces the output voltage. I²C alert is asserted immediately thanks to VCONN_SW_OCP_FAULT bits
Overcurrent	CC output pin connected to a load that sinks current above programmed limit	Power switch limits the current and reduces the output voltage. I²C alert is asserted immediately thanks to VCONN_SW_OCP_FAULT bits
Overheating	Junction temperature exceeding 145 °C due to any reason	Power switch is disabled immediately until the temperature falls below 145 °C minus hysteresis of 15 °C. I²C alert is asserted immediately thanks to THERMAL_FAULT bit. The STUSB1702 goes into transient error recovery state
Undervoltage	V_{CONN} input voltage drops below UVLO threshold minus hysteresis	Power switch is disabled immediately until the input voltage rises above the UVLO threshold. I²C alert is asserted immediately thanks to VCONN_PRESENCE bit
Overvoltage	CC output pin voltage exceeds maximum operating limit of 6.0 V	Power switch is opened immediately until the voltage falls below the voltage limit. I²C alert is asserted immediately thanks to VCONN_SW_OVP_FAULT bits

Fault types	Fault conditions	Expected actions
Reverse current	CC output pin voltage exceeds V_{CONN} input voltage when the power switch is turned off	The reverse biased body diode of the back- to-back MOS switches is naturally disabled preventing current from flowing from CC output pin to the input
Reverse voltage	CC output pin voltage exceeds V_{CONN} input voltage of more than 0.35 V for 5 V when the power switch is turned on	Power switch is opened immediately until the voltage difference falls below the voltage limit. I²C alert is asserted immediately thanks to VCONN_SW_RVP_FAULT bits

3.5 High voltage protection

The STUSB1702 can be safely used in systems or connected to systems that handle high voltage on the V_{BUS} power path. The device integrates an internal circuitry on the CC pins that tolerates high voltages and ensures protection up to 22 V in case of unexpected short-circuits with the V_{BUS} or in the case of a connection to a device supplying high voltage on the V_{BUS}.

3.6 Hardware fault management

The STUSB1702 handles hardware fault conditions related to the device itself and to the V_{BUS} power path during system operation.

When such conditions occur, the circuit goes into a transient error recovery state named ErrorRecovery in the Type-C FSM. In this state, the device de-asserts the V_{BUS} power path by disabling the VBUS_EN_SRC pin and it removes the terminations from the CC pins during several tens of milliseconds. Then, it goes to the unattached source state.

The STUSB1702 goes into error recovery state when at least one condition listed below is met:

- If an overtemperature is detected, the “THERMAL_FAULT” flag is asserted
- If an internal pull-up voltage on the CC pins is below the UVLO threshold, the “VPU_VALID” flag is asserted
- If an overvoltage is detected on the CC pins, the “VPU_OVP_FAULT” flag is asserted
- If the VBUS voltage is out of the valid voltage range during attachment, the “VBUS_VALID” flag is asserted
- If an undervoltage is detected on the VDD pin during attachment when UVLO detection is enabled, the “VDD_UVLO_DISABLE” flag is asserted
- If an overvoltage is detected on the VDD pin during attachment when OVLO detection is enabled, the “VDD_OVLO_DISABLE” flag is asserted

The I²C register bits mentioned above give either the state of the hardware fault when it occurs or the setting condition to detect the hardware fault.

3.7 Accessory mode detection

The STUSB1702 supports the detection of audio accessory mode and debug accessory mode as defined in the USB Type-C standard specification with the following Type-C power modes (see Section 6 Start-up configuration):

- Source power role with accessory support

3.7.1 Audio accessory mode detection

The STUSB1702 detects an audio accessory device when both CC1 and CC2 pins are pulled down to ground by an R_a resistor from the connected device. The audio accessory detection is advertised through the CC_ATTACHED_MODE bits of the I²C register CC_CONNECTION_STATUS.

3.7.2 Debug accessory mode detection

The STUSB1702 detects a connection to a debug and test system (DTS). The debug accessory detection is advertised through the CC_ATTACHED_MODE bits of the I²C register CC_CONNECTION_STATUS.

- In source power role, a debug accessory device is detected when both the CC1 and CC2 pins are pulled down to ground by an R_d resistor from the connected device. The orientation detection is performed in two

steps as described in the table below. The DEBUG2 pin is asserted to advertise the DTS detection and the A_B_SIDE pin indicates the orientation of the connection. The orientation detection is advertised through the TYPEC_FSM_STATE bits of the I²C register CC_OPERATION_STATUS.

Table 7. Orientation detection

#	CC1 pin (CC2 pin)	CC2 pin (CC1 pin)	Detection process	A_B_SIDE pin CC1/CC2 (CC2/CC1)	Orientation detection state TYPEC_FSM_STATE bits value
1	R_d	R_d	1st step: debug accessory mode detected	HiZ (HiZ)	UnorientedDebugAccessory.SRC
2	R_d	≤ R_a	2nd step: orientation detected (DTS presents a resistance to GND with a value ≤ R_a on its CC2 pin)	HiZ (0)	OrientedDebugAccessory.SRC

4 Managing USB PD transactions

Due to specific HW/SW partitioning, the STUSB1702 requires a specific alignment between the lower protocol stack (managed by the STUSB1702) and the higher protocol stack (managed by the external MCU). Therefore, dedicated read and write I²C accesses are needed to perform the following actions:

- Acknowledge a HW reset request
- Request a HW reset
- Perform a V_{CONN} SWAP
- Perform a data role SWAP

5 I²C interface

5.1 Read and write operations

The I²C interface is used to configure, control and read the operation status of the device. It is compatible with the Philips I²C BUS® (version 2.1). The I²C is a slave serial interface based on two signals:

- SCL - serial clock line: input clock used to shift data
- SDA - serial data line: input/output bidirectional data transfers

A filter rejects the potential spikes on the bus data line to preserve data integrity.

The bidirectional data line supports transfers up to 400 Kbit/s (fast mode). The data are shifted to and from the chip on the SDA line, MSB first.

The first bit must be high (START) followed by the 7-bit device address and the read/write control bit.

Two 7-bit device addresses are available for the STUSB1702 thanks to external programming of DevADDR0 through ADDR0 pin setting, i.e. 0x28 or 0x29. This allows two STUSB1702 devices to be connected on the same I²C bus.

Table 8. Device address format

Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
DevADDR6	DevADDR5	DevADDR4	DevADDR3	DevADDR2	DevADDR1	DevADDR0	R/W
0	1	0	1	0	0	ADDR0	0/1

Table 9. Register address format

Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
RegADDR7	RegADDR6	RegADDR5	RegADDR4	RegADDR3	RegADDR2	RegADDR1	RegADDR0

Table 10. Register data format

Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
DATA7	DATA6	DATA5	DATA4	DATA3	DATA2	DATA1	DATA0

Figure 5. Read operation

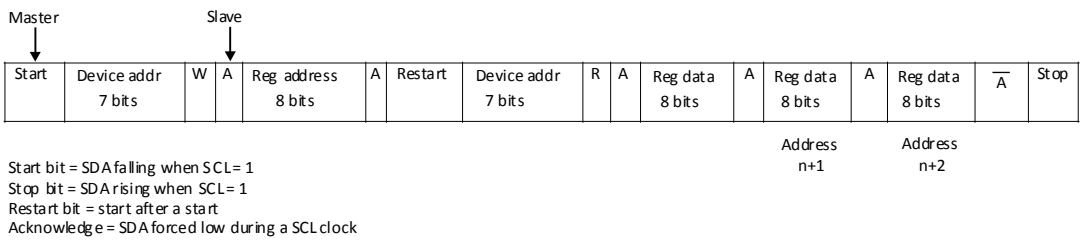


Figure 6. Write operation

Start	Device addr 7 bits	W	A	Reg address 8 bits	A	Reg data 8 bits	A	Reg data 8 bits	A	Reg data 8 bits	A	Stop
								Address n+1		Address n+2		

Start bit = SDA falling when SCL = 1
Stop bit = SDA rising when SCL = 1
Restart bit = start after a start

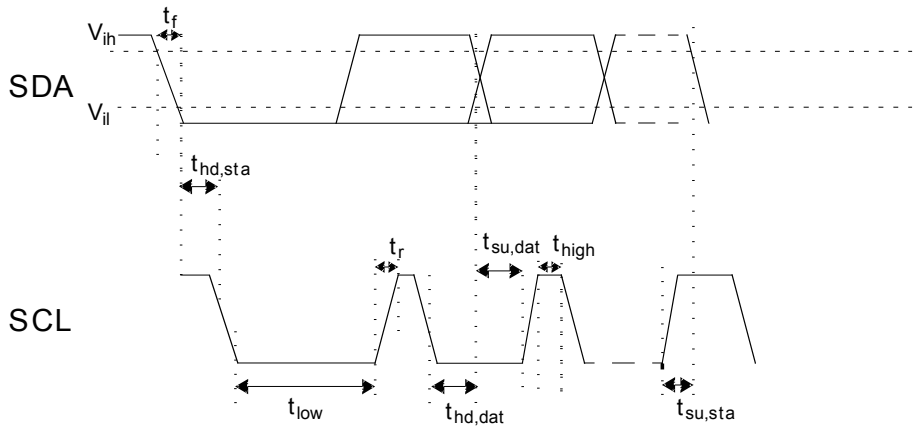
5.2 Timing specifications

The device uses a standard slave I²C channel at speed up to 400 kHz.

Table 11. I²C timing parameters - V_{DD} = 5 V

Symbol	Parameter	Min.	Typ.	Max.	Unit
F_{scl}	SCL clock frequency	0	-	400	kHz
$t_{hd,sta}$	Hold time (repeated) START condition	0.6	-	-	µs
t_{low}	LOW period of the SCL clock	1.3	-	-	
t_{high}	HIGH period of the SCL clock	0.6	-	-	
$t_{su,dat}$	Set-up time for repeated START condition	0.6	-	-	
$t_{hd,dat}$	Data hold time	0.04	-	0.9	
$t_{su,dat}$	Data setup time	100	-	-	
t_r	Rise time of both SDA and SCL signals	20 + 0.1 C_b	-	300	ns
t_f	Fall time of both SDA and SCL signals	20 + 0.1 C_b	-	300	
$t_{su,sto}$	Set-up time for STOP condition	0.6	-	-	µs
t_{buf}	Bus free time between a STOP and START condition	1.3	-	-	
C_b	Capacitive load for each bus line	-	-	400	pF

Figure 7. I²C timing diagram



5.3 I²C register map

Table 12. **Register access legend**

Access code	Expanded name	Description
RO	Read only	Register can be read only
R/W	Read /write	Register can be read or written
RC	Read and clear	Register can be read and is cleared after it is read

Table 13. **STUSB1702 register map overview**

Address	Register name	Access	Description
00h to 0Ah	Reserved	RO	Do not use
0Bh	ALERT_STATUS	RC	Alerts register linked to transition registers
0Ch	ALERT_STATUS_MASK_CTRL	R/W	Allows the interrupt mask on the ALERT_STATUS register to be changed
0Dh	CC_DETECTION_STATUS_TRANS	RC	Alerts about transition in CC_DETECTION_STATUS register
0Eh	CC_DETECTION_STATUS	RO	CC detection status
0Fh	TYPE_C_HANDSHAKE and MONITORING_STATUS_TRANS	RC	Allows Type-C FSM to be synchronized with software. Alerts about transition in MONITORING_STATUS register
10h	MONITORING_STATUS	RO	Gives status on V_{BUS} and V_{CONN} voltage monitoring
11h	CC_CONNECTION_STATUS	RO	CC connection status
12h	HW_FAULT_STATUS_TRANS	RC	Alerts about transition in HW_FAULT_STATUS register
13h	HW_FAULT_STATUS	RO	Gives status on hardware faults
14h to 17h	Reserved	RO	Do not use
18h	CC_CAPABILITY_STATUS_CTRL	R/W	Allows the CC capabilities to be changed
19h to 1Dh	Reserved	RO	Do not use
1Eh	CC_VCONN_SWITCH_CTRL	R/W	Allows the current limit of V_{CONN} power switches to be changed
1Fh	TYPE_C_CTRL	R/W	Allows software to be synchronized with Type- C FSM
20h	VCONN_MONITORING_CTRL	R/W	Allows the monitoring conditions of V_{CONN} voltage to be changed
21h	VBUS_SELECT	R/W	Allows the DAC value related to the targeted V_{BUS} voltage to be changed
22h	VBUS_RANGE_MONITORING_CTRL	R/W	Allows the voltage range for V_{BUS} monitoring to be changed
23h	RESET_CTRL	R/W	Controls the device reset by software
25h	VBUS_DISCHARGE_TIME_CTRL	R/W	Allows the V_{BUS} discharge time to be changed
26h	VBUS_DISCHARGE_CTRL	R/W	Controls the V_{BUS} discharge path
27h	VBUS_ENABLE_STATUS	R/W	Gives status on V_{BUS} power path activation
29h to 2Dh	Reserved	RO	Do not use
2Eh	VBUS_MONITORING_CTRL	R/W	Allows the monitoring conditions of V_{BUS} voltage to be changed
2Fh	Reserved	RO	Do not use

6 Start-up configuration

6.1 User-defined parameters

The STUSB1702 has a set of user-defined parameters that can be customized by NVM reprogramming and/or by software through the I²C interface. This feature allows the customer to change the preset configuration of the USB Type-C interface and to define a new configuration to meet specific customer requirements addressing various applications, use cases, or specific implementations.

The NVM re-programming overrides the initial default setting to define a new default setting that is used at power-up or after a reset. The default value is copied at power-up, or after a reset, from the embedded NVM into dedicated I²C register bits. The NVM re-programming is possible only once with a customer password.

When a default value is changed during functioning by software, the new setting remains in effect as long as the STUSB1702 runs or when it is changed again. But after power- off and power-up, or after a reset, the STUSB1702 takes back the default values defined in the NVM.

6.2 Default start-up configuration

The table below lists the user-defined parameters and indicates the default start-up configuration of the STUSB1702.

Three types of user-defined parameters are specified in the table with respect to the “Customization type” column:

- SW: indicates parameters that can be customized only by software through the I²C interface during system operation
- NVM: indicates parameters that can be customized only by NVM re-programming
- NVM/SW: indicates parameters that can be customized by NVM re-programming and/or by software through the I²C interface during system operation

Table 14. STUSB1702 user-defined parameters and default setting

Customization type	Parameter	Default value and description	I²Cregister address
NVM/SW	CC_CONNECTION_STATUS_AL_MASK	1b: interrupt masked	0Ch
NVM/SW	MONITORING_STATUS_AL_MASK	1b: interrupt masked	0Ch
NVM/SW	HW_FAULT_STATUS_AL_MASK	1b: interrupt masked	0Ch
NVM	STANDBY_POWER_MODE_DISABLE	1b: disables standby power mode	n.a.
NVM/SW	CC_CURRENT_ADVERTISED	01b: 1.5 A	18h
NVM/SW	CC_VCONN_DISCHARGE_EN	0b: V_{CONN} discharge disabled on CC pin	18h
NVM/SW	CC_VCONN_SUPPLY_EN	1b: V_{CONN} supply capability enabled on CC pin	18h
NVM/SW	CC_VCONN_SWITCH_ILIM	0000b: 350 mA	1Eh
SW	VCONN_MONITORING_EN	1b: enables UVLO threshold detection on VCONN pin	20h
SW	VCONN_UVLO_THRESHOLD	0b: high UVLO threshold of 4.65 V	20h
NVM/SW	SHIFT_HIGH_VBUS_LIMIT_SOURCE	0101b: in source power role, shifts nominal high voltage limit by 5% of V_{BUS}	22h
NVM/SW	SHIFT_LOW_VBUS_LIMIT_SOURCE	0101b: in source power role, shifts nominal low voltage limit by -5% of V_{BUS}	22h
SW	SW_RESET_EN	0b: device reset is performed from hardware RESET pin	23h

Customization type	Parameter	Default value and description	I²Cregister address
NVM/SW	VBUS_DISCHARGE_TIME_TO_0V	1010b: 840 ms discharge time	25h
NVM/SW	VBUS_DISCHARGE_TIME_TRANSITION	1010b: 200 ms discharge time	25h
NVM	VBUS_DISCHARGE_DISABLE	0b: enables V_{BUS} discharge path	n. a.
NVM/SW	VDD_OVLO_DISABLE	0b: enables OVLO threshold detection on VDD pin	2Eh
NVM/SW	VBUS_VALID_RANGE_DISABLE	0b: enables valid V_{BUS} voltagerange detection	2Eh
NVM/SW	VBUS_VSAFE0V_THRESHOLD	00b: V_{BUS} vSafe0Vthreshold = 0.6 V	2Eh
NVM/SW	VDD_UVLO_DISABLE	1b: disables UVLO threshold detection on VDD pin	2Eh

7 Application

The sections below are not part of the ST product specifications. They are intended to give a generic application overview to be used by the customer as a starting point for further implementation and customization. ST does not warrant compliancy with customer specifications. Full system implementation and validation are under the customer's responsibility.

7.1 General description

7.1.1 Power supplies

The STUSB1702 can be supplied in three different ways depending on the targeted application:

- Through the VDD pin only for applications powered by V_{BUS} that operate either in source power role
- Through the VSYS pin only for AC powered applications with a system power supply delivering 3.3 V or 5 V
- Through the VDD and VSYS pins for applications powered by V_{BUS} with a system power supply delivering 3.3 V or 5 V. When both VDD and VSYS power supplies are present, the low power supply VSYS is selected when VSYS voltage is above 3.1 V. Otherwise VDD is selected

7.1.2 Connection to MCU or application processor

The I²C interface is used to provide extensive functionality during system operation. For instance:

1. Define the port configuration during system boot (in case NVM parameters are not customized during manufacturing)
2. Change the default configuration at any time during operation
3. Adjust the port power capability in source power role according to contextual power availability and/or the power partitioning with other ports
4. Save system power by shutting down the DC-DC converter according to the attachment detection state
5. Provide a diagnostic of the Type-C connection and the V_{BUS} power path in real time

7.2 USB Type-C typical applications

7.2.1 Source type application schematic

Figure 8. Typical STUSB1702 implementation in source type application

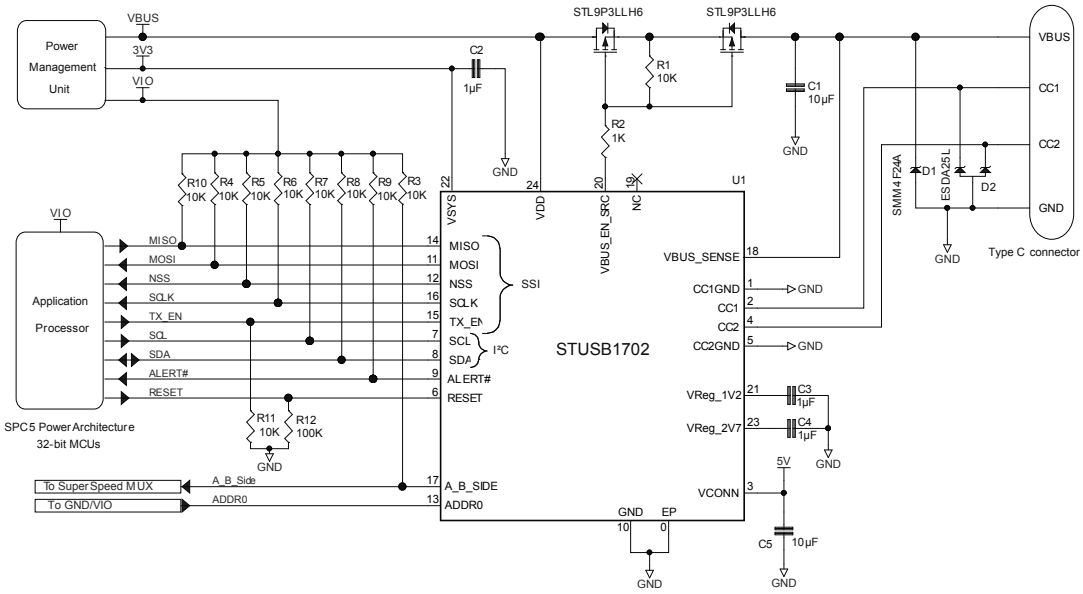


Table 15. Default setting for a source type application

I²C register address	I²C register field name	I²C register reset value/description	Customization type
0Eh	START_UP_POWER_MODE	0b: device starts in normal mode	NVM/SW
18h	CC_CURRENT_ADVERTISED	01b: 1.5 A	NVM/SW
18h	CC_VCONN_DISCHARGE_EN	0b: V_{CONN} discharge disabled on CC pin	NVM/SW
18h	CC_VCONN_SUPPLY_EN	1b: V_{CONN} supply capability enabled on CC pin	NVM/SW
1Eh	CC_VCONN_SWITCH_ILIM	0000b: 350 mA	NVM/SW
20h	VCONN_MONITORING_EN	1b: enables UVLO threshold detection on V_{CONN} pin	SW
20h	VCONN_UVLO_THRESHOLD	0b: high UVLO threshold of 4.65 V	SW
22h	SHIFT_HIGH_VBUS_LIMIT_SOURCE	0101b: in source power role, shifts nominal high voltage limit by +5% of V_{BUS}	NVM/SW
22h	SHIFT_LOW_VBUS_LIMIT_SOURCE	0101b: in source power role, shifts nominal low voltage limit by -5% of V_{BUS}	NVM/SW
25h	VBUS_DISCHARGE_TIME_TO_0V	1010b: 840 ms discharge time	NVM/SW
25h	VBUS_DISCHARGE_TIME_TRANSITION	1010b: 200 ms discharge time	NVM/SW
26h	VBUS_DISCHARGE_EN	1b: enables the V_{BUS} discharge path	NVM/SW
2Eh	VDD_OVLO_DISABLE	0b: enables OVLO threshold detection on VDD pin	SW

I²C register address	I²C register field name	I²C register reset value/description	Customization type
2Eh	VBUS_RANGE_DISABLE	0b: enables V_{BUS} voltage range detection	SW
2Eh	VBUS_VSAFE0V_THRESHOLD	00b: V_{BUS} vSafe0V threshold = 0.6 V	SW
2Eh	VDD_UVLO_DISABLE	1b: disables UVLO threshold detection on VDD pin	SW

Table 16. Conditions for V_{BUS} power path assertion in source power role

Pin	Electrical value	Operation conditions			Comment
		Type-C attached state	VDD pin monitoring	VBUS_SENSEpin monitoring	
VBUS_EN_SRC	0	Attached.SRC or UnorientedDebug Accessory.SRC or OrientedDebug Accessory.SRC	VDD < OVLO if VDD pin is supplied	V_{BUS} within valid voltage range	The signal is asserted only if all the valid operation conditions are met
	HiZ	Anyother state	VDD > OVLO if VDD pin is supplied	V_{BUS} is out ofvalid voltage range	The signal is de-asserted when at least one non valid operation condition is met.

Table 17. Source power role with accessory support

Connection state	CC1 pin	CC2 pin	Type-C device state CC_OPERATION_STATUS register @11h	A_B_SIDE pin	VCONN supply	VBUS_EN_SRC pin	CC_CONNECTION_STATUS register @0Eh
Nothing attached	Open	Open	Unattached.SRC	HiZ	OFF	HiZ	00h
Sink attached	Rd	Open	Attached.SRC	HiZ	OFF	0	2Dh
	Open	Rd		0	OFF	0	2Dh
Powered cable withoutsink attached	Open	Ra	Unattached.SRC	HiZ	OFF	HiZ	00h
	Ra	Open		HiZ	OFF	HiZ	00h
Powered cable with sink attached or VCONN-powered accessory attached	Rd	Ra	Attached.SRC	HiZ	CC2	0	2Fh
	Ra	Rd		0	CC1	0	2Fh
Debug accessory mode attached source role	Rp	Rp	Unattached.SRC	HiZ	OFF	HiZ	00h
Debug accessory mode attached sink role	Rd	Rd	UnorientedDebug Accessory.SRC	HiZ	OFF	0	6Dh

Connection state	CC1 pin	CC2 pin	Type-C device state CC_OPERATION_STATUS register @11h	A_B_SIDE pin	VCONN supply	VBUS_EN_SRC pin	CC_CONNECTION_STATUS register @0Eh
Debug accessory mode attached sink role	Rd	≤Ra	OrientedDebug Accessory.SRC	HiZ	OFF	0	6Dh
	≤ Ra	Rd		0	OFF	0	6Dh
Audio adapter accessory mode attached	Ra	Ra	AudioAccessory	HiZ	OFF	HiZ	81h

The value of the CC1 and CC2 pins is defined from a termination perspective and corresponds to the termination presented by the connected device. The CC_CONNECTION_STATUS register can report other values than the one presented in table above. In this table, it reflects the state transitions in Type-C FSM that can be ignored from the application stand point.

8 Electrical characteristics

8.1 Absolute maximum ratings

All voltages are referenced to GND.

Table 18. Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_{DD}	Supply voltage	28	V
V_{SYS}	Supply voltage on VSYS pin	6	
V_{CC1}, V_{CC2}, V_{CC1GND}, V_{CC2GND}	High voltage on CC pins	22	
$V_{VBUS\_EN\_SRC}$, V_{VBUS_SENSE}	High voltage on V_{BUS} pins	28	
V_{SCL}, V_{SDA}, $V_{ALERT\#}$, V_{RESET}, $V_{A\_B\_SIDE}$ V_{MOSI}, V_{MISO}, V_{NSS}, V_{TX_EN}, V_{SCLK}	Operating voltage on I/O pins	-0.3 to 6	
V_{CONN}	V_{CONN} voltage	6	
T_{STG}	Storagetemperature	-55 to 150	°C
T_J	Maximum junction temperature	145	
ESD	HBM	4	kV
	CDM	1.5	

8.2 Operating conditions

Table 19. Operating conditions

Symbol	Parameter	Value	Unit
V_{DD}	Supply voltage	4.1 to 22	V
V_{SYS}	Supply voltage on V_{SYS} pin	3.0 to 5.5	
V_{CC1}, V_{CC2}, V_{CC1GND}, V_{CC2GND}	CC pins	-0.3 to 5.5	
$V_{VBUS\_EN\_SRC}$, V_{VBUS_SENSE}	High voltage pins	0 to 22	
V_{SCL}, V_{SDA}, $V_{ALERT\#}$, V_{RESET}, $V_{A\_B\_SIDE}$ V_{MOSI}, V_{MISO}, V_{NSS}, V_{TX_EN}, V_{SCLK}	Operating voltage on I/O pins	0 to 4.5	
V_{CONN}	V_{CONN} voltage	2.7 to 5.5	
I_{CONN}	V_{CONN} rated current (default = 0.35 A)	0.1 to 0.6	A
T_A	Operating temperature	-40 to 105	°C

Note: The transient voltage on the CC1 and CC2 pins drops to -0.3 during BMC communication.

8.3 Electrical and timing characteristics

Unless otherwise specified: V_{DD} = 5 V, T_A = +25 °C, all voltages are referenced to GND.

Table 20. Electrical characteristics

Symbol	Parameter	Conditions		Min.	Typ.	Max.	Unit
$I_{DD\ (SRC)}$	Current consumption	Device idle as a SOURCE (not connected, no communication)	V_{SYS} @ 3.3 V		158		µA
			V_{DD} @ 5.0 V		188		
I_{STDBY}	Standby current consumption	Device in standby (not connected, low power)	V_{SYS} @ 3.3 V		33		µA
			V_{DD} @ 5.0 V		53		
CC1 and CC2 pins							
I_{P-USB}	CC current sources	CC pin voltage, V_{CC} = -0.3 to 2.6 V, 40 °C < T_A < 105 °C		-20%	80	+20%	µA
$I_{P-1.5}$				-8%	180	+8%	
$I_{P-3.0}$				-8%	330	+8%	
V_{CCO}	CC open pin voltage	CC unconnected, V_{DD} = 3.0 to 5.5 V		2.75			V
R_d	CC pull-down resistors	40 °C < T_A < 105 °C		-10%	5.1	10%	kΩ
R_{INCC}	CC input impedance	Pull-up and pull-down resistors off		200			kΩ
$V_{TH0.2}$	Detection threshold 1	Max. R_a detection by DFP at I_P = I_{P-USB}, min. I_{P_USB} detection by UFP on R_d, min CC voltage for connected UFP		0.15	0.20	0.25	V
$V_{TH0.4}$	Detection threshold 2	Max. R_a detection by DFP at I_P = $I_{P-1.5}$		0.35	0.40	0.45	V
$V_{TH0.8}$	Detection threshold 4	Max. R_a detection by DFP at I_P = $I_{P-3.0}$		0.75	0.80	0.85	V
$V_{TH1.6}$	Detection threshold 6	Max. R_d detection by DFP at I_P = I_{P-USB} and I_P = $I_{P-1.5}$		1.50	1.60	1.65	V
$V_{TH2.6}$	Detection threshold 7	Max. R_d detection by DFP at $I_{P-3.0}$, max. CC voltage for connected UFP		2.45	2.60	2.75	V
V_{CONN} protection							
R_{VCONN}	V_{CONN} power path resistance	I_{VCONN} = 0.2 A-		0.25	0.50	0.975	Ω
I_{OCP}	Overcurrent protection	Programmable current limit threshold (from 100 mA to 600 mA by step of 50 mA)		85	100	125	mA
				300	350	400	
				550	600	650	
V_{OVP}	Output overvoltage protection			5.9	6.0	6.1	V
V_{UVP}	Input undervoltage protection	Low UVLO threshold		2.6		2.7	V
		High UVLO threshold (default)		4.6		4.8	
V_{BUS} monitoring and driving							
V_{THUSB}	V_{BUS} presence threshold	V_{SYS} = 3.0 to 5.5 V		3.8	3.9	4.0	V

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
V_{TH0V}	V_{BUS} safe 0 V threshold (vSafe0V)	V_{SYS} = 3.0 to 5.5 V	0.5	0.6	0.7	V
		Programmable threshold	0.8	0.9	1	V
		Programmable threshold from 0.6 V to 1.8 V	1.1	1.2	1.3	V
		Default V_{THOV} = 0.6 V	1.7	1.8	1.9	V
R_{DISUSB}	V_{BUS} discharge resistor		600	700	800	Ω
T_{DISUSB} (1)	V_{BUS} discharge time to 0V	Default $T_{DISPARAM}$ = 840 ms, the coefficient $T_{DISPARAM}$ is programmable by NVM	70	84	100	ms
	V_{BUS} discharge time to PDO	Default $T_{DISPARAM}$ = 200 ms, the coefficient $T_{DISPARAM}$ is programmable by NVM	20	24	28	
$V_{MONUSBH}$	V_{BUS} monitoring high voltage threshold	V_{BUS} = nominal target value, default $V_{MONUSBH}$ = V_{BUS} +10 %, the threshold limit is programmable by NVM from +5 % to +20 %		V_{BUS} + 10%		V
$V_{MONUSBL}$	V_{BUS} monitoring low voltage threshold	V_{BUS} = nominal target value, default $V_{MONUSBL}$ = V_{BUS} -10 %, the threshold limit is programmable by NVM from -20 % to -5 %		V_{BUS} - 10%		V
Digital input/output (SCL, SDA, ALERT#, A_B_SIDE, MOSI, MISO, NSS, TX_EN, SCLK)						
V_{IH}	High level input voltage		1.2			V
V_{IL}	Low level input voltage				0.35	V
V_{OL}	Low level output voltage	Ioh = 3 mA			0.4	V
20 V open drain outputs (VBUS_EN_SRC)						
V_{OL}	Low level output voltage	Ioh = 3 mA			0.4	V

1. $T_{DISPARAM}$

8.4 Thermal Information

Table 21. Thermal information

Symbol	Parameter	Value	Unit
$R_{\theta JA}$	Junction to ambient thermal resistance	37	°C/W
$R_{\theta JC}$	Junction to case thermal resistance	5	°C/W

9 Ordering information

Table 22. **Order code**

Order code	AEC-Q100	Package	Temperature range	Marking
STUSB1702YQTR	Yes	QFN24 EP 4x4 mm wettable flanks	- 40 °C up to105 °C	1702Y

10 Terms and abbreviations

Table 23. List of terms and abbreviations

Term	Description
Accessory modes	Audio adapter accessory mode. It is defined by the presence of R_a/R_a on the CC1/CC2 pins.
	Debug accessory mode. It is defined by the presence of R_d/R_d on CC1/CC2 pins in source power role or R_p/R_p on CC1/CC2 pins in sink power role.
DFP	Downstream facing port, specifically associated with the flow of data in a USB connection. Typically, the ports on a HOST or the ports on a hub to which devices are connected. In its initial state, DFP sources V_{BUS} and V_{CONN}, and supports data.
DRP	Dual-role port. A port that can operate as either a source or a sink. The port role may be changed dynamically.
Sink	Port asserting R_d on the CC pins and consuming power from the V_{BUS}; most commonly a device.
Source	Port asserting R_p on the CC pins and providing power over the V_{BUS}; most commonly a host or hub DFP.
UFP	Upstream facing port, specifically associated with the flow of data in a USB connection. The port on a device or a hub that connects to a host or the DFP of a hub. In its initial state, the UFP sinks the V_{BUS} and supports data.

11 Package information

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: www.st.com. ECOPACK® is an ST trademark.

11.1 QFN24 EP 4x4 mm wettable flank package information

Figure 9. **QFN24 EP 4x4 mm wetable flank package outline**

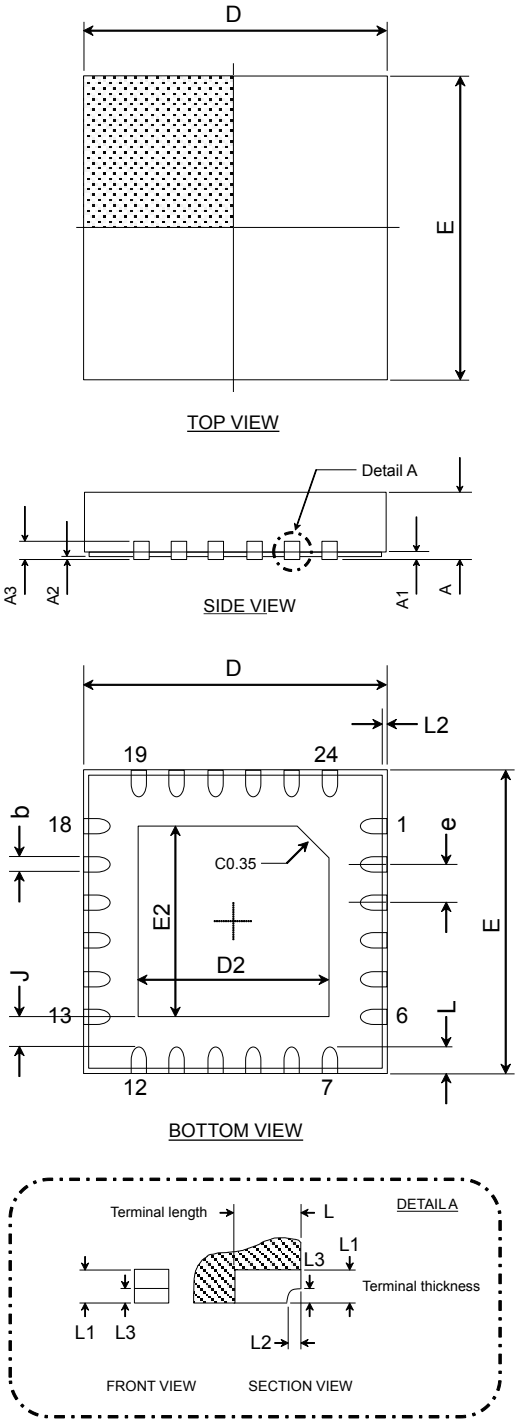
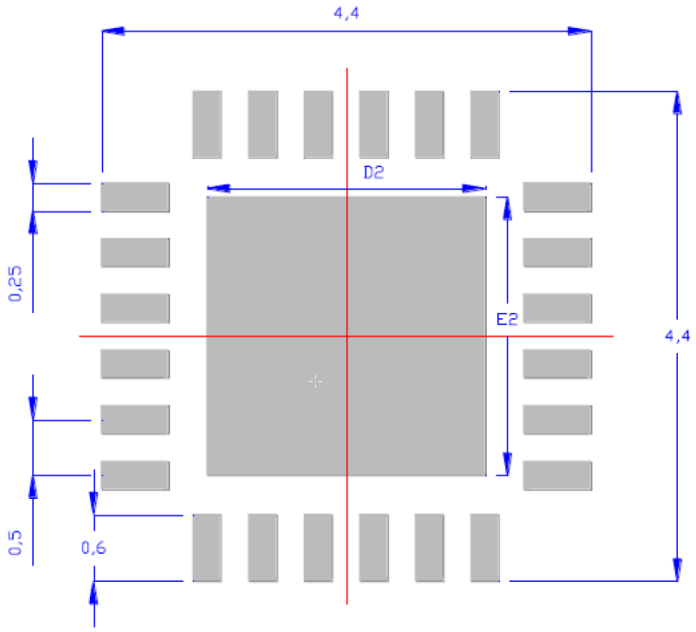


Table 24. **QFN24 EP 4x4 mm wetable flank mechanical data**

Ref.	Dimensions (mm)		
	Min.	Typ.	Max.
A	0.90	0.95	1.00
A1		0.10	
A2	0.00	0.02	0.05
A3		0.20	
b	0.20	0.25	0.30
D	3.85	4.00	4.15
D2	2.40	2.50	2.60
E	3.85	4.00	4.15
E2	2.40	2.50	2.60
e		0.50	
J		0.35	
L	0.30	0.40	0.50
L1		0.20	
L2		0.05	
L3		0.10	

Figure 10. **QFN24 EP 4x4 mm wetable flank recommended footprint**



Revision history

Table 25. **Document revision history**

Date	Revision	Changes
06-Jul-2018	1	Initial release.

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