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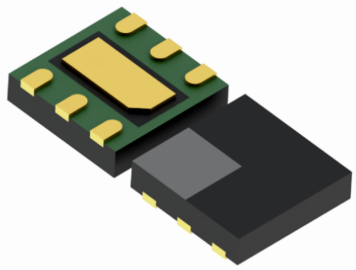
STTS22H

Datasheet

Low-voltage, ultra-low-power, 0.5 °C accuracy I²C/SMBus 3.0 temperature sensor



UDFN-6L 2.0 x 2.0 x 0.5 mm

Product status link
STTS22H

Product summary		
Order code	STTS22HTR	STTS22H
Temp. range [°C]	-40 to +125	
Package	UDFN-6L	
Packing	Tape and reel	Tray

Product labels

SUSTAINABLE TECHNOLOGY

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Features

Key features

- Integrated high-accuracy temperature sensor
- Factory calibrated
- One-shot mode for power saving

Electrical specifications

- Supply voltage: 1.5 to 3.6 V
- I²C, SMBus 3.0 with ALERT (ARA) support
- Programmable thresholds with interrupt pin
- Supports up to 1 MHz serial clock
- Up to 2 I²C/SMBus slave addresses
- Ultra-low current: 1.75 µA in one-shot mode

Sensing specifications

- Operating temperature -40 °C to +125 °C
- Temperature accuracy (max.):
  ± 0.5 °C (-10 °C to +60 °C)
- 16-bit temperature data output

Package specifications

- UDFN 2.0 x 2.0 x 0.50 mm, 6 leads with exposed pad down
- ECOPACK, RoHS and “Green” compliant

Applications

- Wearable devices
- Smart home automation
- Asset and goods tracking
- Smartphones
- HVAC
- Refrigerators
- Air humidifiers
- Portable consumer devices
- White goods
- Thermostats

Description

The STTS22H is an ultra-low-power, high accuracy, digital temperature sensor offering high performance over the entire operating temperature range.

The STTS22H is a band gap temperature sensor coupled with an A/D converter, signal processing logic and an I²C/SMBus 3.0 interface all in a single ASIC.

This sensor is housed in a small 2 x 2 x 0.50 mm 6-lead UDFN package with exposed pad down for a better temperature match with the surrounding environment.

The STTS22H is factory calibrated and requires no additional calibration efforts on the customer side.

1 Overview

The STTS22H is a digital temperature sensor which communicates over a 2-wire I²C/SMBus 3.0 serial interface.

Thanks to its factory calibration, the STTS22H offers high-end accuracy performance over the entire operating temperature range reaching as low as ±0.5 °C without requiring any further calibration at the application level.

The sensor operating mode is user-configurable and allows selecting between different ODRs (down to 1 Hz) or the one-shot mode for battery saving. In one-shot mode, the sensor current consumption falls to 1.75 µA.

The STTS22H comes in a 6-pin device that supports user-configurable slave addresses. By connecting the Addr pin to either GND or V_{DD}, two different addresses can be specified, thus allowing to have up to two STTS22H sharing the same I²C/SMBus bus line. An interrupt pin is also available to signal the application whenever the user-selectable high and low threshold have been exceeded.

2 Pin description

Figure 1. **Pin configuration**

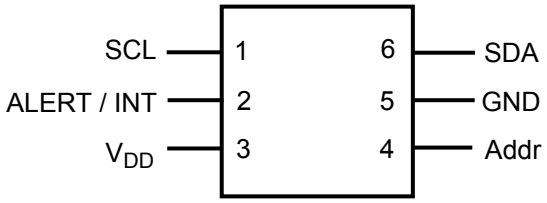


Table 1. **Pin description**

Pin number	Name	Function
1	SCL	SMBus/I²C serial interface clock
2	ALERT / INT	Open-drain interrupt output. The output supports the SMBus Alert (ARA).
3	V_{DD}	Power supply V_{DD}
4	Addr	SMBus/I²C address selection. The pin at power-up determines the SMBus slave address according to the connection shown in Table 2.
5	GND	0 V supply
6	SDA	SMBus/I²C serial data line

Table 2. **STTS22H address definition**

Addr pin connection	SMBus slave address
V_{DD}	0111 000 (0x70 Write, 0x71 Read)
GND	0111 111 (0x7E Write, 0x7F Read)

3 Sensor parameters and electrical specifications

Conditions at V_{DD} = 2.5 V, T = 25 °C.

Table 3. Temperature sensor specifications

Symbol	Parameter	Test condition	Min.	Typ.(1)	Max.	Unit
T_{op}	Operating temperature range		-40		125	°C
T_{bit}	Temperature output data		-	16	-	bit
T_n	Temperature noise	AVG [1:0] = 3		0.055		°C RMS
		AVG [1:0] = 2		0.04		
		AVG [1:0] = 1		0.03		
		AVG [1:0] = 0		0.02		
T_s	Temperature sensitivity		-	0.01	-	°C/LSB
			-	100	-	LSB/°C
T_{acc}	Temperature accuracy	-10 to 60 °C	-0.5	±0.25	0.5	°C
		-40 to 125 °C	-1.0	±0.7	1.0	
ODR	Temperature digital output data rate	LOW_ODR_START = 1, FREERUN = 0, AVG[1:0] = don't care		1		Hz
		LOW_ODR_START = 0, FREERUN = 1, AVG[1:0] = 0		25		
		LOW_ODR_START = 0, FREERUN = 1, AVG[1:0] = 1		50		
		LOW_ODR_START = 0, FREERUN = 1, AVG[1:0] = 2		100		
		LOW_ODR_START = 0, FREERUN = 1, AVG[1:0] = 3		200		

1. *Typical specifications are not guaranteed.*

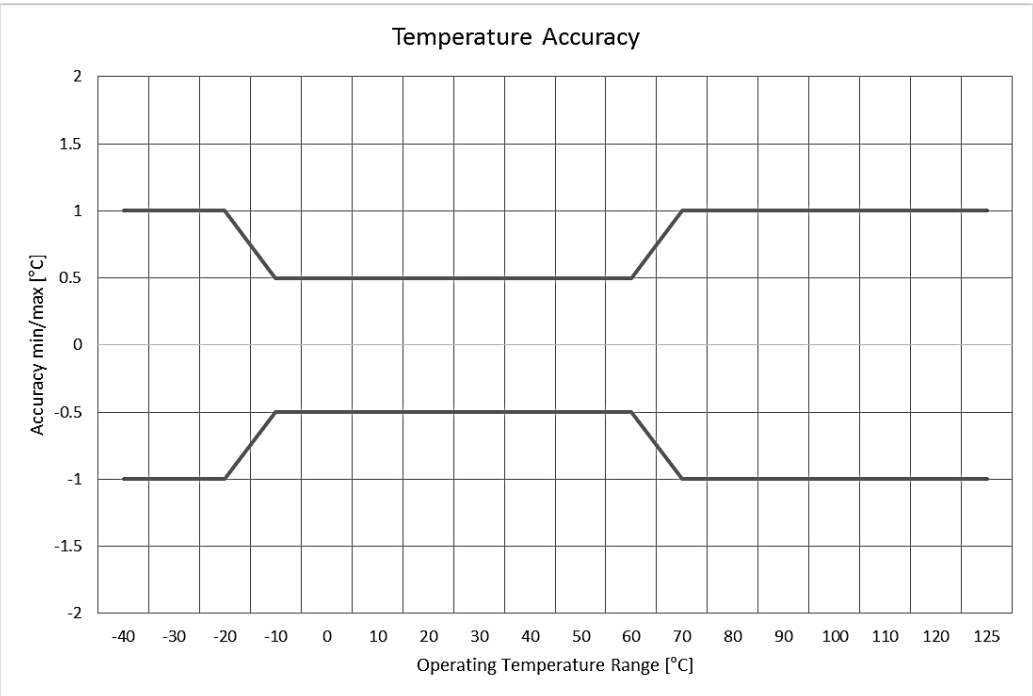
Table 4. Electrical specifications

Symbol	Parameter	Test condition	Min.	Typ.(1)	Max.	Unit
V_{DD}	Supply voltage		1.5	-	3.6	V
I_{DD}	Supply current	One-shot mode		1.75(2)		µA
		1 Hz ODR, AVG[1:0] = 3		2.0		
		During sensor measurements		120	180	
Idd_{PDN}	Power-down supply current			0.5		µA
Ton	Turn-on time				12(3)	ms
Top	Operating temperature range		-40	-	125	°C

1. *Typical specifications are not guaranteed.*
2. *One sample per second averaged supply current.*
3. *The user must wait at least 12 ms for the device to fully boot.*

3.1 Sensor accuracy specifications

Figure 2. Min/max temperature accuracy specifications



4 Absolute maximum ratings

Stresses above those listed as “Absolute maximum ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device under these conditions is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

Table 5. Absolute maximum ratings

Symbol	Ratings	Maximum value	Unit
V_{DD}	Supply voltage	-0.3 to 4.8	V
Vin	Input voltage on any control pin	-0.3 to V_{DD}+0.3	V
T_{STG}	Storage temperature range	-40 to +125	°C
ESD	Electrostatic discharge protection	2 (HBM)	kV

Note: Supply voltage on any pin should never exceed 4.8 V.

This device is sensitive to mechanical shock, improper handling can cause permanent damage to the part.

This device is sensitive to electrostatic discharge (ESD), improper handling can cause permanent damage to the part.

5 Digital interfaces

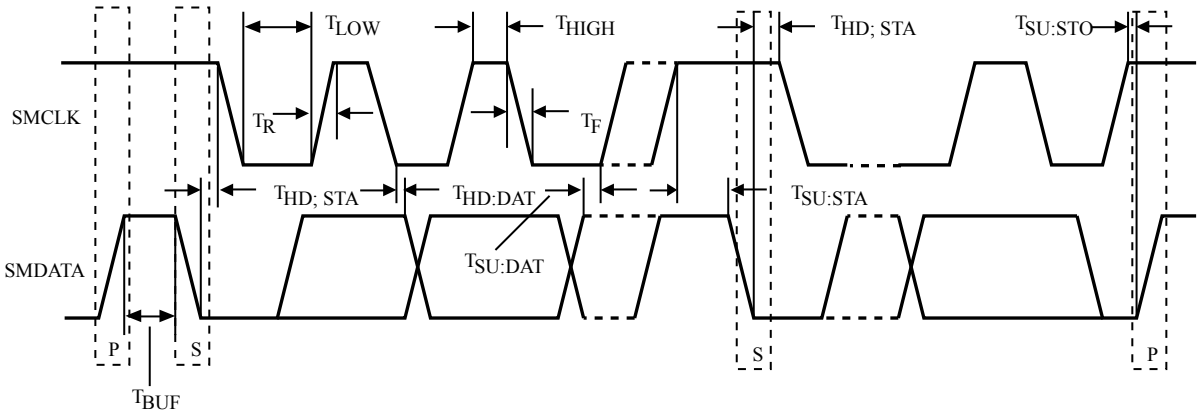
The STTS22H communicates over a 2-wire serial interface compatible with the SMBus 3.0 standard and I²C standard.

5.1 SMBus interface

5.1.1 SMBus protocol

The STTS22H communicates over a 2-wire serial interface compatible with the SMBus standard. Temperature data, alarm limits and configuration information are communicated over the bus. A detailed timing diagram is shown below in following figure.

Figure 3. SMBus timing diagram



S - start condition

P - stop condition

The STTS22H supports standard SMBus 3.0 protocols (see corresponding tables in the following sections).

- WRITE byte
- READ byte
- SEND byte
- RECEIVE byte
- Alert response address

5.1.2 WRITE byte

The WRITE byte protocol is used to write one byte of data to the registers as shown in the following table. ACK data are sent by the STTS22H while all other data are sent by the host.

Table 6. SMBus WRITE protocol

Start	Slave address	WR	ACK	Register address	ACK	data	ACK	stop
1 bit	7 bits	1 bit	1 bit	8 bits	1 bit	8 bits	1 bit	1 bit

5.1.3 READ byte

The READ byte protocol is used to read one byte of data from the registers as shown in the following table.

Table 7. SMBus READ protocol

Start	Slave address	WR	ACK	Register address	ACK	start	Slave address	RD	ACK	data	NACK	stop
1 bit	7 bits	1 bit	1 bit	8 bits	1 bit					8 bits	1 bit	1 bit

5.1.4 SEND byte

The SEND byte protocol is used to set the internal address register to the correct address. It sends a register address with no data (see following table). The SEND byte can be followed by the RECEIVE byte protocol described in the following section in order to read data from the register

Table 8. SMBus SEND protocol

Start	Slave address	WR	ACK	Register address	ACK	stop
1 bit	7 bits	1 bit	1 bit	8 bits	1 bit	1 bit

5.1.5 RECEIVE byte

The RECEIVE byte protocol is used to read data from the register when the internal register address pointer is known (see following table). This can be used for consecutive reads of the same register.

Table 9. SMBus RECEIVE protocol

Start	Slave address	RD	ACK	data	NACK	stop
1 bit	7 bits	1 bit	1 bit	8 bits	1 bit	1 bit

5.1.6 SMBus timeout

The STTS22H supports SMBus timeout which is enabled by default at power-up. This can be disabled via bit 1 in the CTRL register. When timeout is enabled, the STTS22H will time out after 30 ms (typ) of inactivity. The STTS22H supports the SMBus timeout feature. If the host holds SCL low for more than $t_{TIMEOUT}$ (max), the STTS22H resets and releases the bus. This feature is turned on by default.

5.1.7 Alert response address

The STTS22H supports the SMBus alert response address (ARA) protocol. In the event of an out-of-limit temperature measurement, the ALERT / INT output will be asserted. In response, the host (supporting the ARA protocol) will send the SMBus Alert Response Address to the general (slave) address of 0001_100b. All devices with active interrupts will respond with their client addresses (with the LSB bit set to 0). The STTS22H will acknowledge the ARA and respond with its slave device address. ARA transfer details are available in the following table.

Table 10. ARA transfer details

Start	Alert response address	RD	ACK	STTS22H slave address	NACK	Stop
1 bit	7 bit	1 bit	1 bit	8 bit	1 bit	1 bit

5.2 I²C interface

Following the correct protocols the device will behave as an I²C slave. The registers embedded inside the ASIC device may be accessed through I²C serial interfaces.

The transaction on the bus is started through a START signal. A START condition is defined as a HIGH to LOW transition on the data line while the SCL line is held HIGH (referred to as an ST condition in the following paragraph). After this signal has been transmitted by the Master, the bus is considered busy. The next byte of data transmitted after the start condition contains the address of the slave in the first 7 bits and the eighth bit tells whether the Master is receiving data from the slave or transmitting data to the slave (SAD subsequences). When an address is sent, each device in the system compares the first seven bits after a start condition with its address. If they match, the device considers itself addressed by the Master. The address can be made up of a programmable part and a fixed part, thus allowing more than one device of the same type to be connected to the I²C bus (see Table 2. STTS22H address definition).

Data transfer with acknowledge is mandatory. The transmitter must release the SDA line during the acknowledge pulse. The receiver must then pull the data line LOW so that it remains stable low during the HIGH period of the acknowledge clock pulse (SAK subsequence). A receiver which has been addressed is obliged to generate an acknowledge after each byte of data has been received. The I²C embedded inside the ASIC behaves like a slave device and the following protocol must be adhered to. After the start condition (ST) a slave address is sent, once a slave acknowledge has been returned (SAK), an 8-bit sub-address will be transmitted (SUB): the 7 LSB represent the actual register address while the MSB has no meaning. The IF_ADD_INC flag inside the CTRL register (11h) enables address auto increment, this flag is set by default to ‘1’, so the auto increment is active.

If the IF_ADD_INC bit is ‘1’, the SUB (register address) will be automatically incremented to allow multiple data read/write at increasing addresses. Otherwise if the IF_ADD_INC bit is ‘0’, the SUB will remain unchanged and multiple read/write on the same address can be performed. If the LSB of the slave address was ‘1’ (read), a repeated START (SR) condition will have to be issued after the sub-address byte; if the LSB is ‘0’ (write) the Master will transmit to the slave with direction unchanged.

5.2.1 I²C protocol

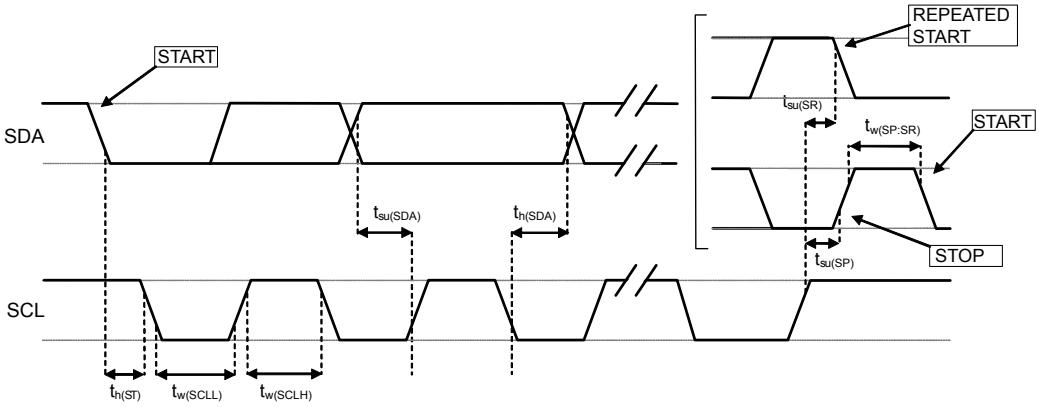
Subject to general operating conditions for V_{DD} and T_{op}.

Table 11. I²C slave timing values

Symbol	Parameter	Values with V_{DD} < 3.0 V(1)			Values with V_{DD} ≥ 3.0 V(1)		
		Min	Max	Unit	Min	Max	Unit
$f_{(SCL)}$	SCL clock frequency	10	400	kHz	0.01	1	MHz
$t_{w(SCLL)}$	SCL clock low time	1.3	-	µs	600	-	ns
$t_{w(SCLH)}$	SCL clock high time	0.6	-		160	-	
$t_{su(SDA)}$	SDA setup time	100	-		50	-	
$t_{h(SDA)}$	SDA data hold time	0	-		0	-	
$t_{h(ST)}$	START condition hold time	0.6	-		260	-	
$t_{su(SR)}$	Repeated START condition setup time	0.6	-		260	-	
$t_{su(SP)}$	STOP condition setup time	0.6	-		0.26	-	µs
$t_{w(SP:SR)}$	Bus free time between STOP and START condition	1.3	-		0.5	-	
C_b	Capacitive load for each bus line	-	400	pF	-	400	pF

1. *Data based on standard I²C protocol requirement, not tested in production. Values measured @ 25°C with V_{DD} = V_{BUS} (pull-up connected to V_{DD}).*

Figure 4. I²C slave timing diagram



5.2.2 I²C read and write sequences

The previous sequences are used to implement actual write and read sequences described in the tables below.
Transfer when the master is writing one byte to slave:

Master	ST	SAD+W		SUB		DATA		SP
Slave			SAK		SAK		SAK	

Transfer when master is writing multiple bytes to slave:

Master	ST	SAD+W		SUB		DATA		DATA		SP
Slave			SAK		SAK		SAK		SAK	

Transfer when master is receiving (reading) one byte of data from slave:

Master	ST	SAD+W		SUB		SR	SAD+R			NMAK	SP
Slave			SAK		SAK			SAK	DATA		

Transfer when master is receiving (reading) multiple bytes of data from slave:

Master	ST	SAD+W		SUB		SR	SAD+R			MAK		MAK		NMAK	SP
Slave			SAK		SAK			SAK	DATA		DATA		DATA		

Data are transmitted in byte format. Each data transfer contains 8 bits. The number of bytes transferred per transfer is unlimited. Data is transferred with the Most Significant Bit (MSB) first. If a receiver can't receive another complete byte of data until it has performed some other function, it can hold the clock line, SCL LOW to force the transmitter into a wait state. Data transfer only continues when the receiver is ready for another byte and releases the data line. If a slave receiver doesn't acknowledge the slave address (i.e. it is not able to receive because it is performing some real-time function) the data line must be left HIGH by the slave. The Master can then abort the transfer. A LOW to HIGH transition on the SDA line while the SCL line is HIGH is defined as a STOP condition (SP). Each data transfer must be terminated by the generation of a STOP condition.

6 Register description

Table 12. **Register map**

Addr	Type[1]	Name	7	6	5	4	3	2	1	0	Default
0x01	RO	WHOAMI	whoami7	whoami6	whoami5	whoami4	whoami3	whoami2	whoami1	whoami0	A0h
0x02	RW	TEMP_H_LIMIT	THL7	THL6	THL5	THL4	THL3	THL2	THL1	THL0	00h
0x03	RW	TEMP_L_LIMIT	TLL7	TLL6	TLL5	TLL4	TLL3	TLL2	TLL1	TLL0	00h
0x04	RW	CTRL	LOW_ODR _START	BDU	AVG1	AVG0	IF_ADD _INC	FREERUN	TIME_OUT _DIS	ONE_ SHOT	00h
0x05	RO	STATUS	0	0	0	0	0	UNDER_THL	OVER_THH	BUSY	output
0x06	RO	TEMP_L_OUT	T7	T6	T5	T4	T3	T2	T1	T0	output
0x07	RO	TEMP_H_OUT	T15	T14	T13	T12	T11	T10	T9	T8	output
0x0C	RW	SOFTWARE _RESET	-	LOW_ODR _ENABLE	-	-	-	-	SW_ RESET	-	00h

1. *RW designates a read/write register. RO designates a read-only register*

6.1 WHOAMI (01h) - RO

7	6	5	4	3	2	1	0
whoami7	whoami6	whoami5	whoami4	whoami3	whoami2	whoami1	whoami0

6.2 TEMP_H_LIMIT (02h) - RW

7	6	5	4	3	2	1	0
THL7	THL6	THL5	THL4	THL3	THL2	THL1	THL0

This register is used to store the unsigned value of the input for the high threshold decoder:
Threshold = (TEMP_H_LIMIT - 63)*0.64°C
If the register value is set to 00h, then the high interrupt is disabled. See Section 7 Interrupt.

6.3 TEMP_L_LIMIT (03h) - RW

7	6	5	4	3	2	1	0
TLL7	TLL6	TLL5	TLL4	TLL3	TLL2	TLL1	TLL0

This register is used to store the unsigned value of the input for the low threshold decoder:
Threshold = (TEMP_L_LIMIT - 63)*0.64°C
If the register value is set to 00h, then the low interrupt is disabled. See Section 7 Interrupt.

6.4 CTRL (04h) - RW

7	6	5	4	3	2	1	0
LOW_ODR START	BDU	AVG1	AVG0	IF_ADD_INC	FREERUN	TIME_OUT_ DIS	ONE_SHOT

LOW_ODR_START	Enables 1 Hz ODR operating mode. This bit must be set to ‘1’ only when the LOW_ODR_ENABLE bit in SOFTWARE_RESET (0Ch) - RW is set to '1' (refer to Section 9.3 Enable sequence for low-ODR mode).
BDU	Default is set to 0 for BDU disabled; 1 for BDU enabled (if BDU is used, TEMP_L_OUT must be read first).
AVG[1:0]	These bits are used to set the number of averages configuration. When in freerun mode, these bits also set the ODR (see Table 13. Average configuration).
IF_ADD_INC	If this bit is set to '1', the automatic address increment is enabled when multiple I²C read and write transactions are used.
FREERUN	Enables freerun mode (see Section 9.2 Enable sequence for freerun mode).
TIME_OUT_DIS	If this bit is set to ‘1’, the timeout function of SMBus is disabled.
ONE_SHOT	If this bit is set to 1, a new one-shot temperature acquisition is executed (see Section 9.1 Enable sequence for one-shot mode).

Table 13. Average configuration

AVG	# means	ODR when in freerun
0	8	25 Hz
1	4	50 Hz
2	2	100 Hz
3	1	200 Hz

6.5 STATUS (05h) - RO

7	6	5	4	3	2	1	0
0	0	0	0	0	UNDER_THL	OVER_THH	BUSY

UNDER_THL	0: Low limit temperature not exceeded (or disabled). 1: Low limit temperature exceeded. The bit is automatically reset to ‘0’ upon reading the STATUS register.
OVER_THH	0: High limit temperature not exceeded (or disabled). 1: High limit temperature exceeded. The bit is automatically reset to ‘0’ upon reading the STATUS register.
BUSY	The BUSY bit is applicable to one-shot mode only : 0: The conversion is complete. 1: The conversion is in progress.

6.6 TEMP_L_OUT (06h) - RO

7	6	5	4	3	2	1	0
T7	T6	T5	T4	T3	T2	T1	T0

T[7:0]	Temperature data out

6.7 TEMP_H_OUT (07h) - RO

7	6	5	4	3	2	1	0
T15	T14	T13	T12	T11	T10	T9	T8

T[15:8]	Temperature data out

6.8 SOFTWARE_RESET (0Ch) - RW

7	6	5	4	3	2	1	0
-	LOW_ODR _ENABLE	-	-	-	-	SW _RESET	-

SW_RESET	0: Enables operating mode 1: Resets all digital blocks
LOW_ODR_ENABLE	0: LOW_ODR mode not enabled 1: LOW_ODR mode selectable through bit LOW_ODR_START in CTRL (04h) - RW

7 Interrupt

There are two interrupt thresholds, 8 bits in size. If threshold registers 02h and 03h are zero, the high and low interrupts are disabled respectively.

The threshold ranges are from -39.68 °C to 122.88 °C with a step of 0.64 °C for each threshold. The value of both thresholds is calculated as follows:

Threshold = (temp_limit_reg -63) *0.64°C

Table 14. Threshold ranges of the interrupt registers

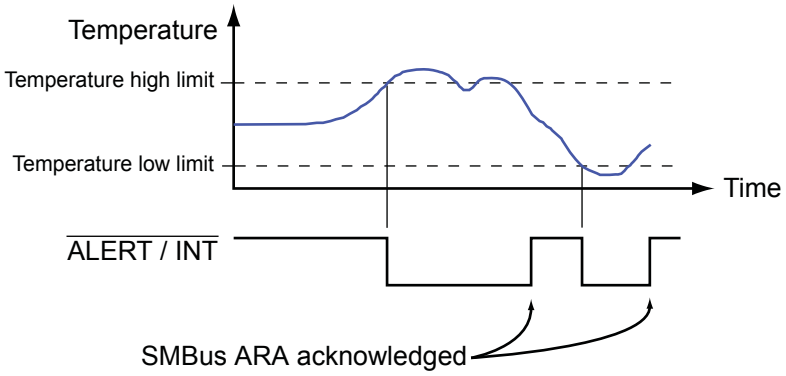
Register	Description	Threshold range
TEMP_H_LIMIT	Unsigned value, the high temperature limit is internally decoded as (TEMP_H_LIMIT-63)*0.64°C. Writing 0 disables the high limit interrupt.	-39.68 °C : 122.88 °C Step 0.64°C/LSB
TEMP_L_LIMIT	Unsigned value, the low temperature limit is internally decoded as (TEMP_L_LIMIT-63)*0.64°C. Writing 0 disables the low limit interrupt.	-39.68 °C : 122.88 °C Step 0.64°C/LSB

TEMP_H_LIMIT TEMP_L_LIMIT	Internal decoded threshold
255	Threshold set to 122.88 °C
...	...
63	Threshold set to 0 °C
...	...
1	Threshold set to -39.68 °C
0	Threshold disabled

8 ALERT / INT output

The STTS22H ALERT / INT output is open drain and requires a pull-up resistor. The ALERT / INT pin is asserted (low) whenever the temperature is equal to or exceeds the high limit or is below the low limit. Once asserted, the output will remain asserted until the STTS22H receives an SMBus Alert Response Address (ARA) from the host and acknowledges with its slave address. The output will be deasserted when the ARA is acknowledged, or the STATUS register (05h) is read by the I²C interface. If the triggering condition is still true, the output will be reasserted at the next temperature conversion. The following figure shows how the ALERT / INT output works.

Figure 5. ALERT / INT output



9 Operating modes

There are three different operating modes: freerun, one-shot and low ODR.

One-shot mode: (default) The measurement chain is switched on when the ONE_SHOT bit (bit 0 of the CTRL register) is set to '1'. When the temperature measurement is completed, the device is put in power-down condition. One-shot mode is available for measuring trigger frequencies up to 1 Hz.

Freerun mode: The measurement chain is always on. The results of temperature data measurements are updated in the output registers at each conversion. Output registers are refreshed @ODR (25 Hz, 50 Hz, 100 Hz and 200 Hz). This operating mode is active when the FREERUN bit of the CTRL register is set to logic value ‘1’.

Low-ODR mode: Temperature data are measured @ ODR = 1 Hz. This operating mode is active when the LOW_ODR_START bit of the CTRL register is set to logic value ‘1’.

Before changing the operating mode or ODR frequency, the user has to power down the device by writing '0' to both the FREERUN and LOW_ODR_START bits.

Table 15. Operating modes

FREERUN	LOW_ODR_START	Operating mode
1	0	**Freerun mode:** - Chain is always ON - Measuremenats are available @ ODR = 25 Hz, 50 Hz, 100 Hz, 200 Hz
0	0	**One-shot mode (default):** - User must ask for a conversion using the ONE_SHOT bit, then the measurement chain is shut down once the conversion ends.
0	1	**Low-ODR mode:** - Data are available @ ODR = 1 Hz

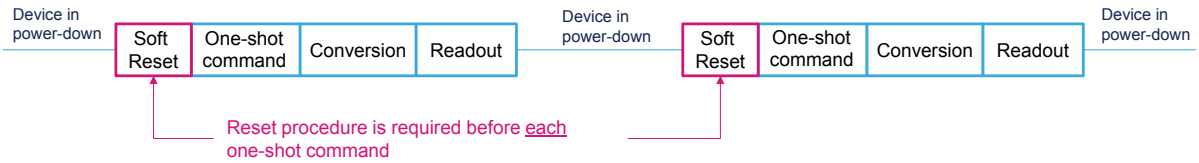
9.1 Enable sequence for one-shot mode

The following sequence must be used for each acquisition in one-shot mode:

1. Write 02h to register 0Ch [software reset]
2. Write 00h to register 0Ch [software reset]
3. Set the ONE_SHOT bit in the CTRL (04h) register [send one-shot command]

Note: After device power-on, wait at least 12 ms before accessing the register interface.

Figure 6. One-shot mode enable sequence



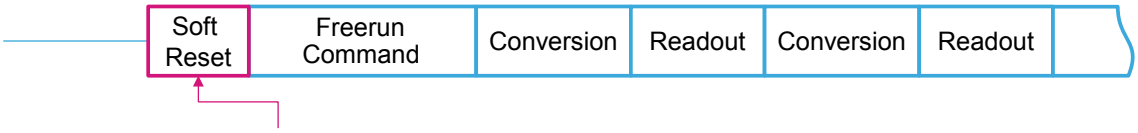
9.2 Enable sequence for freerun mode

The following sequence must be used to enable freerun mode:

1. Write 02h to register 0Ch [software reset]
2. Write 00h to register 0Ch [software reset]
3. Set the FREERUN bit in CTRL (04h) register [send freerun command]

Note: After device power-on, wait at least 12 ms before accessing the register interface.

Figure 7. Freerun/Low-ODR modes enable sequence



Reset procedure is required only when enabling FREERUN mode

9.3 Enable sequence for low-ODR mode

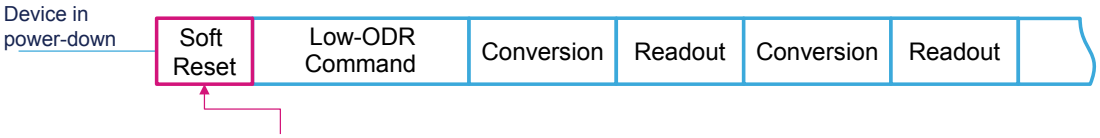
The following sequence must be used to enable low-ODR mode:

1. Write 42h to register 0Ch [software reset]
2. Write 40h to register 0Ch [software reset]
3. Set the LOW_ODR_START bit in the CTRL (04h) register [send low-ODR command]

Note: After device power-on, wait at least 12 ms before accessing the register interface.

Note: Accuracy is not guaranteed in this operating mode.

Figure 8. Low-ODR mode enable sequence



Reset procedure is required only when enabling LOW-ODR mode

10 Package information

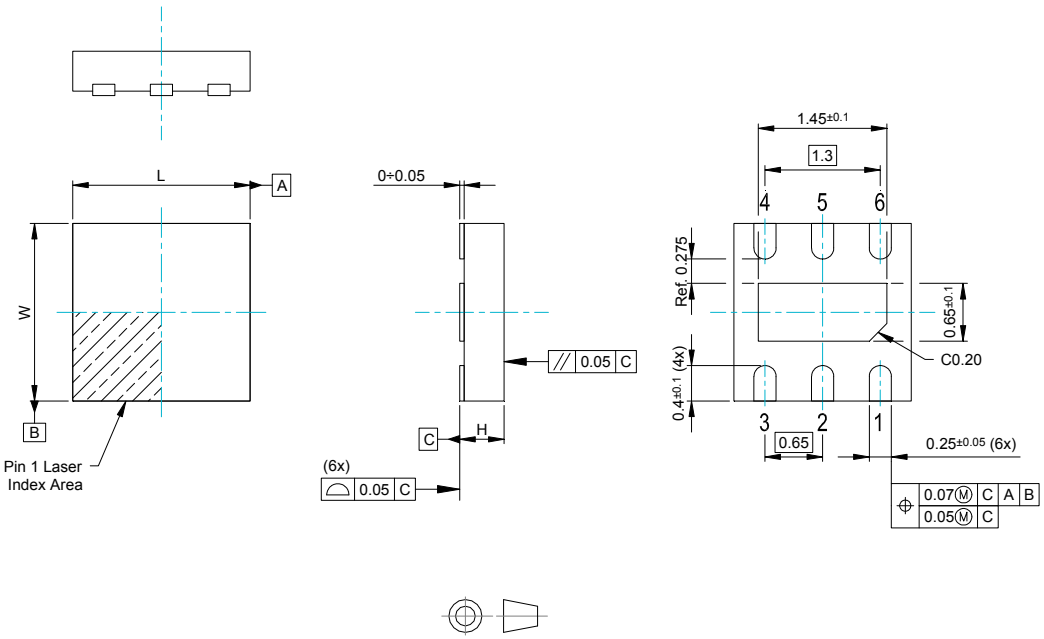
In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK packages, depending on their level of environmental compliance. ECOPACK specifications, grade definitions and product status are available at: www.st.com. ECOPACK is an ST trademark.

10.1 Soldering information

The UDFN package is compliant with the ECOPACK standard, and it is qualified for soldering heat resistance according to JEDEC J-STD-020.

10.2 UDFN-6L package information

Figure 9. UDFN-6L (2.0 x 2.0 x 0.50 mm) package outline and mechanical data



Dimensions are in millimeter unless otherwise specified
General Tolerance is +/-0.10mm unless otherwise specified

OUTER DIMENSIONS

ITEM	DIMENSION [mm]	TOLERANCE [mm]
Length [L]	2	±0.05
Width [W]	2	±0.05
Height [H]	0.55 MAX	/

DM00423052_1

Dimensions are in millimeters unless otherwise specified.

Figure 10. **Landing pattern**

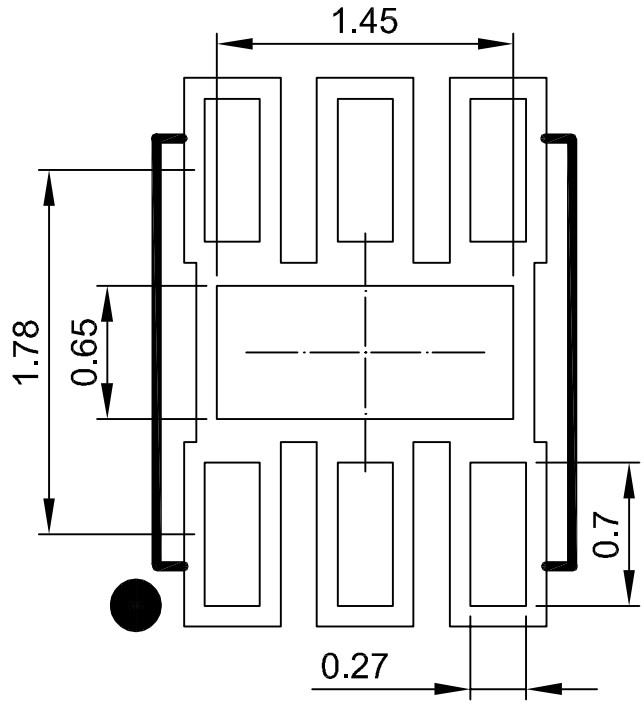
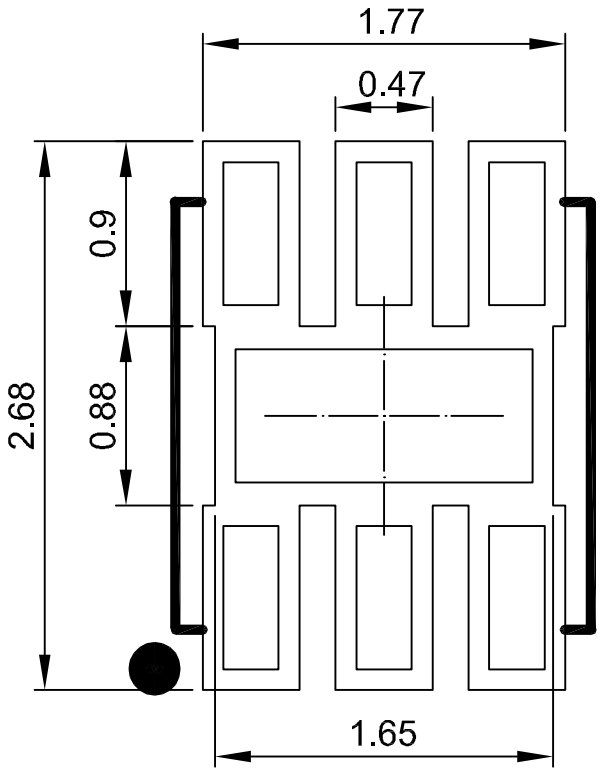
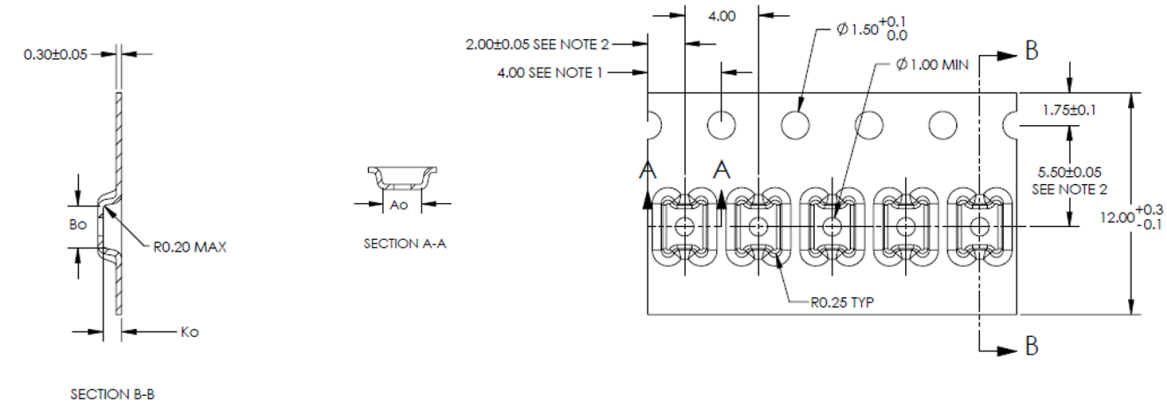


Figure 11. **PCB solder mask openings**



10.3 UDFN-6L packing information

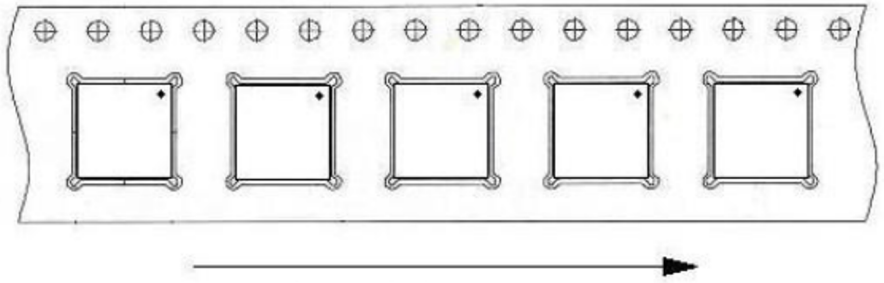
Figure 12. Carrier tape information for UDFN-6L package



NOTES:
1. 10 SPROCKET HOLE PITCH CUMULATIVE TOLERANCE ±0.2
2. POCKET POSITION RELATIVE TO SPROCKET HOLE MEASURED AS TRUE POSITION OF POCKET, NOT POCKET HOLE.
3. Ao AND Bo ARE CALCULATED ON A PLANE AT A DISTANCE "R" ABOVE THE BOTTOM OF THE POCKET.

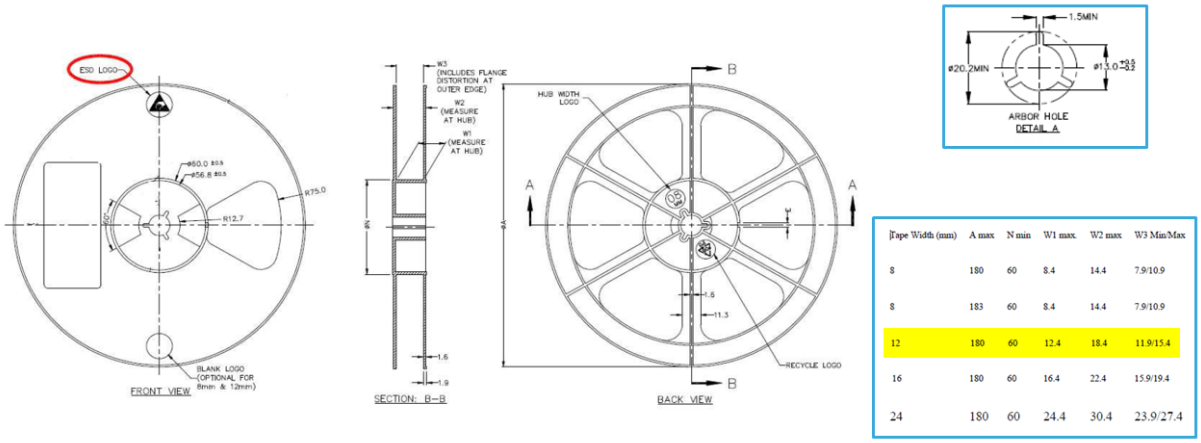
	DIM	±
Ao	2.30	0.05
Bo	2.30	0.05
Ko	1.00	0.1

Figure 13. UDFN-6L package orientation in carrier tape

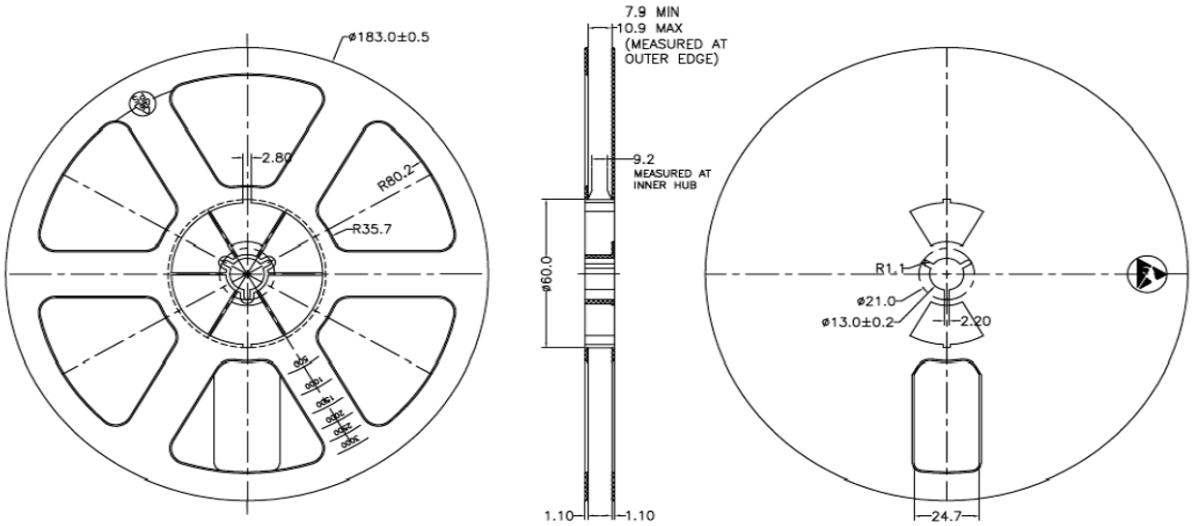


User direction of feed

Figure 14. Reel information



Tape Width (mm)	A max	N min	W1 max	W2 max	W3 Min/Max
8	180	60	8.4	14.4	7.9/10.9
8	183	60	8.4	14.4	7.9/10.9
12	180	60	12.4	18.4	11.9/15.4
16	180	60	16.4	22.4	15.9/19.4
24	180	60	24.4	30.4	23.9/27.4


ø183.0±0.5
2.80
R80.2
R35.7
7.9 MIN
10.9 MAX
(MEASURED AT
OUTER EDGE)
9.2
MEASURED AT
INNER HUB
ø60.0
1.10
1.10
R1.1
ø21.0
ø13.0±0.2
2.20
24.7

Revision history

Table 16. **Document revision history**

Date	Version	Changes
09-Oct-2019	4	First public release

Contents

List of tables

List of figures

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