LP2992 Micropower 250-mA Low-Noise Ultra-Low-Dropout Regulator in SOT-23 and WSON Packages Designed for Use With Very Low-ESR Output Capacitors

1 Features

- Input Voltage Range: 2.2 V to 16 V
- Output Voltage Range: 1.5 V to 5 V
- Wide Supply Voltage Range (16-V Maximum)
- Output Voltage Accuracy 1% (A Grade)
- Ultra-Low-Dropout Voltage
- Specified 250-mA Output Current
- Stable With Low-ESR Output Capacitor
- < 1-µA Quiescent Current When Shut Down
- Low Ground Pin Current at All Loads
- High Peak Current Capability
- Low Z_{OUT}: 0.3-Ω Typical (10 Hz to 1 MHz)
- Overtemperature and Overcurrent Protection
- −40°C to +125°C Junction Temperature Range
- Smallest Possible Size (SOT-23, WSON Package)
- Requires Minimum External Components
- Custom Voltages Available

2 Applications

- Cellular Phones
- Palmtop/Laptop Computers
- Personal Digital Assistants (PDA)
- Camcorders, Personal Stereos, Cameras

3 Description

The LP2992 is a 250-mA, fixed-output voltage regulator designed to provide ultra-low dropout and low noise in battery-powered applications.

Using an optimized vertically integrated PNP (VIP) process, the LP2992 delivers unequaled performance in all specifications critical to battery-powered designs:

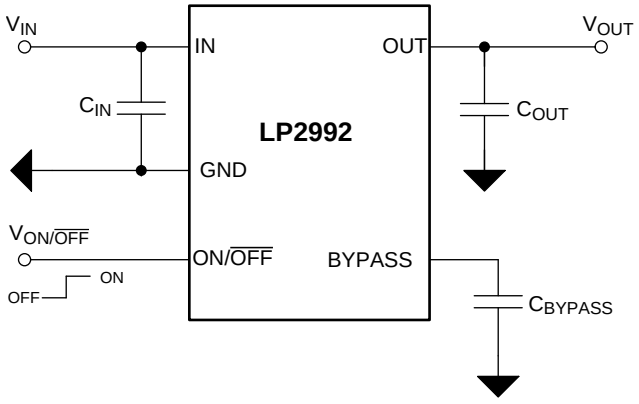
- Dropout voltage: Typically 450 mV at 250-mA load, and 5 mV at 1-mA load.
- Ground pin current: Typically 1500 µA at 250-mA load, and 75 µA at 1-mA load.
- Enhanced stability: The LP2992 is stable with output capacitor equivalent series resistance (ESR) as low as 5 mΩ, which allows the use of ceramic capacitors on the output.
- Sleep mode: Less than 1-µA quiescent current when ON/$\overline{\text{OFF}}$ pin is pulled low.
- Smallest possible size: SOT-23 and WSON packages use absolute minimum board space.
- Precision output: 1% tolerance output voltages available (A grade).
- Low noise: By adding a 10-nF bypass capacitor, output noise can be reduced to 30 µV (typical).
- Multiple voltage options, from 1.5 V to 5 V, are available as standard products. Consult factory for custom voltages.

Device Information[1]

PART NUMBER	PACKAGE	BODY SIZE (NOM)
LP2992	WSON (6)	3.29 mm × 2.92 mm
	SOT-23 (5)	2.90 mm × 1.60 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.

Simplified Schematic



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4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision I (November 2015) to Revision J — **Page**

- Deleted specific values from capacitors in *Simplified Schematic* drawing ... 1
- Added *Receiving Notification of Documentation Updates* ... 22

Changes from Revision H (January 2015) to Revision I — **Page**

- Added top navigator icon for TI Design ... 1
- Changed "174.2°C/W" to "169.7°C/W" in footnote 3 to *Abs Max* table. ... 4
- Changed *ESD Ratings* table to differentiate different values for different pins/packages. ... 4
- Added new footnotes 2 and 3 to *Thermal Information* table; update thermal values for DBV (SOT-23) package. ... 5
- Added *Power Dissipation* and *Estimating Junction Temperature* subsections ... 18
- Added additional related document links ... 22

Changes from Revision G (March 2013) to Revision H — **Page**

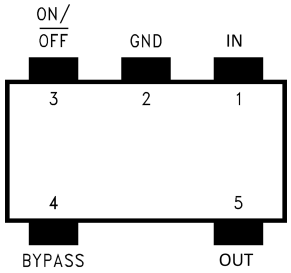
- Added *Device Information* and *ESD Ratings* tables, *Pin Configuration and Functions*, *Feature Description* , *Device Functional Modes*, *Application and Implementation*, *Power Supply Recommendations*, *Layout* , *Device and Documentation Support* , and *Mechanical, Packaging, and Orderable Information* sections; update *Thermal Values* and pin names ... 1

Changes from Revision F (March 2013) to Revision G — **Page**

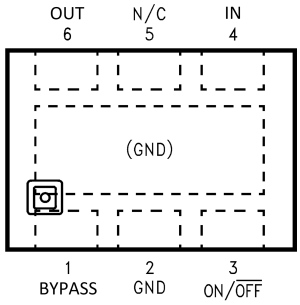
- Changed Changed layout of National Semiconductor data sheet to TI format ... 1

5 Pin Configuration and Functions

DBV Package
5-Pin SOT-23
Top View



NGD Package
6-Pin WSON
Top View



Pin Functions

PIN				I/O	DESCRIPTION
NAME	DBV	NAME	NGD		
BYPASS	4	BYPASS	1	I	Bypass capacitor for low-noise operation.
GND	2	GND	2	–	Ground.
IN	1	IN	4	I	Unregulated input voltage.
–	–	N/C	5	–	No internal connection. Connect to GND or leave open.
ON/$\overline{\text{OFF}}$	3	ON/$\overline{\text{OFF}}$	3	I	A low voltage on this pin disables the device, and the regulator enters a sleep mode. A high voltage on this pin enables the device.
OUT	5	OUT	6	O	Regulated output voltage. This pin requires an output capacitor to maintain stability. See the *Detailed Design Procedure* for output capacitor details.
—	—	DAP	Exposed thermal pad	—	The exposed die attach pad on the bottom of the package must be connected to a copper thermal pad on the PCB at ground potential. Connect to ground potential or leave floating. Do not connect to any potential other than the same ground potential seen at device pin 2.

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)(2)

	MIN	MAX	UNIT
Lead temperature (soldering, 5 seconds)		260	°C
Power dissipation(3)	Internally Limited		
Input supply voltage (survival)	−0.3	16	V
Shutdown input voltage (survival)	−0.3	16	V
Output voltage (survival)(4)	−0.3	9	V
I_{OUT} (survival)	Short-circuit protected		
Input-output voltage (survival)(5)	−0.3	16	V
Storage temperature, T_{stg}	−65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) If Military- or Aerospace-specified devices are required, contact the Texas Instruments Sales Office/Distributors for availability and specifications.
(3) The maximum allowable power dissipation is a function of the maximum junction temperature, $T_{J(MAX)}$, the junction-to-ambient thermal resistance, $R_{\theta JA}$, and the ambient temperature, T_A. The maximum allowable power dissipation at any ambient temperature is calculated using:
$P_{(MAX)} = (T_{J(MAX)} – T_A) / R_{\theta JA}$
Where the value of $R_{\theta JA}$ for the SOT-23 package is 169.7°C/W in a typical PC board mounting and the WSON package is 72.3°C/W. Exceeding the maximum allowable dissipation causes excessive die temperature, and the regulator goes into thermal shutdown.
(4) If used in a dual-supply system where the regulator load is returned to a negative supply, the LP2992 output must be diode-clamped to ground.
(5) The output PNP structure contains a diode between the IN to OUT pins that is normally reverse-biased. Reversing the polarity from V_{IN} to V_{OUT} turns on this diode.

6.2 ESD Ratings

				VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	Pins 3 and 4 (SOT) Pins 1 and 3 (WSON)	±1000	V
			All pins except 3 and 4 (SOT) All pins except 1 and 3 (WSON)	±2000	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	MAX	UNIT
V_{IN}	Input supply voltage	2.2(1)	16	V
$V_{ON/\overline{OFF}}$	ON/$\overline{OFF}$ input voltage	0	V_{IN}	V
I_{OUT}	Output current		250	mA
T_J	Operating junction temperature	–40	125	°C

(1) Recommended minimum V_{IN} is the greater of 2.2 V or V_{OUT} + rated dropout voltage (maximum) for operating load current.

6.4 Thermal Information

THERMAL METRIC[1]		LP2992		UNIT
		DBV (SOT-23)	NGD (WSON)[2]	
		5 PINS	6 PINS	
$R_{\theta JA}$[3]	Junction-to-ambient thermal resistance	169.7	72.3	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance, High K	122.6	81.6	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	29.9	39.5	°C/W
ψ_{JT}	Junction-to-top characterization parameter	16.7	2.0	°C/W
ψ_{JB}	Junction-to-board characterization parameter	29.4	39.2	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	n/a	11.6	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics*.
(2) The PCB for the NGD (WSON) package $R_{\theta JA}$ includes two (2) thermal vias under the exposed thermal pad per EIA/JEDEC JESD51-5.
(3) Thermal resistance value $R_{\theta JA}$ is based on the EIA/JEDEC High-K printed circuit board defined by: JESD51-7 - High Effective Thermal Conductivity Test Board for Leaded Surface Mount Packages.

6.5 Electrical Characteristics

Unless otherwise specified: $V_{IN} = V_{OUT(NOM)} + 1$ V, $I_L = 1$ mA, $C_{IN} = 1$ µF, $C_{OUT} = 4.7$ µF, $V_{ON/\overline{OFF}} = 2$ V. MIN (minimum) and MAX (maximum) limits apply over the recommended operating temperature range unless otherwise noted; typical limits apply for $T_A = T_J = 25°C$.

PARAMETER		TEST CONDITIONS	TYP	LP2992AI-X.X[1]		LP2992I-X.X[1]		UNIT
				MIN	MAX	MIN	MAX	
ΔV_{OUT}	Output voltage tolerance	I_L = 1 mA, T_J = 25°C		−1	1	−1.5	1.5	$\%V_{NOM}$
		1 mA ≤ I_L ≤ 50 mA, T_J = 25°C		−1.5	1.5	−2.5	2.5	
		1 mA ≤ I_L ≤ 50 mA		−2.5	2.5	−3.5	3.5	
		1 mA ≤ I_L ≤ 250 mA, T_J = 25°C		−3.5	3.5	−4	4	
		1 mA ≤ I_L ≤ 250 mA		−4.5	4.5	−5	5	
$\Delta V_{OUT}/\Delta V_{IN}$	Output voltage line regulation	$V_{OUT(NOM)}$ + 1 V ≤ V_{IN} ≤ 16 V T_J = 25°C	0.007		0.014		0.014	%/V
		$V_{OUT(NOM)}$ + 1 V ≤ V_{IN} ≤ 16 V			0.032		0.032	
V_{IN}(min)	Minimum input voltage required to maintain output regulation		2.05		2.2		2.2	V
$V_{IN} - V_{OUT}$	Dropout voltage[2]	I_L = 0 mA, T_J = 25°C	0.5		2.5		2.5	mV
		I_L = 0 mA			4		4	
		I_L = 1 mA, T_J = 25°C	5		9		9	
		I_L = 1 mA			12		12	
		I_L = 50 mA, T_J = 25°C	100		125		125	
		I_L = 50 mA			180		180	
		I_L = 150 mA, T_J = 25°C	260		325		325	
		I_L = 150 mA			470		470	
		I_L = 250 mA, T_J = 25°C	450		575		575	
		I_L = 250 mA			850		850	

(1) Limits are 100% production tested at 25°C. Limits over the operating temperature range are specified through correlation using Statistical Quality Control (SQC) methods. The limits are used to calculate TI's Average Outgoing Quality Level (AOQL).
(2) V_{IN} must be the greater of 2.2 V or $V_{OUT(NOM)}$ + dropout voltage to maintain output regulation. Dropout voltage is defined as the input-to-output differential at which the output voltage drops 2% below the value measured with a 1-V differential.

Electrical Characteristics (continued)

Unless otherwise specified: $V_{IN} = V_{OUT(NOM)} + 1$ V, $I_L = 1$ mA, $C_{IN} = 1$ µF, $C_{OUT} = 4.7$ µF, $V_{ON/\overline{OFF}} = 2$ V. MIN (minimum) and MAX (maximum) limits apply over the recommended operating temperature range unless otherwise noted; typical limits apply for $T_A = T_J = 25°C$.

PARAMETER		TEST CONDITIONS	TYP	LP2992AI-X.X(1)		LP2992I-X.X(1)		UNIT
				MIN	MAX	MIN	MAX	
I_{GND}	Ground pin current	I_L = 0 mA, T_J = 25°C	65		95		95	µA
		I_L = 0 mA			125		125	
		I_L = 1 mA, T_J = 25°C	75		110		110	
		I_L = 1 mA			170		170	
		I_L = 50 mA, T_J = 25°C	350		600		600	
		I_L = 50 mA			1000		1000	
		I_L = 150 mA, T_J = 25°C	850		1500		1500	
		I_L = 150 mA			2500		2500	
		I_L = 250 mA, T_J = 25°C	1500		2300		2300	
		I_L = 250 mA			4000		4000	
		$V_{ON/\overline{OFF}}$ < 0.3 V, T_J = 25°C	0.01		0.8		0.8	
		$V_{ON/\overline{OFF}}$ < 0.15 V	0.05		2		2	
$V_{ON/\overline{OFF}}$	ON/$\overline{OFF}$ input voltage(3)	High = O/P ON	1.4	1.6		1.6		V
		Low = O/P OFF	0.55		0.15		0.15	
$I_{ON/\overline{OFF}}$	ON/$\overline{OFF}$ input current	$V_{ON/\overline{OFF}}$ = 0	0.01		–2		–2	µA
		$V_{ON/\overline{OFF}}$ = 5 V	5		15		15	
e_n	Output noise voltage (RMS)	Bandwidth = 300 Hz to 50 kHz C_{OUT} = 10 µF C_{BYPASS} = 10 nF	30					µV
$\Delta V_{OUT}/\Delta V_{IN}$	Ripple rejection	f = 1 kHz, C_{BYPASS} = 10 nF C_{OUT} = 10 µF	45					dB
I_O(SC)	Short-circuit current	R_L = 0 (steady state)(4)	400					mA
I_O(PK)	Peak output current	$V_{OUT} \geq V_{O(NOM)} - 5\%$	350					mA

(3) The ON/$\overline{OFF}$ input must be properly driven to prevent possible mis-operation. For details, see *Operation with ON/$\overline{OFF}$ Control*.
(4) The LP2992 has thermal foldback current limiting which allows a high peak current when $V_{OUT} > 0.5$ V, and then reduces the maximum output current as V_{OUT} is forced to ground (see *Typical Characteristics* curves).

6.6 Typical Characteristics

Unless otherwise specified: C_{IN} = 1 µF, C_{OUT} = 4.7 µF, V_{IN} = $V_{OUT(NOM)}$ + 1 V, T_A = 25°C, ON/$\overline{OFF}$ pin is tied to the IN pin.

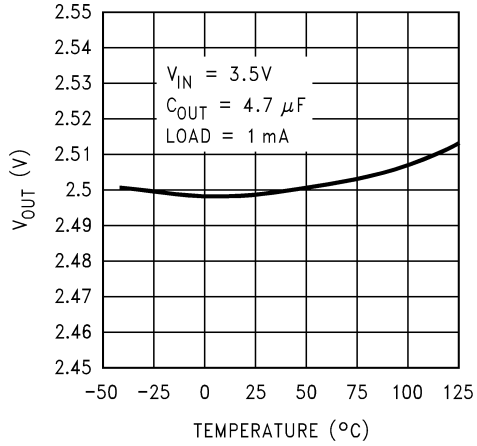


Figure 1. V_{OUT} vs Temperature

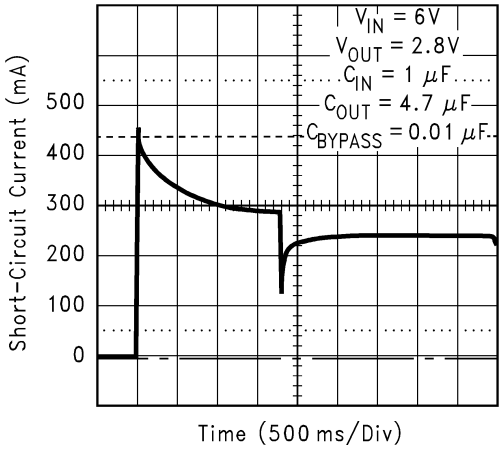


Figure 2. Short-Circuit Current

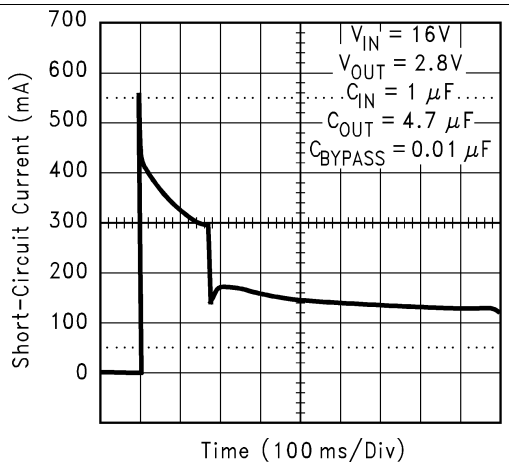


Figure 3. Short-Circuit Current

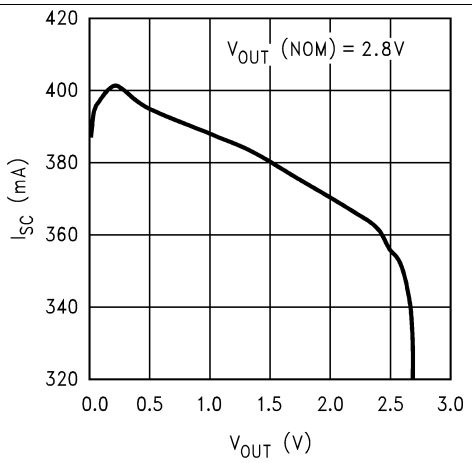


Figure 4. Short-Circuit Current vs Output Voltage

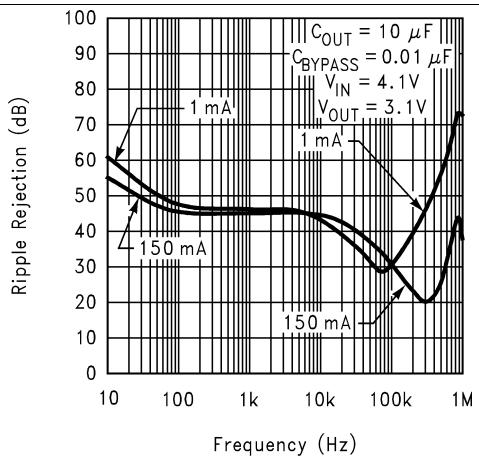


Figure 5. Ripple Rejection

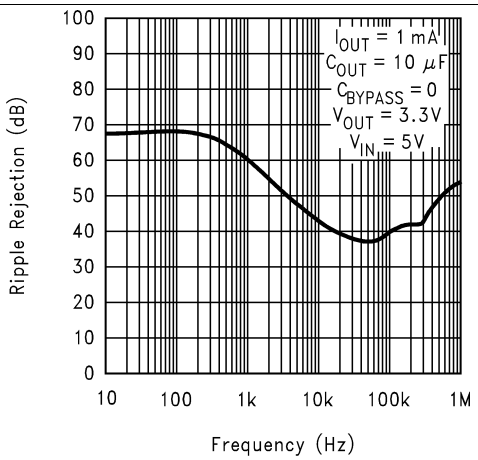


Figure 6. Ripple Rejection

Typical Characteristics (continued)

Unless otherwise specified: C_{IN} = 1 µF, C_{OUT} = 4.7 µF, V_{IN} = $V_{OUT(NOM)}$ + 1 V, T_A = 25°C, ON/$\overline{OFF}$ pin is tied to the IN pin.

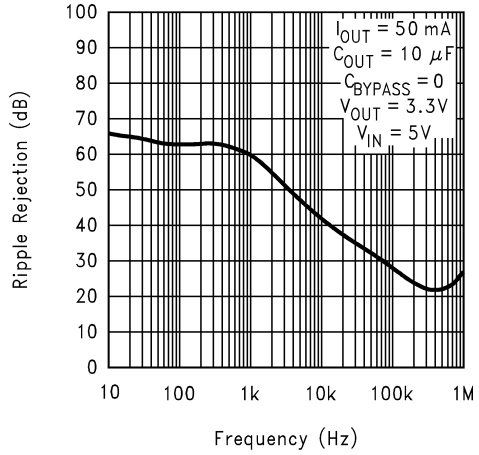


Figure 7. Ripple Rejection

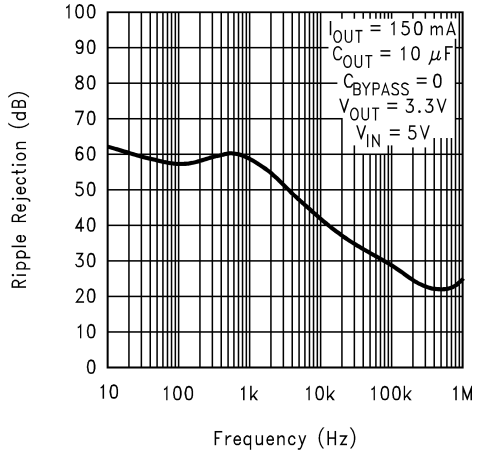


Figure 8. Ripple Rejection

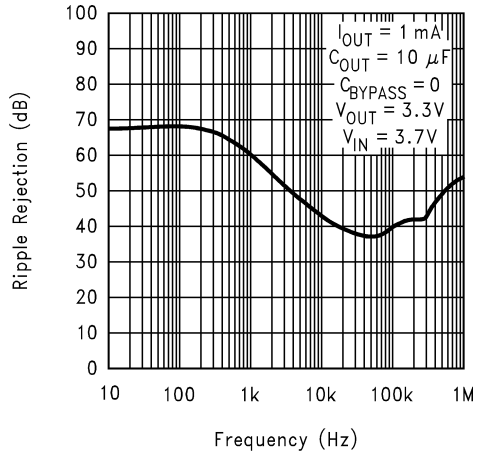


Figure 9. Ripple Rejection

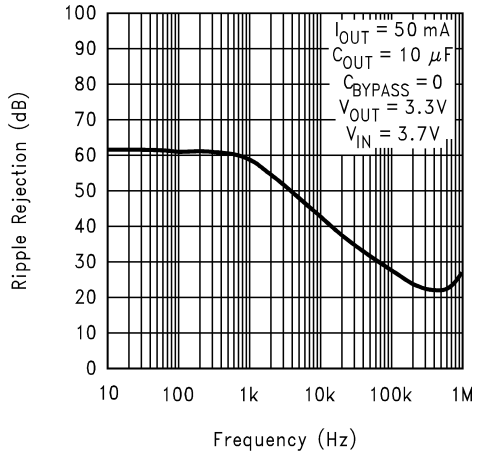


Figure 10. Ripple Rejection

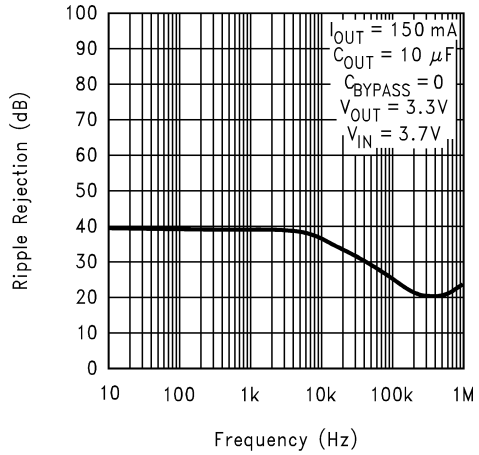


Figure 11. Ripple Rejection

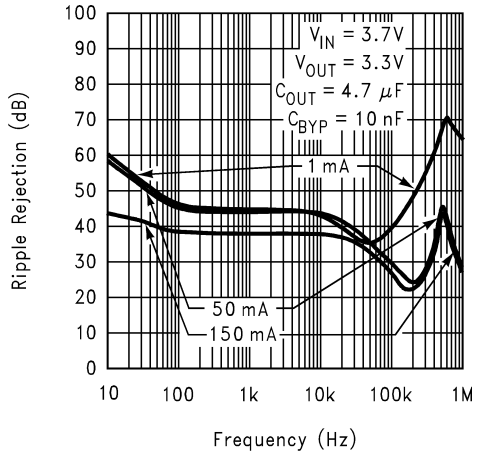


Figure 12. Ripple Rejection

Typical Characteristics (continued)

Unless otherwise specified: C_{IN} = 1 µF, C_{OUT} = 4.7 µF, V_{IN} = $V_{OUT(NOM)}$ + 1 V, T_A = 25°C, ON/$\overline{OFF}$ pin is tied to the IN pin.

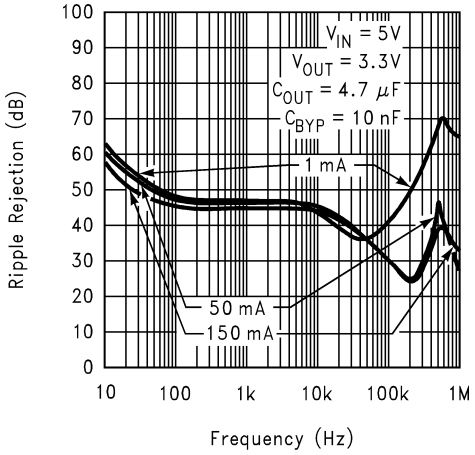


Figure 13. Ripple Rejection

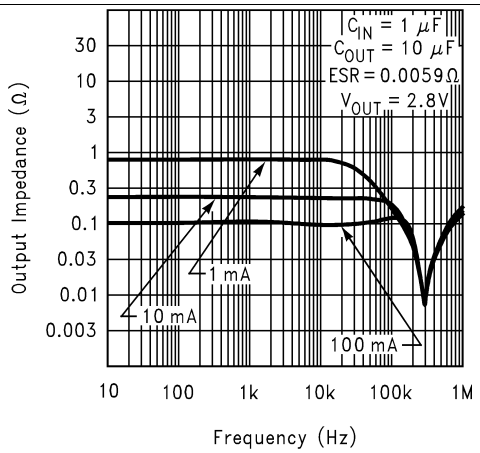


Figure 14. Output Impedance vs Frequency

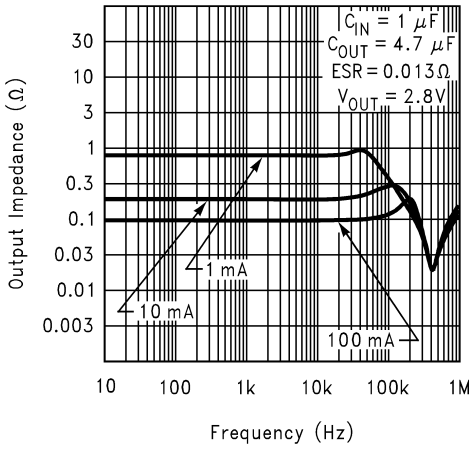


Figure 15. Output Impedance vs Frequency

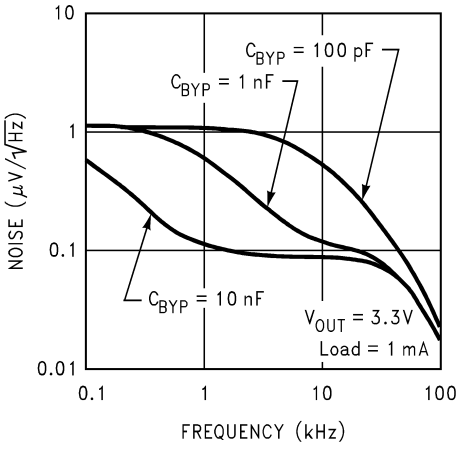


Figure 16. Output Noise Density

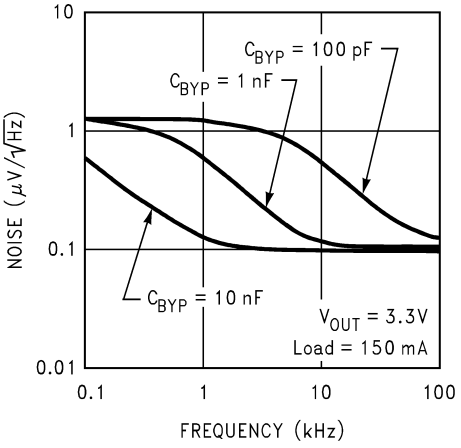


Figure 17. Output Noise Density

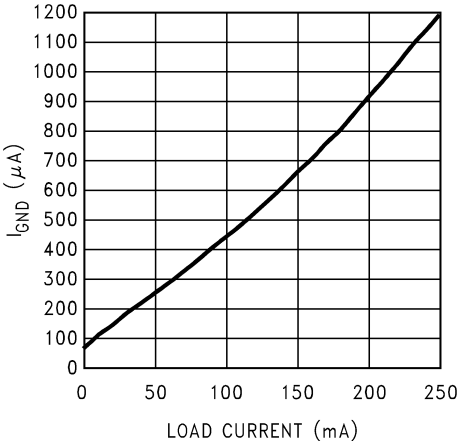


Figure 18. GND Pin vs Load Current

Typical Characteristics (continued)

Unless otherwise specified: C_{IN} = 1 µF, C_{OUT} = 4.7 µF, V_{IN} = $V_{OUT(NOM)}$ + 1 V, T_A = 25°C, ON/$\overline{OFF}$ pin is tied to the IN pin.

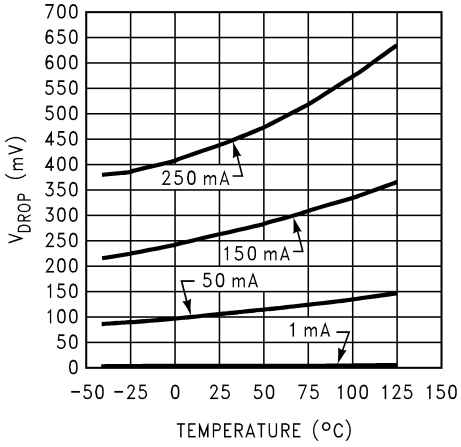


Figure 19. Dropout Voltage vs Temperature

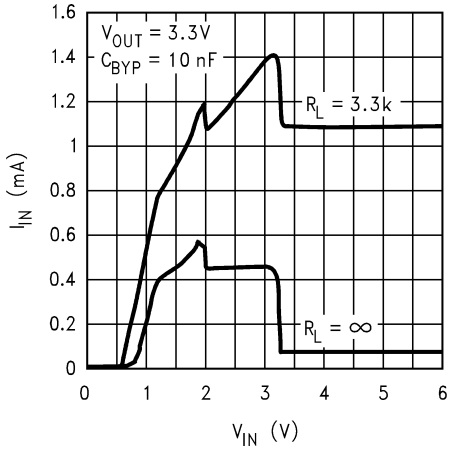


Figure 20. Input Current vs Pin

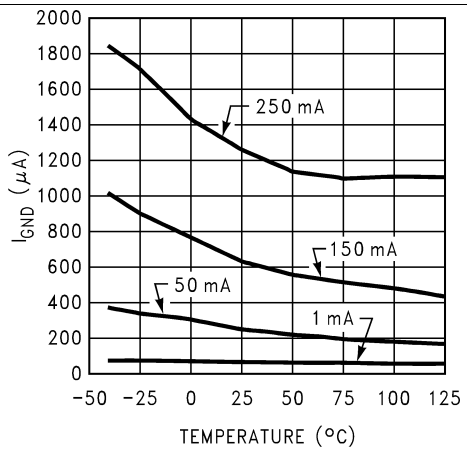


Figure 21. I_{GND} vs Load and Temperature

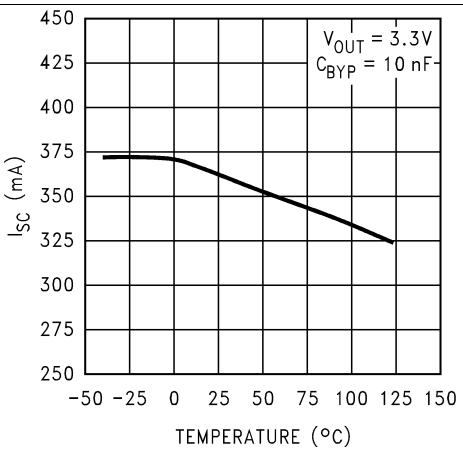


Figure 22. Instantaneous Short-Circuit Current

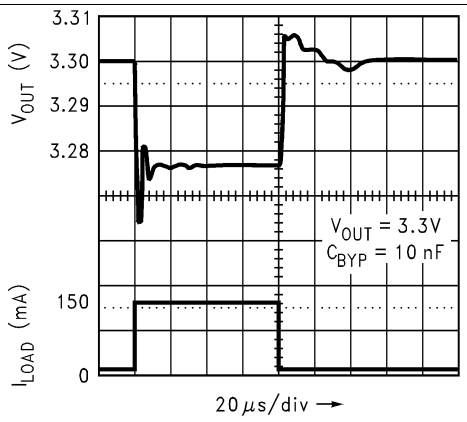


Figure 23. Load Transient Response

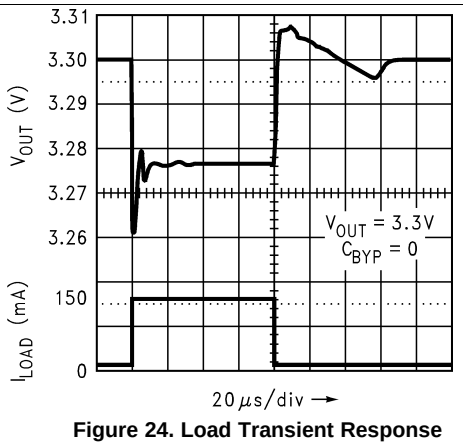


Figure 24. Load Transient Response

Typical Characteristics (continued)

Unless otherwise specified: C_{IN} = 1 µF, C_{OUT} = 4.7 µF, V_{IN} = $V_{OUT(NOM)}$ + 1 V, T_A = 25°C, ON/$\overline{OFF}$ pin is tied to the IN pin.

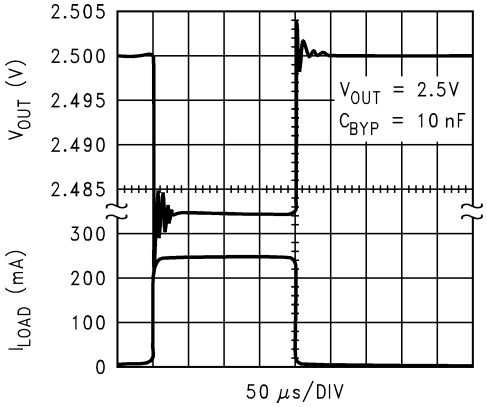


Figure 25. Load Transient Response

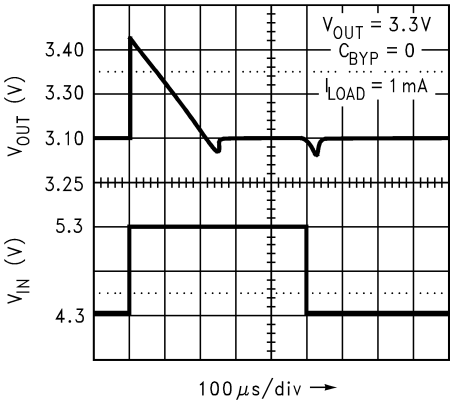


Figure 26. Line Transient Response

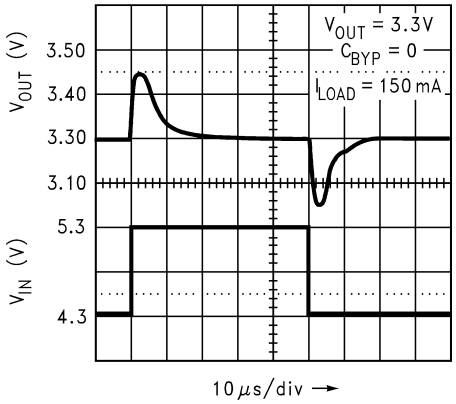


Figure 27. Line Transient Response

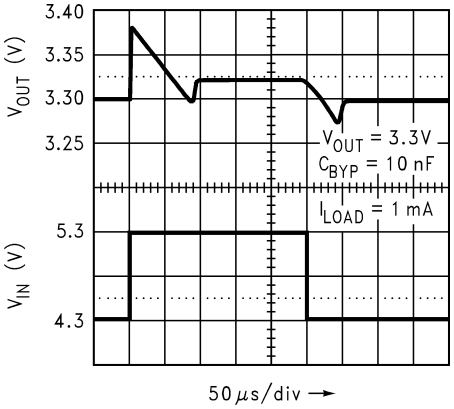


Figure 28. Line Transient Response

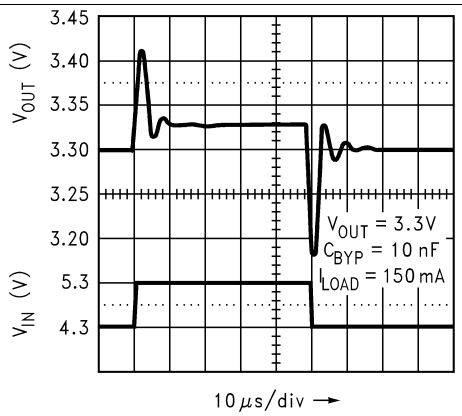


Figure 29. Line Transient Response

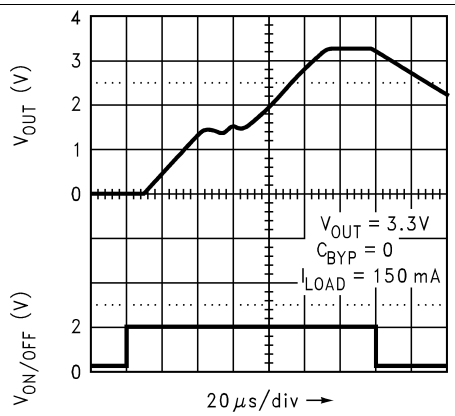


Figure 30. Turnon Time

Typical Characteristics (continued)

Unless otherwise specified: C_{IN} = 1 µF, C_{OUT} = 4.7 µF, V_{IN} = $V_{OUT(NOM)}$ + 1 V, T_A = 25°C, ON/$\overline{OFF}$ pin is tied to the IN pin.

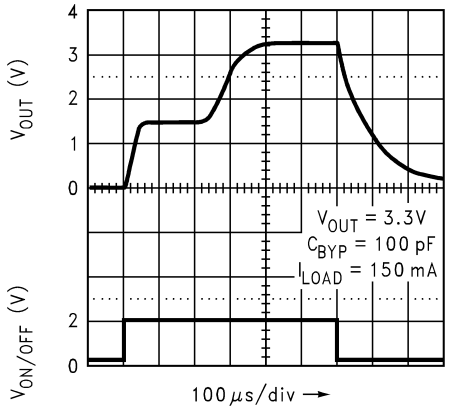


Figure 31. Turnon Time

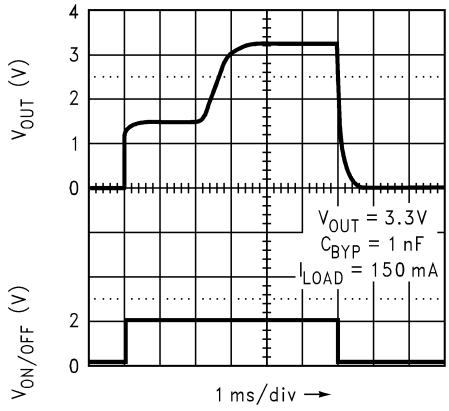


Figure 32. Turnon Time

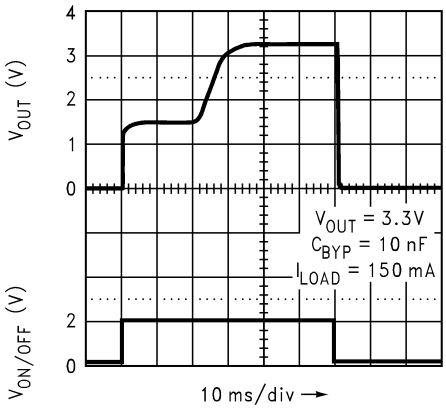


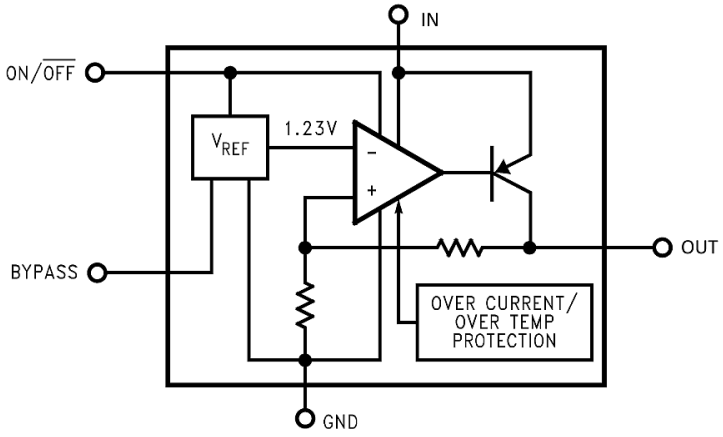
Figure 33. Turnon Time

7 Detailed Description

7.1 Overview

The LP2992 family of fixed-output, ultralow-dropout, and low-noise regulators offer exceptional and cost-effective performance for battery-powered applications. Available in output voltages from 1.5 V to 5 V, the family has an output tolerance of 1% for the A version and is capable of delivering 250-mA continuous load current. Using an optimized vertically integrated PNP (VIP) process, the LP2992 delivers unequaled performance. The dropout voltage and the GND pin current with 250 mA of load current are typically 450 mV and 1500 µA, respectively.

7.2 Functional Block Diagram



7.3 Feature Description

7.3.1 Sleep Mode

When the ON/$\overline{\text{OFF}}$ pin is pulled low, the LP2992 enters a sleep mode, and less than 1-µA quiescent current is consumed. This function is designed for the application which needs a sleep mode to effectively enhance battery life cycle.

7.3.2 Low Ground Current

The LP2992 uses a vertical PNP process which allows for quiescent currents which are considerably lower than those associated with traditional lateral PNP regulators, typically 1500 µA at 250-mA load and 75 µA at 1-mA load.

7.3.3 Low Noise

The LP2992 includes a low-noise reference ensuring minimal noise during operation because the internal reference is normally the dominant term in a noise analysis. Further noise reduction can be achieved by adding an external bypass capacitor between the BYPASS pin and the GND pin. For more detailed information on noise reduction using the BYPASS pin, see *Noise Bypass Capacitor*.

7.3.4 Enhanced Stability

The LP2992 is designed specifically to work with ceramic output capacitors using circuitry that allows the regulator to be stable across the entire range of output current with an output capacitor whose ESR is as low as 5 mΩ. For output capacitor requirements, see *Output Capacitor*.

Feature Description (continued)

7.3.5 Overcurrent Protection

The internal current-limit circuit is used to protect the LDO against high-current faults or shorting events. The LDO is not designed to operate in a steady-state current limit. During a current-limit event, the LDO sources constant current. Therefore, the output voltage falls when the output impedance decreases. Note also that if a current limit occurs and the resulting output voltage is low, excessive power may be dissipated across the LDO, resulting in a thermal shutdown of the output.

The LP2992 is featured with the foldback current limit that allows a high peak current when V_{OUT} > 0.5 V, and then reduces the maximum output current as V_{OUT} is forced to ground.

7.3.6 Overtemperature Protection

The LP2992 is designed with the thermal shutdown circuitry to turn off the output when excessive heat is dissipated in the LDO. The internal protection circuitry of the LP2992 is designed to protect against thermal overload conditions. Continuously running the device into thermal shutdown degrades its reliability.

7.4 Device Functional Modes

7.4.1 Operation with $V_{OUT(TARGET)}$ + 0.9 V ≥ V_{IN} ≥ 16 V

The LP2992 operates if the input voltage is equal to or exceeds $V_{OUT(TARGET)}$ + 0.9 V. At input voltages below the minimum V_{IN} requirement, the device does not operate correctly and output voltage may not reach a target value.

7.4.2 Operation with ON/$\overline{\text{OFF}}$ Control

If the voltage on the ON/$\overline{\text{OFF}}$ pin is less than 0.15 V, the device is disabled and, in this shutdown state, current does not exceed 2 µA. Raising the voltage at the ON/$\overline{\text{OFF}}$ pin above 1.6 V initiates the start-up sequence of the device. If this feature is not to be used, the ON/$\overline{\text{OFF}}$ input must be tied to V_{IN} to keep the regulator output on at all times.

To assure proper operation, the signal source used to drive the ON/$\overline{\text{OFF}}$ input must be able to swing above and below the specified turnon/turnoff voltage thresholds listed in the *Electrical Characteristics* section under $V_{ON/\overline{OFF}}$. To prevent mis-operation, the turnon (and turnoff) voltage signals applied to the ON/$\overline{\text{OFF}}$ input must have a slew rate which is ≥ 40 mV/µs.

CAUTION

The regulator output voltage can not be ensured if a slow-moving AC (or DC) signal is applied that is in the range between the specified turnon and turnoff voltages listed under the electrical specification $V_{ON/OFF}$ (see *Electrical Characteristics*).

8 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

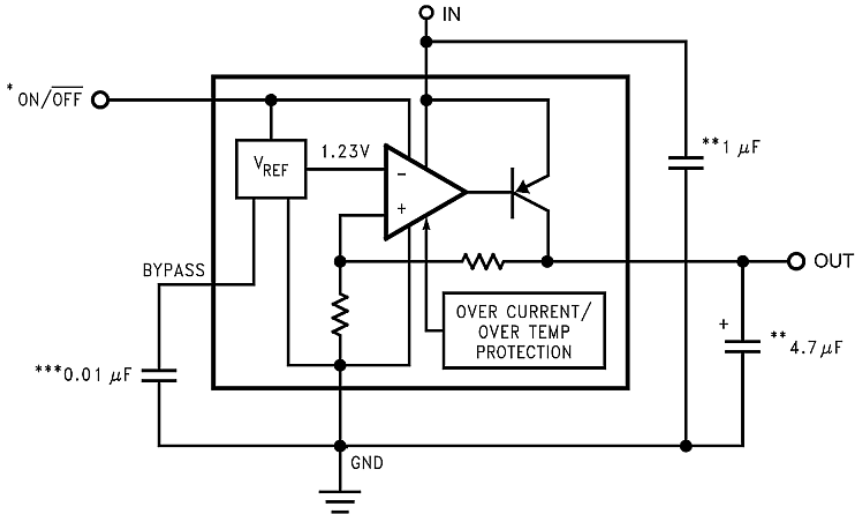
8.1 Application Information

The LP2992 is a 250-mA, fixed-output voltage regulator designed to provide ultralow-dropout and low noise in battery powered applications. The device is stable with output capacitor equivalent series resistance (ESR) as low as 5 mΩ which allows the use of ceramic capacitors on the output.

At 250-mA loading, the dropout voltage of the LP2992 is 850 mV maximum over temperature; thus, 1000-mV headroom is sufficient for operation over input and output voltage accuracy. The efficiency of the LP2992 in this configuration is V_{OUT}/V_{IN} = 76.7%. To achieve the smallest form factor, the SOT-23 package is selected.

Input and output capacitors are selected in accordance with *Capacitor Characteristics*. Ceramic capacitance of 1 µF for the input and that of 4.7 µF for the output are selected. With efficiency of 76.7% and a 250-mA load current, the internal power dissipation is 250 mW, which corresponds to 43.55°C junction temperature rise for the SOT-23 package. To minimize noise, a bypass capacitor (C_{BYPASS}) of 0.01 µF is selected.

8.2 Typical Application



*ON/$\overline{OFF}$ input must be actively terminated. Tie to the IN pin if this function is not to be used.
**Minimum capacitance is shown to ensure stability (may be increased without limit). Ceramic capacitor required for output (see *Output Capacitor*).
***Reduces output noise (may be omitted if application is not noise critical). Use ceramic or film type with very low leakage current (see *Capacitor Characteristics*).

Figure 34. Basic Application Circuit

Typical Application (continued)

8.2.1 Design Requirements

For basic design parameters, see Table 1.

Table 1. Design Parameters

DESIGN PARAMETER	VALUE
Input voltage	4.3 V
Output voltage	3.3 V
Output current	150 mA (maximum) 1 mA (minimum)
Output capacitor range	4.7 µF

8.2.2 Detailed Design Procedure

8.2.2.1 External Capacitors

Like any low-dropout regulator, the LP2992 requires external capacitors for regulator stability. These capacitors must be correctly selected for good performance.

8.2.2.1.1 Input Capacitor

An input capacitor whose capacitance is ≥ 1 µF is required between the LP2992 input and ground (the amount of capacitance may be increased without limit).

This capacitor must be located a distance of not more than 1 cm from the IN pin and returned to a clean analog ground. Any good quality ceramic, tantalum, or film capacitor may be used at the input.

NOTE

Tantalum capacitors can suffer catastrophic failure due to surge current when connected to a low-impedance source of power (like a battery or very large capacitor). If a tantalum capacitor is used at the input, it must be specified by the manufacturer to have a surge current rating sufficient for the application.

There are no requirements for ESR on the input capacitor, but tolerance and temperature coefficient must be considered when selecting the capacitor to ensure the capacitance is ≥ 1 µF over the entire operating temperature range.

8.2.2.1.2 Output Capacitor

The LP2992 is designed specifically to work with ceramic output capacitors, using circuitry that allows the regulator to be stable across the entire range of output current with an output capacitor whose ESR is as low as 5 mΩ. It may also be possible to use tantalum or film capacitors at the output, but these are not as attractive for reasons of size and cost (see *Capacitor Characteristics*).

The output capacitor must meet the requirement for minimum amount of capacitance and also have an ESR value which is within the stable range. Curves are provided which show the stable ESR range as a function of load current (see Figure 35).

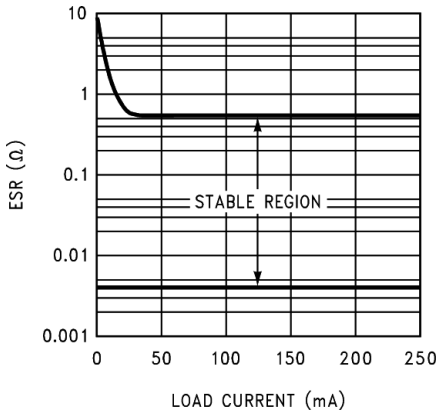


Figure 35. Stable ESR Range vs Load Current

The output capacitor must maintain its ESR within the stable region over the full operating temperature range of the application to assure stability.

The LP2992 requires a minimum of 4.7 µF on the output (output capacitor size can be increased without limit).

It is important to remember that capacitor tolerance and variation with temperature must be taken into consideration when selecting an output capacitor so that the minimum required amount of output capacitance is provided over the full operating temperature range. It must be noted that ceramic capacitors can exhibit large changes in capacitance with temperature (see *Capacitor Characteristics*).

The output capacitor must be located not more than 1 cm from the output pin and returned to a clean analog ground.

8.2.2.1.3 Noise Bypass Capacitor

Connecting a 10-nF capacitor to the BYPASS pin significantly reduces noise on the regulator output. It should be noted that the capacitor is connected directly to a high-impedance circuit in the bandgap reference.

Because this circuit has only a few microamperes flowing in it, any significant loading on this node causes a change in the regulated output voltage. For this reason, dc leakage current through the noise bypass capacitor must never exceed 100 nA, and must be kept as low as possible for best output voltage accuracy.

The types of capacitors best suited for the noise bypass capacitor are ceramic and film. High-quality ceramic capacitors with either NPO or COG dielectric typically have very low leakage. 10-nF polypropolene and polycarbonate film capacitors are available in small surface-mount packages and typically have extremely low leakage current.

8.2.2.2 Capacitor Characteristics

The LP2992 was designed to work with ceramic capacitors on the output to take advantage of the benefits they offer. For capacitance values in the 2.2-µF to 10-µF range, ceramics are the least expensive and also have the lowest ESR values (which makes them best for eliminating high-frequency noise). The ESR of a typical 4.7-µF ceramic capacitor is in the range of 5 mΩ to 10 mΩ, which easily meets the ESR limits required for stability by the LP2992.

One disadvantage of ceramic capacitors is that their capacitance can vary with temperature. Most large value ceramic capacitors (≥ 2.2 µF) are manufactured with the Z5U or Y5V temperature characteristic, which results in the capacitance dropping by more than 50% as the temperature goes from 25°C to 85°C.

This could cause problems if a 4.7-µF capacitor were used on the output because it drops down to approximately 2.3 µF at high ambient temperatures (which could cause the LP2992 to oscillate). If Z5U or Y5V capacitors are used on the output, a minimum capacitance value of 10 µF must be observed.

A better choice for temperature coefficient in ceramic capacitors is X7R, which holds the capacitance within ±15%. Unfortunately, the larger values of capacitance are not offered by all manufacturers in the X7R dielectric.

8.2.2.2.1 Tantalum

Tantalum capacitors are less desirable than ceramics for use as output capacitors because they are more expensive when comparing equivalent capacitance and voltage ratings in the 1-µF to 4.7-µF range.

Another important consideration is that tantalum capacitors have higher ESR values than equivalent size ceramics. This means that while it may be possible to find a Tantalum capacitor with an ESR value within the stable range, it would have to be larger in capacitance (which means bigger and more costly) than a ceramic capacitor with the same ESR value.

It should also be noted that the ESR of a typical tantalum increases about 2:1 as the temperature goes from 25°C down to −40°C, so some guard band must be allowed.

8.2.2.3 Reverse Input-Output Voltage

The PNP power transistor used as the pass element in the LP2992 has an inherent diode connected between the regulator output and input. During normal operation (where the input voltage is higher than the output) this diode is reverse-biased.

However, if the output is pulled above the input, this diode turns ON and current flows into the regulator output. In such cases, a parasitic SCR can latch which allows a high current to flow into V_{IN} (and out the ground pin), which can damage the part.

In any application where the output may be pulled above the input, an external Schottky diode must be connected from V_{IN} to V_{OUT} (cathode on V_{IN}, anode on V_{OUT}), to limit the reverse voltage across the LP2992 to 0.3 V (see *Absolute Maximum Ratings*).

8.2.2.4 Power Dissipation

Knowing the device power dissipation and proper sizing of the thermal plane connected to the tab or pad is critical to ensuring reliable operation. Device power dissipation depends on input voltage, output voltage, and load conditions and can be calculated with Equation 1.

$$P_{D(MAX)} = (V_{IN(MAX)} - V_{OUT}) \times I_{OUT} \quad (1)$$

Power dissipation can be minimized, and greater efficiency can be achieved, by using the lowest available voltage drop option that would still be greater than the dropout voltage (V_{DO}). However, keep in mind that higher voltage drops result in better dynamic (that is, PSRR and transient) performance.

On the WSON (NGD) package, the primary conduction path for heat is through the exposed power pad to the PCB. To ensure the device does not overheat, connect the exposed pad, through thermal vias, to an internal ground plane with an appropriate amount of copper PCB area.

On the SOT-23 (DBV) package, the primary conduction path for heat is through the pins to the PCB. The maximum allowable junction temperature ($T_{J(MAX)}$)determines maximum power dissipation allowed ($P_{D(MAX)}$) for the device package.

Power dissipation and junction temperature are most often related by the junction-to-ambient thermal resistance ($R_{\theta JA)}$ of the combined PCB and device package and the temperature of the ambient air (T_A), according to Equation 2 or Equation 2:

$$T_{J(MAX)} = T_{A(MAX)} + (R_{\theta JA} \times P_{D(MAX)}) \quad (2)$$

$$P_D = T_{J(MAX)} - T_{A(MAX)} / R_{\theta JA} \quad (3)$$

Unfortunately, this $R_{\theta JA}$ is highly dependent on the heat-spreading capability of the particular PCB design, and therefore varies according to the total copper area, copper weight, and location of the planes. The $R_{\theta JA}$ recorded in *Thermal Information* is determined by the specific EIA/JEDEC JESD51-7 standard for PCB and copper-spreading area, and is to be used only as a relative measure of package thermal performance. For a well-designed thermal layout, $R_{\theta JA}$ is actually the sum of the package junction-to-case (bottom) thermal resistance ($R_{\theta JCbot}$) plus the thermal resistance contribution by the PCB copper area acting as a heat sink.

8.2.2.5 Estimating Junction Temperature

The EIA/JEDEC standard recommends the use of psi (Ψ) thermal characteristics to estimate the junction temperatures of surface mount devices on a typical PCB board application. These characteristics are not true thermal resistance values, but rather package specific thermal characteristics that offer practical and relative means of estimating junction temperatures. These psi metrics are determined to be significantly independent of copper-spreading area. The key thermal characteristics (Ψ_{JT} and Ψ_{JB}) are given in *Thermal Information* and are used in accordance with Equation 4 or Equation 5.

$$T_{J(MAX)} = T_{TOP} + (\Psi_{JT} \times P_{D(MAX)}) \quad (4)$$

where

- $P_{D(MAX)}$ is explained in Equation 3
- T_{TOP} is the temperature measured at the center-top of the device package.

$$T_{J(MAX)} = T_{BOARD} + (\Psi_{JB} \times P_{D(MAX)}) \quad (5)$$

where

- $P_{D(MAX)}$ is explained in Equation 3.
- T_{BOARD} is the PCB surface temperature measured 1-mm from the device package and centered on the package edge.

For more information about the thermal characteristics Ψ_{JT} and Ψ_{JB}, see *Semiconductor and IC Package Thermal Metrics*; for more information about measuring T_{TOP} and T_{BOARD}, *Using New Thermal Metrics* (SBVA025); and for more information about the EIA/JEDEC JESD51 PCB used for validating $R_{\theta JA}$, see *Thermal Characteristics of Linear and Logic Packages Using JEDEC PCB Designs*. These application notes are available at www.ti.com.

8.2.3 Application Curves

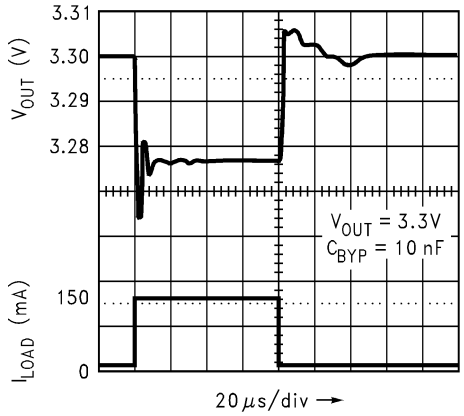


Figure 36. Load Transient Response

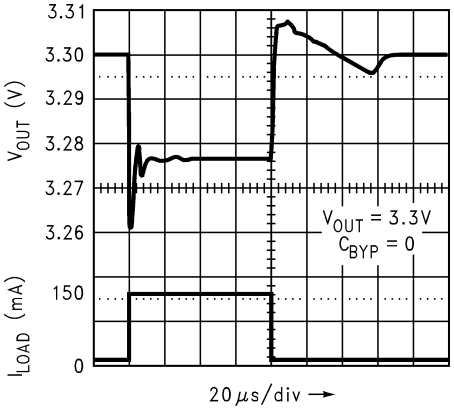


Figure 37. Load Transient Response

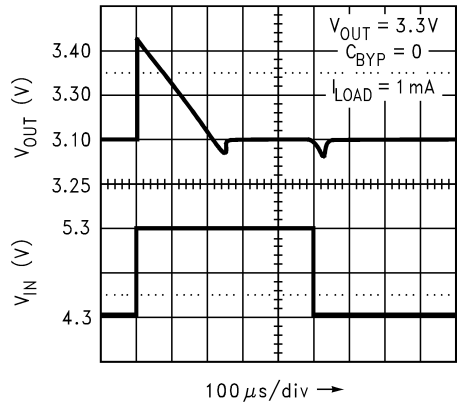


Figure 38. Line Transient Response

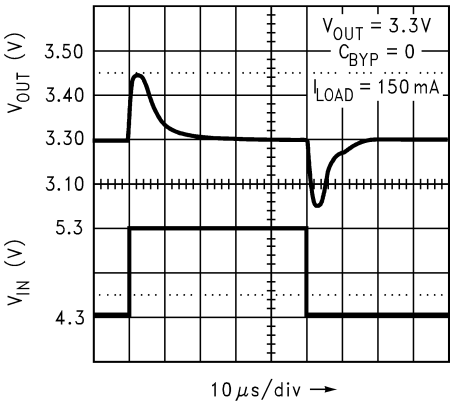


Figure 39. Line Transient Response

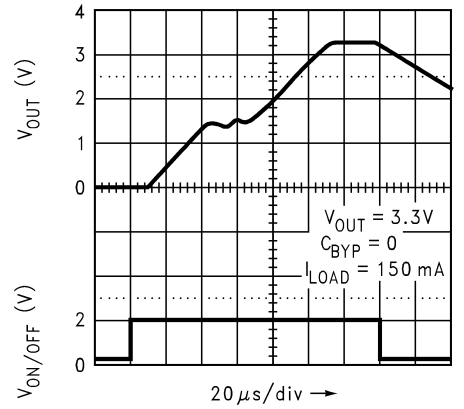


Figure 40. Turnon Time

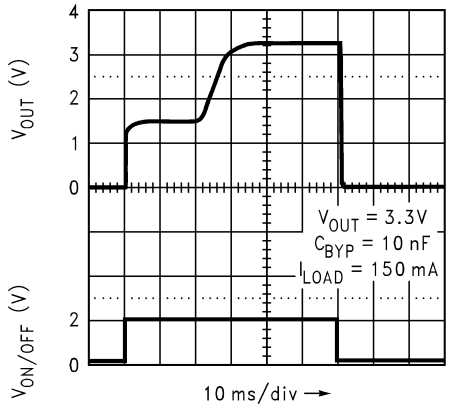


Figure 41. Turnon Time

9 Power Supply Recommendations

The LP2992 is designed to operate from an input voltage supply range from 2.2 V to 16 V. The input voltage range provides the adequate headroom in order for the device to have a regulated output. This input supply must be well regulated. If the input supply is noisy, additional input capacitors with low ESR can help to improve the output noise performance.

10 Layout

10.1 Layout Guidelines

For best overall performance, place all circuit components on the same side of the circuit board and as near as practical to the respective LDO pin connections. Place ground return connections to the input and output capacitors, and to the LDO ground pin as close as possible to each other, connected by a wide, component-side, copper surface. The use of vias and long traces to create LDO circuit connections is strongly discouraged and negatively affects system performance. This grounding and layout scheme minimizes inductive parasitics, and thereby reduces load-current transients, minimizes noise, and increases circuit stability.

TI also recommends a ground reference plane either embedded in the PCB itself or located on the bottom side of the PCB opposite the components. This reference plane serves to assure accuracy of the output voltage, shield noise, and behaves similar to a thermal plane to spread (or sink) heat from the LDO device. In most applications, this ground plane is necessary to meet thermal requirements.

10.2 Layout Examples

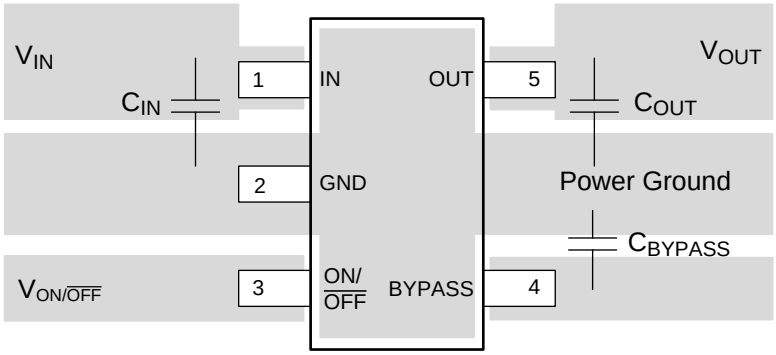


Figure 42. LP2992 SOT-23 Package Typical Layout

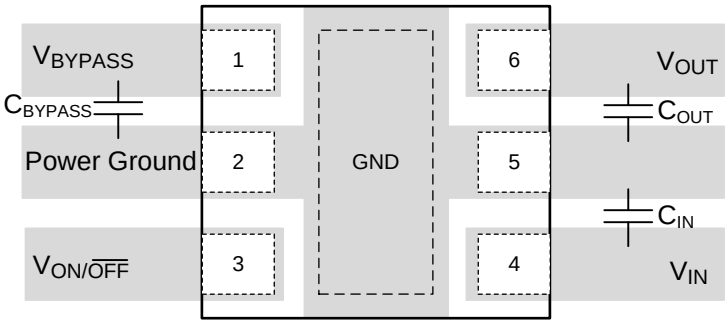


Figure 43. LP2992 WSON Package Typical Layout

10.3 WSON Mounting

The WSON package requires specific mounting techniques which are detailed in *AN-1187 Leadless Leadframe Package (LLP)*. Referring to the section *PCB Design Recommendations*, note that the pad style which must be used with the WSON package is the NSMD (non-solder mask defined) type.

The thermal dissipation of the WSON package is directly related to the printed circuit board construction and the amount of additional copper area.

11 Device and Documentation Support

11.1 Documentation Support

11.1.1 Related Documentation

For related documentation see the following:

- *AN-1187 Leadless Leadframe Package (LLP)*
- *Semiconductor and IC Package Thermal Metrics*
- *Using New Thermal Metrics* (SBVA025)
- *Thermal Characteristics of Linear and Logic Packages Using JEDEC PCB Designs*

11.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. In the upper right corner, click on *Alert me* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

11.3 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

TI E2E™ Online Community ***TI's Engineer-to-Engineer (E2E) Community.*** Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support ***TI's Design Support*** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

11.4 Trademarks

E2E is a trademark of Texas Instruments.
All other trademarks are the property of their respective owners.

11.5 Electrostatic Discharge Caution

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

11.6 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
LP2992AILD-1.5/NOPB	ACTIVE	WSON	NGD	6	1000	RoHS & Green	SN	Level-3-260C-168 HR	-40 to 125	L011A	Samples
LP2992AILD-1.8/NOPB	ACTIVE	WSON	NGD	6	1000	RoHS & Green	NIPDAU | SN	Level-3-260C-168 HR	-40 to 125	L012A	Samples
LP2992AILD-3.3/NOPB	ACTIVE	WSON	NGD	6	1000	RoHS & Green	NIPDAU | SN	Level-3-260C-168 HR	-40 to 125	L014A	Samples
LP2992AILD-5.0/NOPB	ACTIVE	WSON	NGD	6	1000	RoHS & Green	NIPDAU | SN	Level-3-260C-168 HR	-40 to 125	L015A	Samples
LP2992AILDX-3.3/NOPB	ACTIVE	WSON	NGD	6	4500	RoHS & Green	NIPDAU | SN	Level-3-260C-168 HR	-40 to 125	L014A	Samples
LP2992AILDX-5.0/NOPB	ACTIVE	WSON	NGD	6	4500	RoHS & Green	NIPDAU | SN	Level-3-260C-168 HR	-40 to 125	L015A	Samples
LP2992AIM5-1.5/NOPB	ACTIVE	SOT-23	DBV	5	1000	RoHS & Green	SN	Level-1-260C-UNLIM	-40 to 125	LFBA	Samples
LP2992AIM5-1.8/NOPB	ACTIVE	SOT-23	DBV	5	1000	RoHS & Green	SN	Level-1-260C-UNLIM	-40 to 125	LFCA	Samples
LP2992AIM5-2.5	NRND	SOT-23	DBV	5	1000	Non-RoHS & Green	Call TI	Call TI	-40 to 125	LFDA	
LP2992AIM5-2.5/NOPB	ACTIVE	SOT-23	DBV	5	1000	RoHS & Green	SN	Level-1-260C-UNLIM	-40 to 125	LFDA	Samples
LP2992AIM5-3.3	NRND	SOT-23	DBV	5	1000	Non-RoHS & Green	Call TI	Call TI	-40 to 125	LFEA	
LP2992AIM5-3.3/NOPB	ACTIVE	SOT-23	DBV	5	1000	RoHS & Green	SN	Level-1-260C-UNLIM	-40 to 125	LFEA	Samples
LP2992AIM5-5.0/NOPB	ACTIVE	SOT-23	DBV	5	1000	RoHS & Green	SN	Level-1-260C-UNLIM	-40 to 125	LFFA	Samples
LP2992AIM5X-1.5/NOPB	ACTIVE	SOT-23	DBV	5	3000	RoHS & Green	SN	Level-1-260C-UNLIM	-40 to 125	LFBA	Samples
LP2992AIM5X-1.8/NOPB	ACTIVE	SOT-23	DBV	5	3000	RoHS & Green	SN	Level-1-260C-UNLIM	-40 to 125	LFCA	Samples
LP2992AIM5X-2.5/NOPB	ACTIVE	SOT-23	DBV	5	3000	RoHS & Green	SN	Level-1-260C-UNLIM	-40 to 125	LFDA	Samples
LP2992AIM5X-3.3/NOPB	ACTIVE	SOT-23	DBV	5	3000	RoHS & Green	SN	Level-1-260C-UNLIM	-40 to 125	LFEA	Samples
LP2992AIM5X-5.0/NOPB	ACTIVE	SOT-23	DBV	5	3000	RoHS & Green	SN	Level-1-260C-UNLIM	-40 to 125	LFFA	Samples
LP2992ILD-1.8/NOPB	ACTIVE	WSON	NGD	6	1000	RoHS & Green	NIPDAU | SN	Level-3-260C-168 HR	-40 to 125	L012A B	Samples

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
LP2992ILD-2.5/NOPB	ACTIVE	WSON	NGD	6	1000	RoHS & Green	SN	Level-3-260C-168 HR	-40 to 125	L013A B	Samples
LP2992ILD-3.3/NOPB	ACTIVE	WSON	NGD	6	1000	RoHS & Green	NIPDAU | SN	Level-3-260C-168 HR	-40 to 125	L014A B	Samples
LP2992ILD-5.0/NOPB	ACTIVE	WSON	NGD	6	1000	RoHS & Green	NIPDAU | SN	Level-3-260C-168 HR	-40 to 125	L015A B	Samples
LP2992ILDX-1.5/NOPB	ACTIVE	WSON	NGD	6	4500	RoHS & Green	NIPDAU | SN	Level-3-260C-168 HR	-40 to 125	L011A B	Samples
LP2992ILDX-3.3/NOPB	ACTIVE	WSON	NGD	6	4500	RoHS & Green	NIPDAU | SN	Level-3-260C-168 HR	-40 to 125	L014A B	Samples
LP2992ILDX-5.0/NOPB	ACTIVE	WSON	NGD	6	4500	RoHS & Green	SN	Level-3-260C-168 HR	-40 to 125	L015A B	Samples
LP2992IM5-1.5/NOPB	ACTIVE	SOT-23	DBV	5	1000	RoHS & Green	SN	Level-1-260C-UNLIM	-40 to 125	LFBB	Samples
LP2992IM5-1.8/NOPB	ACTIVE	SOT-23	DBV	5	1000	RoHS & Green	SN	Level-1-260C-UNLIM	-40 to 125	LFCB	Samples
LP2992IM5-2.5	NRND	SOT-23	DBV	5	1000	Non-RoHS & Green	Call TI	Call TI	-40 to 125	LFDB	
LP2992IM5-2.5/NOPB	ACTIVE	SOT-23	DBV	5	1000	RoHS & Green	SN	Level-1-260C-UNLIM	-40 to 125	LFDB	Samples
LP2992IM5-3.0/NOPB	ACTIVE	SOT-23	DBV	5	1000	RoHS & Green	SN	Level-1-260C-UNLIM		LF8B	Samples
LP2992IM5-3.3	NRND	SOT-23	DBV	5	1000	Non-RoHS & Green	Call TI	Call TI	-40 to 125	LFEB	
LP2992IM5-3.3/NOPB	ACTIVE	SOT-23	DBV	5	1000	RoHS & Green	SN	Level-1-260C-UNLIM	-40 to 125	LFEB	Samples
LP2992IM5-5.0/NOPB	ACTIVE	SOT-23	DBV	5	1000	RoHS & Green	SN	Level-1-260C-UNLIM	-40 to 125	LFFB	Samples
LP2992IM5X-1.5/NOPB	ACTIVE	SOT-23	DBV	5	3000	RoHS & Green	SN	Level-1-260C-UNLIM	-40 to 125	LFBB	Samples
LP2992IM5X-1.8/NOPB	ACTIVE	SOT-23	DBV	5	3000	RoHS & Green	SN	Level-1-260C-UNLIM	-40 to 125	LFCB	Samples
LP2992IM5X-2.5/NOPB	ACTIVE	SOT-23	DBV	5	3000	RoHS & Green	SN	Level-1-260C-UNLIM	-40 to 125	LFDB	Samples
LP2992IM5X-3.3/NOPB	ACTIVE	SOT-23	DBV	5	3000	RoHS & Green	SN	Level-1-260C-UNLIM	-40 to 125	LFEB	Samples
LP2992IM5X-5.0/NOPB	ACTIVE	SOT-23	DBV	5	3000	RoHS & Green	SN	Level-1-260C-UNLIM	-40 to 125	LFFB	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

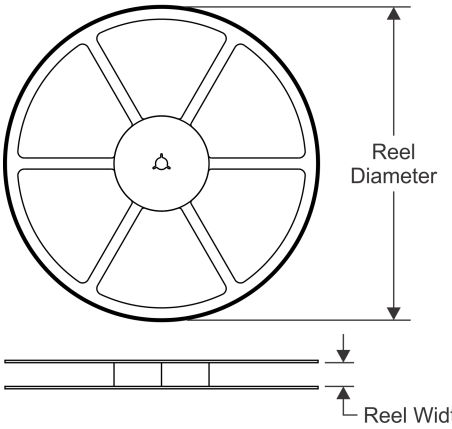
(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

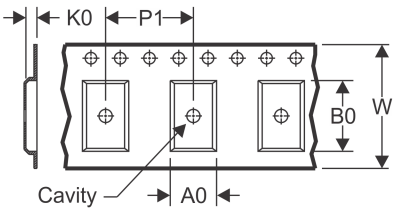
(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

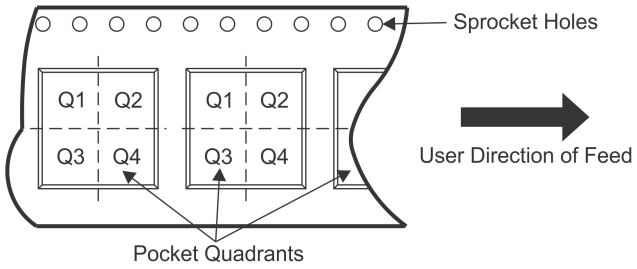


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE

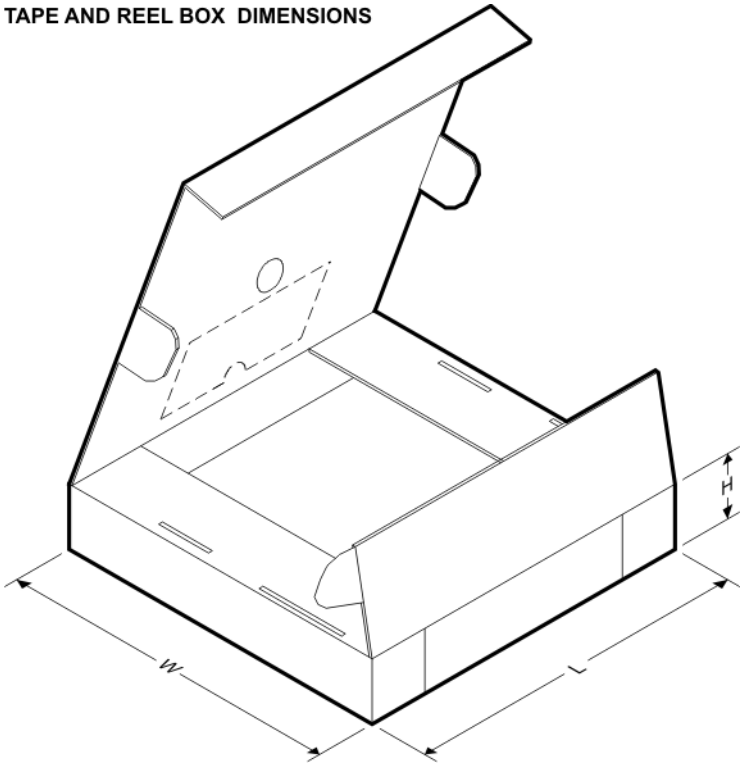


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
LP2992AILD-1.5/NOPB	WSON	NGD	6	1000	178.0	12.4	3.6	3.2	1.0	8.0	12.0	Q1
LP2992AILD-1.8/NOPB	WSON	NGD	6	1000	178.0	12.4	3.6	3.2	1.0	8.0	12.0	Q1
LP2992AILD-3.3/NOPB	WSON	NGD	6	1000	180.0	12.4	3.6	3.2	1.0	8.0	12.0	Q1
LP2992AILD-5.0/NOPB	WSON	NGD	6	1000	180.0	12.4	3.6	3.2	1.0	8.0	12.0	Q1
LP2992AILDX-3.3/NOPB	WSON	NGD	6	4500	330.0	12.4	3.6	3.2	1.0	8.0	12.0	Q1
LP2992AILDX-5.0/NOPB	WSON	NGD	6	4500	330.0	12.4	3.6	3.2	1.0	8.0	12.0	Q1
LP2992AIM5-1.5/NOPB	SOT-23	DBV	5	1000	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
LP2992AIM5-1.8/NOPB	SOT-23	DBV	5	1000	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
LP2992AIM5-2.5	SOT-23	DBV	5	1000	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
LP2992AIM5-2.5/NOPB	SOT-23	DBV	5	1000	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
LP2992AIM5-3.3	SOT-23	DBV	5	1000	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
LP2992AIM5-3.3/NOPB	SOT-23	DBV	5	1000	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
LP2992AIM5-5.0/NOPB	SOT-23	DBV	5	1000	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
LP2992AIM5X-1.5/NOPB	SOT-23	DBV	5	3000	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
LP2992AIM5X-1.8/NOPB	SOT-23	DBV	5	3000	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
LP2992AIM5X-2.5/NOPB	SOT-23	DBV	5	3000	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
LP2992AIM5X-3.3/NOPB	SOT-23	DBV	5	3000	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
LP2992AIM5X-5.0/NOPB	SOT-23	DBV	5	3000	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
LP2992ILD-1.8/NOPB	WSON	NGD	6	1000	180.0	12.4	3.6	3.2	1.0	8.0	12.0	Q1
LP2992ILD-2.5/NOPB	WSON	NGD	6	1000	178.0	12.4	3.6	3.2	1.0	8.0	12.0	Q1
LP2992ILD-3.3/NOPB	WSON	NGD	6	1000	180.0	12.4	3.6	3.2	1.0	8.0	12.0	Q1
LP2992ILD-5.0/NOPB	WSON	NGD	6	1000	180.0	12.4	3.6	3.2	1.0	8.0	12.0	Q1
LP2992ILDX-1.5/NOPB	WSON	NGD	6	4500	330.0	12.4	3.6	3.2	1.0	8.0	12.0	Q1
LP2992ILDX-3.3/NOPB	WSON	NGD	6	4500	330.0	12.4	3.6	3.2	1.0	8.0	12.0	Q1
LP2992ILDX-5.0/NOPB	WSON	NGD	6	4500	330.0	12.4	3.6	3.2	1.0	8.0	12.0	Q1
LP2992IM5-1.5/NOPB	SOT-23	DBV	5	1000	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
LP2992IM5-1.8/NOPB	SOT-23	DBV	5	1000	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
LP2992IM5-2.5	SOT-23	DBV	5	1000	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
LP2992IM5-2.5/NOPB	SOT-23	DBV	5	1000	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
LP2992IM5-3.0/NOPB	SOT-23	DBV	5	1000	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
LP2992IM5-3.3	SOT-23	DBV	5	1000	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
LP2992IM5-3.3/NOPB	SOT-23	DBV	5	1000	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
LP2992IM5-5.0/NOPB	SOT-23	DBV	5	1000	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
LP2992IM5X-1.5/NOPB	SOT-23	DBV	5	3000	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
LP2992IM5X-1.8/NOPB	SOT-23	DBV	5	3000	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
LP2992IM5X-2.5/NOPB	SOT-23	DBV	5	3000	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
LP2992IM5X-3.3/NOPB	SOT-23	DBV	5	3000	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
LP2992IM5X-5.0/NOPB	SOT-23	DBV	5	3000	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

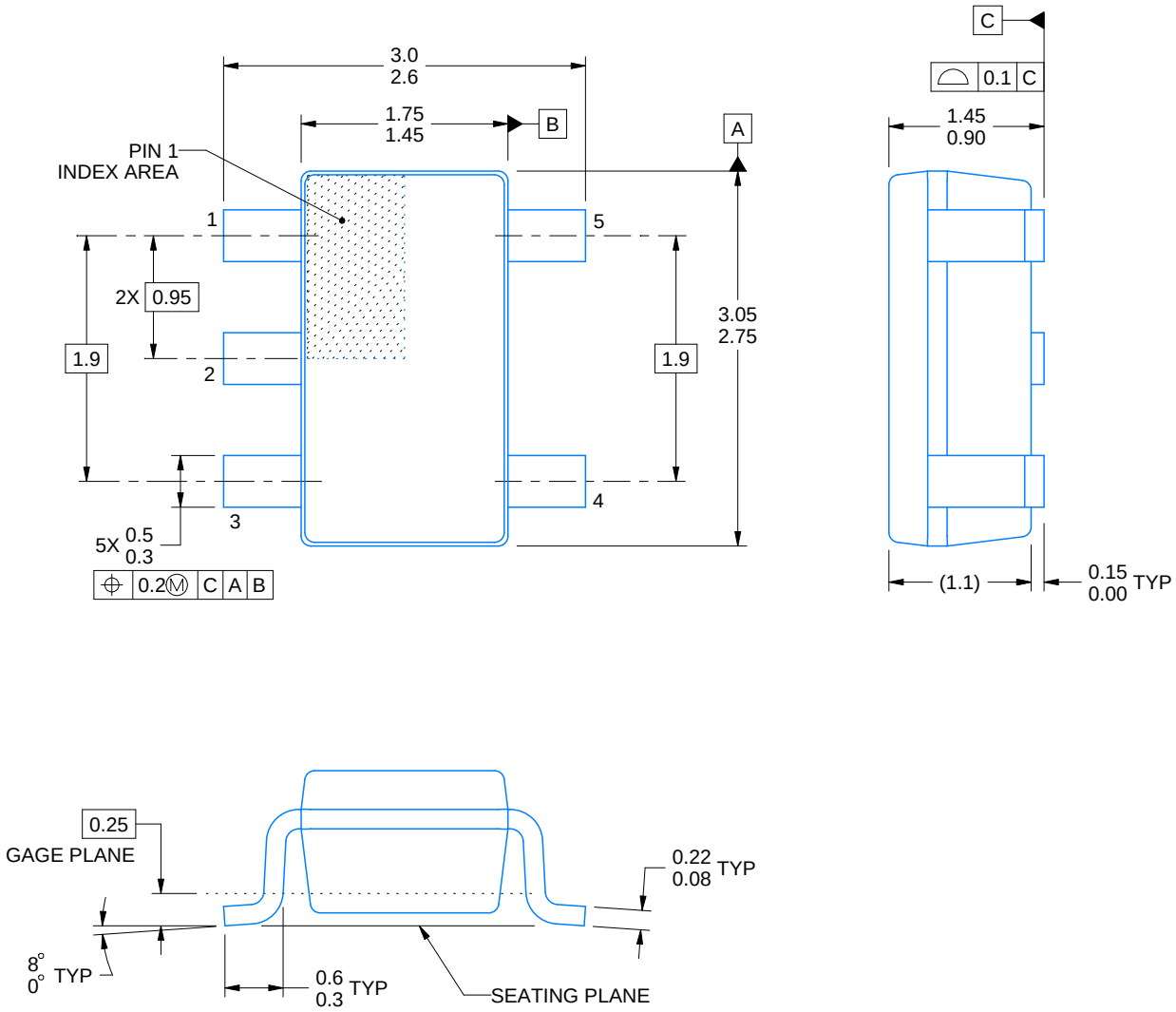
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
LP2992AILD-1.5/NOPB	WSON	NGD	6	1000	210.0	185.0	35.0
LP2992AILD-1.8/NOPB	WSON	NGD	6	1000	210.0	185.0	35.0
LP2992AILD-3.3/NOPB	WSON	NGD	6	1000	213.0	191.0	35.0
LP2992AILD-5.0/NOPB	WSON	NGD	6	1000	213.0	191.0	35.0
LP2992AILDX-3.3/NOPB	WSON	NGD	6	4500	367.0	367.0	38.0
LP2992AILDX-5.0/NOPB	WSON	NGD	6	4500	367.0	367.0	38.0
LP2992AIM5-1.5/NOPB	SOT-23	DBV	5	1000	210.0	185.0	35.0
LP2992AIM5-1.8/NOPB	SOT-23	DBV	5	1000	210.0	185.0	35.0
LP2992AIM5-2.5	SOT-23	DBV	5	1000	210.0	185.0	35.0
LP2992AIM5-2.5/NOPB	SOT-23	DBV	5	1000	210.0	185.0	35.0
LP2992AIM5-3.3	SOT-23	DBV	5	1000	210.0	185.0	35.0
LP2992AIM5-3.3/NOPB	SOT-23	DBV	5	1000	210.0	185.0	35.0
LP2992AIM5-5.0/NOPB	SOT-23	DBV	5	1000	210.0	185.0	35.0
LP2992AIM5X-1.5/NOPB	SOT-23	DBV	5	3000	210.0	185.0	35.0
LP2992AIM5X-1.8/NOPB	SOT-23	DBV	5	3000	210.0	185.0	35.0
LP2992AIM5X-2.5/NOPB	SOT-23	DBV	5	3000	210.0	185.0	35.0
LP2992AIM5X-3.3/NOPB	SOT-23	DBV	5	3000	210.0	185.0	35.0
LP2992AIM5X-5.0/NOPB	SOT-23	DBV	5	3000	210.0	185.0	35.0
LP2992ILD-1.8/NOPB	WSON	NGD	6	1000	213.0	191.0	35.0
LP2992ILD-2.5/NOPB	WSON	NGD	6	1000	210.0	185.0	35.0
LP2992ILD-3.3/NOPB	WSON	NGD	6	1000	213.0	191.0	35.0
LP2992ILD-5.0/NOPB	WSON	NGD	6	1000	213.0	191.0	35.0
LP2992ILDX-1.5/NOPB	WSON	NGD	6	4500	367.0	367.0	38.0
LP2992ILDX-3.3/NOPB	WSON	NGD	6	4500	367.0	367.0	38.0
LP2992ILDX-5.0/NOPB	WSON	NGD	6	4500	367.0	367.0	35.0
LP2992IM5-1.5/NOPB	SOT-23	DBV	5	1000	210.0	185.0	35.0
LP2992IM5-1.8/NOPB	SOT-23	DBV	5	1000	210.0	185.0	35.0
LP2992IM5-2.5	SOT-23	DBV	5	1000	210.0	185.0	35.0
LP2992IM5-2.5/NOPB	SOT-23	DBV	5	1000	210.0	185.0	35.0
LP2992IM5-3.0/NOPB	SOT-23	DBV	5	1000	210.0	185.0	35.0
LP2992IM5-3.3	SOT-23	DBV	5	1000	210.0	185.0	35.0
LP2992IM5-3.3/NOPB	SOT-23	DBV	5	1000	210.0	185.0	35.0
LP2992IM5-5.0/NOPB	SOT-23	DBV	5	1000	210.0	185.0	35.0
LP2992IM5X-1.5/NOPB	SOT-23	DBV	5	3000	210.0	185.0	35.0
LP2992IM5X-1.8/NOPB	SOT-23	DBV	5	3000	210.0	185.0	35.0
LP2992IM5X-2.5/NOPB	SOT-23	DBV	5	3000	210.0	185.0	35.0
LP2992IM5X-3.3/NOPB	SOT-23	DBV	5	3000	210.0	185.0	35.0
LP2992IM5X-5.0/NOPB	SOT-23	DBV	5	3000	210.0	185.0	35.0

PACKAGE OUTLINE

DBV0005A

SOT-23 - 1.45 mm max height

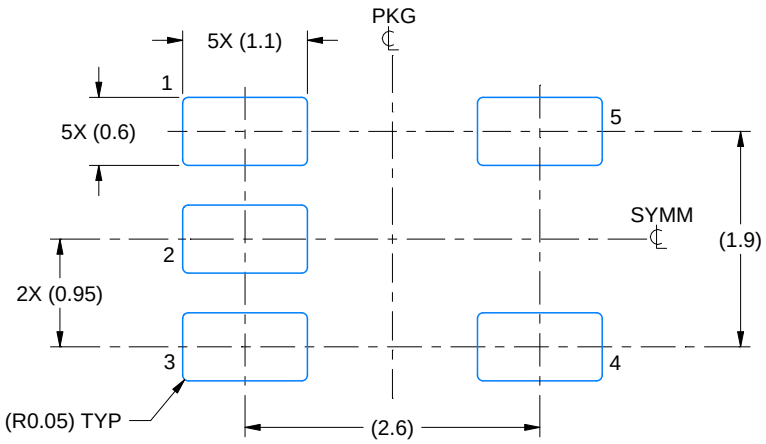
SMALL OUTLINE TRANSISTOR



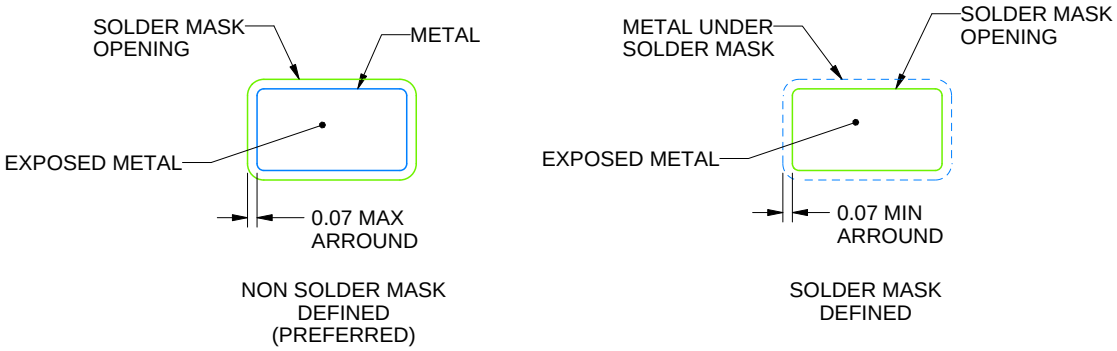
4214839/E 09/2019

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Refernce JEDEC MO-178.
4. Body dimensions do not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:15X

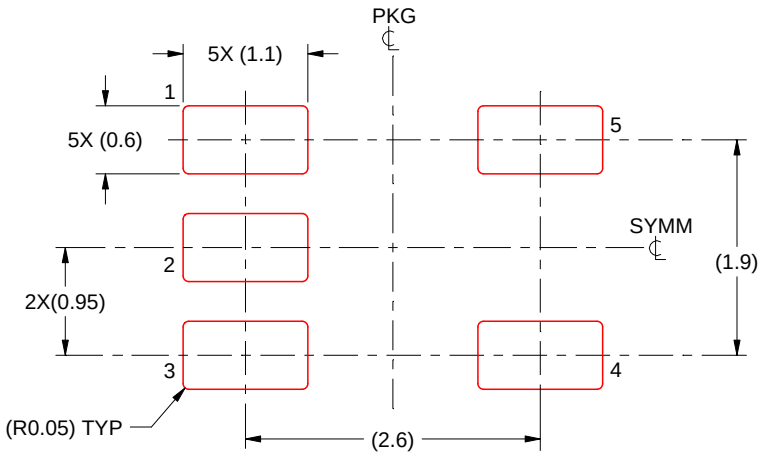


SOLDER MASK DETAILS

4214839/E 09/2019

NOTES: (continued)

5. Publication IPC-7351 may have alternate designs.
6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:15X

4214839/E 09/2019

NOTES: (continued)

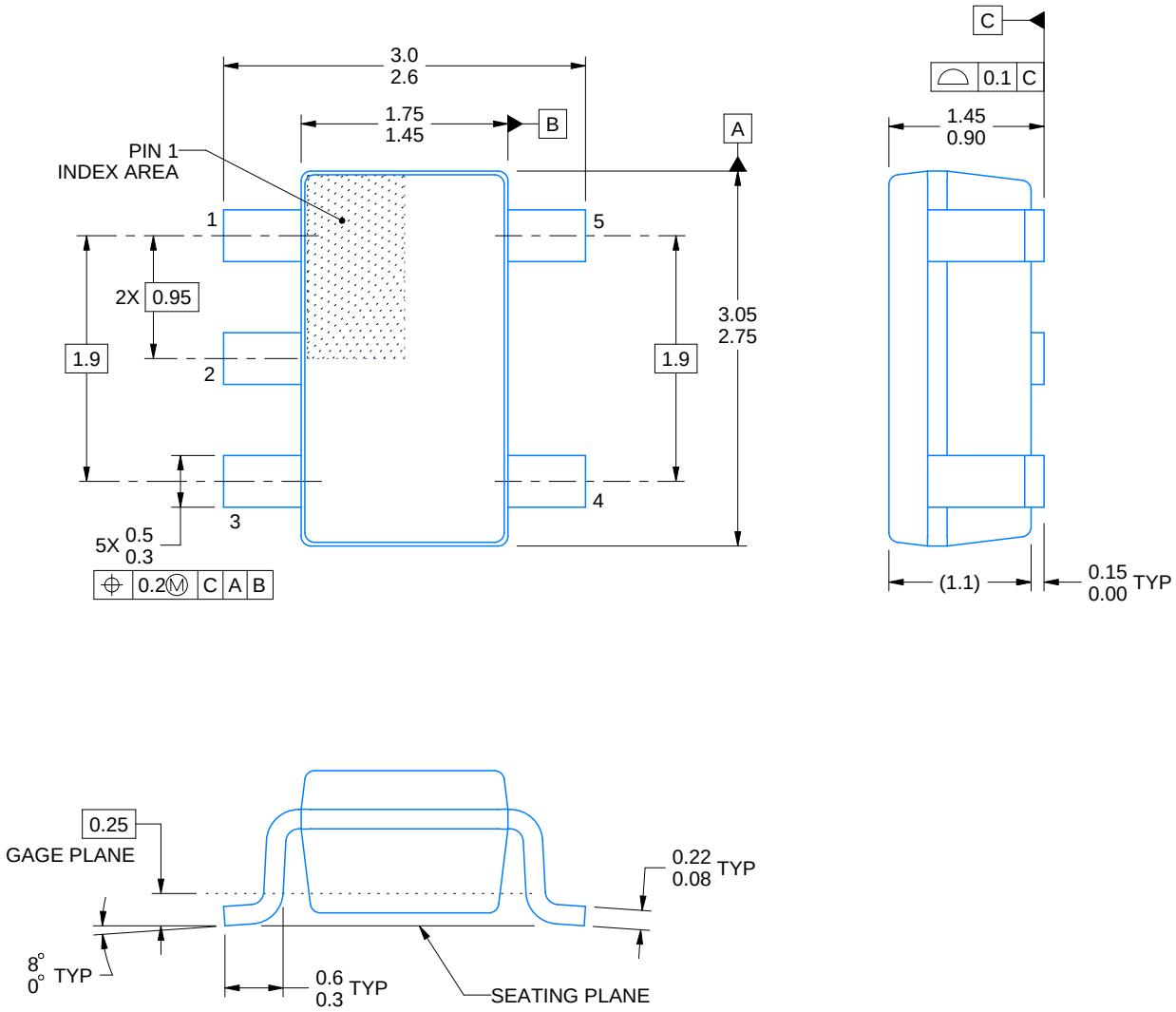
7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
8. Board assembly site may have different recommendations for stencil design.

PACKAGE OUTLINE

DBV0005A

SOT-23 - 1.45 mm max height

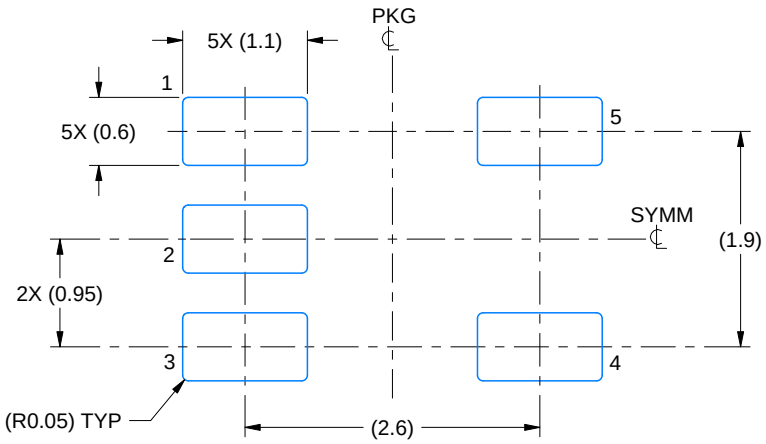
SMALL OUTLINE TRANSISTOR



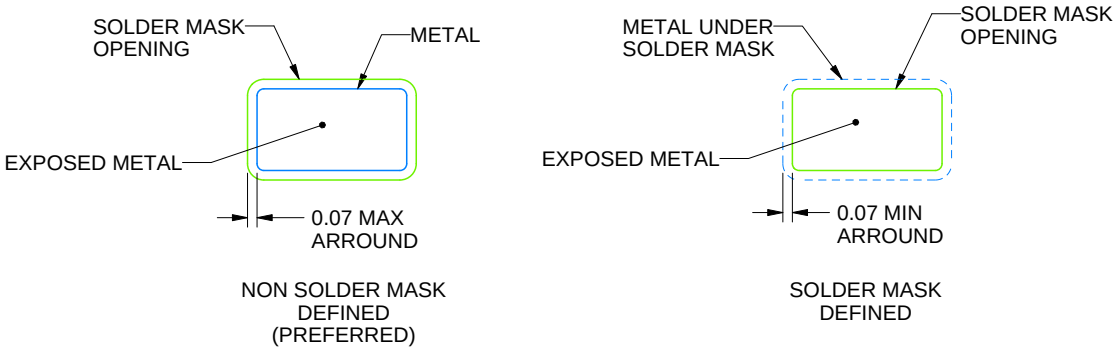
4214839/F 06/2021

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Refernce JEDEC MO-178.
4. Body dimensions do not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.25 mm per side.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:15X

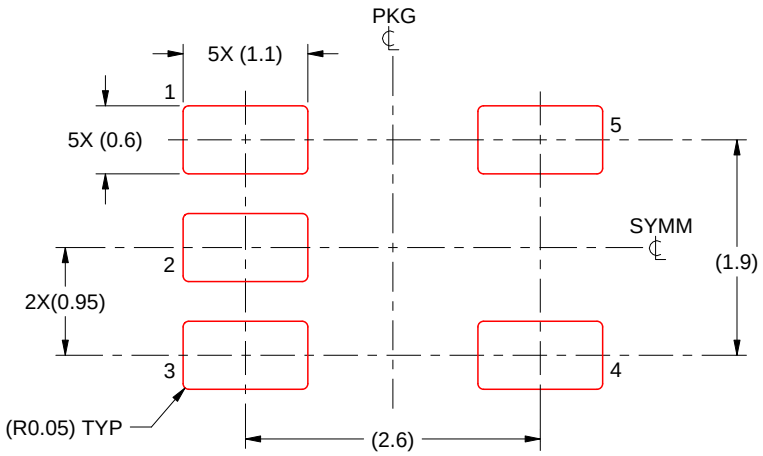


SOLDER MASK DETAILS

4214839/F 06/2021

NOTES: (continued)

5. Publication IPC-7351 may have alternate designs.
6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



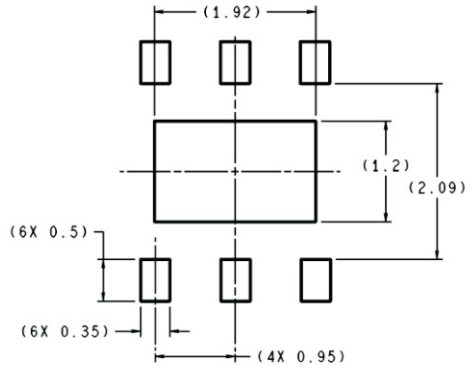
SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:15X

4214839/F 06/2021

NOTES: (continued)

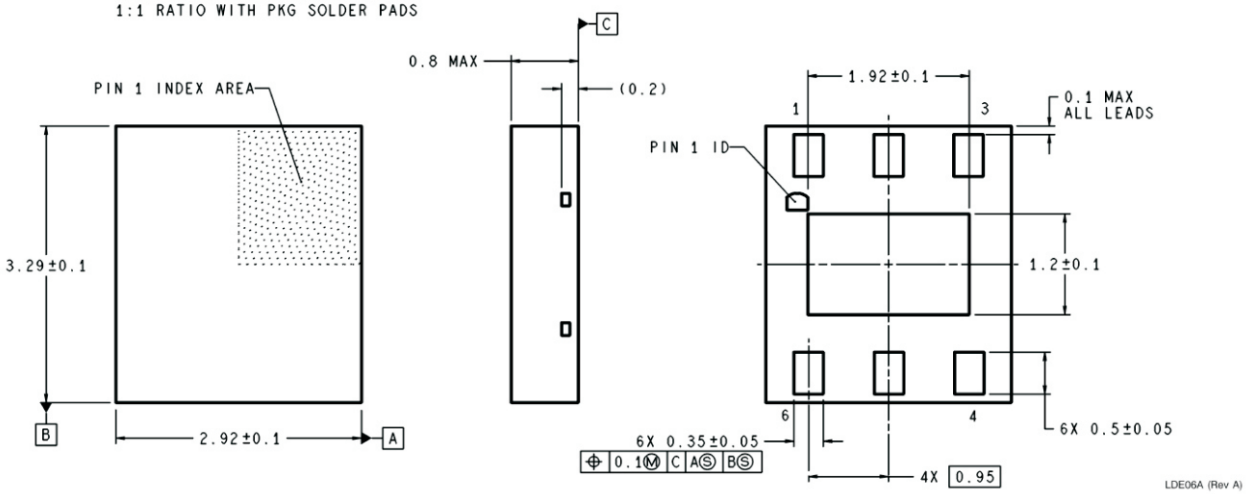
7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
8. Board assembly site may have different recommendations for stencil design.

NGD0006A



DIMENSIONS ARE IN MILLIMETERS

RECOMMENDED LAND PATTERN
1:1 RATIO WITH PKG SOLDER PADS



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Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265