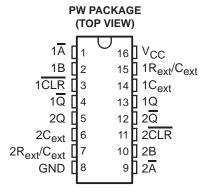
SCLS498A - MAY 2003 - REVISED MAY 2004

- Controlled Baseline
 - One Assembly/Test Site, One Fabrication Site
- Extended Temperature Performance of -40°C to 105°C
- Enhanced Diminishing Manufacturing Sources (DMS) Support
- Enhanced Product-Change Notification
- Qualification Pedigree†
- Typical V_{OLP} (Output Ground Bounce)
 <0.8 V at V_{CC} = 3.3 V, T_A = 25°C
- Typical V_{OHV} (Output V_{OH} Undershoot)
 >2.3 V at V_{CC} = 3.3 V, T_A = 25°C
- Supports Mixed-Mode Voltage Operation on All Ports
- Schmitt-Trigger Circuitry on A, B, and CLR Inputs for Slow Input Transition Rates

T Component qualification in accordance with JEDEC and industry standards to ensure reliable operation over an extended temperature range. This includes, but is not limited to, Highly Accelerated Stress Test (HAST) or biased 85/85, temperature cycle, autoclave or unbiased HAST, electromigration, bond intermetallic life, and mold compound life. Such qualification testing should not be viewed as justifying use of this component beyond specified performance and environmental limits.

- Edge Triggered From Active-High or Active-Low Gated Logic Inputs
- I_{off} Supports Partial-Power-Down Mode Operation
- Retriggerable for Very Long Output Pulses, Up To 100% Duty Cycle
- Overriding Clear Terminates Output Pulse
- Glitch-Free Power-Up Reset on Outputs
- ESD Protection Exceeds JESD 22
 - 2000-V Human-Body Model (A114-A)
 - 200-V Machine Model (A115-A)
 - 1000-V Charged-Device Model (C101)



description/ordering information

The SN74LV123A is a dual retriggerable monostable multivibrator designed for 2-V to 5.5-V V_{CC} operation.

This edge-triggered multivibrator features output pulse-duration control by three methods. In the first method, the \overline{A} input is low, and the B input goes high. In the second method, the B input is high, and the \overline{A} input goes low. In the third method, the \overline{A} input is low, the B input is high, and the clear (\overline{CLR}) input goes high.

The output pulse duration is programmable by selecting external resistance and capacitance values. The external timing capacitor must be connected between C_{ext} and R_{ext}/C_{ext} (positive) and an external resistor connected between R_{ext}/C_{ext} and V_{CC} . To obtain variable pulse durations, connect an external variable resistance between R_{ext}/C_{ext} and V_{CC} . The output pulse duration also can be reduced by taking \overline{CLR} low.

Pulse triggering occurs at a particular voltage level and is not directly related to the transition time of the input pulse. The \overline{A} , B, and \overline{CLR} inputs have Schmitt triggers with sufficient hysteresis to handle slow input transition rates with jitter-free triggering at the outputs.

ORDERING INFORMATION

TA	PACK	AGE‡	ORDERABLE PART NUMBER	TOP-SIDE MARKING
-40°C to 105°C	TSSOP - PW	Tape and reel	SN74LV123ATPWREP	L123AEP

[‡] Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.



SCLS498A - MAY 2003 - REVISED MAY 2004

description/ordering information (continued)

Once triggered, the basic pulse duration can be extended by retriggering the gated low-level-active (\overline{A}) or high-level-active (B) input. Pulse duration can be reduced by taking \overline{CLR} low. The input/output timing diagram illustrates pulse control by retriggering the inputs and early clearing.

During power up, Q outputs are in the low state, and \overline{Q} outputs are in the high state. The outputs are glitch free, without applying a reset pulse.

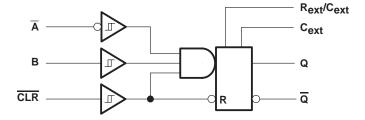
This device is fully specified for partial-power-down applications using I_{off}. The I_{off} circuitry disables the outputs, preventing damaging current backflow through the device when it is powered down.

FUNCTION TABLE (each multivibrator)

	INPUTS	:	OUTI	PIITS
	141 013		0011	
CLR	Ā	В	Q	Q
L	Х	Х	L	Н
X	Н	X	∟†	H [†]
X	Χ	L	∟†	H [†]
Н	L	\uparrow	Л	П
Н	\downarrow	Н	Л	Т
↑	L	Н	Л	T

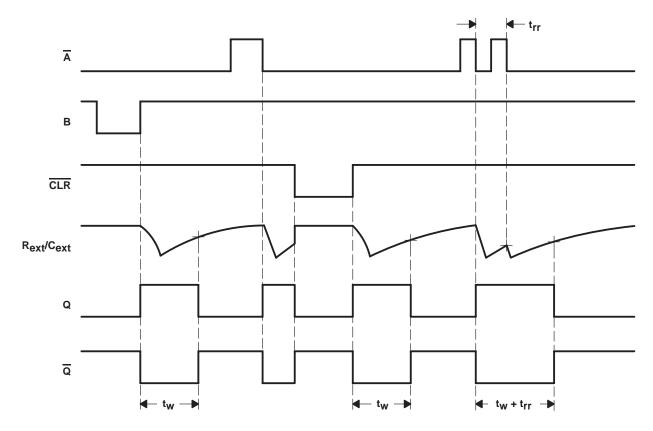
[†] These outputs are based on the assumption that the indicated steady-state conditions at the A and B inputs have been set up long enough to complete any pulse started before the setup.

logic diagram, each multivibrator (positive logic)



SCLS498A - MAY 2003 - REVISED MAY 2004

input/output timing diagram



absolute maximum ratings over operating free-air temperature (unless otherwise noted)†

Supply voltage range, V _{CC} –0).5 V to 7 V
Input voltage range, V _I (see Note 1)).5 V to 7 V
Voltage range applied to any output in the high-impedance	
or power-off state, V _O (see Note 1)).5 V to 7 V
Output voltage range in high or low state, VO (see Notes 1 and 2)	'CC + 0.5 V
Output voltage range in power-off state, V _O (see Note 1)).5 V to 7 V
Input clamp current, I_{IK} ($V_I < 0$)	–20 mA
Output clamp current, I_{OK} ($V_O < 0$)	–50 mA
Continuous output current, I_O ($V_O = 0$ to V_{CC})	±25 mA
Continuous current through V _{CC} or GND	±50 mA
Package thermal impedance, θ_{JA} (see Note 3)	. 113°C/W
Storage temperature range, T _{stg} 65°	C to 150°C

[†] Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES: 1. The input and output negative-voltage ratings may be exceeded if the input and output current ratings are observed.
 - 2. This value is limited to 5.5 V maximum.
 - 3. The package thermal impedance is calculated in accordance with JESD 51-7.



SCLS498A - MAY 2003 - REVISED MAY 2004

recommended operating conditions (see Note 4)

			MIN	MAX	UNIT	
VCC	Supply voltage		2	5.5	V	
		V _{CC} = 2 V	1.5			
\ ,,	High level secutively as	$V_{CC} = 2.3 \text{ V to } 2.7 \text{ V}$	V _{CC} ×0.7		V	
V _{IH}	High-level input voltage	$V_{CC} = 3 \text{ V to } 3.6 \text{ V}$	V _{CC} ×0.7		V	
		$V_{CC} = 4.5 \text{ V to } 5.5 \text{ V}$	$V_{CC} \times 0.7$			
		$V_{CC} = 2 V$		0.5		
V	Low lovel input voltage	$V_{CC} = 2.3 \text{ V to } 2.7 \text{ V}$		$VCC \times 0.3$	V	
VIL	Low-level input voltage	$V_{CC} = 3 \text{ V to } 3.6 \text{ V}$		$V_{CC} \times 0.3$	V	
		$V_{CC} = 4.5 \text{ V to } 5.5 \text{ V}$		$VCC \times 0.3$		
VI	Input voltage		0	5.5	V	
VO	Output voltage		0	Vcc	V	
		$V_{CC} = 2 V$		-50	μΑ	
1	Herb level extract express	$V_{CC} = 2.3 \text{ V to } 2.7 \text{ V}$		-2		
ЮН	High-level output current	$V_{CC} = 3 \text{ V to } 3.6 \text{ V}$		-6	mA	
		$V_{CC} = 4.5 \text{ V to } 5.5 \text{ V}$		-12		
		V _{CC} = 2 V		50	μΑ	
1	Laveland autout aumont	$V_{CC} = 2.3 \text{ V to } 2.7 \text{ V}$		2		
lOL	Low-level output current	V _{CC} = 3 V to 3.6 V		6	mA	
		$V_{CC} = 4.5 \text{ V to } 5.5 \text{ V}$		12		
	Enternal Carlos and Indian	V _{CC} = 2 V	5k			
R _{ext}	External timing resistance	$V_{CC} \ge 3 \text{ V}$	1k		Ω	
C _{ext}	External timing capacitance		No res	triction	pF	
Δt/ΔV _{CC}	Power-up ramp rate		1		ms/V	
T _A	Operating free-air temperature		-40	105	°C	

NOTE 4: All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, Implications of Slow or Floating CMOS Inputs, literature number SCBA004.



SCLS498A - MAY 2003 - REVISED MAY 2004

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PA	RAMETER	TEST CONDITIONS		VCC	MIN	TYP	MAX	UNIT	
		I _{OH} = -50 μA		2 V to 5.5 V	V _{CC} -0.1				
,,		I _{OH} = −2 mA		2.3 V	2			.,	
VOH		I _{OH} = -6 mA	3 V	2.48			V		
		I _{OH} = −12 mA	4.5 V	3.8					
		I _{OL} = 50 μA		2 V to 5.5 V			0.1		
\/ - ·		I _{OL} = 2 mA		2.3 V			0.4	.,	
VOL		I _{OL} = 6 mA		3 V			0.44	V	
		I _{OL} = 12 mA		4.5 V			0.55		
	R _{ext} /C _{ext} †	V _I = 5.5 V or GND		2 V to 5.5 V			±2.5		
l _I	- B 1 - 1 - 1 - 1	V 55V 0ND		0			±1	μΑ	
	A, B, and CLR	V _I = 5.5 V or GND	0 to 5.5 V			±1			
Icc	Quiescent	$V_I = V_{CC}$ or GND,) = 0	5.5 V			20	μΑ	
				3 V			280		
ICC	Active state (per circuit)	$V_I = V_{CC}$ or GND, $R_{AM}/C_{CM} = 0.5 V_{CC}$		4.5 V			650	μΑ	
	(per circuit)	$R_{\text{ext}}/C_{\text{ext}} = 0.5 \text{ VCC}$		5.5 V			975	-	
l _{off}		V_I or $V_O = 0$ to 5.5 V		0			5	μΑ	
_		V V cr CND		3.3 V		1.9			
Ci		$V_I = V_{CC}$ or GND		5 V		1.9	·	pF	

[†]This test is performed with the terminal in the off-state condition.

timing requirements over recommended operating free-air temperature range, V_{CC} = 3.3 V \pm 0.3 V (unless otherwise noted) (see Figure 1)

			TEST OF	ONDITIONS	T	λ = 25°C	;	MINI	MAY	LINUT
			TEST CC	MIN	TYP	MAX	MIN	MAX	UNIT	
	Pulse	CLR			5			5		
t _W	duration	A or B trigger	1		5			5		ns
	t _{rr} Pulse retrigger time		5 416	C _{ext} = 100 pF	‡	76		‡		ns
trr			$R_{ext} = 1 k\Omega$	$C_{ext} = 0.01 \mu F$	‡	1.8		‡		μS

[‡] See retriggering data in the *application information* section.

timing requirements over recommended operating free-air temperature range, V_{CC} = 5 V \pm 0.5 V (unless otherwise noted) (see Figure 1)

			TEOT 00	NIDITIONO	T	չ = 25°C	;		MAY	
			TEST CC	ONDITIONS	MIN	TYP	MAX	MIN	MAX	UNIT
	Pulse	CLR			5			5		
t _W	duration	A or B trigger]		5			5		ns
	Date and decoration		D 410	C _{ext} = 100 pF	‡	59		‡		ns
trr	t _{rr} Pulse retrigger time		$R_{ext} = 1 k\Omega$	$C_{ext} = 0.01 \mu F$	‡	1.5		‡		μS

[‡] See retriggering data in the application information section.



SCLS498A - MAY 2003 - REVISED MAY 2004

switching characteristics over recommended operating free-air temperature range, V_{CC} = 3.3 V \pm 0.3 V (unless otherwise noted) (see Figure 1)

DADAMETER	FROM	то	TEST	T,	Վ = 25° C	;	MAINI	MAY	
PARAMETER	(INPUT)	(OUTPUT)	CONDITIONS	MIN	TYP	MAX	MIN	MAX	UNIT
	A or B	Q or Q			11.8	24.1	1	27.5	
^t pd	CLR	Q or $\overline{\mathbb{Q}}$	C _L = 50 pF		10.5	19.3	1	22	ns
	CLR trigger	Q or Q			12.3	25.9	1	29.5	
			$C_L = 50 \text{ pF},$ $C_{ext} = 28 \text{ pF},$ $R_{ext} = 2 \text{ k}\Omega$		182	240		300	ns
_{tw} †		Q or $\overline{\mathbb{Q}}$	$C_L = 50 \text{ pF},$ $C_{ext} = 0.01 \mu\text{F},$ $R_{ext} = 10 k\Omega$	90	100	110	90	110	μs
			$C_L = 50 \text{ pF},$ $C_{ext} = 0.1 \mu\text{F},$ $R_{ext} = 10 k\Omega$	0.9	1	1.1	0.9	1.1	ms
Δt _W ‡			C _L = 50 pF		±1				%

switching characteristics over recommended operating free-air temperature range, V_{CC} = 5 V \pm 0.5 V (unless otherwise noted) (see Figure 1)

00	•	, ,	•						
DADAMETED	FROM	то	TEST	T	λ = 25°C	;	MIN	MAV	LIMIT
PARAMETER	(INPUT)	(OUTPUT)	CONDITIONS	MIN	TYP	MAX	IVIIN	MAX	UNIT
	A or B	Q or $\overline{\mathbb{Q}}$			8.3	14	1	16	
^t pd	CLR	Q or Q	C _L = 50 pF		7.4	11.4	1	13	ns
	CLR trigger	Q or $\overline{\mathbb{Q}}$]		8.7	14.9	1	17	
			$C_L = 50 \text{ pF},$ $C_{\text{ext}} = 28 \text{ pF},$ $R_{\text{ext}} = 2 \text{ k}\Omega$		167	200		240	ns
_{tw} †		Q or $\overline{\mathbb{Q}}$	C_L = 50 pF, C_{ext} = 0.01 μ F, R_{ext} = 10 k Ω	90	100	110	90	110	μS
			C_L = 50 pF, C_{ext} = 0.1 μ F, R_{ext} = 10 k Ω	0.9	1	1.1	0.9	1.1	ms
∆t _W ‡					±1				%

 $[\]dagger t_W = Duration of pulse at Q and <math>\overline{Q}$ outputs

operating characteristics, T_A = 25°C

	PARAMETER	TEST CO	NDITIONS	VCC	TYP	UNIT
_	Davies discination consistence	0. 505	f 40 MH-	3.3 V	44	
Cpd	Power dissipation capacitance	$C_L = 50 \text{ pF},$	f = 10 MHz	5 V	49	p⊦

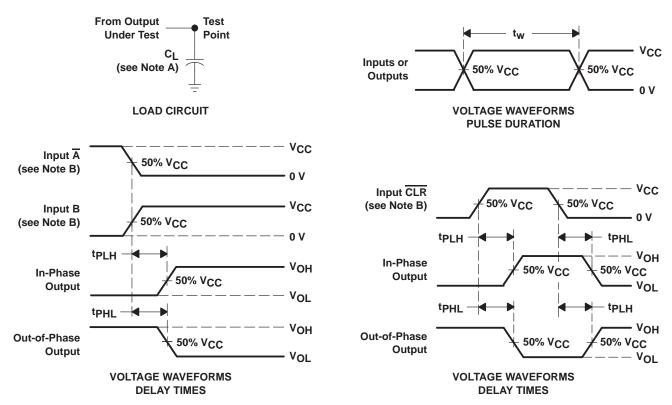


[†] t_W = Duration of pulse at Q and \overline{Q} outputs ‡ Δt_W = Output pulse-duration variation (Q and \overline{Q}) between circuits in same package

 $^{^{\}ddagger}\Delta t_W = \text{Output pulse-duration variation (Q and } \overline{Q})$ between circuits in same package

SCLS498A - MAY 2003 - REVISED MAY 2004

PARAMETER MEASUREMENT INFORMATION

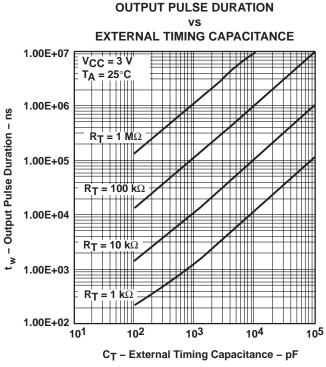


NOTES: A. C_L includes probe and jig capacitance.

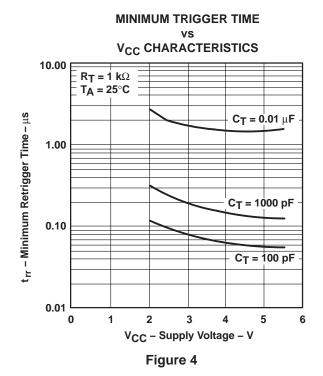
- B. All input pulses are supplied by generators having the following characteristics: PRR \leq 1 MHz, $Z_O = 50 \Omega$, $t_f = 3 \text{ ns}$.
- C. The outputs are measured one at a time, with one input transition per measurement.

Figure 1. Load Circuit and Voltage Waveforms

APPLICATION INFORMATION[†]







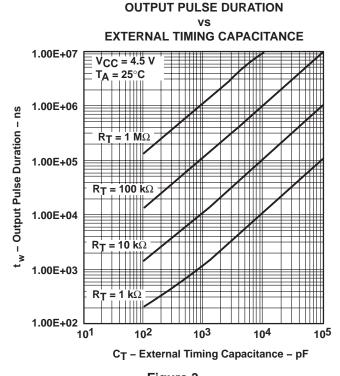
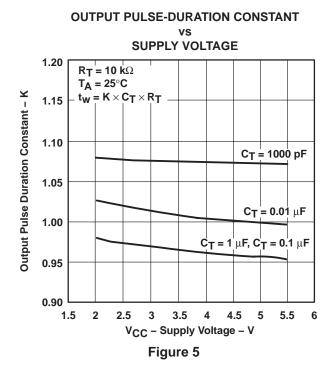


Figure 3



[†]Operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied.





PACKAGE OPTION ADDENDUM

10-Dec-2020

PACKAGING INFORMATION

www.ti.com

Orderable Device	Status	Package Type	Package Drawing	Pins	Package Qty	Eco Plan	Lead finish/ Ball material	MSL Peak Temp	Op Temp (°C)	Device Marking (4/5)	Samples
SN74LV123ATPWREP	ACTIVE	TSSOP	PW	16	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	L123AEP	Samples
V62/03661-01XE	ACTIVE	TSSOP	PW	16	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	L123AEP	Samples

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

(2) RoHS: TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

Green: TI defines "Green" to mean the content of Chlorine (CI) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

- (3) MSL, Peak Temp. The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.
- (4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.
- (5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.
- (6) Lead finish/Ball material Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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PACKAGE OPTION ADDENDUM

10-Dec-2020

OTHER QUALIFIED VERSIONS OF SN74LV123A-EP:

• Automotive: SN74LV123A-Q1

NOTE: Qualified Version Definitions:

- Catalog TI's standard catalog product
- Automotive Q100 devices qualified for high-reliability automotive applications targeting zero defects

PACKAGE MATERIALS INFORMATION

www.ti.com 16-Oct-2020

TAPE AND REEL INFORMATION





A0	Dimension designed to accommodate the component width
	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing		SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74LV123ATPWREP	TSSOP	PW	16	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1

PACKAGE MATERIALS INFORMATION

www.ti.com 16-Oct-2020



*All dimensions are nominal

Device	Device Package Type		Pins	SPQ	Length (mm)	Width (mm)	Height (mm)	
SN74LV123ATPWREP	TSSOP	PW	16	2000	853.0	449.0	35.0	

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