

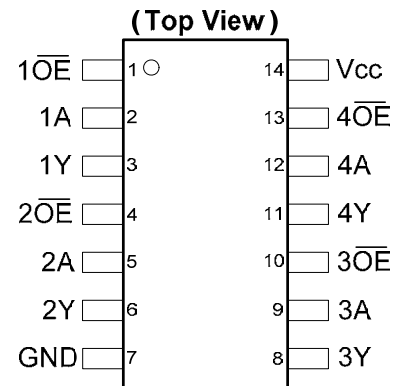
QUADRUPLE 3-STATE BUFFERS
Description

The 74LVC125A provides four independent buffers with three state outputs. Each output is independently controlled by an associated output enable pin (OE) which places the device in the high impedance state when driven high. The device is designed for operation with a power supply range of 1.65V to 5.5V. The inputs are tolerant to 5.5V allowing this device to be used in a mixed voltage environment. The device is fully specified for partial power down applications using IOFF. The IOFF circuitry disables the output preventing damaging current backflow when the device is powered down.

Features

- Supply Voltage Range from 1.65V to 5.5V
- Sinks 24mA at Vcc = 3.3V
- CMOS low power consumption
- IOFF Supports Partial-Power-Down Mode Operation
- Inputs or outputs accept up to 5.5V
- Inputs can be driven by 3.3V or 5.5V allowing for voltage translation applications.
- ESD Protection Exceeds JESD 22
 - 200-V Machine Model (A115-A)
 - 2000-V Human Body Model (A114-A)
 - Exceeds 1000-V Charged Device Model (C101C)
- Latch-Up Exceeds 250mA per JESD 78, Class II
- Range of Package Options SO-14 and TSSOP-14
- **Totally Lead-Free & Fully RoHS Compliant (Notes 1 & 2)**
- **Halogen and Antimony Free. "Green" Device (Note 3)**

Notes: 1. No purposely added lead. Fully EU Directive 2002/95/EC (RoHS) & 2011/65/EU (RoHS 2) compliant.
 2. See <http://www.diodes.com> for more information about Diodes Incorporated's definitions of Halogen- and Antimony-free, "Green" and Lead-free.
 3. Halogen- and Antimony-free "Green" products are defined as those which contain <900ppm bromine, <900ppm chlorine (<1500ppm total Br + Cl) and <1000ppm antimony compounds.

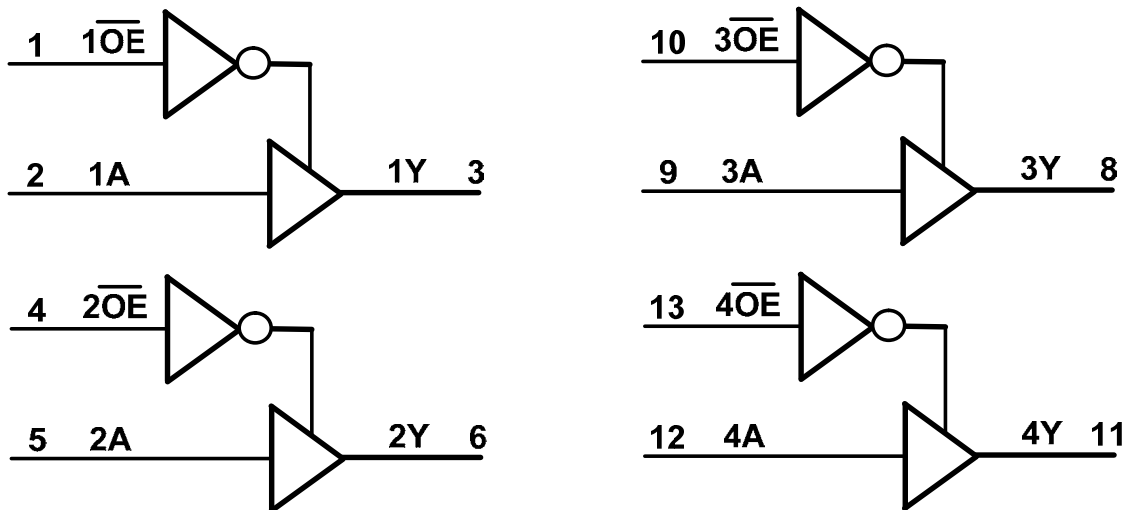
Pin Assignments

SO-14 / TSSOP-14
Applications

- Voltage Level Shifting
- General Purpose Logic
- Power Down Signal Isolation
- Wide array of products such as:
 - PCs, networking, notebooks, ultrabooks, netbooks
 - Computer peripherals, hard drives, CD/DVD ROM
 - TV, DVD, DVR, set top box

Pin Descriptions

Pin Number	Pin Name	Description
1	1OE	Data Enable Input (active low)
2	1A	Data Input
3	1Y	Data Output
4	2OE	Data Enable Input (active low)
5	2A	Data Input
6	2Y	Data Output
7	GND	Ground
8	3Y	Data Output
9	3A	Data Input
10	3OE	Data Enable Input (active low)
11	4Y	Data Output
12	4A	Data Input
13	4OE	Data Enable Input (active low)
14	V _{CC}	Supply Voltage

Logic Diagram



Function Table

Inputs		Output
OE	A	Y
L	H	H
L	L	L
H	X	Z

Absolute Maximum Ratings (Note 4) (@T_A = +25°C, unless otherwise specified.)

Symbol	Description	Rating	Unit
ESD HBM	Human Body Model ESD Protection	2	KV
ESD CDM	Charged Device Model ESD Protection	1	KV
ESD MM	Machine Model ESD Protection	200	V
V _{CC}	Supply Voltage Range	-0.5 to 6.5	V
V _I	Input Voltage Range	-0.5 to 6.5	V
V _O	Voltage applied to output in high impedance or I _{OFF} state	-0.5 to 6.5	V
V _O	Voltage applied to output in high or low state	-0.3 to V _{CC} +0.5	V
I _{IK}	Input Clamp Current V _I < 0	-50	mA
I _{OK}	Output Clamp Current V _O < 0	-50	mA
I _O	Continuous output current	±50	mA
I _{CC} , I _{GND}	Continuous current through V _{CC} or GND	±100	mA
T _J	Operating Junction Temperature	-40 to +150	°C
T _{STG}	Storage Temperature	-65 to +150	°C
P _{TOT}	Total Power Dissipation	500	mW

Note: 4. Stresses beyond the absolute maximum may result in immediate failure or reduced reliability. These are stress values and device operation should be within recommend values.

Recommended Operating Conditions (Note 5) (@T_A = +25°C, unless otherwise specified.)

Symbol	Parameter	Conditions	Min	Max	Unit
V _{CC}	Supply Voltage		1.65	5.50	V
V _I	Input Voltage		0	5.5	V
V _O	Output Voltage	Active Mode	0	V _{CC}	V
		V _{CC} = 0V; Power Down Mode	0	5.5	V
Δt/ΔV	Input transition rise or fall rate	V _{CC} = 1.65V to 2.7V		20	ns/V
		V _{CC} = 2.7V to 3.6V		10	
T _A	Operating free-air temperature		-40	+125	°C

Note: 5. Unused inputs should be held at V_{CC} or Ground.

Electrical Characteristics (@ $T_A = +25^\circ\text{C}$, unless otherwise specified.)

Symbol	Parameter	Test Conditions	V_{CC}	$T_A = -40^\circ\text{C to } 85^\circ\text{C}$		$T_A = -40^\circ\text{C to } 125^\circ\text{C}$		Unit
				Min	Max	Min	Max	
V_{IH}	High-level Input Voltage		1.65V to 1.95V	$0.65 \times V_{CC}$		$0.65 \times V_{CC}$		V
			2.3V to 2.7V	1.7		1.6		
			2.7V to 3.6V	2.0		2.0		
V_{IL}	Low-level input voltage		1.65V to 1.95V		$0.35 \times V_{CC}$		$0.35 \times V_{CC}$	V
			2.3V to 2.7V		0.7		0.7	
			2.7V to 3.6V		0.8		0.8	
V_{OH}	High Level Output Voltage	$I_{OH} = -100\mu\text{A}$	1.65V to 3.6V	$V_{CC} - 0.2$		$V_{CC} - 0.3$		V
		$I_{OH} = -4\text{mA}$	1.65V	1.2				
		$I_{OH} = -8\text{mA}$	2.3V	1.9				
		$I_{OH} = -12\text{mA}$	2.7V	2.2		2.05		
			3.0V	2.3		2.1		
$I_{OH} = -24\text{mA}$	3.0V	2.2		2.0				
V_{OL}	High-level Output Voltage	$I_{OH} = 100\mu\text{A}$	1.65V to 3.6V		0.2		0.3	V
		$I_{OH} = 4\text{mA}$	1.65V		0.45		0.6	
		$I_{OH} = 8\text{mA}$	2.3V		0.70		0.85	
		$I_{OH} = 12\text{mA}$	2.7V		0.40		0.6	
			3.0V		0.55		0.6	
$I_{OH} = -24\text{mA}$	3.0V		0.55		0.6			
I_I	Input Current	$V_I = \text{GND to } 5.5\text{V}$	3.6V		± 5		± 20	μA
I_{OZ}	Z State Leakage Current	$V_O = \text{GND or } 5.5\text{V}$	3.6V		± 10		± 20	μA
I_{OFF}	Power Down Leakage Current	$V_I \text{ or } V_O = 0\text{V to } 3.6\text{V}$	0		10		20	μA
I_{CC}	Supply Current	$V_I = \text{GND or } V_{CC} \text{ } I_O = 0$	3.6V		10		40	μA
ΔI_{CC}	Additional Supply Current	One input at V_{CC} -0.6V Other	2.7V to 3.6V		500		5000	μA

Switching Characteristics

Parameter	From (Input)	To (Output)	Test Conditions See Figure 1	T _A = +25°C			-40°C to +85°C		-40°C to +125°C		Unit
				Min	Typ	Max	Min	Max	Min	Max	
t _{pd}	A	Y	V _{CC} = 1.8V ± 0.15V	1.0	4.5	11.8	1.0	12.3	1.0	13.8	ns
			V _{CC} = 2.5V ± 0.2V	1.0	2.7	5.8	1.0	6.3	1.0	8.4	
			V _{CC} = 2.7V	1.0	3.0	5.3	1.0	5.5	1.0	7.0	
			V _{CC} = 3.3V ± 0.3V	1.0	2.5	4.6	1.0	4.8	1.0	6.0	
t _{en}	$\overline{\text{OE}}$	Y	V _{CC} = 1.8V ± 0.15V	1.0	4.3	13.8	1.0	14.3	1.0	15.8	ns
			V _{CC} = 2.5V ± 0.2V	1.0	2.7	6.6	1.0	7.4	1.0	9.5	
			V _{CC} = 2.7V	1.0	3.3	6.4	1.0	6.6	1.0	8.5	
			V _{CC} = 3.3V ± 0.3V	1.0	2.4	5.2	1.0	5.4	1.0	7.0	
t _{dis}	$\overline{\text{OE}}$	Y	V _{CC} = 1.8V ± 0.15V	1.0	4.3	10.6	1.0	11.1	1.0	12.6	ns
			V _{CC} = 2.5V ± 0.2V	1.0	2.2	5.1	1.0	5.6	1.0	7.7	
			V _{CC} = 2.7V	1.0	2.5	4.8	1.0	5.0	1.0	6.5	
			V _{CC} = 3.3V ± 0.3V	1.0	2.4	4.4	1.0	4.6	1.0	6.0	
t _{SK(0)}			V _{CC} = 3.3V ± 0.3V			1.0		1.0		1.5	ns

Operating Characteristics (@T_A = +25°C, unless otherwise specified.)

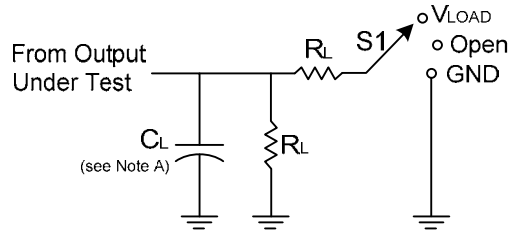
Parameter		Test Conditions	V _{CC} = 1.8V	V _{CC} = 2.5V	V _{CC} = 3.3V	Unit
			Typ	Typ	Typ	
C _{pd}	Power dissipation capacitance per gate	f = 10 MHz	7.3	11.2	14.9	pF
C _i	Input Capacitance	V _i = V _{CC} – or GND	4	4	4	pF

Package Characteristics

Symbol	Parameter	Test Conditions	V _{CC}	Min	Typ	Max	Unit
θ _{JA}	Thermal Resistance Junction-to-Ambient	SO-14	(Note 6)		TBD		°C/W
		TSSOP-14			159		
θ _{JC}	Thermal Resistance Junction-to-Case	SO-14	(Note 6)		TBD		°C/W
		TSSOP-14			25		

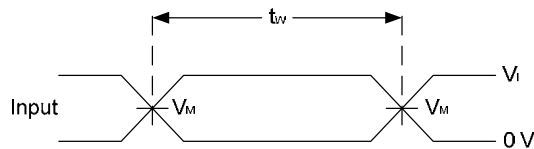
Note: 6. Test condition for SO-14 and TSSOP-14: Device mounted on FR-4 substrate PC board, 2oz copper, with minimum recommended pad layout.

Parameter Measurement Information

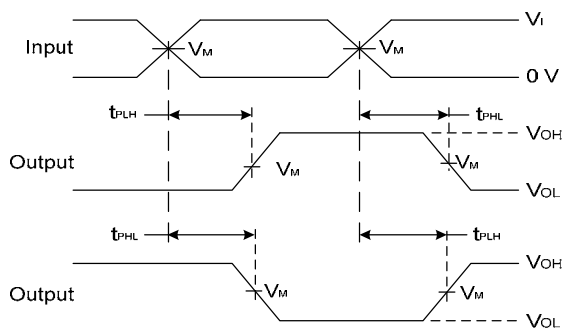


TEST	S1
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	V_{LOAD}
t_{PHZ}/t_{PZH}	GND

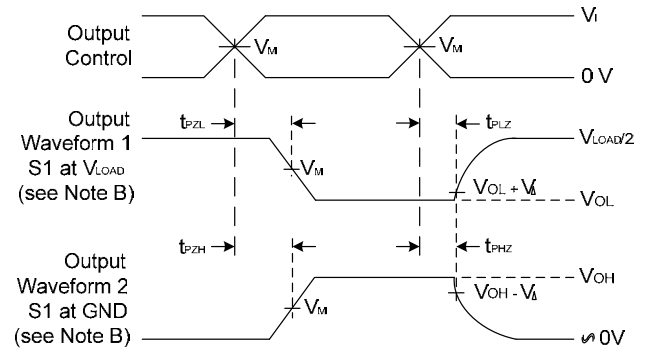
V_{CC}	Inputs		V_M	V_{LOAD}	C_L	R_L	V_{Δ}
	V_I	t_r/t_f					
$1.8V \pm 0.15V$	V_{CC}	$\leq 2ns$	$V_{CC}/2$	$2 \times V_{CC}$	30pF	1K Ω	0.15V
$2.5V \pm 0.2V$	V_{CC}	$\leq 2ns$	$V_{CC}/2$	$2 \times V_{CC}$	30pF	500 Ω	0.15V
2.7V	2.7V	$\leq 2.5ns$	1.5V	6V	50pF	500 Ω	0.3V
$3.3V \pm 0.3V$	2.7V	$\leq 2.5ns$	1.5V	6V	50pF	500 Ω	0.3V



Voltage Waveform Pulse Duration



Voltage Waveform Propagation Delay Times Inverting and Non Inverting Outputs

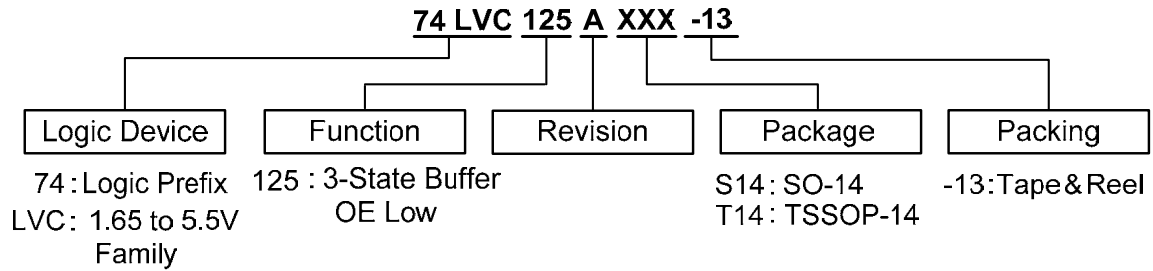


Voltage Waveform Enable and Disable Times Low and High Level Enabling

- Notes:
- A. Includes test lead and test apparatus capacitance.
 - B. All pulses are supplied at pulse repetition rate ≤ 10 MHz.
 - C. Inputs are measured separately one transition per measurement.
 - D. t_{PLZ} and t_{PHZ} are the same as t_{dis} .
 - E. t_{PZL} and t_{PZH} are the same as t_{EN0}
 - F. t_{PLH} and t_{PHL} are the same as t_{PD} .

Figure 1. Load Circuit and Voltage Waveforms

Ordering Information

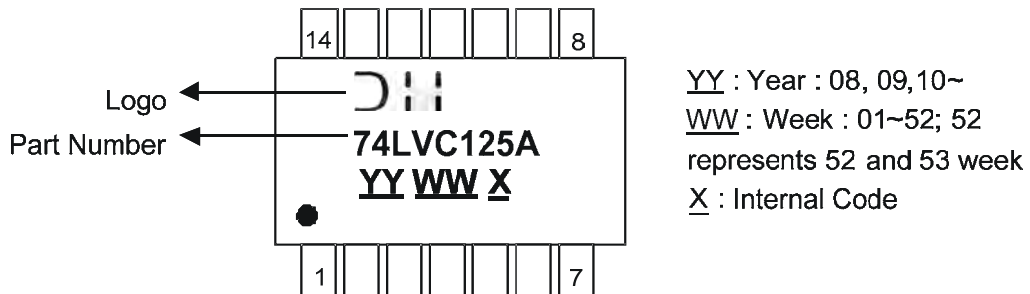


Device	Package Code	Packaging (Note 7)	13" Tape and Reel	
			Quantity	Part Number Suffix
74LVC125AS14-13	S14	SO-14	2500/Tape & Reel	-13
74LVC125AT14-13	T14	TSSOP-14	2500/Tape & Reel	-13

Notes: 7. The taping orientation and tape details can be found at <http://www.diodes.com/datasheets/ap02007.pdf>

Marking Information

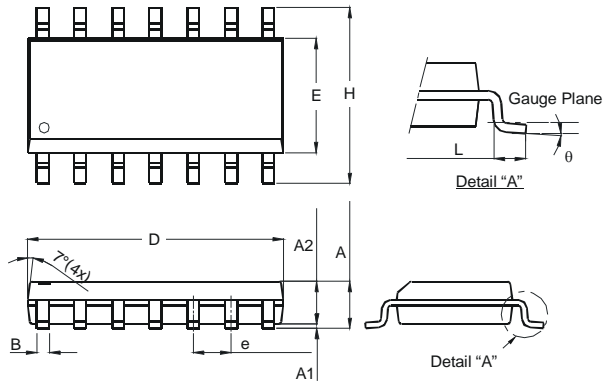
(1) SO-14 , TSSOP-14



Part Number	Package
74LVC125AS14	SO-14
74LVC125AT14	TSSOP-14

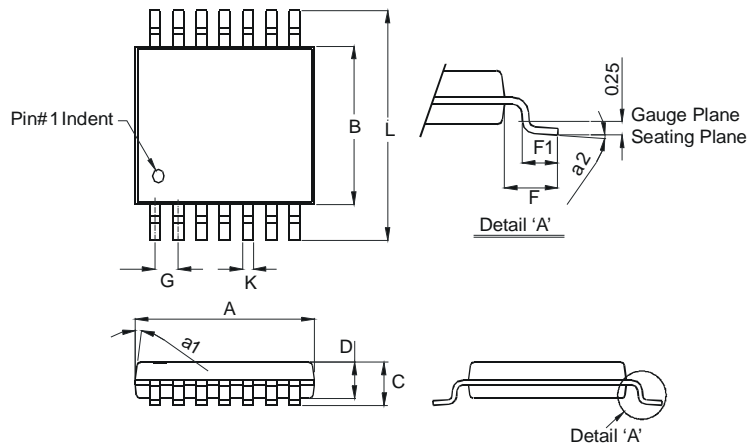
Package Outline Dimensions (All dimensions in mm.)

Package Type: SO-14



SO-14		
Dim	Min	Max
A	1.47	1.73
A1	0.10	0.25
A2	1.45 Typ	
B	0.33	0.51
D	8.53	8.74
E	3.80	3.99
e	1.27 Typ	
H	5.80	6.20
L	0.38	1.27
θ	0°	8°
All Dimensions in mm		

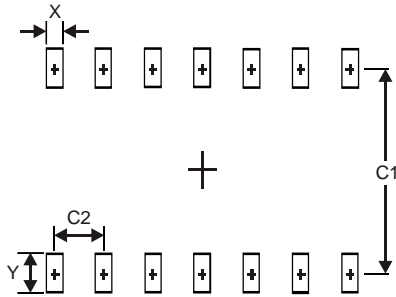
Package Type: TSSOP-14



TSSOP-14		
Dim	Min	Max
a1	7° (4X)	
a2	0°	8°
A	4.9	5.10
B	4.30	4.50
C	—	1.2
D	0.8	1.05
F	1.00 Typ	
F1	0.45	0.75
G	0.65 Typ	
K	0.19	0.30
L	6.40 Typ	
All Dimensions in mm		

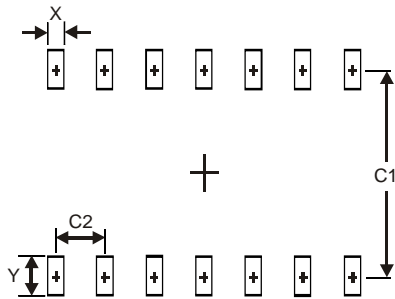
Suggested Pad Layout

Package Type: SO-14



Dimensions	Value (in mm)
X	0.60
Y	1.50
C1	5.4
C2	1.27

Package Type: TSSOP-14



Dimensions	Value (in mm)
X	0.45
Y	1.45
C1	5.9
C2	0.65

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