

# CD4067B, CD4097B Types

## CMOS Analog Multiplexers/Demultiplexers

High-Voltage Types (20-Volt Rating)

CD4067B – Single 16-Channel Multiplexer/Demultiplexer

CD4097B – Differential 8-Channel Multiplexer/Demultiplexer

■ CD4067B and CD4097B CMOS analog multiplexers/demultiplexers\* are digitally controlled analog switches having low ON impedance, low OFF leakage current, and internal address decoding. In addition, the ON resistance is relatively constant over the full input-signal range.

The CD4067B is a 16-channel multiplexer with four binary control inputs, A, B, C, D, and an inhibit input, arranged so that any combination of the inputs selects one switch.

The CD4097B is a differential 8-channel multiplexer having three binary control inputs A, B, C, and an inhibit input. The inputs permit selection of one of eight pairs of switches.

A logic "1" present at the inhibit input turns all channels off.

The CD4067B and CD4097B types are supplied in 24-lead hermetic dual-in-line ceramic packages (F3A suffix), 24-lead dual-in-line plastic packages (E suffix), 24-lead small-outline packages (M, M96, and NSR suffixes), and 24-lead thin shrink small-outline packages (P and PWR suffixes).

\*When these devices are used as demultiplexers, the channel in/out terminals are the outputs and the common out/in terminals are the inputs.

### Recommended Operating Conditions at $T_A = 25^\circ\text{C}$ (Unless Otherwise Specified)

For maximum reliability, nominal operating conditions should be selected so that operation is always within the following ranges. Values shown apply to all types except as noted.

Characteristic	Min.	Max.	Units
Supply-Voltage Range ( $T_A$ =Full Package-Temp. Range)	3	18	V
Multiplexer Switch Input Current Capability	–	25	mA
Output Load Resistance	100	–	$\Omega$

#### NOTE:

In certain applications, the external load-resistor current may include both  $V_{DD}$  and signal-line components. To avoid drawing  $V_{DD}$  current when switch current flows into the transmission gate inputs, the voltage drop across the bidirectional switch must not exceed 0.8 volt (calculated from  $R_{ON}$  values shown in ELECTRICAL CHARACTERISTICS CHART). No  $V_{DD}$  current will flow through  $R_L$  if the switch current flows into terminal 1 on the CD4067; terminals 1 and 17 on the CD4097.

#### Features:

- Low ON resistance:  $125 \Omega$  (typ.) over 15  $V_{pp}$  signal-input range for  $V_{DD}-V_{SS}=15 \text{ V}$
- High OFF resistance: channel leakage of  $\pm 10 \text{ pA}$  (typ.) @  $V_{DD}-V_{SS}=10 \text{ V}$
- Matched switch characteristics:  $R_{ON}=5 \Omega$  (typ.) for  $V_{DD}-V_{SS}=15 \text{ V}$
- Very low quiescent power dissipation under all digital-control input and supply conditions:  $0.2 \mu\text{W}$  (typ.) @  $V_{DD}-V_{SS}=10 \text{ V}$
- Binary address decoding on chip
- 5-V, 10-V, and 15-V parametric ratings
- 100% tested for quiescent current at 20 V
- Standardized symmetrical output characteristics
- Maximum input current of  $1 \mu\text{A}$  at 18 V over full package temperature range;  $100 \text{ nA}$  at 18 V and  $25^\circ\text{C}$
- Meets all requirements of JEDEC Tentative Standard No. 13B, "Standard Specifications for Description of 'B' Series CMOS Devices"

#### Applications:

- Analog and digital multiplexing and demultiplexing
- A/D and D/A conversion
- Signal gating

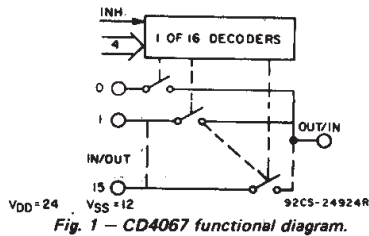
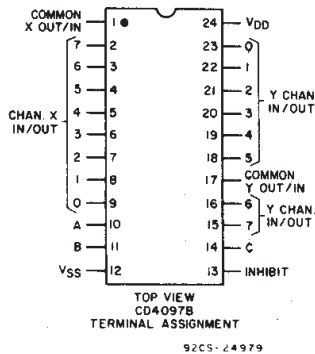
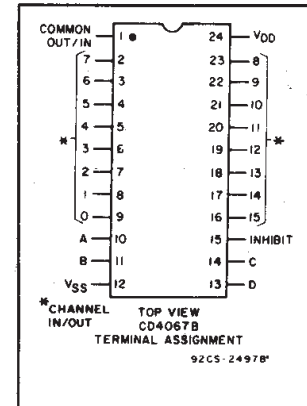


Fig. 1 – CD4067 functional diagram.

CD4067 TRUTH TABLE

A	B	C	D	Inh	Selected Channel
X	X	X	X	1	None
0	0	0	0	0	0
1	0	0	0	0	1
0	1	0	0	0	2
1	1	0	0	0	3
0	0	1	0	0	4
1	0	1	0	0	5
0	1	1	0	0	6
1	1	1	0	0	7
0	0	0	1	0	8
1	0	0	1	0	9
0	1	0	1	0	10
1	1	0	1	0	11
0	0	1	1	0	12
1	0	1	1	0	13
0	1	1	1	0	14
1	1	1	1	0	15

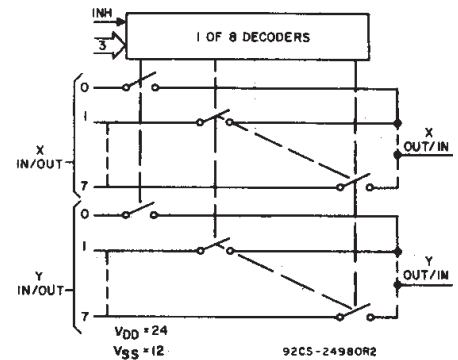


Fig. 2 – CD4097 functional diagram.

CD4097 TRUTH TABLE

A	B	C	Inh	Selected Channel
X	X	X	1	None
0	0	0	0	0X, 0Y
1	0	0	0	1X, 1Y
0	1	0	0	2X, 2Y
1	1	0	0	3X, 3Y
0	0	1	0	4X, 4Y
1	0	1	0	5X, 5Y
0	1	1	0	6X, 6Y
1	1	1	0	7X, 7Y

# CD4067B, CD4097B Types

## ELECTRICAL CHARACTERISTICS

CHARACTERISTIC	CONDITIONS			LIMITS AT INDICATED TEMPERATURES (°C)						Units	
	$V_{is}$ (V)	$V_{SS}$ (V)	$V_{DD}$ (V)	-55	-40	+85	+125	+25			
								Min.	Typ.		Max.
<b>SIGNAL INPUTS (<math>V_{is}</math>) AND OUTPUTS (<math>V_{OS}</math>)</b>											
Quiescent Device Current, $I_{DD}$ Max.			5	5	5	150	150	—	0.04	5	$\mu A$
			10	10	10	300	300	—	0.04	10	
			15	20	20	600	600	—	0.04	20	
			20	100	100	3000	3000	—	0.08	100	
ON-state Resistance $V_{SS} \leq V_{is} \leq V_{DD}$ $r_{on}$ Max.		0	5	800	850	1200	1300	—	470	1050	$\Omega$
		0	10	310	330	520	550	—	180	400	
		0	15	200	210	300	320	—	125	240	
Change in on-state Resistance (Between Any Two Channels) $\Delta r_{on}$		0	5	—	—	—	—	—	15	—	$\Omega$
		0	10	—	—	—	—	—	10	—	
		0	15	—	—	—	—	—	5	—	
OFF Channel Leakage Current: Any Channel OFF (Common OUT/IN) Max. or All Channels OFF		0	18	$\pm 100^*$		$\pm 1000^*$			$\pm 0.1$	$\pm 100^*$	$nA$
Capacitance: Input, $C_{is}$ Output, $C_{os}$ CD4067 CD4097 Feed-through, $C_{ios}$				—	—	—	—	—	5	—	$pF$
		-5	5	—	—	—	—	—	55	—	
				—	—	—	—	—	35	—	
Propagation Delay Time (Signal Input to Output)	$V_{DD}$ 	$R_L = 200 K\Omega$ $C_L = 50 pF$ $t_r, t_f = 20 ns$	5	—	—	—	—	—	30	60	$ns$
			10	—	—	—	—	—	15	30	
			15	—	—	—	—	—	10	20	
<b>CONTROL (ADDRESS or INHIBIT) <math>V_C</math></b>											
Input Low Voltage, $V_{IL}$ Max.	$=V_{DD}$ thru $1 K\Omega$	$R_L = 1 K\Omega$ to $V_{SS}$ $I_{IS} < 2 \mu A$ on all OFF Channels	5	1.5	—	—	—	—	—	1.5	$V$
			10	3	—	—	—	—	3		
			15	4	—	—	—	—	4		
Input High Voltage, $V_{IH}$ Min.	$=V_{DD}$ thru $1 K\Omega$	$R_L = 1 K\Omega$ to $V_{SS}$ $I_{IS} < 2 \mu A$ on all OFF Channels	5	3.5	3.5	—	—	—	—	—	
			10	7	7	—	—	—	—		
			15	11	11	—	—	—	—		

\* Determined by minimum feasible leakage measurement for automatic testing.

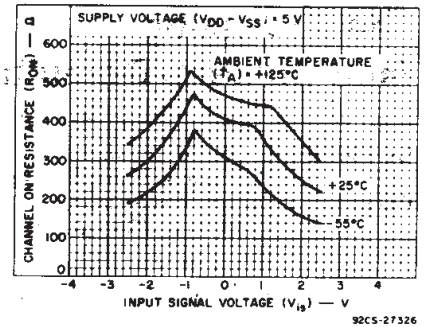


Fig. 3—Typical ON resistance vs. input signal voltage (all types).

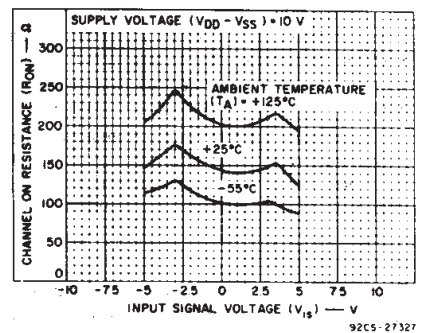


Fig. 4—Typical ON resistance vs. input signal voltage (all types).

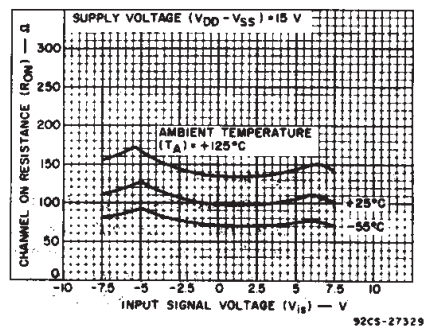


Fig. 5—Typical ON resistance vs. input signal voltage (all types).

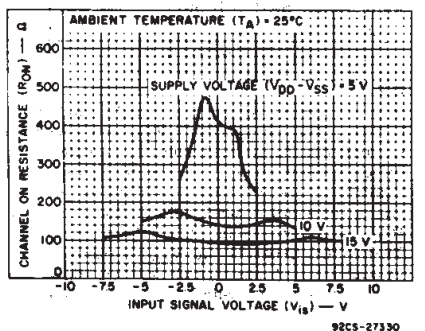


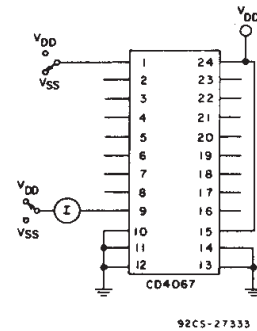
Fig. 6—Typical ON resistance vs. input signal voltage (all types).

# CD4067B, CD4097B Types

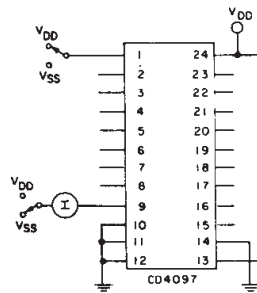
## ELECTRICAL CHARACTERISTICS (Cont'd)

CHARACTERISTIC	CONDITIONS			LIMITS AT INDICATED TEMPERATURES (°C)							Units
	V <sub>is</sub> (V)	V <sub>SS</sub> (V)	V <sub>DD</sub> (V)	-55	-40	+85	+125	+25			
								Min.	Typ.	Max.	
Input Current, I <sub>IN</sub> Max.	V <sub>IN</sub> = 0, 18 V			±0.1	±0.1	±1	±1	—	±10 <sup>-5</sup>	±0.1	μA
Propagation Delay Time: Address or Inhibit-to-Signal OUT (Channel turning ON)	R <sub>L</sub> = 10 KΩ, C <sub>L</sub> = 50 pF, t <sub>r</sub> , t <sub>f</sub> = 20 ns			—	—	—	—	—	325	650	ns
	0	5	—	—	—	—	—	—	135	270	
	0	10	—	—	—	—	—	—	95	190	
Address or Inhibit-to-Signal OUT (Channel turning OFF)	R <sub>L</sub> = 300 Ω, C <sub>L</sub> = 50 pF, t <sub>r</sub> , t <sub>f</sub> = 20 ns			—	—	—	—	—	220	440	ns
	0	5	—	—	—	—	—	—	90	180	
	0	15	—	—	—	—	—	—	65	130	
Input Capacitance, C <sub>IN</sub>	Any Address or Inhibit Input			—	—	—	—	—	5	7.5	pF

## TEST CIRCUITS



92CS-27333

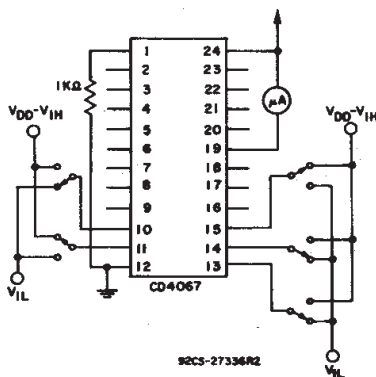


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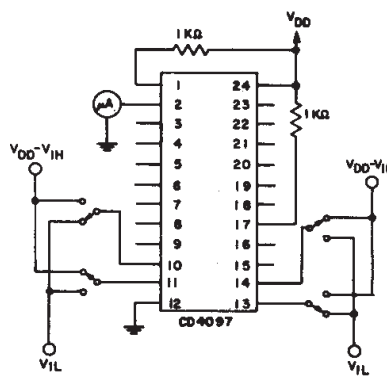
Fig. 7—OFF channel leakage current—any channel OFF.

## MAXIMUM RATINGS, Absolute-Maximum Values:

- DC SUPPLY-VOLTAGE RANGE, (V<sub>DD</sub>)  
Voltages referenced to V<sub>SS</sub> Terminal) ..... -0.5V to +20V
- INPUT VOLTAGE RANGE, ALL INPUTS ..... -0.5V to V<sub>DD</sub> +0.5V
- DC INPUT CURRENT, ANY ONE INPUT ..... ±10mA
- POWER DISSIPATION PER PACKAGE (P<sub>D</sub>):  
For T<sub>A</sub> = -55°C to +100°C ..... 500mW  
For T<sub>A</sub> = +100°C to +125°C ..... Derate Linearly at 12mW/°C to 200mW
- DEVICE DISSIPATION PER OUTPUT TRANSISTOR  
FOR T<sub>A</sub> = FULL PACKAGE-TEMPERATURE RANGE (All Package Types) ..... 100mW
- OPERATING-TEMPERATURE RANGE (T<sub>A</sub>) ..... -55°C to +125°C
- STORAGE TEMPERATURE RANGE (T<sub>stg</sub>) ..... -65°C to +150°C
- LEAD TEMPERATURE (DURING SOLDERING):  
At distance 1/16 ± 1/32 inch (1.59 ± 0.79mm) from case for 10s max ..... +265°C

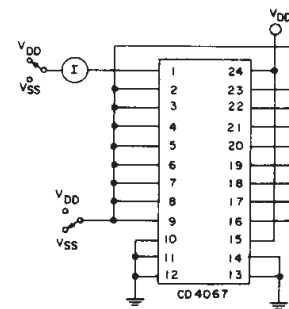


92CS-27336R2

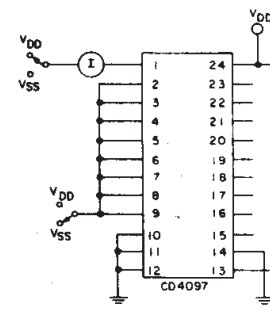


92CS-27337R2

Fig. 8—Input voltage—measure < 2 μA on all OFF channels (e.g., channel 12).



92CS-27334



92CS-27335

Fig. 9—OFF channel leakage current—all channels OFF.

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# CD4067B, CD4097B Types

## ELECTRICAL CHARACTERISTICS (Cont'd)

CHARACTERISTIC	TEST CONDITIONS			TYPICAL VALUES	UNITS	
	V <sub>is</sub> (V)	V <sub>DD</sub> (V)	R <sub>L</sub> (KΩ)			
Cutoff (-3 dB) Frequency Channel ON (Sine Wave Input)	5 <sup>●</sup>	10	1	CD4067	14	MHz
	20 log $\frac{V_{os}}{V_{is}} = -3$ dB			CD4097	20	
				V <sub>os</sub> at Common OUT/IN		
				V <sub>os</sub> at Any Channel		
Total Harmonic Distortion, THD	2 <sup>●</sup>	5	10			0.3
	3 <sup>●</sup>	10				0.2
	5 <sup>●</sup>	15				0.12
	f <sub>is</sub> = 1 kHz sine wave					
-40 dB Feedthrough Frequency (All Channels OFF)	5 <sup>●</sup>	10	1	CD4067	20	MHz
	20 log $\frac{V_{os}}{V_{is}} = -40$ dB			CD4097	12	
				V <sub>os</sub> at Any Channel		8
Signal Crosstalk (Frequency at -40 dB)	5 <sup>●</sup>	10	1	Between Any 2 Channels <sup>▲</sup>		1
	20 log $\frac{V_{os}}{V_{is}} = -40$ dB			Between Sections CD4097 Only	Measured on Common	10
					Measured on Any Channel	18
Address-or-Inhibit-to-Signal Crosstalk	V <sub>SS</sub> =0, t <sub>r</sub> , t <sub>f</sub> =20 ns, V <sub>C</sub> =V <sub>DD</sub> -V <sub>SS</sub> (Square Wave)					75
						mV (Peak)

● Peak-to-peak voltage symmetrical about  $\frac{V_{DD}-V_{SS}}{2}$ .

▲ Worst case.

\* Both ends of channel.

## TEST CIRCUITS (Cont'd)

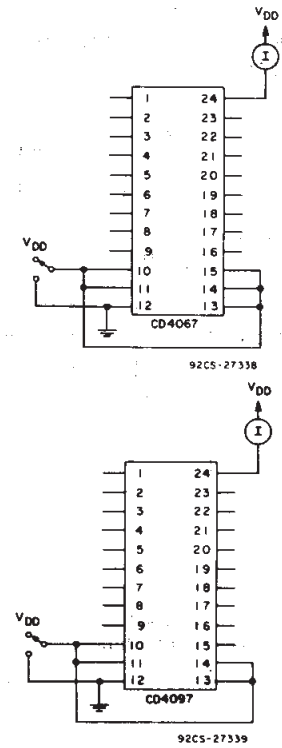


Fig. 10—Quiescent device current.

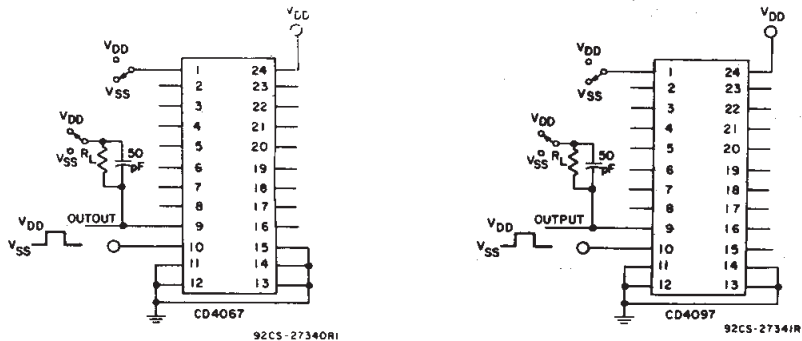


Fig. 11—Turn-on and turn-off propagation delay—address select input to signal output (e.g. measured on channel 0).

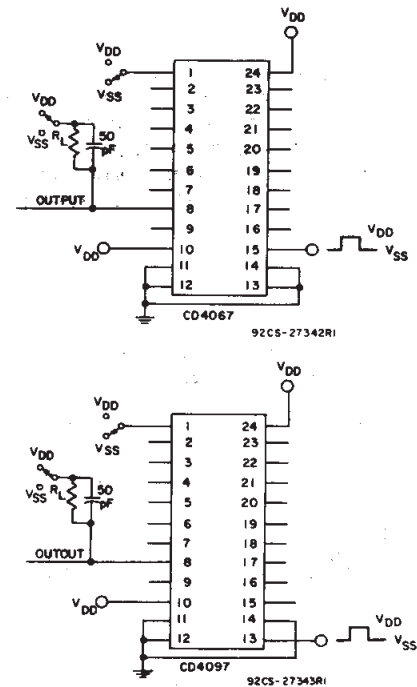


Fig. 12—Turn-on and turn-off propagation delay—  
inhibit input to signal output (e.g. measured on channel 1).

# CD4067B, CD4097B Types

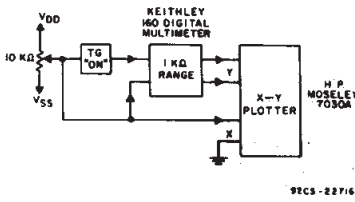


Fig. 13- Channel ON resistance measurement circuit.

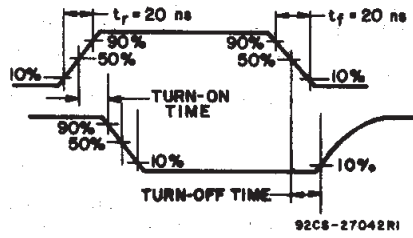


Fig. 14- Propagation delay waveform channel being turned ON ( $R_L = 10\text{ K}\Omega$ ,  $C_L = 50\text{ pF}$ ).

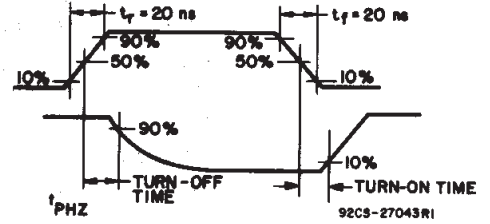


Fig. 15- Propagation delay waveform, channel being turned OFF ( $R_L = 300\Omega$ ,  $C_L = 50\text{ pF}$ ).

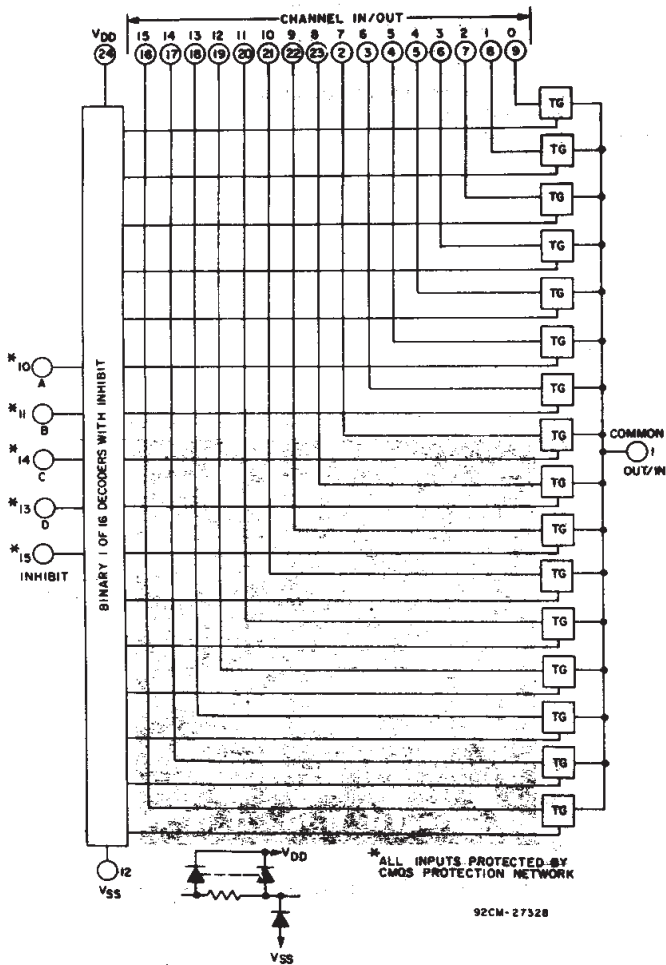


Fig. 16- CD4067 logic diagram.

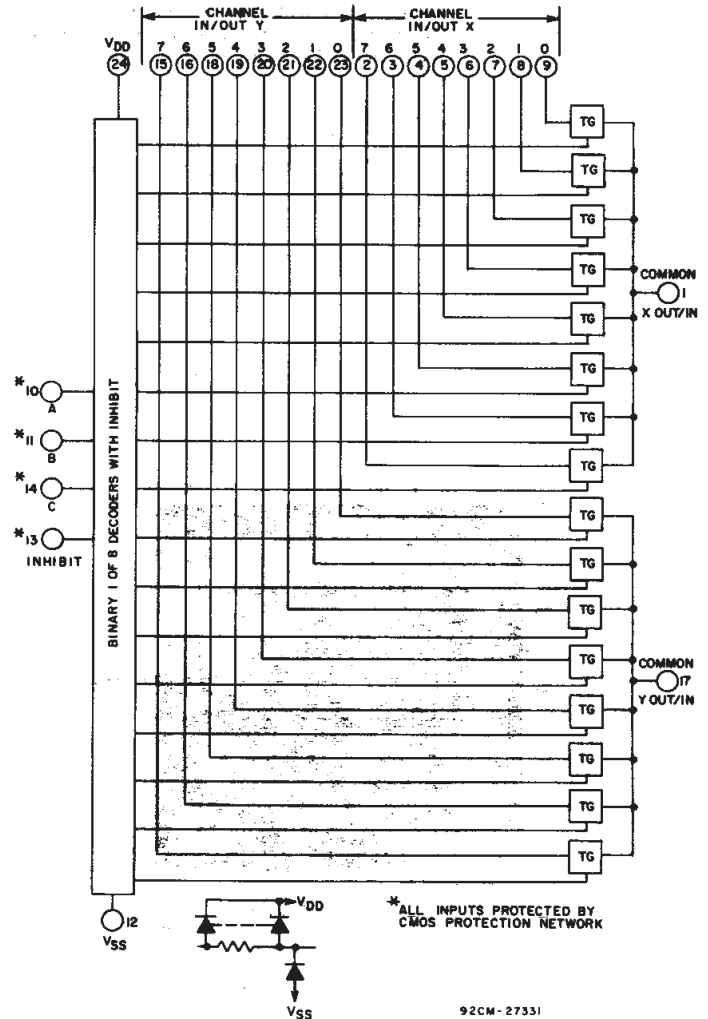


Fig. 17- CD4097 logic diagram.

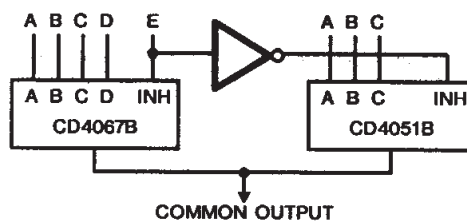


Fig. 18-24-to-1 MUX Addressing

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## CD4067B, CD4097B Types

### SPECIAL CONSIDERATIONS

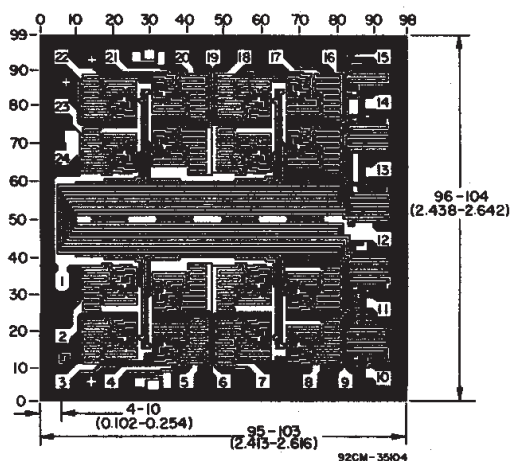
In applications where separate power sources are used to drive  $V_{DD}$  and the signal inputs, the  $V_{DD}$  current capability should exceed  $V_{DD}/R_L$  ( $R_L$ =effective external load). This provision avoids permanent current flow or clamp action on the  $V_{DD}$  supply when power is applied or removed from the CD4067B or CD4097B.

When switching from one address to another, some of the ON periods of the channels of the multiplexers will overlap momentarily, which may be objectionable in certain applications. Also when a channel is turned on or off by an address input, there is a momentary conductive path from the channel to  $V_{SS}$ , which will dump some charge from any capacitor connected to the input or output of the channel. The inhibit input turning on a channel will similarly dump some charge to  $V_{SS}$ .

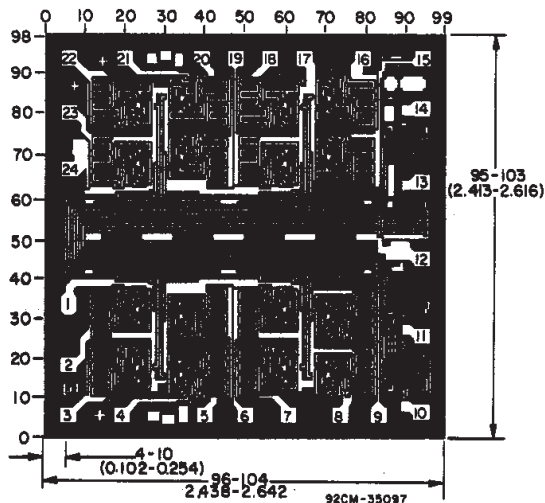
The amount of charge dumped is mostly a function of the signal level above  $V_{SS}$ . Typically, at  $V_{DD}-V_{SS}=10$  V, a 100-pF

capacitor connected to the input or output of the channel will lose 3-4% of its voltage at the moment the channel turns on or off. This loss of voltage is essentially independent of the address or inhibit signal transition time, if the transition time is less than 1-2  $\mu$ s. When the inhibit signal turns a channel off, there is no charge dumping to  $V_{SS}$ . Rather, there is a slight rise in the channel voltage level (65 mV typ.) due to capacitive coupling from inhibit input to channel input or output. Address inputs also couple some voltage steps onto the channel signal levels.

In certain applications, the external load-resistor current may include both  $V_{DD}$  and signal-line components. To avoid drawing  $V_{DD}$  current when switch current flows into the transmission gate inputs, the voltage drop across the bidirectional switch must not exceed 0.8 volt (calculated from  $R_{ON}$  values shown in ELECTRICAL CHARACTERISTICS CHART). No  $V_{DD}$  current will flow through  $R_L$  if the switch current flows into terminal 1 on the CD4067B, terminals 1 and 17 on the CD4097B.



Dimensions and pad layout for CD4067BH.



Dimensions and pad layout for CD4097BH.

Dimensions in parentheses are in millimeters and are derived from the basic inch dimensions as indicated. Grid graduations are in mils ( $10^{-3}$  inch).



**PACKAGING INFORMATION**

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
CD4067BF	ACTIVE	CDIP	J	24	1	Non-RoHS & Non-Green	Call TI	N / A for Pkg Type	-55 to 125	CD4067BF	<a href="#">Samples</a>
CD4067BF3A	ACTIVE	CDIP	J	24	1	Non-RoHS & Non-Green	Call TI	N / A for Pkg Type	-55 to 125	CD4067BF3A	<a href="#">Samples</a>
CD4067BM	ACTIVE	SOIC	DW	24	25	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-55 to 125	CD4067BM	<a href="#">Samples</a>
CD4067BM96	ACTIVE	SOIC	DW	24	2000	RoHS & Green	NIPDAU   SN	Level-1-260C-UNLIM	-55 to 125	CD4067BM	<a href="#">Samples</a>
CD4067BM96E4	ACTIVE	SOIC	DW	24	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-55 to 125	CD4067BM	<a href="#">Samples</a>
CD4067BM96G4	ACTIVE	SOIC	DW	24	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-55 to 125	CD4067BM	<a href="#">Samples</a>
CD4067BPW	ACTIVE	TSSOP	PW	24	60	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-55 to 125	CM067B	<a href="#">Samples</a>
CD4067BPWG4	ACTIVE	TSSOP	PW	24	60	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-55 to 125	CM067B	<a href="#">Samples</a>
CD4067BPWR	ACTIVE	TSSOP	PW	24	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-55 to 125	CM067B	<a href="#">Samples</a>
CD4097BF	ACTIVE	CDIP	J	24	1	Non-RoHS & Non-Green	Call TI	N / A for Pkg Type	-55 to 125	CD4097BF	<a href="#">Samples</a>
CD4097BM	ACTIVE	SOIC	DW	24	25	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-55 to 125	CD4097BM	<a href="#">Samples</a>
CD4097BME4	ACTIVE	SOIC	DW	24	25	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-55 to 125	CD4097BM	<a href="#">Samples</a>
CD4097BMG4	ACTIVE	SOIC	DW	24	25	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-55 to 125	CD4097BM	<a href="#">Samples</a>
CD4097BPW	ACTIVE	TSSOP	PW	24	60	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-55 to 125	CM097B	<a href="#">Samples</a>
CD4097BPWR	ACTIVE	TSSOP	PW	24	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-55 to 125	CM097B	<a href="#">Samples</a>
CD4097BPWRE4	ACTIVE	TSSOP	PW	24	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-55 to 125	CM097B	<a href="#">Samples</a>

(1) The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSELETE:** TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

**RoHS Exempt:** TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

**Green:** TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of  $\leq 1000$ ppm threshold. Antimony trioxide based flame retardants must also meet the  $\leq 1000$ ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "-" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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**OTHER QUALIFIED VERSIONS OF CD4067B, CD4067B-MIL, CD4097B, CD4097B-MIL :**

● Catalog : [CD4067B](#), [CD4097B](#)

● Military : [CD4067B-MIL](#), [CD4097B-MIL](#)

NOTE: Qualified Version Definitions:

● Catalog - TI's standard catalog product

● Military - QML certified for Military and Defense Applications



**TAPE AND REEL INFORMATION**

**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**


\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
CD4067BM96	SOIC	DW	24	2000	330.0	24.4	10.75	15.7	2.7	12.0	24.0	Q1
CD4067BM96G4	SOIC	DW	24	2000	330.0	24.4	10.75	15.7	2.7	12.0	24.0	Q1
CD4067BPWR	TSSOP	PW	24	2000	330.0	16.4	6.95	8.3	1.6	8.0	16.0	Q1
CD4097BPWR	TSSOP	PW	24	2000	330.0	16.4	6.95	8.3	1.6	8.0	16.0	Q1

**TAPE AND REEL BOX DIMENSIONS**


\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
CD4067BM96	SOIC	DW	24	2000	350.0	350.0	43.0
CD4067BM96G4	SOIC	DW	24	2000	350.0	350.0	43.0
CD4067BPWR	TSSOP	PW	24	2000	853.0	449.0	35.0
CD4097BPWR	TSSOP	PW	24	2000	853.0	449.0	35.0

**TUBE**

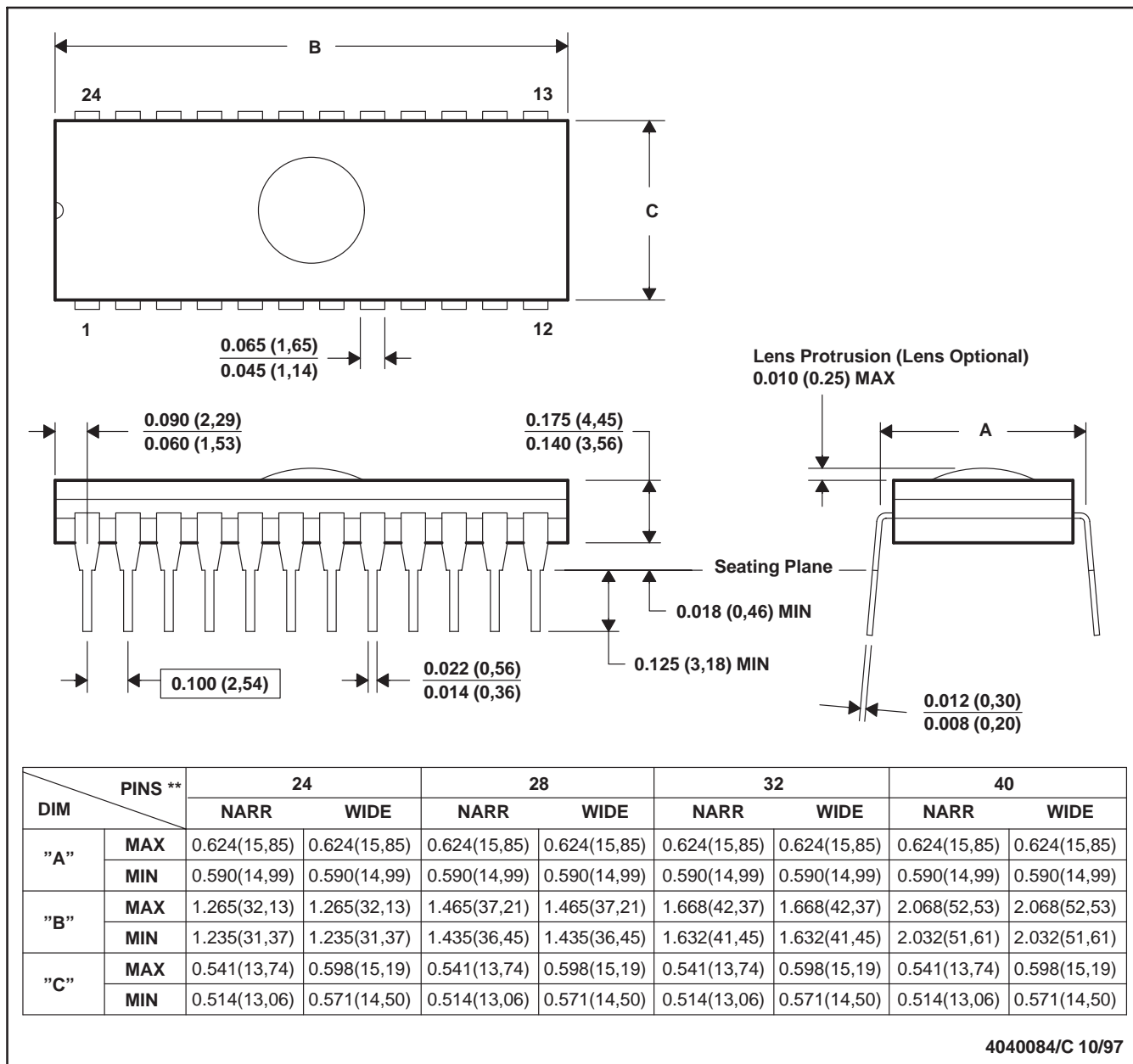

\*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (μm)	B (mm)
CD4067BM	DW	SOIC	24	25	506.98	12.7	4826	6.6
CD4067BPW	PW	TSSOP	24	60	530	10.2	3600	3.5
CD4067BPWG4	PW	TSSOP	24	60	530	10.2	3600	3.5
CD4097BM	DW	SOIC	24	25	506.98	12.7	4826	6.6
CD4097BME4	DW	SOIC	24	25	506.98	12.7	4826	6.6
CD4097BMG4	DW	SOIC	24	25	506.98	12.7	4826	6.6
CD4097BPW	PW	TSSOP	24	60	530	10.2	3600	3.5

J (R-GDIP-T\*\*)

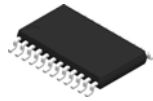
CERAMIC DUAL-IN-LINE PACKAGE

24 PINS SHOWN



- NOTES: A. All linear dimensions are in inches (millimeters).  
 B. This drawing is subject to change without notice.  
 C. Window (lens) added to this group of packages (24-, 28-, 32-, 40-pin).  
 D. This package can be hermetically sealed with a ceramic lid using glass frit.  
 E. Index point is provided on cap for terminal identification.

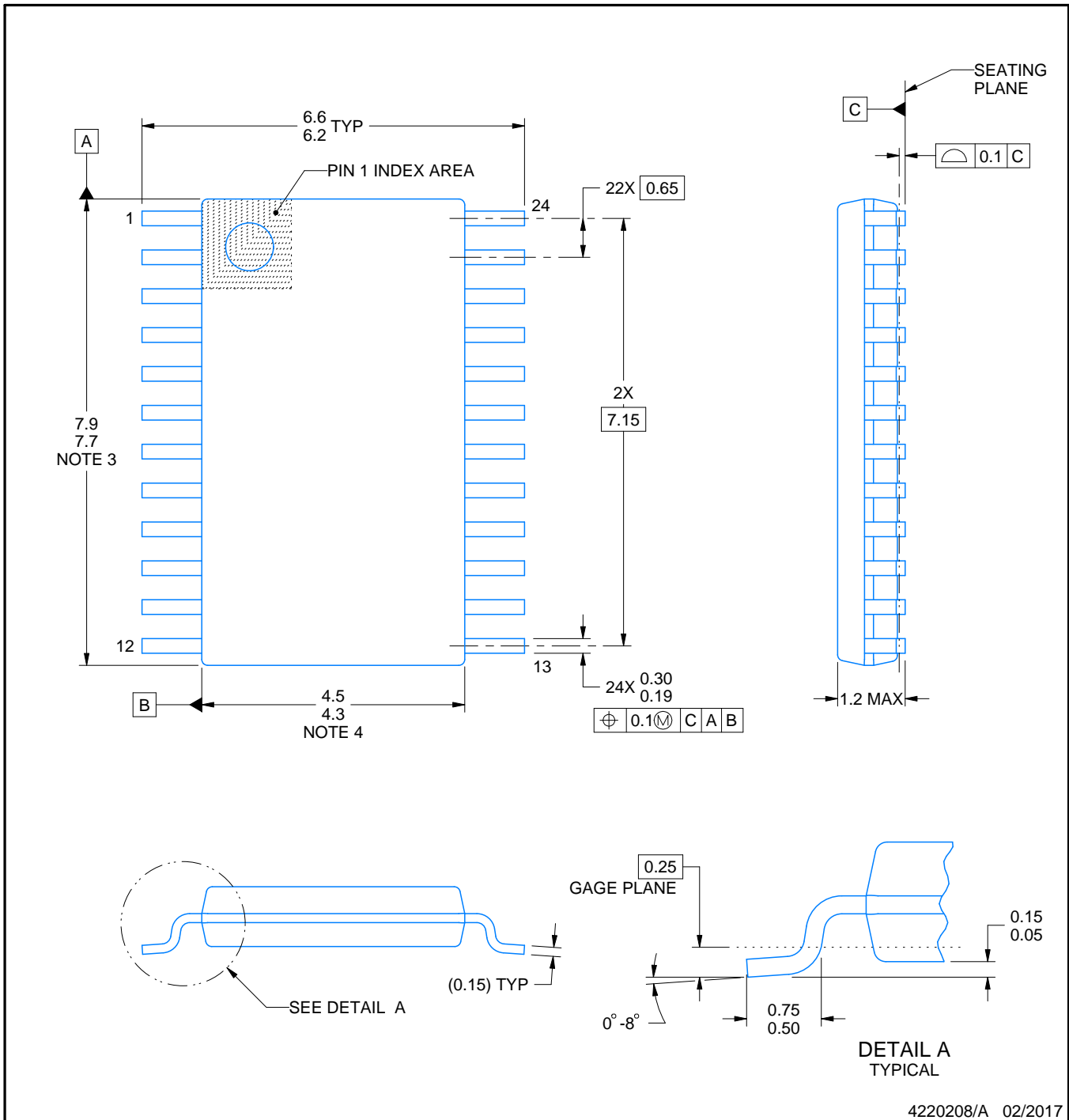
PW0024A



# PACKAGE OUTLINE

## TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



### NOTES:

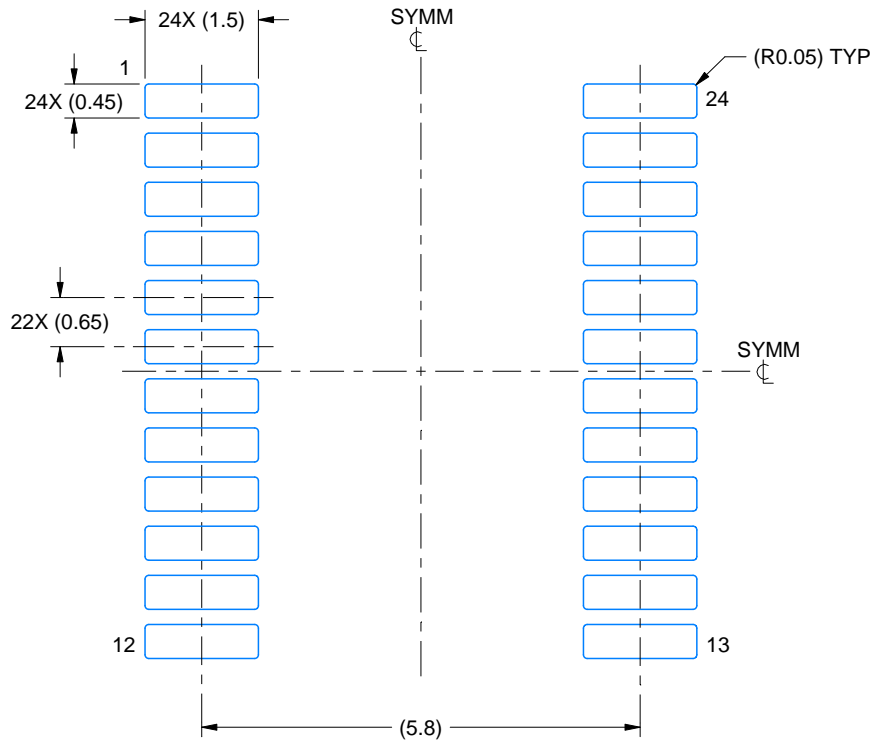
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153.

# EXAMPLE BOARD LAYOUT

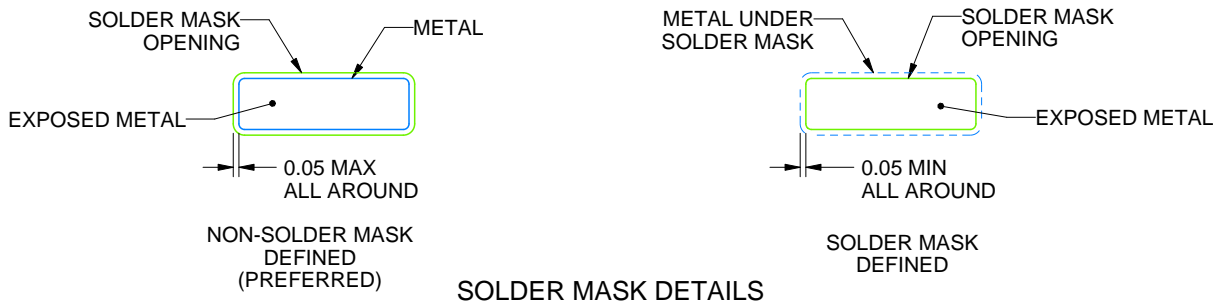
PW0024A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



LAND PATTERN EXAMPLE  
EXPOSED METAL SHOWN  
SCALE: 10X



SOLDER MASK DETAILS

4220208/A 02/2017

NOTES: (continued)

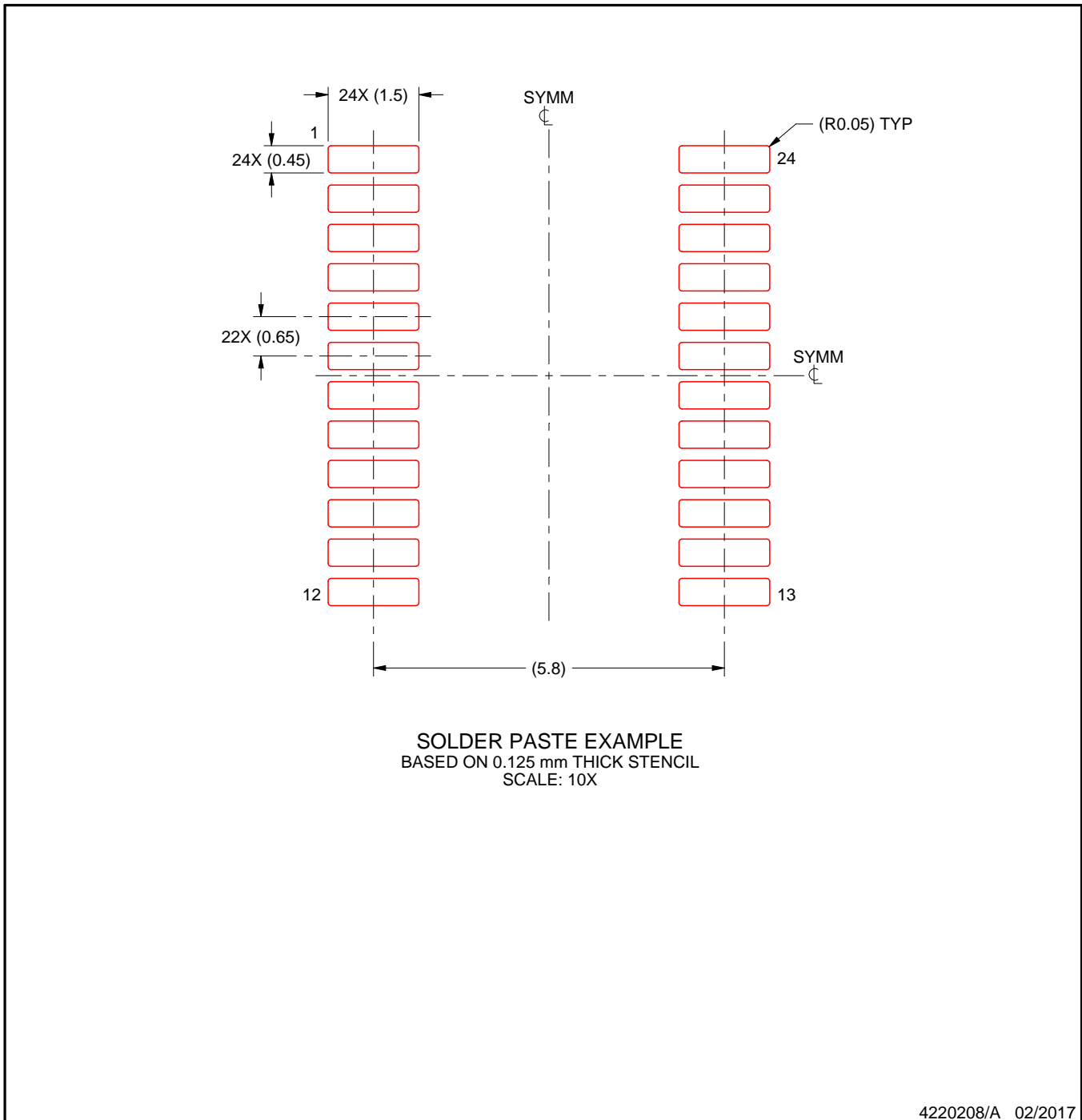
- 6. Publication IPC-7351 may have alternate designs.
- 7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

# EXAMPLE STENCIL DESIGN

PW0024A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



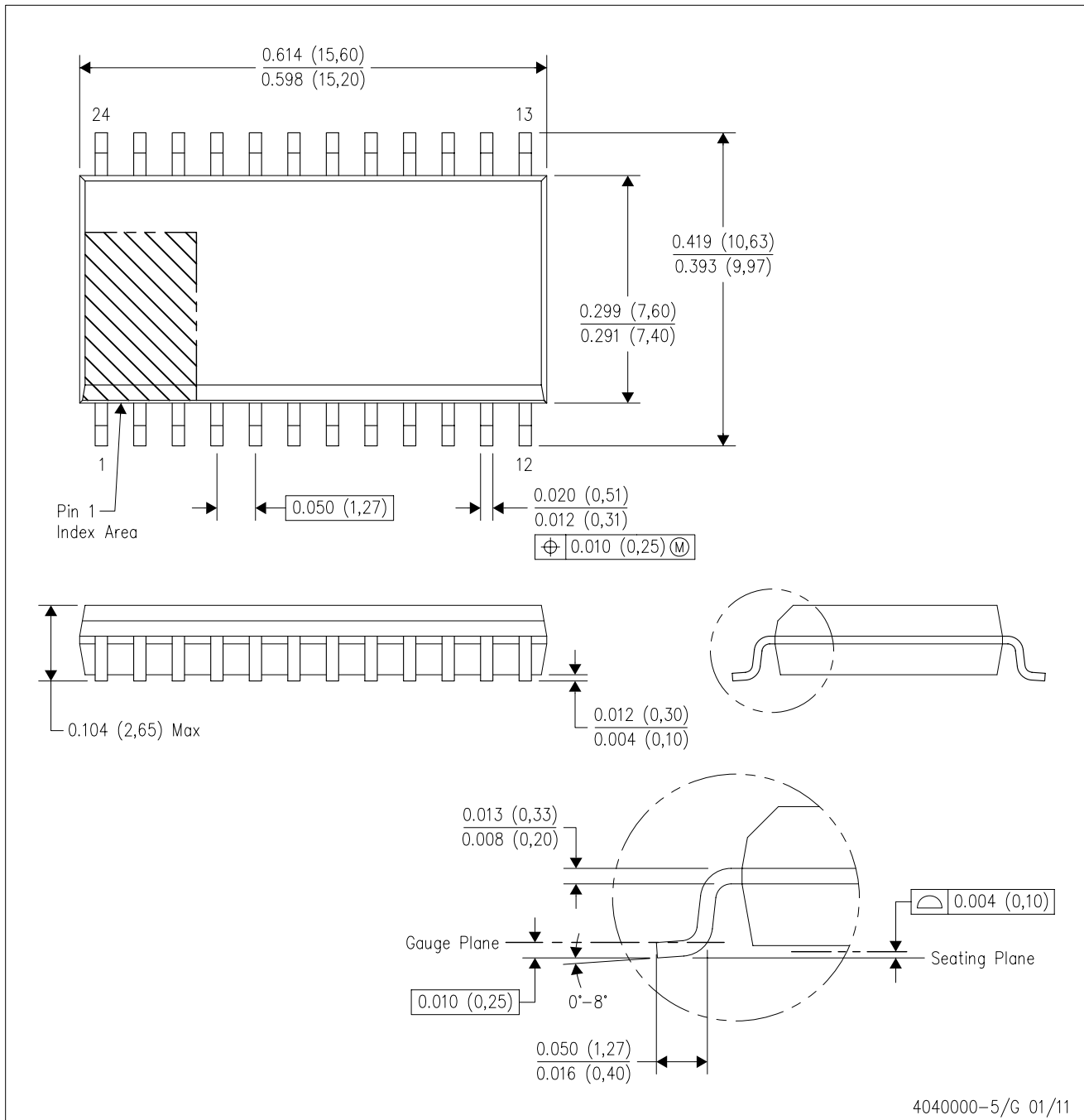
NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.



DW (R-PDSO-G24)

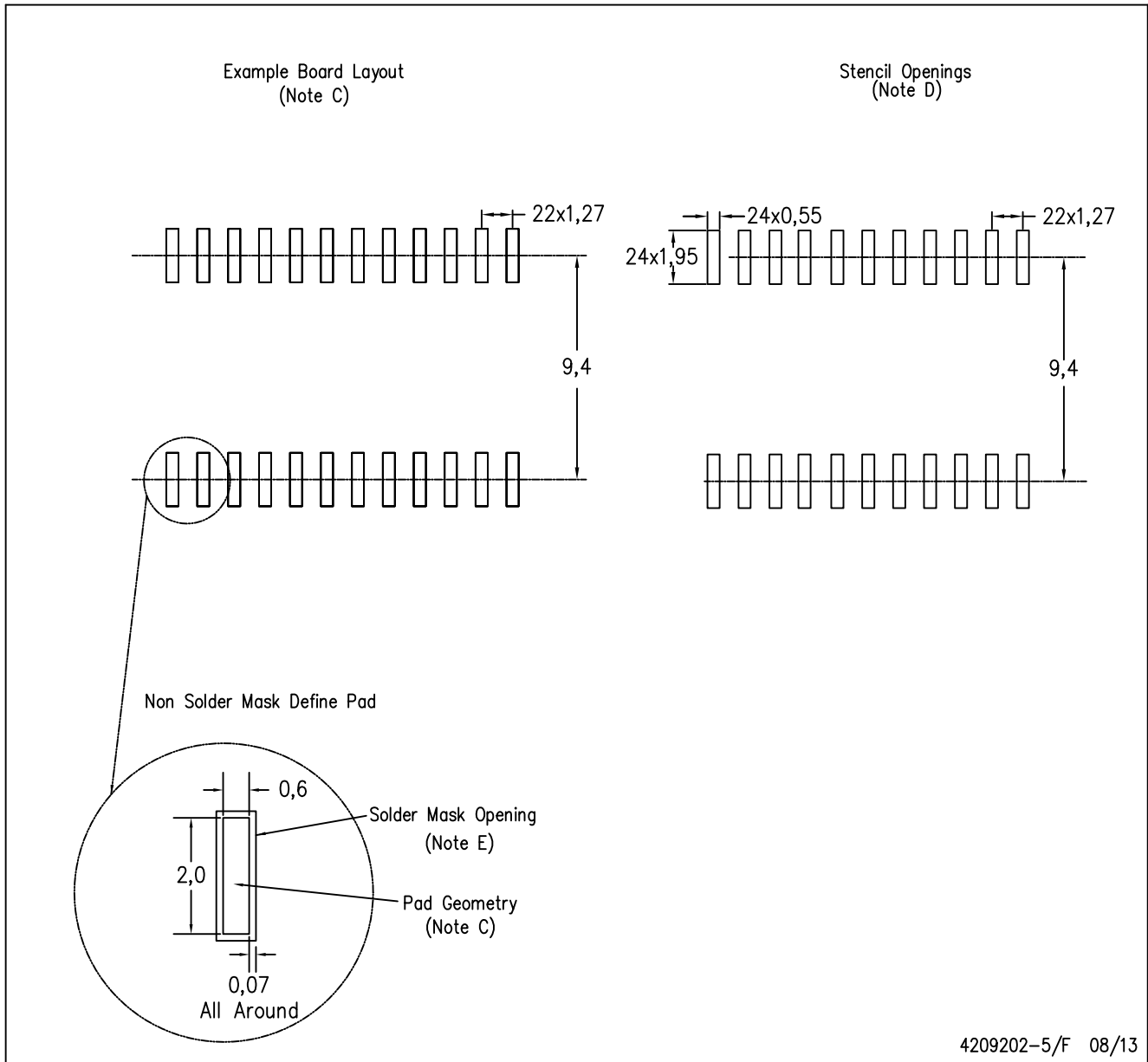
PLASTIC SMALL OUTLINE



- NOTES:
- All linear dimensions are in inches (millimeters). Dimensioning and tolerancing per ASME Y14.5M-1994.
  - This drawing is subject to change without notice.
  - Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).
  - Falls within JEDEC MS-013 variation AD.

DW (R-PDSO-G24)

PLASTIC SMALL OUTLINE



- NOTES:
- A. All linear dimensions are in millimeters.
  - B. This drawing is subject to change without notice.
  - C. Refer to IPC7351 for alternate board design.
  - D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525
  - E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

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