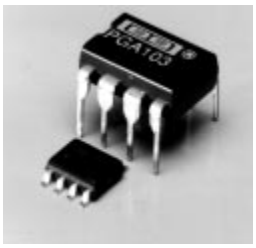
BURR - BROWN®



PGA103

Programmable Gain AMPLIFIER

FEATURES

- DIGITALLY PROGRAMABLE GAINS: G=1, 10, 100V/V
- CMOS/TTL-COMPATIBLE INPUTS
- LOW GAIN ERROR: ±0.05% max, G=10
- LOW OFFSET VOLTAGE DRIFT: 2μV/°C
- LOW QUIESCENT CURRENT: 2.6mA
- LOW COST
- 8-PIN PLASTIC DIP, SO-8 PACKAGES

APPLICATIONS

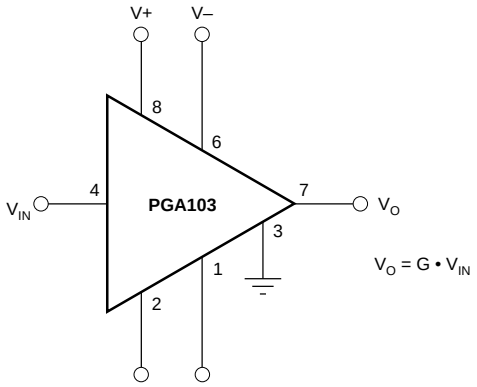
- DATA ACQUISITION SYSTEMS
- GENERAL PURPOSE ANALOG BOARDS
- MEDICAL INSTRUMENTATION

DESCRIPTION

The PGA103 is a programmable-gain amplifier for general purpose applications. Gains of 1, 10, or 100 are digitally selected by two CMOS/TTL-compatible inputs. The PGA103 is ideal for systems that must handle wide dynamic range signals.

The PGA103's high speed circuitry provides fast settling time, even at G=100 (8μs to 0.01%). Bandwidth is 250kHz at G=100, yet quiescent current is only 2.6mA. It operates from ±4.5V to ±18V power supplies.

The PGA103 is available in 8-pin plastic DIP and SO-8 surface-mount packages, specified for the –40°C to +85°C temperature range.



GAIN	A_1	A_0
1	0	0
10	0	1
100	1	0

International Airport Industrial Park • Mailing Address: PO Box 11400 • Tucson, AZ 85734 • Street Address: 6730 S. Tucson Blvd. • Tucson, AZ 85706
Tel: (520) 746-1111 • Twx: 910-952-1111 • Cable: BBRCORP • Telex: 066-6491 • FAX: (520) 889-1510 • Immediate Product Info: (800) 548-6132

©1993 Burr-Brown Corporation
PDS-1208B
Printed in U.S.A. November, 1993

SBOS031

SPECIFICATIONS

ELECTRICAL

T_A = +25°C, V_S = ±15V, R_L = 2kΩ unless otherwise specified.

PARAMETER	CONDITIONS	PGA103P, U			UNITS
		MIN	TYP	MAX	
INPUT					
Offset Voltage, RTI					
G = 1	T_A = +25°C		±200	±1500	µV
G = 10			±100	±500	µV
G = 100			±100	±500	µV
vs Temperature	$T_A = T_{MIN}$ to T_{MAX}				
G = 1			±5		µV/°C
G = 10			±2		µV/°C
G = 100			±2		µV/°C
vs Power Supply	V_S = ±4.5V to ±18V				
G = 1			30	70	µV/V
G = 10			10	35	µV/V
G = 100			10	35	µV/V
Impedance			10^8 || 2		Ω || pF
INPUT BIAS CURRENT					
Initial Bias Current			±50	±150	nA
vs Temperature			±100		pA/°C
NOISE VOLTAGE, RTI	G = 100, R_S = 0Ω				
f = 10Hz			16		nV/√Hz
f = 100Hz			11		nV/√Hz
f = 1kHz			11		nV/√Hz
f_B = 0.1Hz to 10Hz			0.6		µVp-p
NOISE CURRENT					
f = 10Hz			2.8		pA/√Hz
f = 1kHz			0.3		pA/√Hz
f_B = 0.1Hz to 10Hz			76		pAp-p
GAIN					
Gain Error					
G = 1			±0.005	±0.02	%
G = 10			±0.02	±0.05	%
G = 100			±0.04	±0.2	%
Gain vs Temperature					
G = 1			±2		ppm/°C
G = 10			±10		ppm/°C
G = 100			±30		ppm/°C
Nonlinearity					
G = 1			±0.001	±0.003	% of FSR
G = 10			±0.002	±0.005	% of FSR
G = 100			±0.004	±0.01	% of FSR
OUTPUT					
Voltage, Positive		(V+) –3.5	(V+) –2.5		V
Negative		(V–) +3.5	(V–) +2.5		V
Load Capacitance, max			1000		pF
Short-Circuit Current			±25		mA
FREQUENCY RESPONSE					
Bandwidth, –3dB					
G = 1			1.5		MHz
G = 10			750		kHz
G = 100			250		kHz
Slew Rate	V_O = ±10V		9		V/µs
Settling Time, 0.1%					
G = 1			2		µs
G = 10			2.2		µs
G = 100			6.5		µs
Settling Time, 0.01%					
G = 1			2.5		µs
G = 10			2.5		µs
G = 100			8		µs
Overload Recovery	50% Overdrive		2.5		µs
DIGITAL LOGIC INPUTS					
Digital Low Voltage		–5.6		0.8	V
Digital Low or High Current			1		µA
Digital High Voltage		2		V+	V

SPECIFICATIONS (CONT)

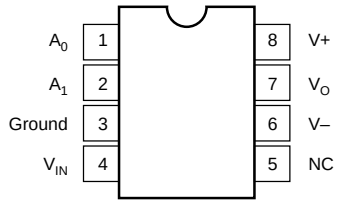
ELECTRICAL

T_A = +25°C, V_S = ±15V, R_L = 2kΩ unless otherwise specified.

PARAMETER	CONDITIONS	PGA103P, U			UNITS
		MIN	TYP	MAX	
POWER SUPPLY					
Voltage Range		±4.5	±15	±18	V
Current	V_{IN} = 0V		±2.6	±3.5	mA
TEMPERATURE RANGE					
Specification		–40		+85	°C
Operating		–40		+125	°C
θ_{JA}: P or U Package			100		°C/W

PIN CONFIGURATION

Top View **DIP/SO-8**



ORDERING INFORMATION

MODEL	PACKAGE	TEMPERATURE RANGE
PGA103P	8-Pin Plastic DIP	–40°C to +85°C
PGA103U	SO-8 Surface-Mount	–40°C to +85°C

ELECTROSTATIC DISCHARGE SENSITIVITY

Any integrated circuit can be damaged by ESD. Burr-Brown recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet published specifications.

ABSOLUTE MAXIMUM RATINGS

Supply Voltage	±18V
Analog Input Voltage Range	V– to V+
Logic Input Voltage Range	V– to V+
Output Short Circuit (to ground)	Continuous
Operating Temperature	–40°C to +125°C
Storage Temperature	–40°C to +125°C
Junction Temperature	+150°C
Lead Temperature (soldering,10s)	+300°C

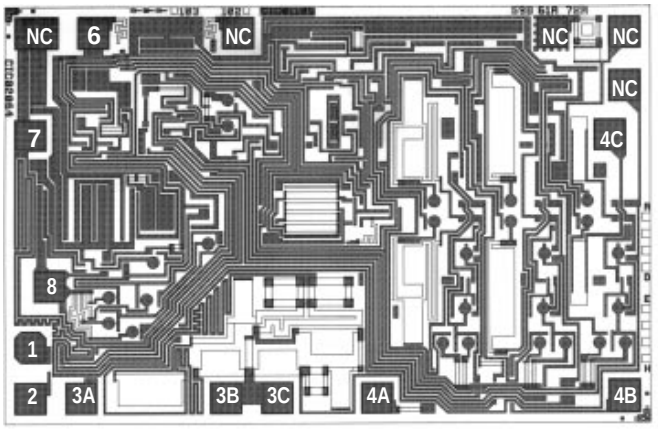
PACKAGE INFORMATION

MODEL	PACKAGE	PACKAGE DRAWING NUMBER(1)
PGA103P	8-Pin Plastic DIP	006
PGA103U	SO-8 Surface-Mount	182

NOTE: (1) For detailed drawing and dimension table, please see end of data sheet, or Appendix D of Burr-Brown IC Data Book.

The information provided herein is believed to be reliable; however, BURR-BROWN assumes no responsibility for inaccuracies or omissions. BURR-BROWN assumes no responsibility for the use of this information, and all use of such information shall be entirely at the user's own risk. Prices and specifications are subject to change without notice. No patent rights or licenses to any of the circuits described herein are implied or granted to any third party. BURR-BROWN does not authorize or warrant any BURR-BROWN product for use in life support devices and/or systems.

DICE INFORMATION



PGA103 DIE TOPOGRAPHY

PAD	FUNCTION
1	A_0
2	A_1
3A, 3B, 3C(1)	Ground
4A, 4B, 4C(2)	V_{IN}
6	V–
7	V_O
8	V+

NC: No Connection
NOTES: (1) Connect all three indicated pads. (2) Connect all three indicated pads.
Substrate Bias: Internally connected to V– power supply.

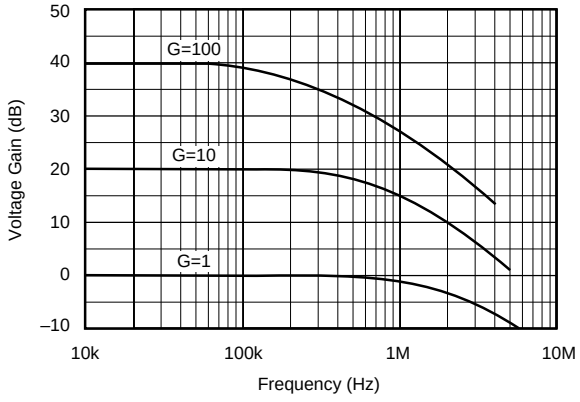
MECHANICAL INFORMATION

	MILS (0.001")	MILLIMETERS
Die Size	69 x 105 ±5	1.75 x 2.67 ±0.13
Die Thickness	20 ±3	0.51 ±0.08
Min. Pad Size	4 x 4	0.1 x 0.1
Backing		Gold

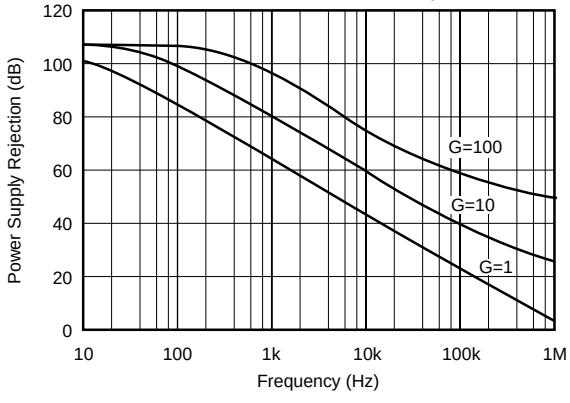
TYPICAL PERFORMANCE CURVES

T_A = +25°C, V_S = ±15V unless otherwise noted.

VOLTAGE GAIN vs FREQUENCY



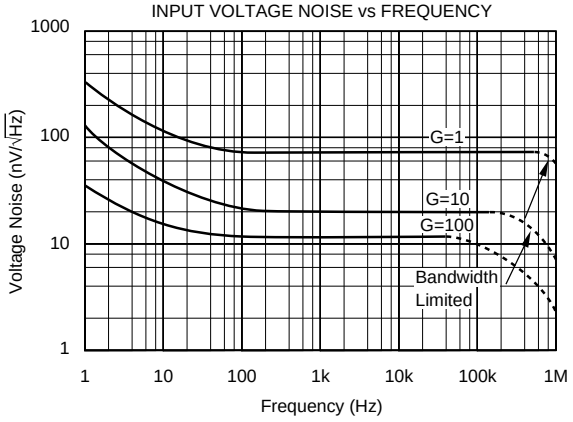
POWER SUPPLY REJECTION vs FREQUENCY



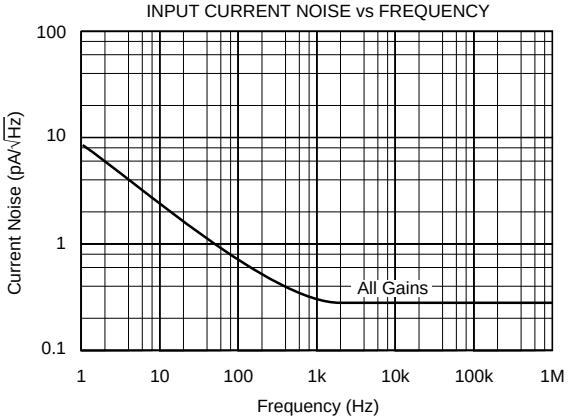
TYPICAL PERFORMANCE CURVES (CONT)

T_A = +25°C, V_S = ±15V unless otherwise noted.

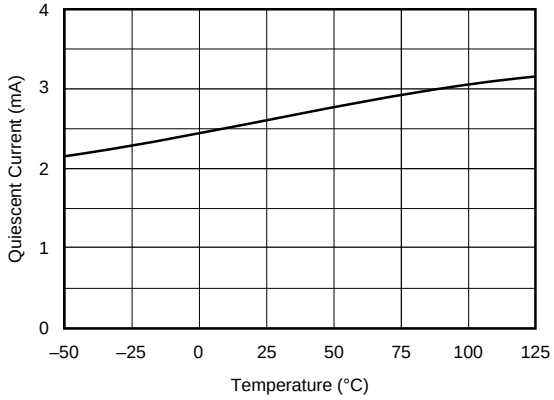
INPUT VOLTAGE NOISE vs FREQUENCY



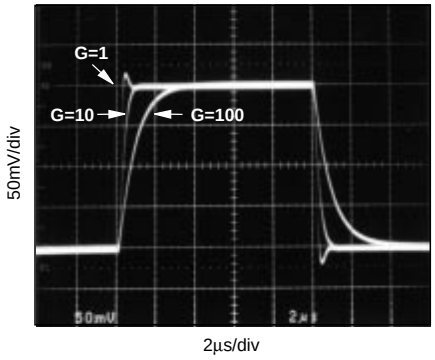
INPUT CURRENT NOISE vs FREQUENCY



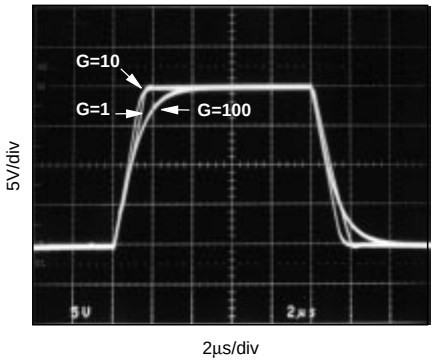
QUIESCENT CURRENT vs TEMPERATURE



SMALL SIGNAL RESPONSE

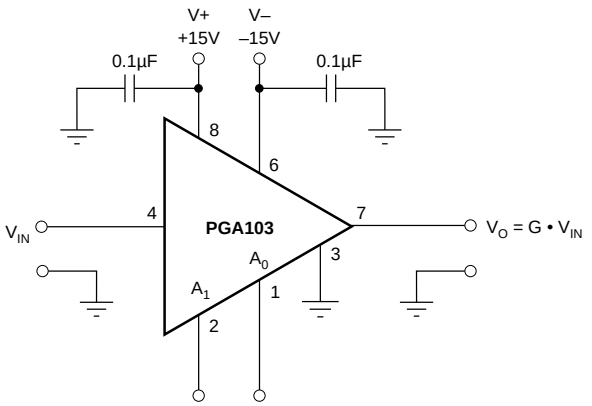


LARGE SIGNAL RESPONSE



APPLICATION INFORMATION

Figure 1 shows the basic connections required for operation of the PGA103. Applications with noisy or high impedance power supplies may require decoupling capacitors close to the device pins as shown.



GAIN	A_1	A_0
1	0	0
10	0	1
100	1	0
Not Valid	1	1

Logic 0: (–5.6) ≤ V ≤ 0.8V
Logic 1: 2V ≤ V ≤ (V+)
Logic voltages referred to pin 3.

NOTE: (1) Low impedance ground connection required for good gain accuracy—see text.

FIGURE 1. Basic Connections.

The input and output are referred to the ground terminal, pin 3. This must be a low-impedance connection to assure good gain accuracy. A resistance of 0.1Ω in series with the ground pin will cause the gain in G=100 to decrease by approximately 0.2%.

DIGITAL INPUTS

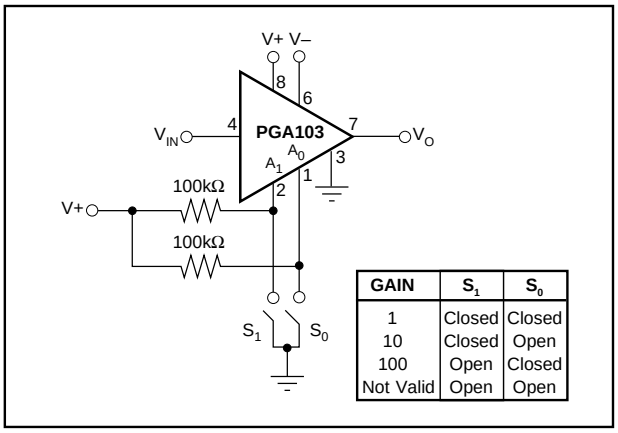
The digital inputs, A_0 and A_1, select the gain according to the logic table in Figure 1. The digital inputs interface directly to common CMOS and TTL logic components. The logic inputs are referenced to the ground terminal, pin 3.

The logic table in Figure 1 shows that logic "1" on both A_0 and A_1 is invalid. This logic code will not cause damage, but the amplifier output will not be predictable while this code is selected. The output will recover when a valid code is selected.

The digital inputs are not latched, so a change in logic inputs immediately selects a new gain. Switching time of the logic is approximately 0.5µs. The time to respond to gain change is equal to the switching time plus the time it takes the amplifier to settle to a new output voltage in the newly selected gain (see settling time specifications).

Many applications use an external logic latch to access gain control signals from a high speed data bus. Using an external latch isolates the high speed digital bus from sensitive analog circuitry. Locate the latch circuitry as far as practical from analog circuitry to avoid coupling digital noise into the analog circuitry.

Some applications select gain of the PGA103 with switches or jumpers. Figure 2 shows pull-up resistors connected to assure a noise-free logic "1" when the switch or jumper is off or open. Fixed-gain applications can connect the logic inputs directly to V+ or ground (or other valid logic level) without a series resistor.

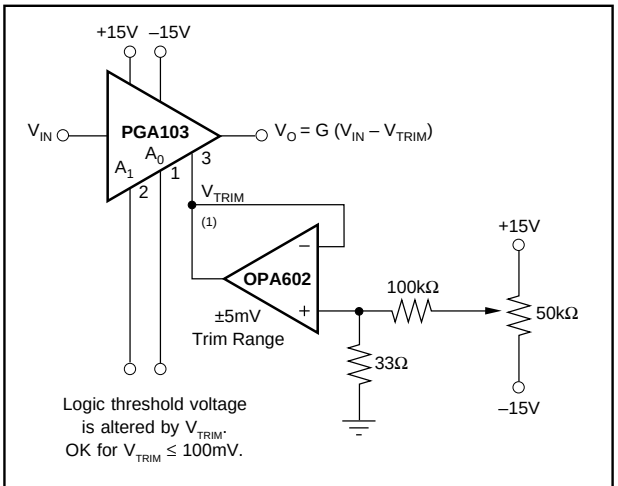


GAIN	S_1	S_0
1	Closed	Closed
10	Closed	Open
100	Open	Closed
Not Valid	Open	Open

FIGURE 2. Switch or Jumper-Selected Gains.

OFFSET TRIMMING

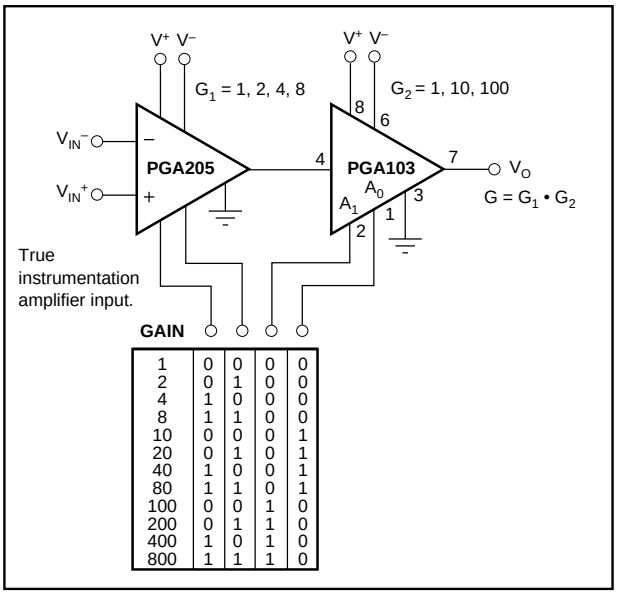
Offset voltage is laser-trimmed to typically less than 200µV (referred to input) in all three gains. The input-referred offset voltage can be different for each gain.



NOTE: (1) Op amp buffer is required to preserve good gain accuracy—see text.

FIGURE 3. Offset Voltage Trim Circuit.

Figure 3 shows a circuit used to trim the offset voltage of the PGA103. An op amp buffers the trim voltage to provide a low impedance at the ground terminal. This is required to maintain accurate gain. Remember that the logic inputs, A_0 and A_1, are referenced to this ground connection, so the logic threshold voltage will be affected by the trim voltage. This is insignificant if the offset adjustment is used only to trim offset voltage. If a large offset is used (greater than 0.1V), be sure that the logic input signals provide valid logic levels when referred to the voltage at the ground terminal, pin 3.



1	0	0	0	0
2	0	1	0	0
4	1	0	0	0
8	1	1	0	0
10	0	0	0	1
20	0	1	0	1
40	1	0	0	1
80	1	1	0	1
100	0	0	1	0
200	0	1	1	0
400	1	0	1	0
800	1	1	1	0

FIGURE 4. Programmable Gain Instrumentation Amplifier.

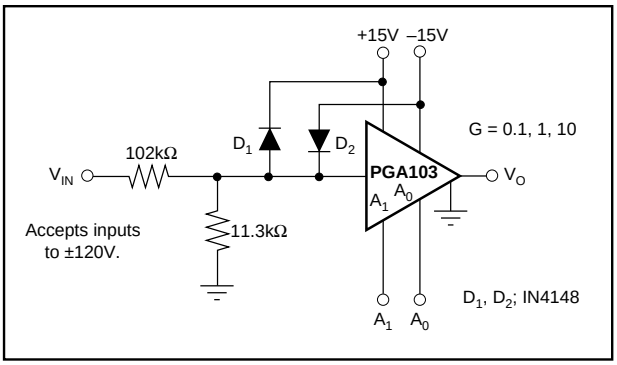


FIGURE 5. Wide Input Voltage Range Amplifer.

MODEL	CHARACTERISTICS
INA103	Low Noise, 1nV/√Hz IA
INA105	G = 1 Difference Amp
INA106	G = 10 Difference Amp
INA114	Resistor-Programmed Gain, Precision
INA117	±200V C-M Input Range Difference Amp
INA111	FET Input, High Speed IA
INA131	Precision, G = 100 IA

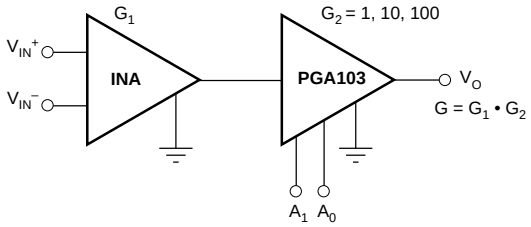


FIGURE 6. Instrumentation Amplifier with Programmable Gain Output Amp.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
PGA103U	ACTIVE	SOIC	D	8	75	RoHS & Green	NIPDAU-DCC	Level-3-260C-168 HR	-40 to 85	PGA 103U	Samples
PGA103UE4	ACTIVE	SOIC	D	8	75	RoHS & Green	NIPDAU-DCC	Level-3-260C-168 HR	-40 to 85	PGA 103U	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

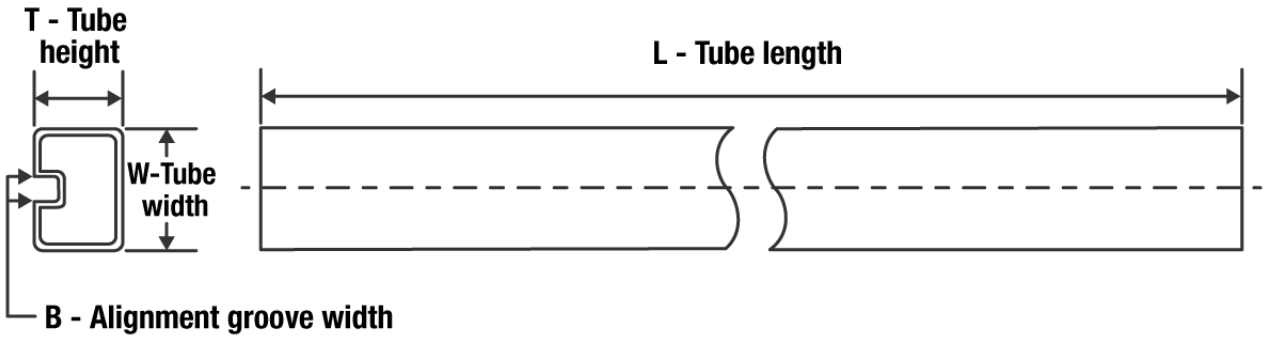
(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TUBE



*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
PGA103U	D	SOIC	8	75	506.6	8	3940	4.32
PGA103UE4	D	SOIC	8	75	506.6	8	3940	4.32

IMPORTANT NOTICE AND DISCLAIMER

TI PROVIDES TECHNICAL AND RELIABILITY DATA (INCLUDING DATA SHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES “AS IS” AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS AND IMPLIED, INCLUDING WITHOUT LIMITATION ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE OR NON-INFRINGEMENT OF THIRD PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for skilled developers designing with TI products. You are solely responsible for (1) selecting the appropriate TI products for your application, (2) designing, validating and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, regulatory or other requirements.

These resources are subject to change without notice. TI grants you permission to use these resources only for development of an application that uses the TI products described in the resource. Other reproduction and display of these resources is prohibited. No license is granted to any other TI intellectual property right or to any third party intellectual property right. TI disclaims responsibility for, and you will fully indemnify TI and its representatives against, any claims, damages, costs, losses, and liabilities arising out of your use of these resources.

TI’s products are provided subject to TI’s Terms of Sale or other applicable terms available either on ti.com or provided in conjunction with such TI products. TI’s provision of these resources does not expand or otherwise alter TI’s applicable warranties or warranty disclaimers for TI products.

TI objects to and rejects any additional or different terms you may have proposed.

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265
Copyright © 2022, Texas Instruments Incorporated