

## N-channel 600 V, 0.150 $\Omega$ typ., 20 A MDmesh™ M2 EP Power MOSFET in TO-220FP package

Datasheet - production data

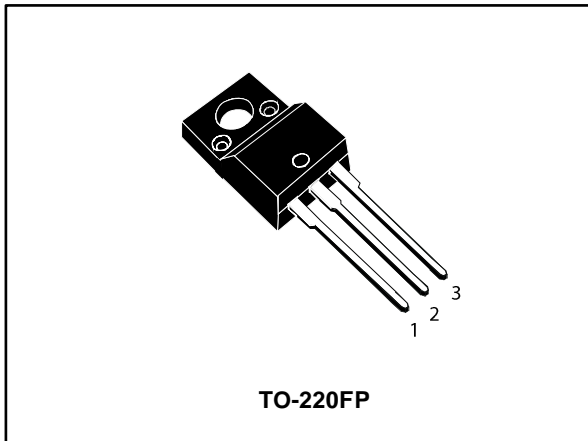
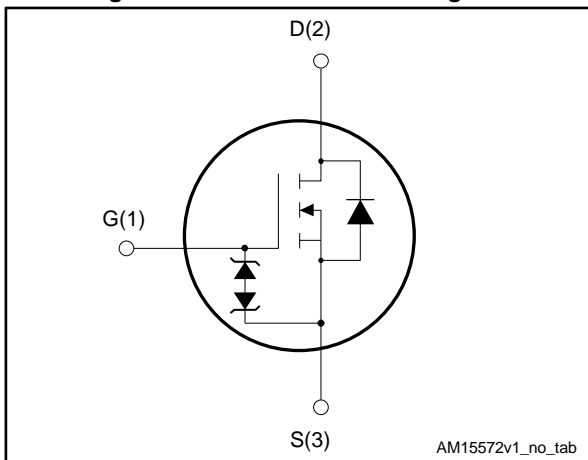


Figure 1: Internal schematic diagram



### Features

Order code	V <sub>DS</sub>	R <sub>DS(on)</sub> max	I <sub>D</sub>
STF27N60M2-EP	600 V	0.163 $\Omega$	20 A

- Extremely low gate charge
- Excellent output capacitance (C<sub>OSS</sub>) profile
- Very low turn-off switching losses
- 100% avalanche tested
- Zener-protected

### Applications

- Switching applications
- Tailored for very high frequency converters (f > 150 kHz)

### Description

These devices are N-channel Power MOSFETs developed using MDmesh™ M2 EP enhanced performance technology. Thanks to their strip layout and an improved vertical structure, these devices exhibit low on-resistance, optimized switching characteristics with very low turn-off switching losses, rendering them suitable for the most demanding very high frequency converters.

Table 1: Device summary

Order code	Marking	Package	Packing
STF27N60M2-EP	27N60M2EP	TO-220FP	Tube

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## Contents

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# 1 Electrical ratings

Table 2: Absolute maximum ratings

Symbol	Parameter	Value	Unit
$V_{GS}$	Gate-source voltage	$\pm 25$	V
$I_D^{(1)}$	Drain current (continuous) at $T_C = 25\text{ }^\circ\text{C}$	20	A
$I_D^{(1)}$	Drain current (continuous) at $T_C = 100\text{ }^\circ\text{C}$	13	A
$I_{DM}^{(2)}$	Drain current (pulsed)	80	A
$P_{TOT}$	Total dissipation at $T_C = 25\text{ }^\circ\text{C}$	30	W
$dv/dt^{(3)}$	Peak diode recovery voltage slope	15	V/ns
$dv/dt^{(4)}$	MOSFET $dv/dt$ ruggedness	50	V/ns
$V_{ISO}$	Insulation withstand voltage (RMS) from all three leads to external heat sink ( $t = 1\text{ s}$ ; $T_C = 25\text{ }^\circ\text{C}$ )	2.5	kV
$T_{stg}$	Storage temperature	- 55 to 150	$^\circ\text{C}$
$T_j$	Operating junction temperature		

**Notes:**

<sup>(1)</sup>Limited by maximum junction temperature

<sup>(2)</sup>Pulse width limited by safe operating area.

<sup>(3)</sup> $I_{SD} \leq 20\text{ A}$ ,  $di/dt \leq 400\text{ A}/\mu\text{s}$ ;  $V_{DS(\text{peak})} < V_{(BR)DSS}$ ,  $V_{DD} = 400\text{ V}$ .

<sup>(4)</sup> $V_{DS} \leq 480\text{ V}$

Table 3: Thermal data

Symbol	Parameter	Value	Unit
$R_{thj\text{-case}}$	Thermal resistance junction-case max	4.2	$^\circ\text{C}/\text{W}$
$R_{thj\text{-amb}}$	Thermal resistance junction-ambient max	62.5	$^\circ\text{C}/\text{W}$

Table 4: Avalanche characteristics

Symbol	Parameter	Value	Unit
$I_{AR}$	Avalanche current, repetetive or not repetetive (pulse width limited by $T_{j\text{max}}$ )	3.6	A
$E_{AS}$	Single pulse avalanche energy (starting $T_j = 25\text{ }^\circ\text{C}$ , $I_D = I_{AR}$ ; $V_{DD} = 50\text{ V}$ )	260	mJ

## 2 Electrical characteristics

$T_C = 25\text{ °C}$  unless otherwise specified

**Table 5: On/off states**

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{(BR)DSS}$	Drain-source breakdown voltage	$V_{GS} = 0\text{ V}$ , $I_D = 1\text{ mA}$	600			V
$I_{DSS}$	Zero gate voltage drain current	$V_{GS} = 0\text{ V}$ , $V_{DS} = 600\text{ V}$			1	$\mu\text{A}$
		$V_{GS} = 0\text{ V}$ , $V_{DS} = 600\text{ V}$ , $T_C = 125\text{ °C}$			100	$\mu\text{A}$
$I_{GSS}$	Gate-body leakage current	$V_{DS} = 0\text{ V}$ , $V_{GS} = \pm 25\text{ V}$			$\pm 10$	$\mu\text{A}$
$V_{GS(th)}$	Gate threshold voltage	$V_{DS} = V_{GS}$ , $I_D = 250\text{ }\mu\text{A}$	2	3	4	V
$R_{DS(on)}$	Static drain-source on-resistance	$V_{GS} = 10\text{ V}$ , $I_D = 10\text{ A}$		0.150	0.163	$\Omega$

**Table 6: Dynamic**

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$C_{iss}$	Input capacitance	$V_{DS} = 100\text{ V}$ , $f = 1\text{ MHz}$ , $V_{GS} = 0\text{ V}$	-	1320	-	pF
$C_{oss}$	Output capacitance		-	70	-	pF
$C_{rss}$	Reverse transfer capacitance		-	1	-	pF
$C_{oss\text{ eq.}}^{(1)}$	Equivalent output capacitance	$V_{DS} = 0\text{ to }480\text{ V}$ , $V_{GS} = 0\text{ V}$	-	146	-	pF
$R_G$	Intrinsic gate resistance	$f = 1\text{ MHz}$ , $I_D = 0\text{ A}$	-	4	-	$\Omega$
$Q_g$	Total gate charge	$V_{DD} = 480\text{ V}$ , $I_D = 20\text{ A}$ , $V_{GS} = 10\text{ V}$ (see <a href="#">Figure 15: "Test circuit for gate charge behavior"</a> )	-	33	-	nC
$Q_{gs}$	Gate-source charge		-	5.2	-	nC
$Q_{gd}$	Gate-drain charge		-	16	-	nC

**Notes:**

<sup>(1)</sup> $C_{oss\text{ eq.}}$  is defined as a constant equivalent capacitance giving the same charging time as  $C_{oss}$  when  $V_{DS}$  increases from 0 to 80%  $V_{DSS}$

**Table 7: Switching times**

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$t_{d(on)}$	Turn-on delay time	$V_{DD} = 300\text{ V}$ , $I_D = 10\text{ A}$ , $R_G = 4.7\text{ }\Omega$ , $V_{GS} = 10\text{ V}$ (see <a href="#">Figure 14: "Test circuit for resistive load switching times"</a> and <a href="#">Figure 19: "Switching time waveform"</a> )	-	13.4	-	ns
$t_r$	Rise time		-	8.1	-	ns
$t_{d(off)}$	Turn-off-delay time		-	55.6	-	ns
$t_f$	Fall time		-	6.3	-	ns

Table 8: Source-drain diode

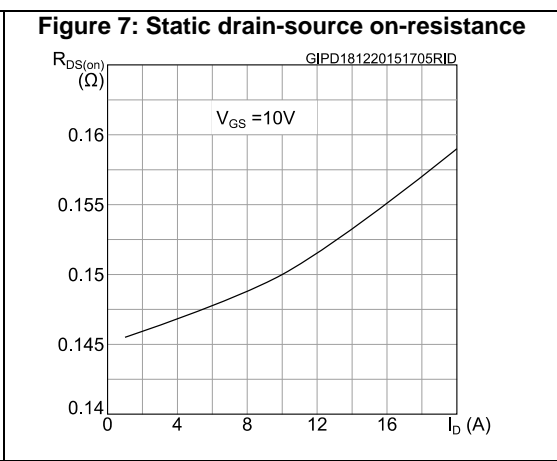
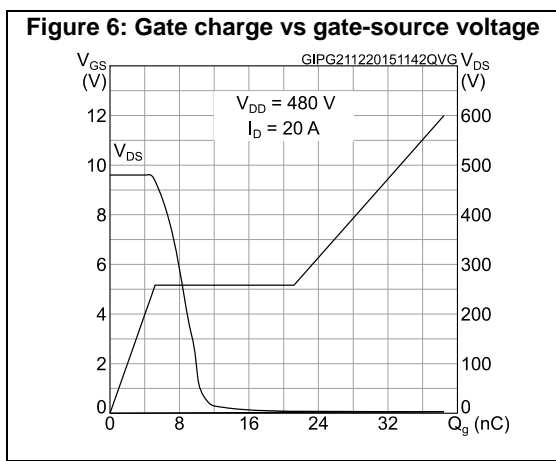
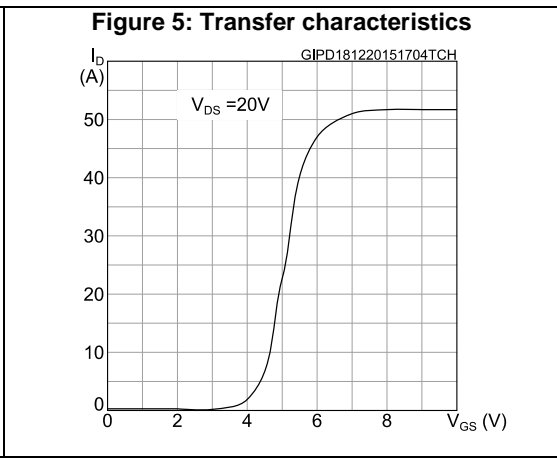
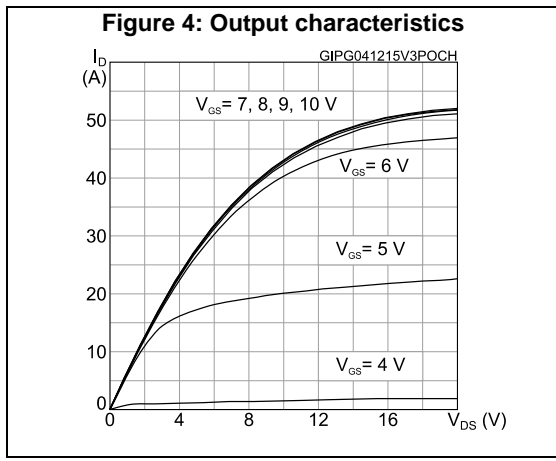
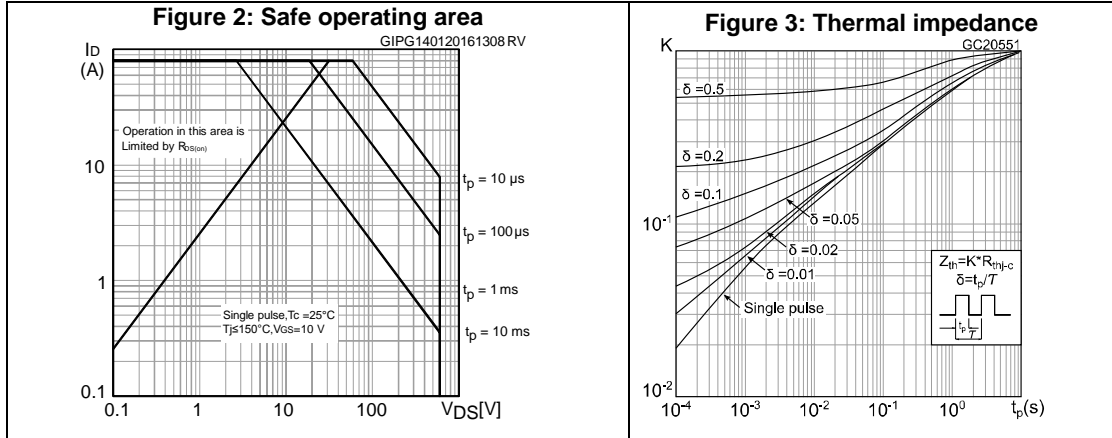
Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$I_{SD}$	Source-drain current		-		20	A
$I_{SDM}^{(1)}$	Source-drain current (pulsed)		-		80	A
$V_{SD}^{(2)}$	Forward on voltage	$V_{GS} = 0\text{ V}$ , $I_{SD} = 20\text{ A}$	-		1.6	V
$t_{rr}$	Reverse recovery time	$I_{SD} = 20\text{ A}$ , $di/dt = 100\text{ A}/\mu\text{s}$ , $V_{DD} = 60\text{ V}$ (see <a href="#">Figure 19: "Switching time waveform"</a> )	-	271		ns
$Q_{rr}$	Reverse recovery charge		-	3.44		$\mu\text{C}$
$I_{RRM}$	Reverse recovery current		-	25.4		A
$t_{rr}$	Reverse recovery time	$I_{SD} = 20\text{ A}$ , $di/dt = 100\text{ A}/\mu\text{s}$ , $V_{DD} = 60\text{ V}$ , $T_j = 150\text{ }^\circ\text{C}$ (see <a href="#">Figure 19: "Switching time waveform"</a> )	-	352		ns
$Q_{rr}$	Reverse recovery charge		-	4.82		$\mu\text{C}$
$I_{RRM}$	Reverse recovery current		-	27.4		A

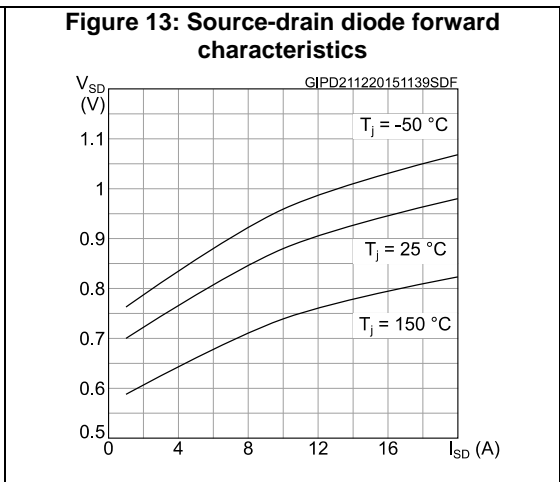
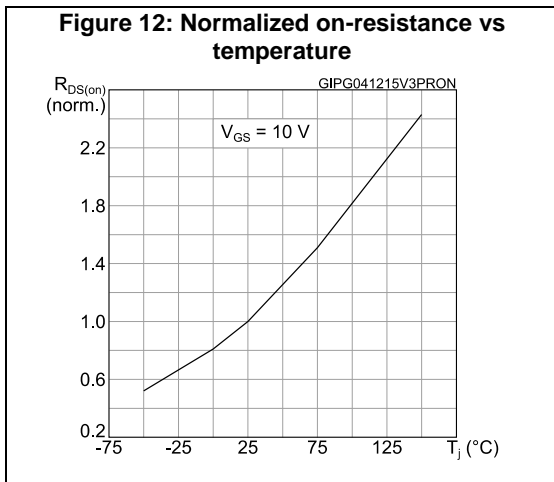
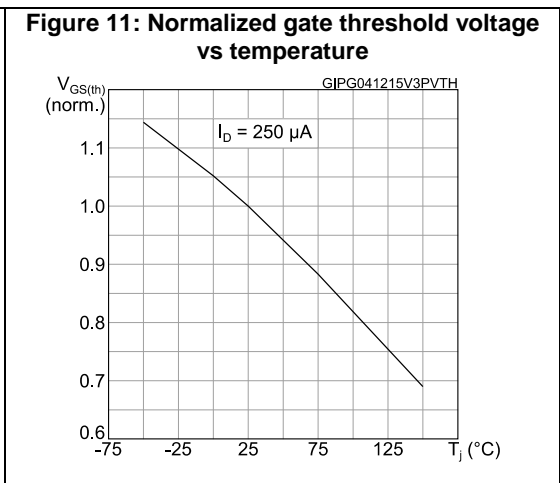
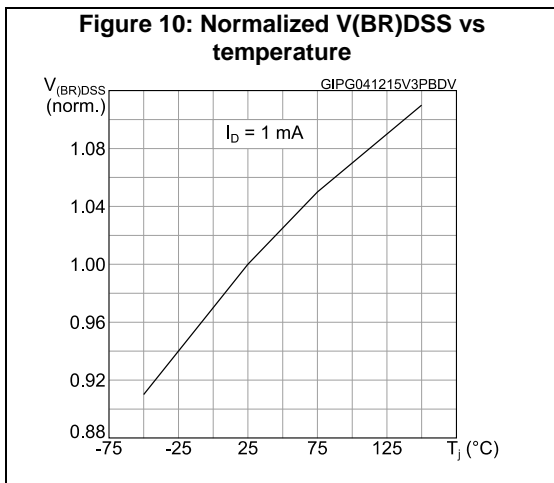
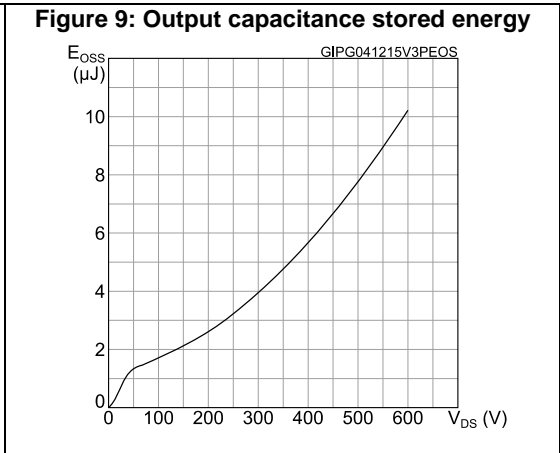
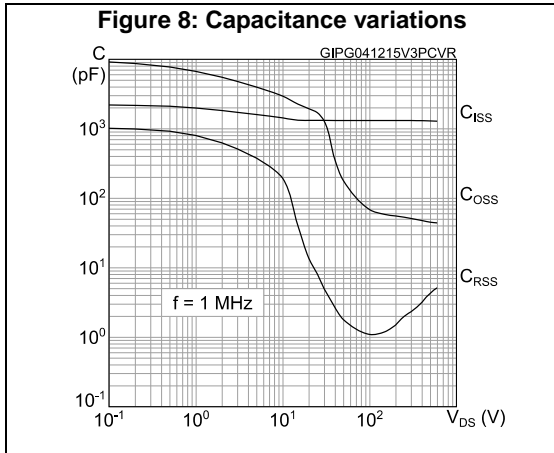
**Notes:**

<sup>(1)</sup>Pulse width is limited by safe operating area

<sup>(2)</sup>Pulsed: pulse duration = 300  $\mu\text{s}$ , duty cycle 1.5%

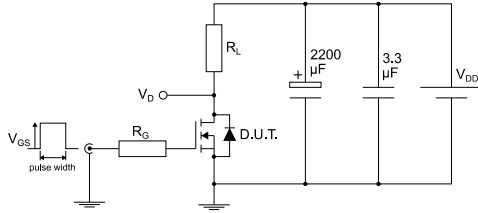
## 2.1 Electrical characteristics (curves)





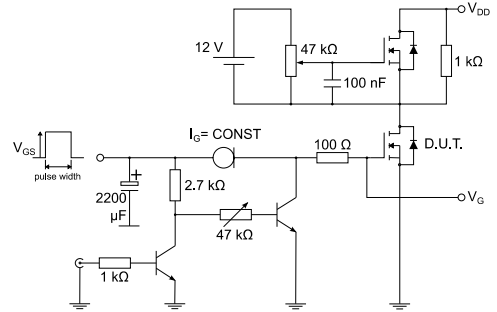
### 3 Test circuits

**Figure 14: Test circuit for resistive load switching times**



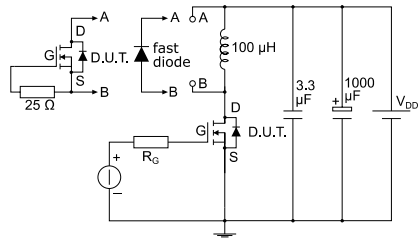
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**Figure 15: Test circuit for gate charge behavior**



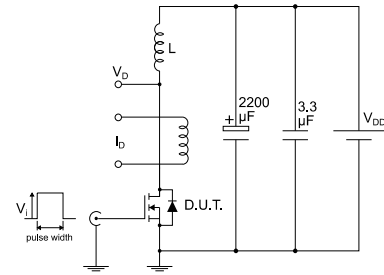
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**Figure 16: Test circuit for inductive load switching and diode recovery times**



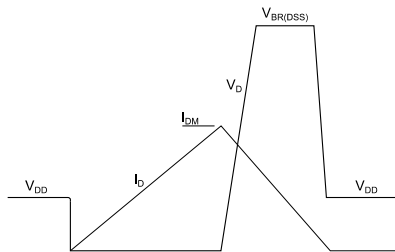
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**Figure 17: Unclamped inductive load test circuit**



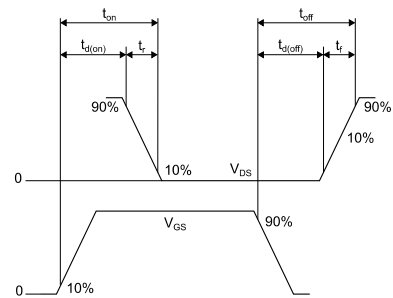
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**Figure 18: Unclamped inductive waveform**



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**Figure 19: Switching time waveform**



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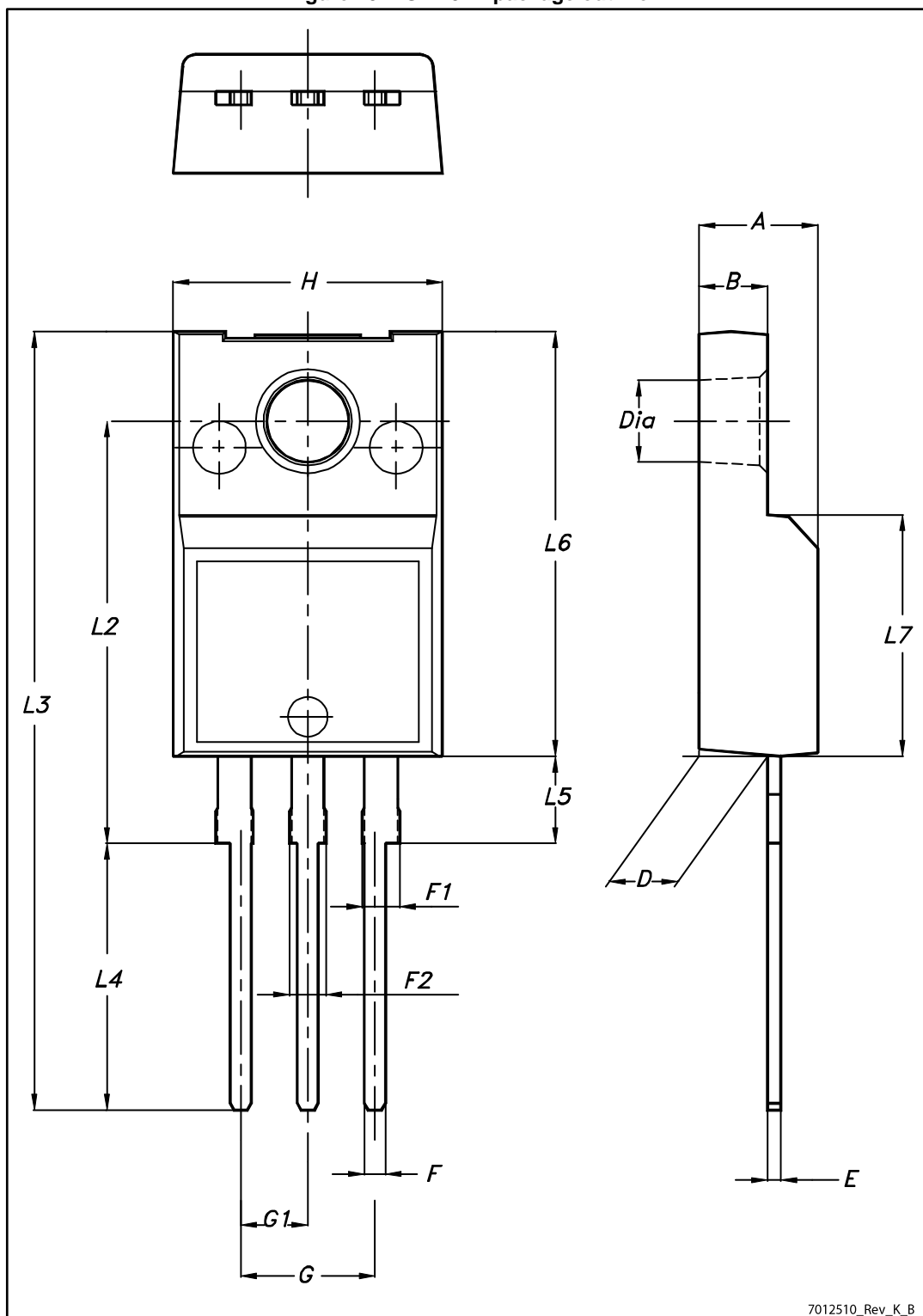


## 4 Package information

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK<sup>®</sup> packages, depending on their level of environmental compliance. ECOPACK<sup>®</sup> specifications, grade definitions and product status are available at: [www.st.com](http://www.st.com). ECOPACK<sup>®</sup> is an ST trademark.

### 4.1 TO-220FP package information

Figure 20: TO-220FP package outline



7012510\_Rev\_K\_B

Table 9: TO-220FP package mechanical data

Dim.	mm		
	Min.	Typ.	Max.
A	4.4		4.6
B	2.5		2.7
D	2.5		2.75
E	0.45		0.7
F	0.75		1
F1	1.15		1.70
F2	1.15		1.70
G	4.95		5.2
G1	2.4		2.7
H	10		10.4
L2		16	
L3	28.6		30.6
L4	9.8		10.6
L5	2.9		3.6
L6	15.9		16.4
L7	9		9.3
Dia	3		3.2

## 5 Revision history

Table 10: Document revision history

Date	Revision	Changes
14-Jan-2016	1	First release.

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