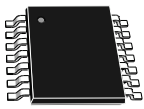
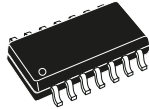


Rail-to-rail inputs and outputs, 36 V, 6 MHz op amps



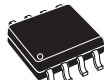
TSSOP14



SO14



MiniSO8



SO8



SOT23-5

Features

- Rail-to-rail input and output
- Low offset voltage: 1.5 mV maximum
- Wide supply voltage range: 2.7 V to 36 V
- Gain bandwidth product: 6 MHz
- Slew rate of 3 V/ μ s
- Low noise: 12 nV/ $\sqrt{\text{Hz}}$
- Integrated EMI filter
- 2 kV HBM ESD tolerance
- Extended temperature range: - 40 °C to + 125 °C
- Automotive-grade available

Applications

- High-side and low-side current sensing
- Hall effect sensors
- Test and measurement equipment
- Motor control
- Industrial process control
- Stain gauge

Maturity status link

[TSB511, TSB512, TSB514](#)

Related products

TSB711	For higher precision
TSB712	
TSB714	

Description

The **TSB511, TSB512, TSB514** is a series of 6 MHz bandwidth amplifiers featuring rail-to-rail input and output, which are guaranteed to operate from 2.7 to 36 V single supply as well as from ± 1.35 V to ± 18 V dual supplies.

These amplifiers have the advantage of offering a large span of supply voltage and a wide bandwidth.

The combination of wide bandwidth, slew rate, low noise, rail-to-rail capability makes the **TSB511, TSB512, TSB514** useful in a wide variety of applications such as: filters, power supply and motor control, actuator driving and resistive transducers.

1 Pin connection

Figure 1. TSB511 pin connections (top view)

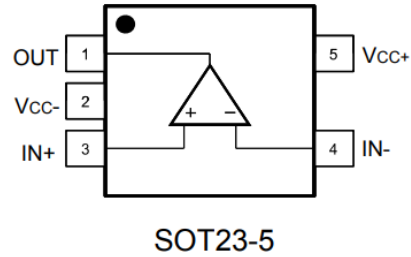


Table 1. TSB511 pin description

Pin	Pin name	Description
1	OUT1	Output
2	VCC -	Negative supply voltage
3	IN+	Positive input voltage
4	IN-	Negative input voltage
5	VCC +	Positive supply voltage

Figure 2. TSB512 pin connections (top view)

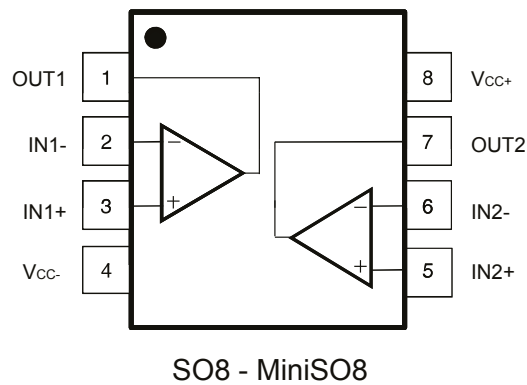


Table 2. TSB512 pin description

Pin	Pin name	Description
1	OUT1	Output
2	IN1-	Negative input voltage
3	IN1+	Positive input voltage
4	VCC-	Negative supply voltage
5	IN2+	Positive input voltage
6	IN2-	Negative input voltage
7	OUT2	Output
8	VCC+	Positive supply voltage

Figure 3. TSB514 pin connections (top view)

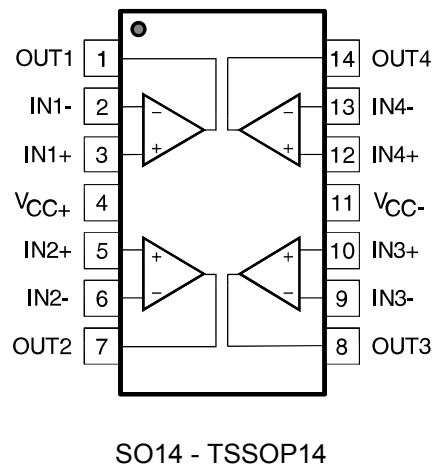


Table 3. TSB514 pin description

Pin	Pin name	Description
1	OUT1	Output
2	IN1-	Negative input voltage
3	IN1+	Positive input voltage
4	VCC+	Positive supply voltage
5	IN2+	Positive input voltage
6	IN2-	Negative input voltage
7	OUT2	Output
8	OUT3	Output
9	IN3-	Negative input voltage
10	IN3+	Positive input voltage
11	VCC-	Negative supply voltage
12	IN4+	Positive input voltage
13	IN4-	Negative input voltage
14	OUT4	Output

2 Maximum ratings

Table 4. Absolute maximum ratings

Symbol	Parameter	Value	Unit
V _{CC}	Supply voltage ⁽¹⁾	+ 40 or ± 20	V
V _{ID}	Differential input voltage ⁽²⁾	± 2	V
V _{IN}	Input voltage ⁽³⁾	(V _{CC-}) - 0.2 to (V _{CC+}) + 0.2	V
I _{IN}	Input current ⁽³⁾	± 10	mA
T _{stg}	Storage temperature	- 65 to 150	°C
T _j	Junction temperature	150	°C
R _{th-ja}	Thermal resistance junction to ambient ^{(4) (5)}		°C/W
	SOT23-5	250	
	MiniSO8	190	
	SO8	125	
	SO14	105	
ESD	TSSOP14	100	
	Human Body Model (HBM) ⁽⁶⁾	2	kV
	Charged Device Model (CDM) ⁽⁷⁾	1	

1. All voltage values, except differential voltage, are with respect to network ground terminal.
2. The differential voltage is the non-inverting input terminal with respect to the inverting input terminal.
3. Input voltage may be extended to the condition that the input current is limited to +/-10 mA. Input current must be limited by a resistor in series with the inputs when the input voltage is beyond the rails or the differential input voltage is above +/-2 V.
4. R_{th} are typical values.
5. Short-circuits can cause excessive heating and destructive dissipation.
6. According to JEDEC standard JESD22-A114F.
7. According to ANSI/ESD STM5.3.1.

Table 5. Operating conditions

Symbol	Parameter	Value	Unit
V _{CC}	Supply voltage	2.7 to 36	V
V _{ICM}	Common mode voltage on input pins	(V _{CC-}) to (V _{CC+}) + 0.1	V
T	Operating free-air temperature range	-40 to 125	°C

3 Electrical characteristics

Table 6. Electrical characteristics at $V_{CC+} = 5\text{ V}$, $V_{CC-} = 0\text{ V}$, $V_{ICM} = V_{OUT} = V_{CC}/2$, $T = 25\text{ }^{\circ}\text{C}$ and R_L connected to $V_{CC}/2$ (unless otherwise specified)

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
DC performance						
V_{IO}	Input offset voltage	$V_{CC-} \leq V_{ICM} \leq V_{CC+}$				mV
		$T = 25\text{ }^{\circ}\text{C}$			± 1.5	
		$T_{min} < T < T_{max}$			± 2	
$ \Delta V_{IO}/\Delta T $	Input offset voltage drift	$T_{min} < T < T_{max}$		2		$\mu\text{V}/^{\circ}\text{C}$
I_{IB}	Input bias current ⁽¹⁾	$V_{ICM} = V_{CC}/2$				nA
		$T = 25\text{ }^{\circ}\text{C}$	-100		0	
		$T_{min} < T < T_{max}$	-200		0	
I_{IO}	Input offset current ⁽²⁾	$V_{ICM} = V_{CC}/2$		10		
A_{VD}	Open loop gain	$(V_{CC-}) + 0.5\text{ V} \leq V_{OUT} \leq (V_{CC+}) - 0.5\text{ V}$, $R_L \geq 10\text{ k}\Omega$				dB
		$T = 25\text{ }^{\circ}\text{C}$	105	120		
		$T_{min} < T < T_{max}$	100			
CMR	Common mode rejection ratio: $20 \log(\Delta V_{icm}/\Delta V_{io})$	$V_{CC-} \leq V_{ICM} \leq V_{CC+}$				dB
		$T = 25\text{ }^{\circ}\text{C}$	75	105		
		$T_{min} < T < T_{max}$	70			
V_{OH}	High level output voltage (drop voltage from V_{CC+})	No load, $T_{min} < T < T_{max}$			90	mV
		$I_{source} = 2\text{ mA}$, $T_{min} < T < T_{max}$			200	
V_{OL}	Low-level output voltage	No load, $T_{min} < T < T_{max}$			90	mV
		$I_{sink} = 2\text{ mA}$, $T_{min} < T < T_{max}$			200	
I_{OUT}	I_{sink}	$V_{OUT} = V_{CC}$				mA
		$T = 25\text{ }^{\circ}\text{C}$	20	50		
	$T_{min} < T < T_{max}$	15				
	I_{source}	$V_{OUT} = 0\text{ V}$				
$T = 25\text{ }^{\circ}\text{C}$		20	50			
$T_{min} < T < T_{max}$	15					
I_{CC}	Supply current (per channel)	No load, $T = 25\text{ }^{\circ}\text{C}$		1.4		mA
		$T_{min} < T < T_{max}$			2.3	
AC performance						
GBP	Gain bandwidth product	$R_L = 10\text{ k}\Omega$, $C_L = 100\text{ pF}$	4.5	6		MHz
SR	Slew rate	3 V step, $R_L = 10\text{ k}\Omega$, $C_L = 100\text{ pF}$, $A_V = 1\text{ V/V}$, 10% to 90%	2	2.7		V/ μs
THD+N	Total harmonic distortion + noise	$V_{IN} = 1\text{ V}_{rms}$, $A_V = +1$, $f = 1\text{ kHz}$, $BW = 22\text{ kHz}$				%
		$R_L = 10\text{ k}\Omega$		0.0003		
		$R_L = 1\text{ k}\Omega$		0.0004		
Φ_m	Phase margin	$R_L = 10\text{ k}\Omega$, $C_L = 100\text{ pF}$, Unity gain		34		$^{\circ}$

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
C_{Load}	Capacitive load drive			100		pF
en	Input voltage noise density	$f = 10 \text{ kHz}$		12		nV/ $\sqrt{\text{Hz}}$
en p-p	Input noise voltage	$0.1 \text{ Hz} \leq f \leq 10 \text{ Hz}$		0.8		μVpp

1. Current is positive when it is sinked into the op amp.
2. I_{IO} is defined as $|I_{ibp} - I_{ibn}|$.

Table 7. Electrical characteristics at $V_{CC+} = 36 \text{ V}$, $V_{CC-} = 0 \text{ V}$, $V_{ICM} = V_{OUT} = V_{CC}/2$, $T = 25 \text{ }^\circ\text{C}$ and R_L connected to $V_{CC}/2$ (unless otherwise specified)

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
DC performance						
V_{IO}	Input offset voltage	$V_{CC-} \leq V_{ICM} \leq V_{CC+}$				mV
		$T = 25 \text{ }^\circ\text{C}$			± 1.5	
		$T_{min} < T < T_{max}$			± 2	
$ \Delta V_{IO}/\Delta T $	Input offset voltage drift	$T_{min} < T < T_{max}$		2		$\mu\text{V}/^\circ\text{C}$
I_{IB}	Input bias current ⁽¹⁾	$V_{ICM} = V_{CC}/2$				nA
		$T = 25 \text{ }^\circ\text{C}$	-100		0	
		$T_{min} < T < T_{max}$	-200		0	
I_{IO}	Input offset current ⁽²⁾	$V_{ICM} = V_{CC}/2$		10		
A_{VD}	Open loop gain	$(V_{CC-}) + 0.5 \text{ V} \leq V_{OUT} \leq (V_{CC+}) - 0.5 \text{ V}$, $R_L \geq 10 \text{ k}\Omega$				dB
		$T = 25 \text{ }^\circ\text{C}$	110	125		
		$T_{min} < T < T_{max}$	105			
CMR	Common mode rejection ratio: $20 \log (\Delta V_{icm}/\Delta V_{io})$	$V_{CC-} \leq V_{ICM} \leq V_{CC+}$				dB
		$T = 25 \text{ }^\circ\text{C}$	90	120		
		$T_{min} < T < T_{max}$	85			
SVR	Power supply rejection ratio: $20 \log (\Delta V_{cc}/\Delta V_{io})$	$5 \text{ V} < (V_{CC+}) - (V_{CC-}) < 36 \text{ V}$, $V_{ICM} = V_{CC}/2$, $T_{min} < T < T_{max}$	100	125		dB
V_{OH}	High level output voltage (drop voltage from V_{CC+})	No load, $T_{min} < T < T_{max}$			120	mV
		$I_{source} = 2 \text{ mA}$, $T_{min} < T < T_{max}$			200	
		$I_{source} = 15 \text{ mA}$, $T_{min} < T < T_{max}$			1000	
V_{OL}	Low-level output voltage	No load, $T_{min} < T < T_{max}$			120	mV
		$I_{sink} = 2 \text{ mA}$, $T_{min} < T < T_{max}$			200	
		$I_{sink} = 15 \text{ mA}$, $T_{min} < T < T_{max}$			1000	
I_{OUT}	I_{sink}	$V_{OUT} = V_{CC}$				mA
		$T = 25 \text{ }^\circ\text{C}$	25	50		
	$T_{min} < T < T_{max}$	20				
	I_{source}	$V_{OUT} = 0 \text{ V}$				
$T = 25 \text{ }^\circ\text{C}$		25	50			
$T_{min} < T < T_{max}$	20					
I_{CC}	Supply current (per channel)	No load, $T = 25 \text{ }^\circ\text{C}$		1.8		mA
		$T_{min} < T < T_{max}$			3	

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit	
AC performance							
GBP	Gain bandwidth product	$R_L = 10\text{ k}\Omega$, $C_L = 100\text{ pF}$	4.5	6		MHz	
SR	Slew rate	9 V step, $R_L = 10\text{ k}\Omega$, $C_L = 100\text{ pF}$, $A_V = 1\text{ V/V}$, 10% to 90%	2.2	3		V/ μ s	
THD+N	Total harmonic distortion + noise	$V_{IN} = 1\text{ V}_{rms}$, $A_V = +1$, $f = 1\text{ kHz}$, $BW = 22\text{ kHz}$					%
		$R_L = 10\text{ k}\Omega$		0.0003			
		$R_L = 1\text{ k}\Omega$		0.0003			
Φ_m	Phase margin	$R_L = 10\text{ k}\Omega$, $C_L = 100\text{ pF}$, Unity gain		45		$^\circ$	
C_{Load}	Capacitive load drive			100		pF	
e_n	Input voltage noise density	$f = 10\text{ kHz}$		12		nV/ $\sqrt{\text{Hz}}$	
$e_n\text{ p-p}$	Input noise voltage	$0.1\text{ Hz} \leq f \leq 10\text{ Hz}$		0.5		μ Vpp	
CR	Cross talk	$V_{OUT} = 5\text{ Vpp}$, $A_V = +11$, $R_L = 10\text{ k}\Omega$					dB
		$f = 1\text{ kHz}$		125			
		$f = 10\text{ kHz}$		100			

1. Current is positive when it is sunk into the op amp.
2. I_{io} is defined as $|I_{ibp} - I_{ibn}|$.

4 Typical performance characteristics

Figure 4. Supply current vs. supply voltage

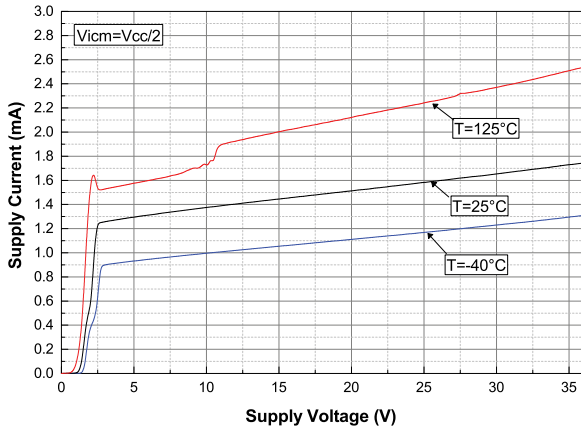


Figure 5. Input offset voltage vs. supply voltage

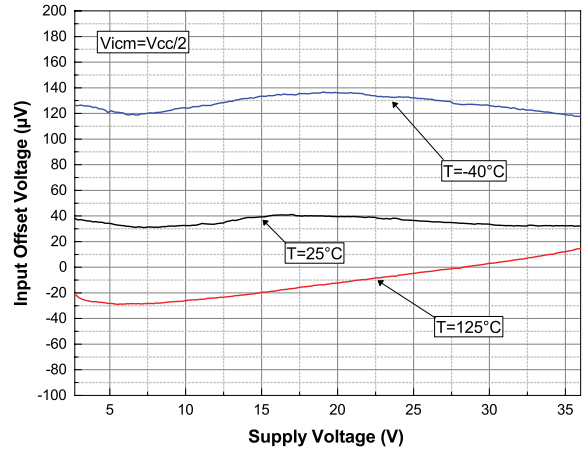


Figure 6. Input offset voltage vs. common mode voltage at $V_{CC} = 5\text{ V}$

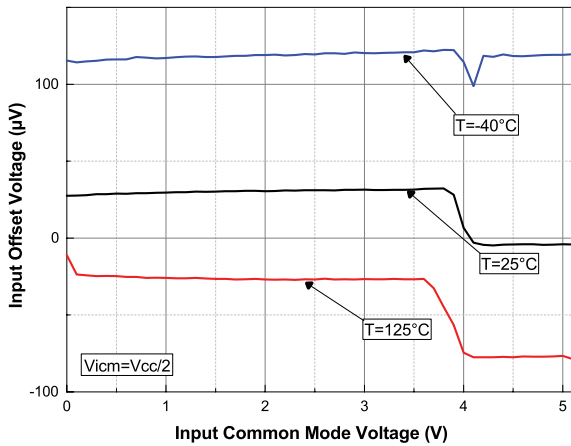


Figure 7. Input offset voltage vs. common mode voltage at $V_{CC} = 36\text{ V}$

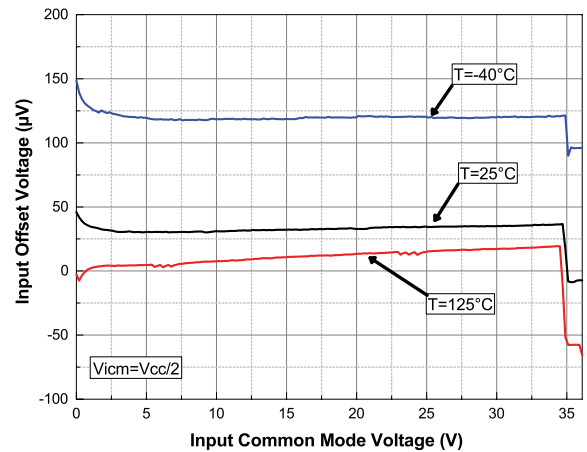


Figure 8. Input bias current vs. temperature at $V_{ICM} = V_{CC}/2$

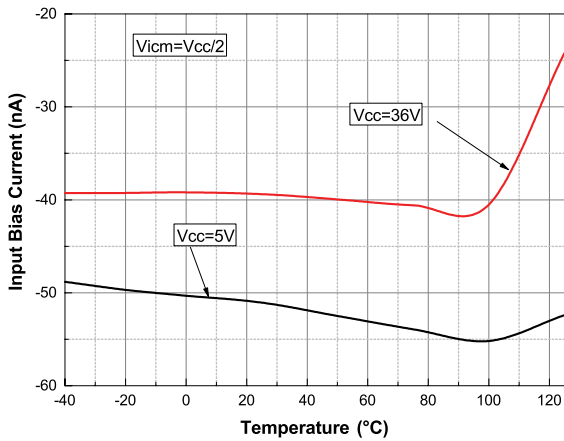


Figure 9. Input bias current vs. common mode voltage at $V_{CC} = 5\text{ V}$

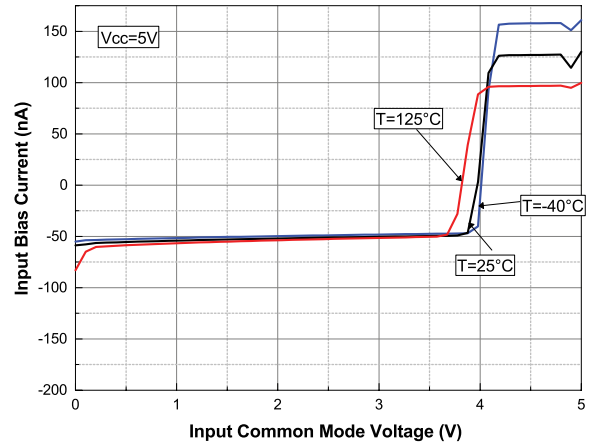


Figure 10. Input bias current vs. common mode voltage at $V_{CC} = 36\text{ V}$

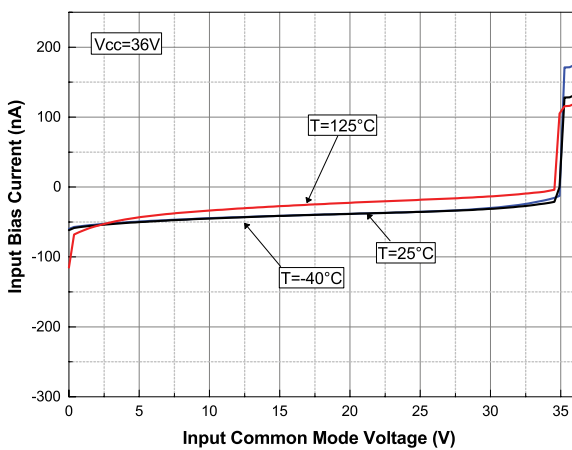


Figure 11. Output current vs. output voltage at $V_{CC} = 5\text{ V}$

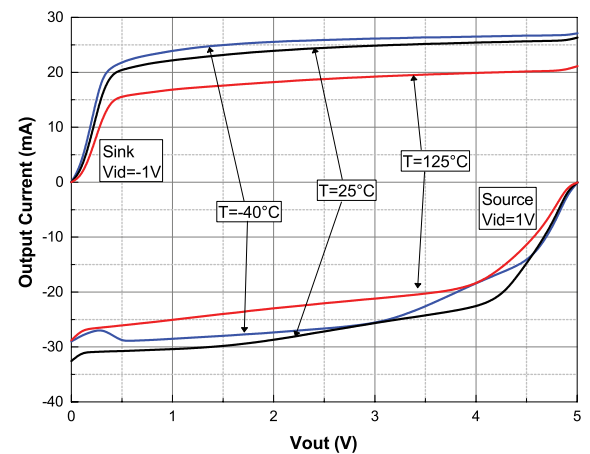


Figure 12. Output current vs. output voltage at $V_{CC} = 36\text{ V}$

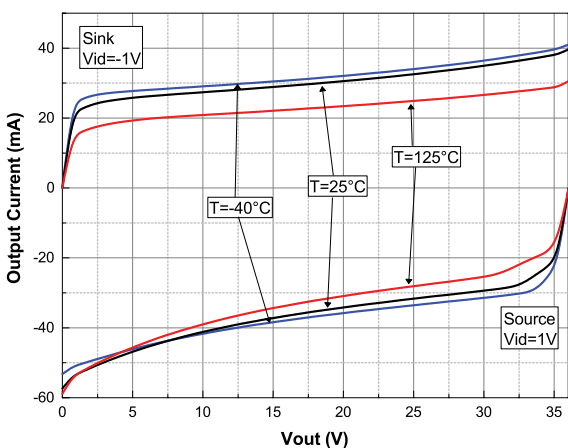


Figure 13. Output voltage (V_{OH}) vs. supply voltage

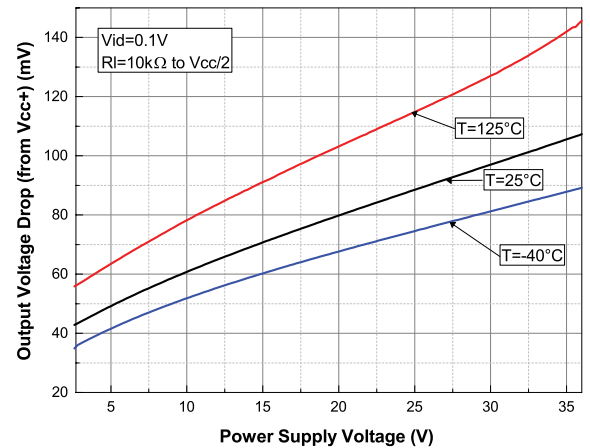


Figure 14. Output voltage (V_{OL}) vs. supply voltage

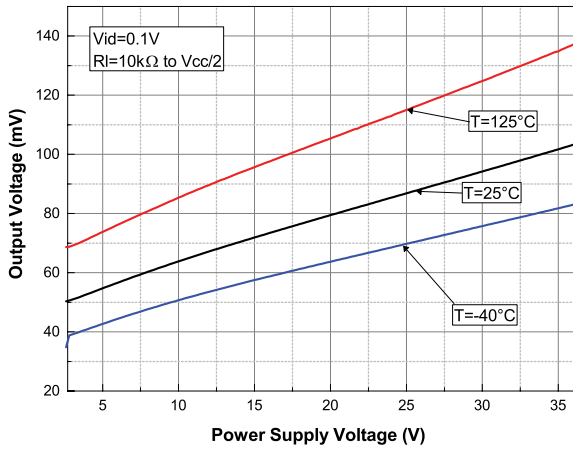


Figure 15. Channel separation vs. frequency at $V_{CC} = 36\text{V}$

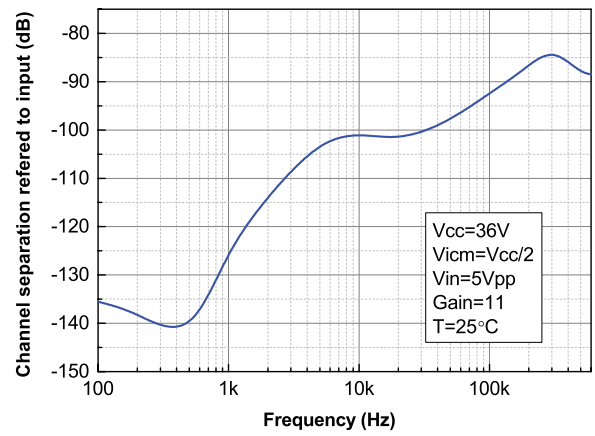


Figure 16. Positive slew rate at $V_{CC} = 36\text{V}$

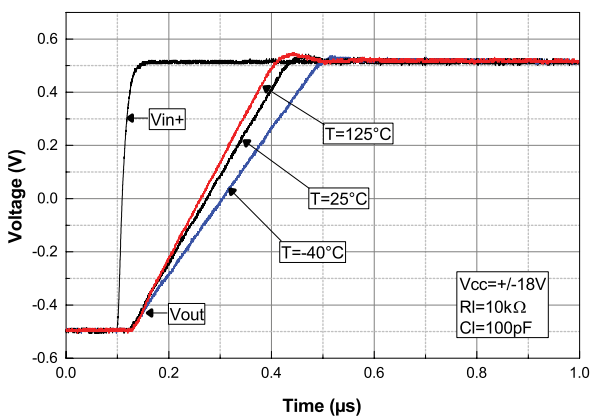


Figure 17. Negative slew rate at $V_{CC} = 36\text{V}$

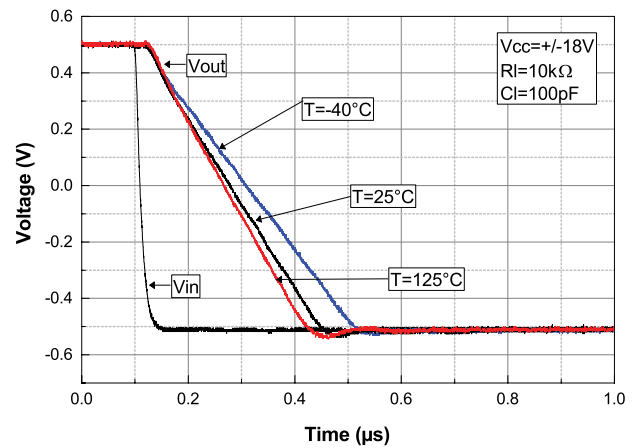


Figure 18. Bode diagram at $V_{CC} = 5\text{V}$

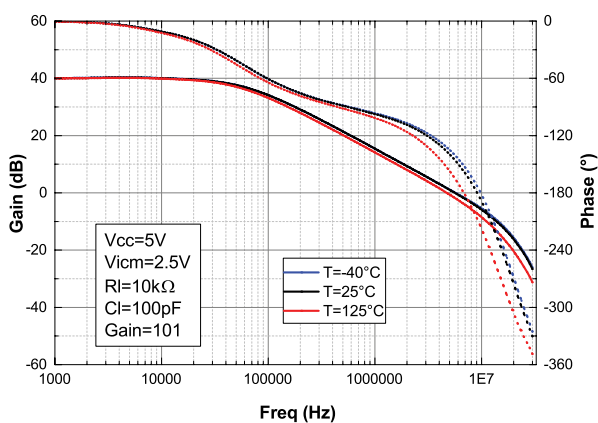


Figure 19. Bode diagram at $V_{CC} = 36\text{V}$

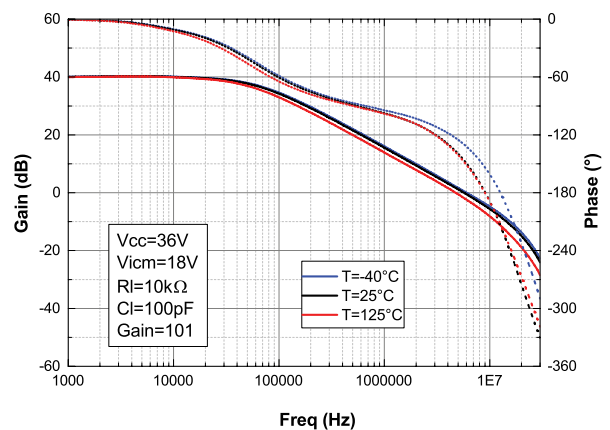


Figure 20. Phase margin vs. output current at $V_{CC} = 5\text{ V}$

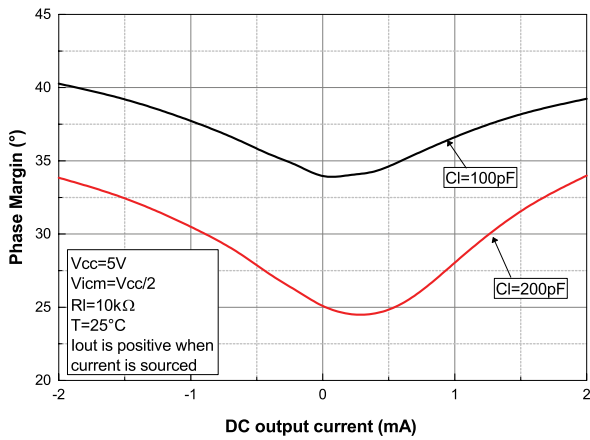


Figure 21. Phase margin vs. output current at $V_{CC} = 36\text{ V}$

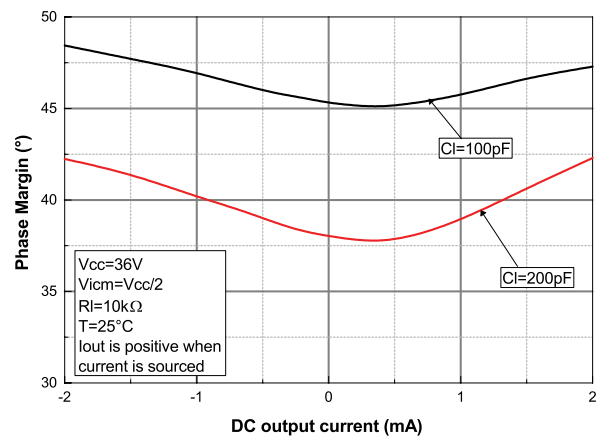


Figure 22. Phase margin vs. capacitive load

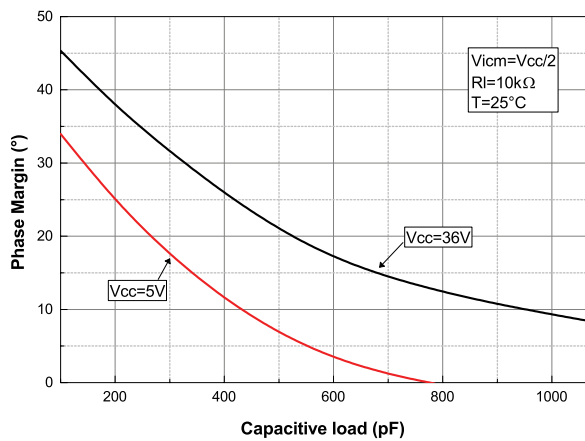


Figure 23. Overshoot vs. capacitive load at $V_{CC} = 36\text{ V}$

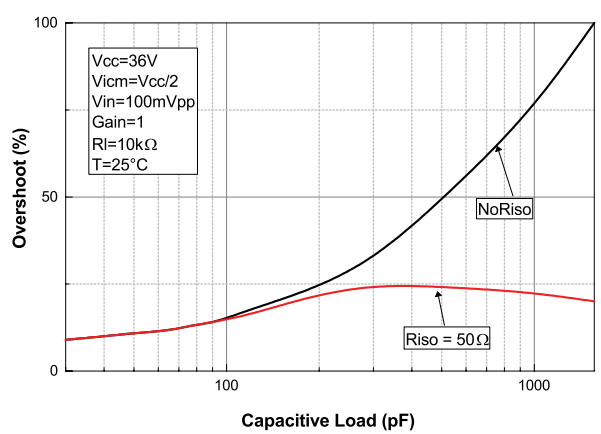


Figure 24. Small step response at $V_{CC} = 5\text{ V}$

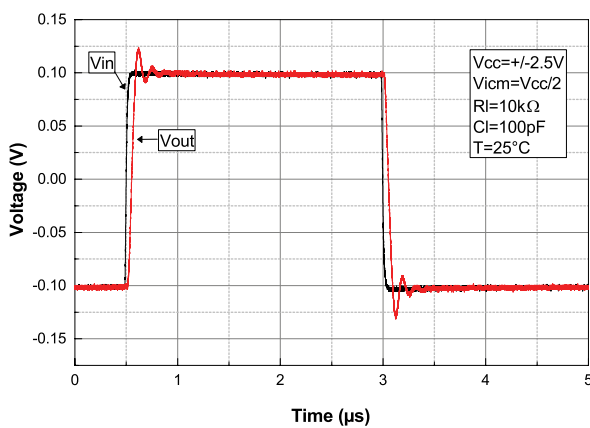


Figure 25. Desaturation time at low rail at $V_{CC} = 5\text{ V}$

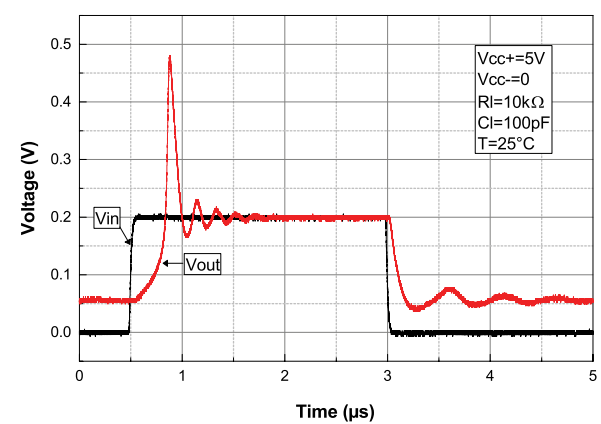


Figure 26. Desaturation time at high rail at $V_{CC} = 5\text{ V}$

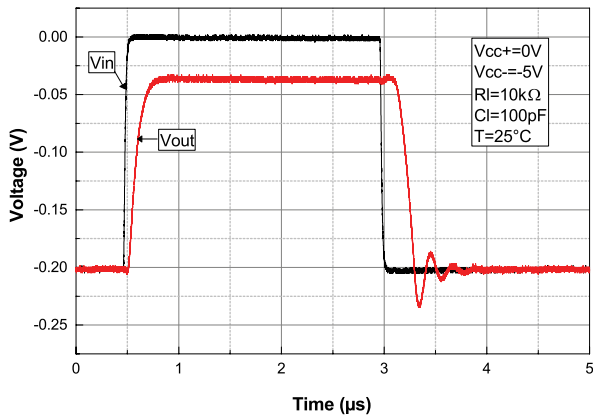


Figure 27. Small step response at $V_{CC} = 36\text{ V}$

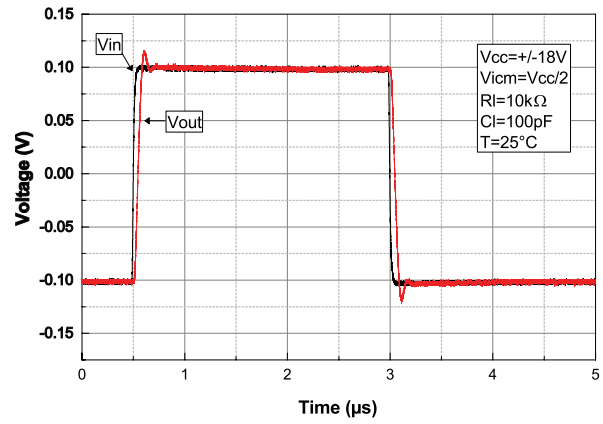


Figure 28. Amplifier behavior close to low rail at $V_{CC} = 36\text{ V}$

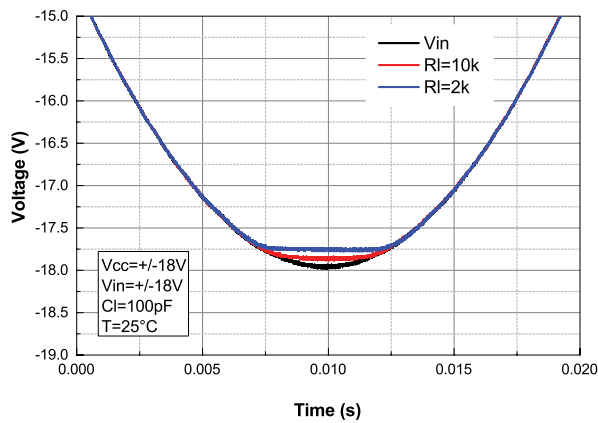


Figure 29. Amplifier behavior close to high rail at $V_{CC} = 36\text{ V}$

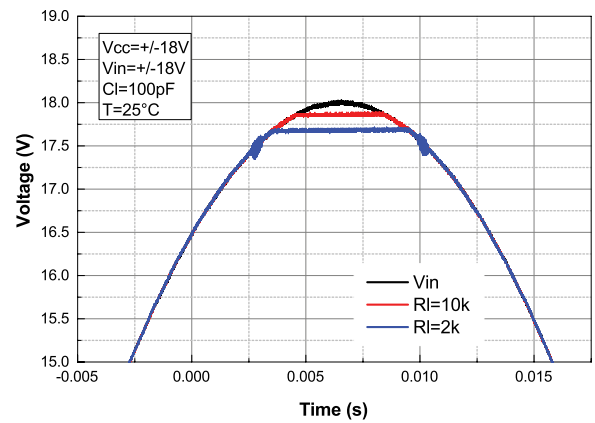


Figure 30. Noise vs. frequency at $V_{CC} = 5\text{ V}$

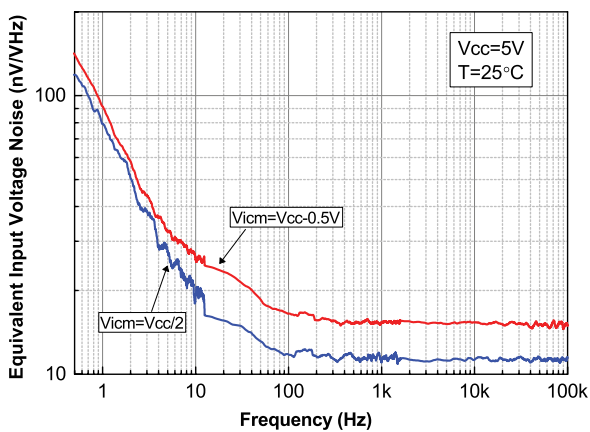


Figure 31. Noise vs. frequency at $V_{CC} = 36\text{ V}$

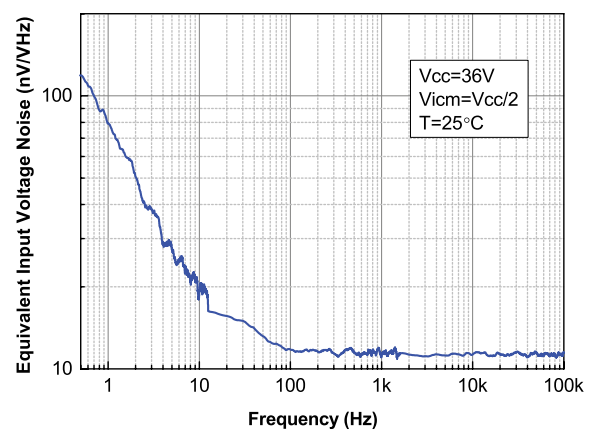


Figure 32. Noise vs. time at $V_{CC} = 36\text{ V}$

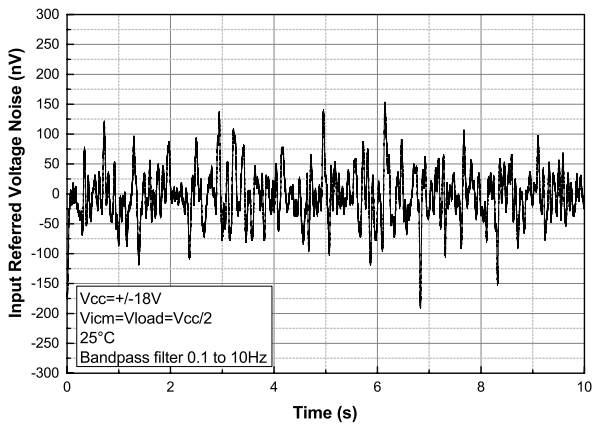


Figure 33. THD+N vs. frequency

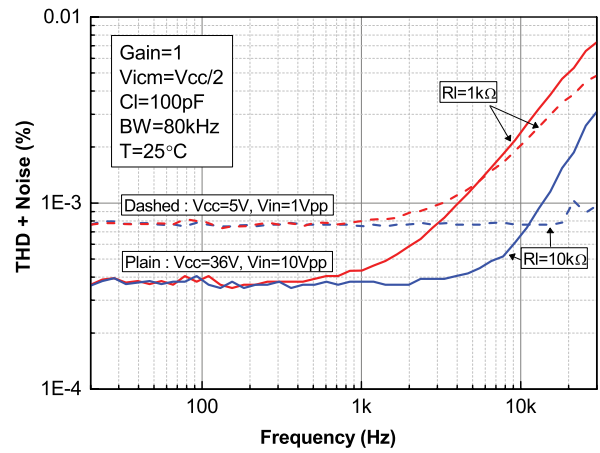


Figure 34. THD+N vs. frequency

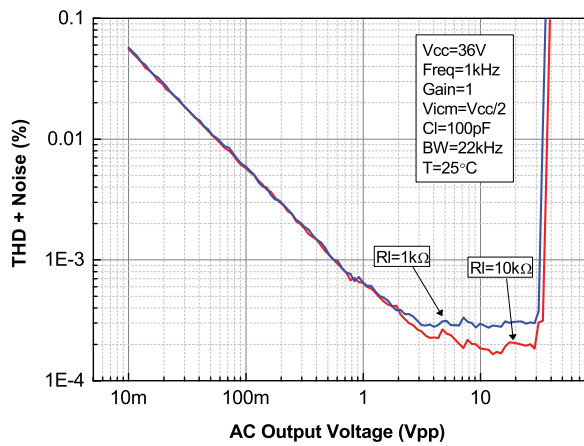


Figure 35. PSRR vs. frequency at $V_{CC} = 10\text{ V}$

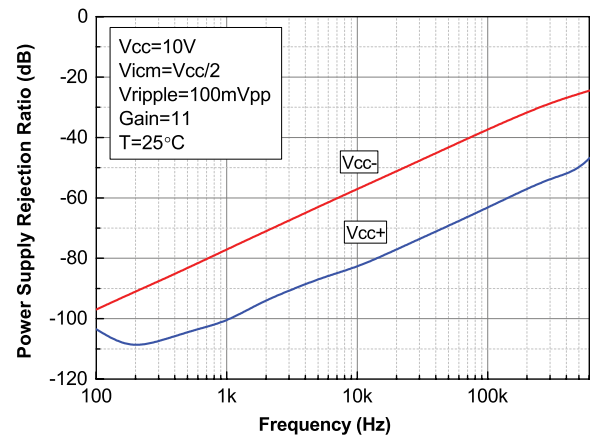
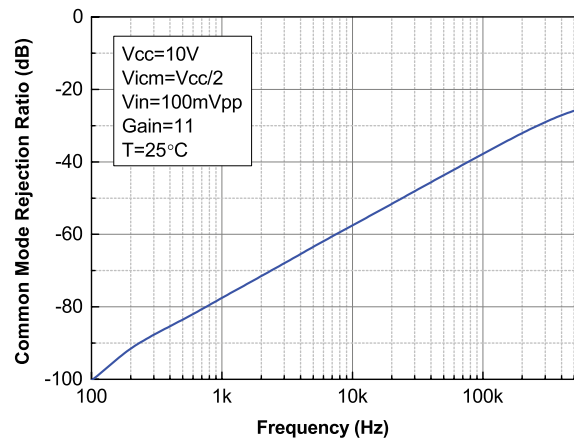


Figure 36. CMRR vs. frequency at $V_{CC} = 10\text{ V}$



5 Ordering information

Table 8. Order codes

Order code	Package	Packaging	Marking
TSB511ILT	SOT23-5	Tape & Reel	K232
TSB511IYLT ⁽¹⁾			K233
TSB512IDT	SO8		TSB512I
TSB512IYDT ⁽¹⁾			TSB512IY
TSB512IST	MiniSO8		K232
TSB512IYST ⁽¹⁾			K233
TSB514IDT	SO14		TSB514I
TSB514IYDT ⁽¹⁾			TSB514IY
TSB514IPT	TSSOP14		B514I
TSB514IYPT ⁽¹⁾			B514IY

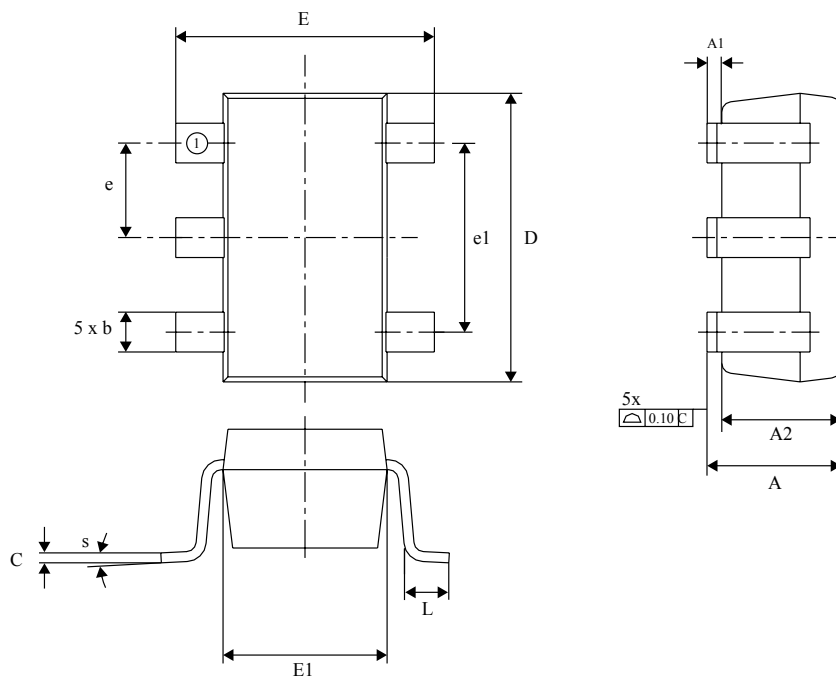
1. Qualified and characterized according to AEC Q100 and Q003 or equivalent, advanced screening according to AEC Q001 & Q002 or equivalent.

6 Package information

In order to meet environmental requirements, ST offers these devices in different grades of **ECOPACK** packages, depending on their level of environmental compliance. ECOPACK specifications, grade definitions and product status are available at: www.st.com. ECOPACK is an ST trademark.

6.1 SOT23-5 package information

Figure 37. SOT23-5 package outline



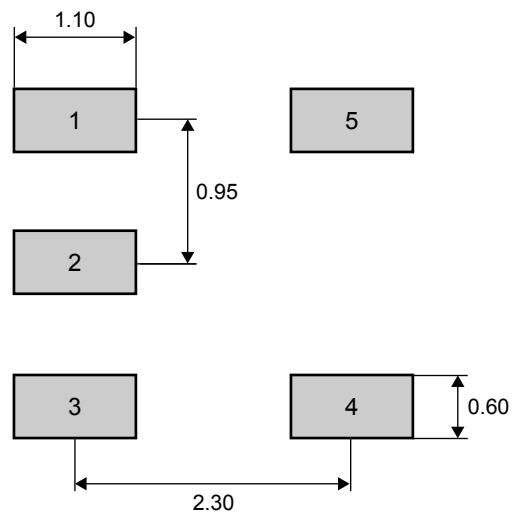
SOT23-5

Table 9. SOT23-5 mechanical data

Symbol	Millimeters			Inches ⁽¹⁾		
	Min.	Typ.	Max.	Min.	Typ.	Max.
A			1.45			0.057
A1	0.00		0.15	0.000		0.006
A2	0.90	1.15	1.30	0.035	0.045	0.051
b	0.30		0.50	0.012		0.020
c	0.08		0.22	0.003		0.009
D		2.90			0.114	
E		2.80			0.110	
E1		1.60			0.063	
e		0.95			0.037	
e1		1.90			0.075	
L	0.30	0.45	0.60	0.012	0.018	0.024
θ	0	4	8	0	4	8

1. Values in inches are converted from mm and rounded to 4 decimal digits.

Figure 38. SOT23-5 recommended footprint



6.2 MiniSO8 package information

Figure 39. MiniSO8 package outline

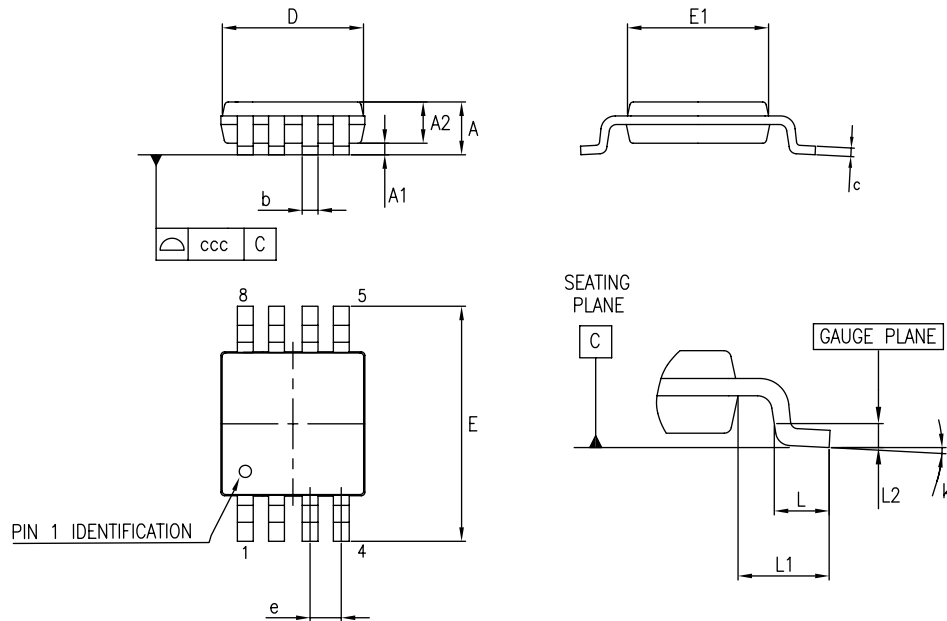


Table 10. MiniSO8 mechanical data

Dim.	Millimeters			Inches		
	Min.	Typ.	Max.	Min.	Typ.	Max.
A			1.1			0.043
A1	0		0.15	0		0.006
A2	0.75	0.85	0.95	0.03	0.033	0.037
b	0.22		0.4	0.009		0.016
c	0.08		0.23	0.003		0.009
D	2.8	3	3.2	0.11	0.118	0.126
E	4.65	4.9	5.15	0.183	0.193	0.203
E1	2.8	3	3.1	0.11	0.118	0.122
e		0.65			0.026	
L	0.4	0.6	0.8	0.016	0.024	0.031
L1		0.95			0.037	
L2		0.25			0.01	
k	0°		8°	0°		8°
ccc			0.1			0.004

6.3 SO8 package information

Figure 40. SO8 package outline

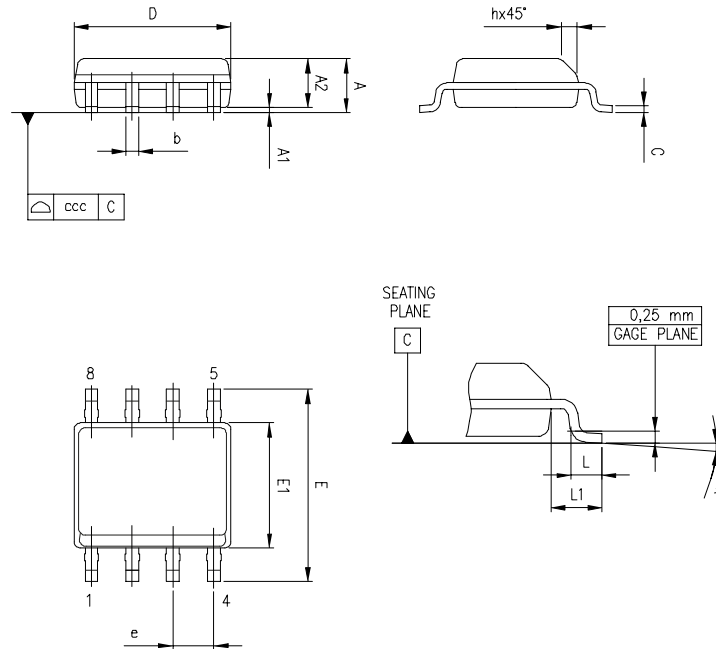
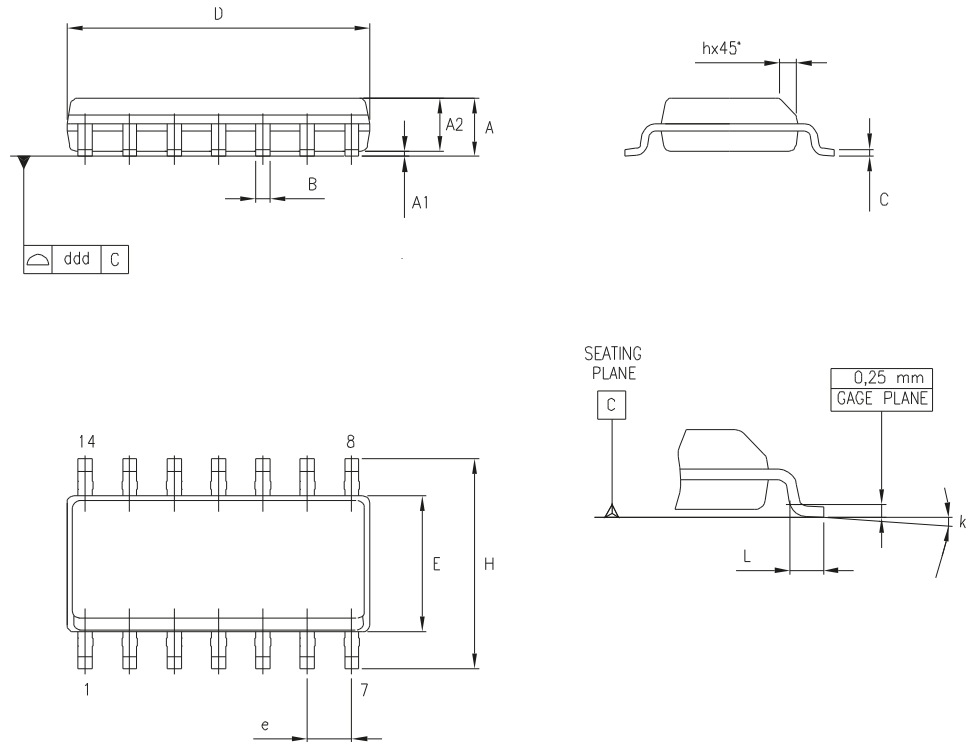


Table 11. SO8 mechanical data

Dim.	mm			Inches		
	Min.	Typ.	Max.	Min.	Typ.	Max.
A			1.75			0.069
A1	0.1		0.25	0.004		0.01
A2	1.25			0.049		
b	0.28		0.48	0.011		0.019
c	0.17		0.23	0.007		0.01
D	4.8	4.9	5	0.189	0.193	0.197
E	5.8	6	6.2	0.228	0.236	0.244
E1	3.8	3.9	4	0.15	0.154	0.157
e		1.27			0.05	
h	0.25		0.5	0.01		0.02
L	0.4		1.27	0.016		0.05
L1		1.04			0.04	
k	0		8 °	1 °		8 °
ccc			0.1			0.004

6.4 SO14 package information

Figure 41. SO14 package outline

Table 12. SO14 mechanical data

Dimensions ⁽¹⁾						
Symbol	Millimeters			Inches		
	Min.	Typ.	Max.	Min.	Typ.	Max.
A	1.35		1.75	0.05		0.068
A1	0.10		0.25	0.004		0.009
A2	1.10		1.65	0.04		0.06
B	0.33		0.51	0.01		0.02
C	0.19		0.25	0.007		0.009
D ⁽²⁾	8.55		8.75	0.33		0.34
E	3.80		4.0	0.15		0.15
e		1.27			0.05	
H	5.80		6.20	0.22		0.24
L	0.40		1.27	0.015		0.05
k	0°		8°	0°		8°
ddd			0.10			0.004

1. Drawing dimensions include "Single" and "Matrix" versions.

2. Dimension "D" does not include mold flash, protrusions or gate burrs. Mold flash, protrusions or gate burrs shall not exceed 0.15 mm per side.

6.5 TSSOP14 package information

Figure 42. TSSOP14 package outline

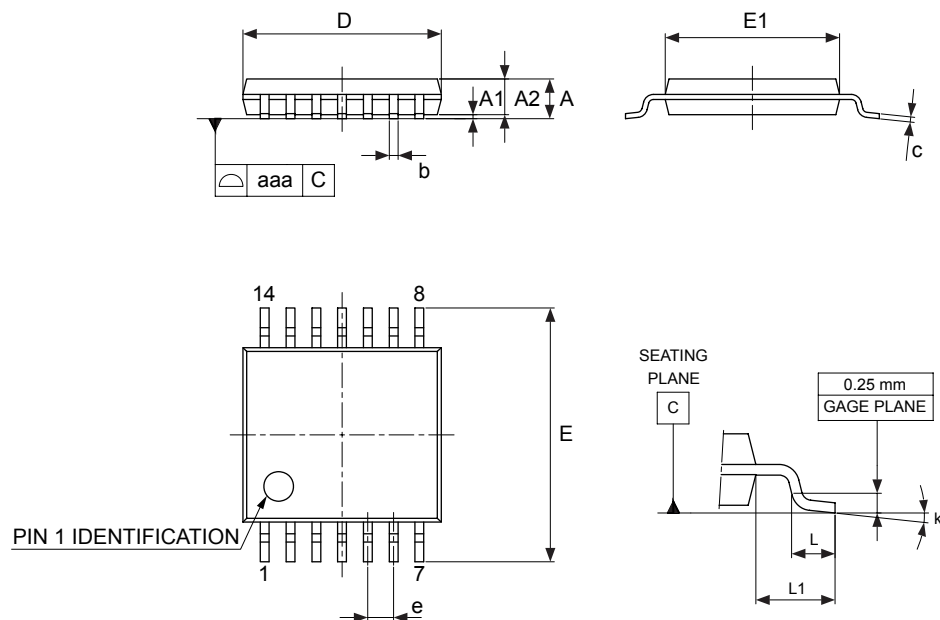


Table 13. TSSOP14 mechanical data

Symbol	Dimensions					
	Millimeters			Inches		
	Min.	Typ.	Max.	Min.	Typ.	Max.
A			1.20			0.047
A1	0.05		0.15	0.002	0.004	0.006
A2	0.80	1.00	1.05	0.031	0.039	0.041
b	0.19		0.30	0.007		0.012
c	0.09		0.20	0.004		0.0089
D	4.90	5.00	5.10	0.193	0.197	0.201
E	6.20	6.40	6.60	0.244	0.252	0.260
E1	4.30	4.40	4.50	0.169	0.173	0.176
e		0.65			0.0256	
L	0.45	0.60	0.75	0.018	0.024	0.030
L1		1.00			0.039	
k	0°		8°	0°		8°
aaa			0.10			0.004

Revision history

Table 14. Document revision history

Date	Revision	Changes
26-Jan-2022	1	Initial release.

Contents

1	Pin connection	2
2	Maximum ratings	4
3	Electrical characteristics	5
4	Typical performance characteristics	8
5	Ordering information	14
6	Package information	15
6.1	SOT23-5 package information	16
6.2	MiniSO8 package information	18
6.3	SO8 package information	19
6.4	SO14 package information	20
6.5	TSSOP14 package information	21
	Revision history	22

List of tables

Table 1.	TSB511 pin description	2
Table 2.	TSB512 pin description	2
Table 3.	TSB514 pin description	3
Table 4.	Absolute maximum ratings	4
Table 5.	Operating conditions	4
Table 6.	Electrical characteristics at $V_{CC+} = 5\text{ V}$, $V_{CC-} = 0\text{ V}$, $V_{ICM} = V_{OUT} = V_{CC}/2$, $T = 25\text{ }^{\circ}\text{C}$ and R_L connected to $V_{CC}/2$ (unless otherwise specified)	5
Table 7.	Electrical characteristics at $V_{CC+} = 36\text{ V}$, $V_{CC-} = 0\text{ V}$, $V_{ICM} = V_{OUT} = V_{CC}/2$, $T = 25\text{ }^{\circ}\text{C}$ and R_L connected to $V_{CC}/2$ (unless otherwise specified)	6
Table 8.	Order codes	14
Table 9.	SOT23-5 mechanical data	16
Table 10.	MiniSO8 mechanical data	18
Table 11.	SO8 mechanical data	19
Table 12.	SO14 mechanical data	20
Table 13.	TSSOP14 mechanical data	21
Table 14.	Document revision history	22

List of figures

Figure 1.	TSB511 pin connections (top view)	2
Figure 2.	TSB512 pin connections (top view)	2
Figure 3.	TSB514 pin connections (top view)	3
Figure 4.	Supply current vs. supply voltage	8
Figure 5.	Input offset voltage vs. supply voltage	8
Figure 6.	Input offset voltage vs. common mode voltage at $V_{CC} = 5\text{ V}$	8
Figure 7.	Input offset voltage vs. common mode voltage at $V_{CC} = 36\text{ V}$	8
Figure 8.	Input bias current vs. temperature at $V_{ICM} = V_{CC}/2$	9
Figure 9.	Input bias current vs. common mode voltage at $V_{CC} = 5\text{ V}$	9
Figure 10.	Input bias current vs. common mode voltage at $V_{CC} = 36\text{ V}$	9
Figure 11.	Output current vs. output voltage at $V_{CC} = 5\text{ V}$	9
Figure 12.	Output current vs. output voltage at $V_{CC} = 36\text{ V}$	9
Figure 13.	Output voltage (V_{OH}) vs. supply voltage	9
Figure 14.	Output voltage (V_{OL}) vs. supply voltage	10
Figure 15.	Channel separation vs. frequency at $V_{CC} = 36\text{ V}$	10
Figure 16.	Positive slew rate at $V_{CC} = 36\text{ V}$	10
Figure 17.	Negative slew rate at $V_{CC} = 36\text{ V}$	10
Figure 18.	Bode diagram at $V_{CC} = 5\text{ V}$	10
Figure 19.	Bode diagram at $V_{CC} = 36\text{ V}$	10
Figure 20.	Phase margin vs. output current at $V_{CC} = 5\text{ V}$	11
Figure 21.	Phase margin vs. output current at $V_{CC} = 36\text{ V}$	11
Figure 22.	Phase margin vs. capacitive load	11
Figure 23.	Overshoot vs. capacitive load at $V_{CC} = 36\text{ V}$	11
Figure 24.	Small step response at $V_{CC} = 5\text{ V}$	11
Figure 25.	Desaturation time at low rail at $V_{CC} = 5\text{ V}$	11
Figure 26.	Desaturation time at high rail at $V_{CC} = 5\text{ V}$	12
Figure 27.	Small step response at $V_{CC} = 36\text{ V}$	12
Figure 28.	Amplifier behavior close to low rail at $V_{CC} = 36\text{ V}$	12
Figure 29.	Amplifier behavior close to high rail at $V_{CC} = 36\text{ V}$	12
Figure 30.	Noise vs. frequency at $V_{CC} = 5\text{ V}$	12
Figure 31.	Noise vs. frequency at $V_{CC} = 36\text{ V}$	12
Figure 32.	Noise vs. time at $V_{CC} = 36\text{ V}$	13
Figure 33.	THD+N vs. frequency	13
Figure 34.	THD+N vs. frequency	13
Figure 35.	PSRR vs. frequency at $V_{CC} = 10\text{ V}$	13
Figure 36.	CMRR vs. frequency at $V_{CC} = 10\text{ V}$	13
Figure 37.	SOT23-5 package outline	16
Figure 38.	SOT23-5 recommended footprint	17
Figure 39.	MiniSO8 package outline	18
Figure 40.	SO8 package outline	19
Figure 41.	SO14 package outline	20
Figure 42.	TSSOP14 package outline	21

IMPORTANT NOTICE – PLEASE READ CAREFULLY

STMicroelectronics NV and its subsidiaries (“ST”) reserve the right to make changes, corrections, enhancements, modifications, and improvements to ST products and/or to this document at any time without notice. Purchasers should obtain the latest relevant information on ST products before placing orders. ST products are sold pursuant to ST’s terms and conditions of sale in place at the time of order acknowledgement.

Purchasers are solely responsible for the choice, selection, and use of ST products and ST assumes no liability for application assistance or the design of Purchasers’ products.

No license, express or implied, to any intellectual property right is granted by ST herein.

Resale of ST products with provisions different from the information set forth herein shall void any warranty granted by ST for such product.

ST and the ST logo are trademarks of ST. For additional information about ST trademarks, please refer to www.st.com/trademarks. All other product or service names are the property of their respective owners.

Information in this document supersedes and replaces information previously supplied in any prior versions of this document.

© 2022 STMicroelectronics – All rights reserved