# 1.1 V to 5.5 V, Slew Rate Controlled Load Switch

## DESCRIPTION

SiP32401A and SiP32402A are slew rate controlled load switches designed for 1.1 V to 5.5 V operation.

The devices guarantee low switch on-resistance at 1.2 V input. They feature a controlled soft-on slew rate of typical 2.5 ms that limits the inrush current for designs of heavy capacitive load and minimizes the resulting voltage droop at the power rails.

These devices feature low voltage control logic interface (On/Off interface) that can interface with low voltage control signal without extra level shifting circuit. SiP32402A also integrates an output discharge switch that enables fast shutdown load discharge.

Both SiP32401A and SiP32402A have exceptionally low shutdown current and provide reverse blocking to prevent high current flowing into the power source.

SiP32401A and SiP32402A are in TDFN4 package of 1.2 mm by 1.6 mm.

## FEATURES

- 1.1 V to 5.5 V operation voltage range
- 62 mΩ typical from 2 V to 5 V
- Low $R_{on}$ down to 1.2 V
- Slew rate controlled turn-on: 2.5 ms at 3.6 V
- Fast shutdown load discharge for SiP32402A
- Low quiescent current
  < 1 µA when disabled
  10.5 µA typical at $V_{IN}$ = 1.2 V
- Reverse current blocking when switch is off
- Material categorization: for definitions of compliance please see www.vishay.com/doc?99912

Pb-free

RoHS COMPLIANT

HALOGEN FREE Available

## APPLICATIONS

- PDAs / smart phones
- Notebook / netbook computers
- Tablet PC
- Portable media players
- Digital camera
- GPS navigation devices
- Data storage devices
- Optical, industrial, medical, and healthcare devices

## TYPICAL APPLICATION CIRCUIT

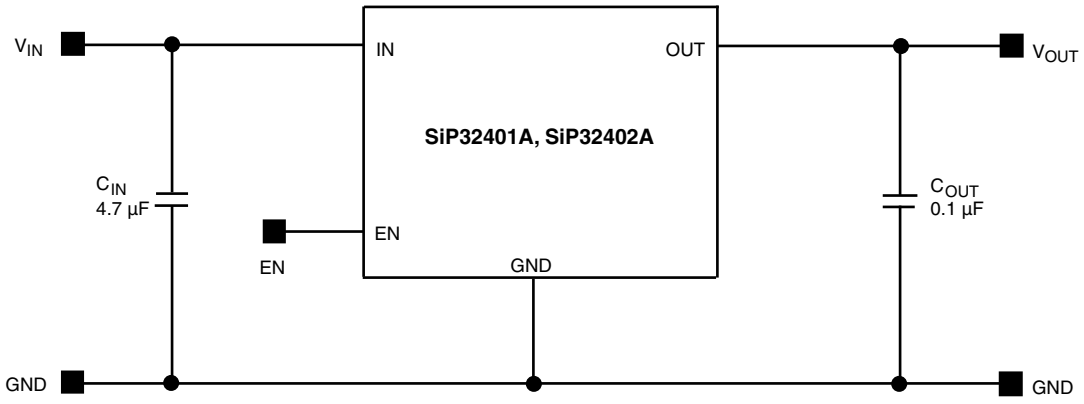



**Fig. 1 - SiP32401A, SiP32402A Typical Application Circuit**

| ORDERING INFORMATION | | | |
|---|---|---|---|
| **TEMPERATURE RANGE** | **PACKAGE** | **MARKING** | **PART NUMBER** |
| -40 °C to +85 °C | TDFN4 1.2 mm x 1.6 mm | Gx | SiP32401ADNP-T1GE4 |
| | | Hx | SiP32402ADNP-T1GE4 |

**Notes**
- x = Lot code
- GE4 denotes halogen-free and RoHS-compliant

| ABSOLUTE MAXIMUM RATINGS | | |
|---|---|---|
| **PARAMETER** | **LIMIT** | **UNIT** |
| Supply Input Voltage ($V_{IN}$) | -0.3 to +6 | V |
| Enable Input Voltage ($V_{EN}$) | -0.3 to +6 | |
| Output Voltage ($V_{OUT}$) | -0.3 to $V_{IN}$ + 0.3 | |
| Maximum Continuous Switch Current ($I_{max.}$) [c] | 2.4 | A |
| Maximum Repetitive Pulsed Current (1 ms, 10 % Duty Cycle) [c] | 3 | |
| ESD Rating (HBM) | 4000 | V |
| Junction Temperature ($T_J$) | -40 to +125 | °C |
| Thermal Resistance ($\theta_{JA}$) [a] | 170 | °C/W |
| Power Dissipation ($P_D$) [a, b] | 324 | mW |

**Notes**
a. Device mounted with all leads and power pad soldered or welded to PC board, see PCB layout.
b. Derate 5.9 mW/°C above $T_A$ = 70 °C, see PCB layout.
c. $T_A$ = 25 °C, see PCB layout

*Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating/conditions for extended periods may affect device reliability.*

| RECOMMENDED OPERATING RANGE | | |
|---|---|---|
| **PARAMETER** | **LIMIT** | **UNIT** |
| Input Voltage Range ($V_{IN}$) | 1.1 to 5.5 | V |
| Operating Junction Temperature Range ($T_J$) | -40 to +125 | °C |

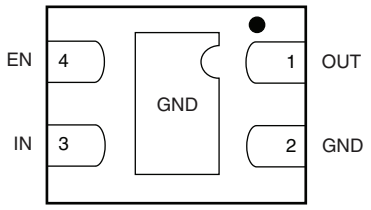
## SPECIFICATIONS

| PARAMETER | SYMBOL | TEST CONDITIONS UNLESS SPECIFIED $V_{IN}$ = 5 V, $T_A$ = -40 °C to +85 °C (typical values are at $T_A$ = 25 °C) | LIMITS -40 °C to +85 °C | | | UNIT |
|---|---|---|---|---|---|---|
| | | | MIN. [a] | TYP. [b] | MAX. [a] | |
| Operating Voltage [c] | $V_{IN}$ | | 1.1 | - | 5.5 | V |
| Quiescent Current | $I_Q$ | $V_{IN}$ = 1.2 V, EN = active | - | 10.5 | 17 | µA |
| | | $V_{IN}$ = 1.8 V, EN = active | - | 21 | 30 | |
| | | $V_{IN}$ = 2.5 V, EN = active | - | 34 | 50 | |
| | | $V_{IN}$ = 3.6 V, EN = active | - | 54 | 90 | |
| | | $V_{IN}$ = 4.3 V, EN = active | - | 68 | 110 | |
| | | $V_{IN}$ = 5 V, EN = active | - | 105 | 180 | |
| Off Supply Current | $I_{Q(off)}$ | EN = inactive, OUT = open | - | - | 1 | |
| Off Switch Current | $I_{DS(off)}$ | EN = inactive, OUT = GND | - | - | 1 | |
| Reverse Blocking Current | $I_{RB}$ | $V_{OUT}$ = 5 V, $V_{IN}$ = 0 V, $V_{EN}$ = inactive | - | - | 10 | |
| On-Resistance | $R_{DS(on)}$ | $V_{IN}$ = 1.2 V, $I_L$ = 100 mA, $T_A$ = 25 °C | - | 66 | 76 | mΩ |
| | | $V_{IN}$ = 1.8 V, $I_L$ = 100 mA, $T_A$ = 25 °C | - | 62 | 72 | |
| | | $V_{IN}$ = 2.5 V, $I_L$ = 100 mA, $T_A$ = 25 °C | - | 62 | 72 | |
| | | $V_{IN}$ = 3.6 V, $I_L$ = 100 mA, $T_A$ = 25 °C | - | 62 | 72 | |
| | | $V_{IN}$ = 4.3 V, $I_L$ = 100 mA, $T_A$ = 25 °C | - | 62 | 72 | |
| | | $V_{IN}$ = 5 V, $I_L$ = 100 mA, $T_A$ = 25 °C | - | 62 | 72 | |
| On-Resistance Temp.-Coefficient | $TC_{RDS}$ | | - | 4250 | - | ppm/°C |
| EN Input Low Voltage [c] | $V_{IL}$ | $V_{IN}$ = 1.2 V | - | - | 0.3 | V |
| | | $V_{IN}$ = 1.8 V | - | - | 0.4 [d] | |
| | | $V_{IN}$ = 2.5 V | - | - | 0.5 [d] | |
| | | $V_{IN}$ = 3.6 V | - | - | 0.6 [d] | |
| | | $V_{IN}$ = 4.3 V | - | - | 0.7 [d] | |
| | | $V_{IN}$ = 5 V | - | - | 0.8 [d] | |
| EN Input High Voltage [c] | $V_{IH}$ | $V_{IN}$ = 1.2 V | 0.9 [d] | - | - | |
| | | $V_{IN}$ = 1.8 V | 1.2 [d] | - | - | |
| | | $V_{IN}$ = 2.5 V | 1.4 [d] | - | - | |
| | | $V_{IN}$ = 3.6 V | 1.6 [d] | - | - | |
| | | $V_{IN}$ = 4.3 V | 1.7 [d] | - | - | |
| | | $V_{IN}$ = 5 V | 1.8 | - | - | |
| EN Input Leakage | $I_{SINK}$ | $V_{EN}$ = 5.5 V | -1 | - | 1 | µA |
| Output Pulldown Resistance | $R_{PD}$ | EN = inactive, $T_A$ = 25 °C (for SiP32402A only) | - | 217 | 280 | Ω |
| Output Turn-On Delay Time | $t_{d(on)}$ | $V_{IN}$ = 3.6 V, $R_{LOAD}$ = 10 Ω, $T_A$ = 25 °C | - | 1.8 | - | ms |
| Output Turn-On Rise Time | $t_{(on)}$ | | 1.2 | 2.5 | 3.8 | |
| Output Turn-Off Delay Time | $t_{d(off)}$ | | - | - | 0.001 | |

**Notes**

a. The algebraic convention whereby the most negative value is a minimum and the most positive a maximum.
b. Typical values are for DESIGN AID ONLY, not guaranteed nor subject to production testing.
c. For $V_{IN}$ outside this range consult typical EN threshold curve.
d. Not tested, guarantee by design.

## PIN CONFIGURATION




Bottom View

**Fig. 2 - TDFN4 1.2 mm x 1.6 mm Package**

| PIN DESCRIPTION | | |
|---|---|---|
| **PIN NUMBER** | **NAME** | **FUNCTION** |
| 1 | OUT | This is the output pin of the switch |
| 2 | GND | Ground connection |
| 3 | IN | This is the input pin of the switch |
| 4 | EN | Enable input |

## TYPICAL CHARACTERISTICS (internally regulated, 25 °C, unless otherwise noted)

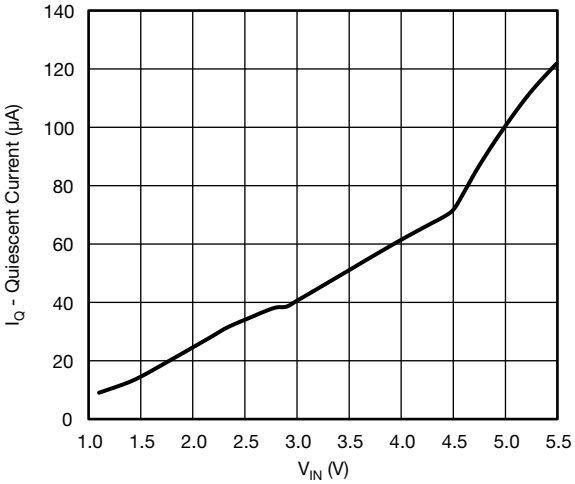



**Fig. 3 - Quiescent Current vs. Input Voltage**

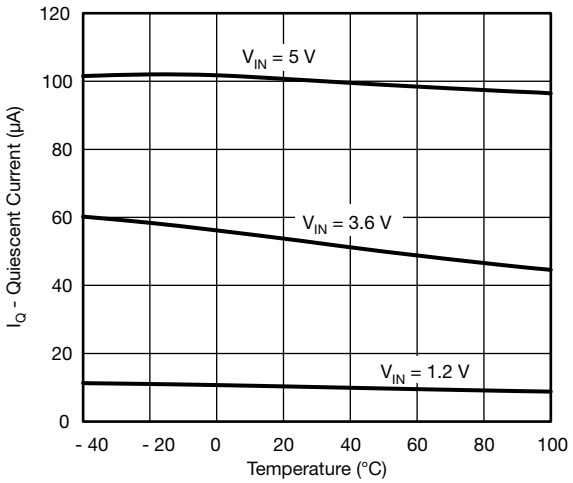



**Fig. 5 - Quiescent Current vs. Temperature**

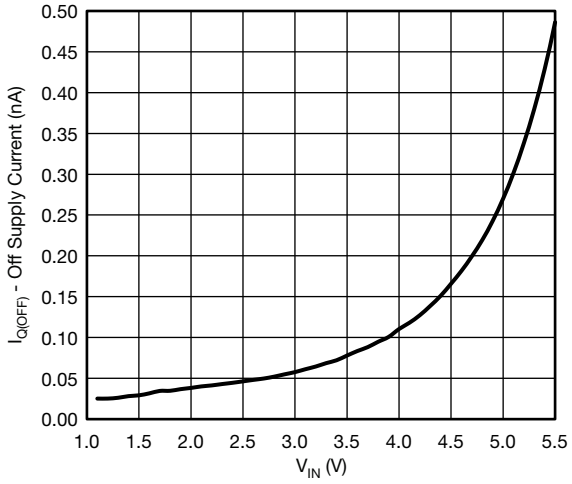



**Fig. 4 - Off Supply Current vs. Input Voltage**

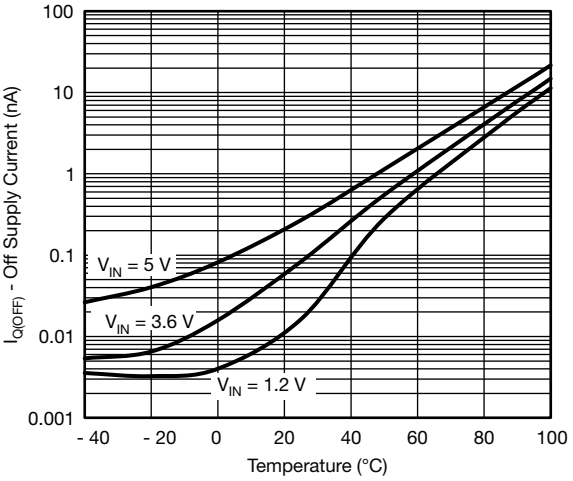



**Fig. 6 - Off Supply Current vs. Temperature**

**TYPICAL CHARACTERISTICS** (internally regulated, 25 °C, unless otherwise noted)

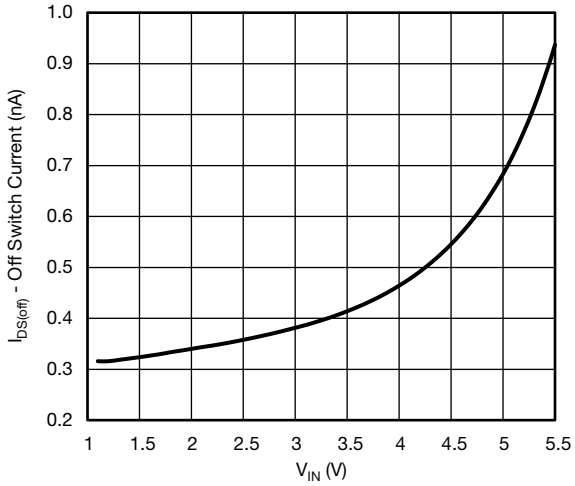



**Fig. 7 - Off Switch Current vs. Input Voltage**

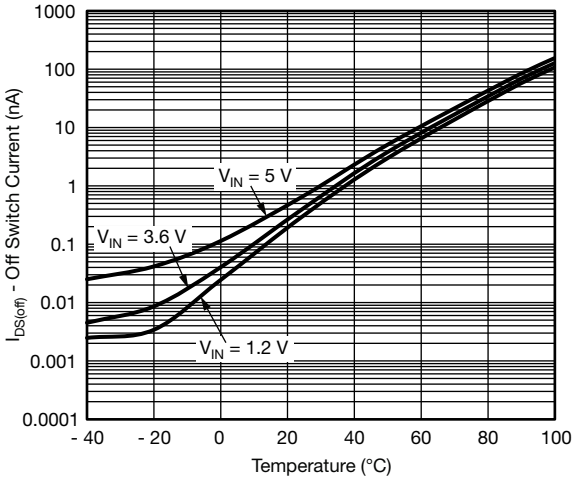



**Fig. 10 - Off Switch Current vs. Temperature**

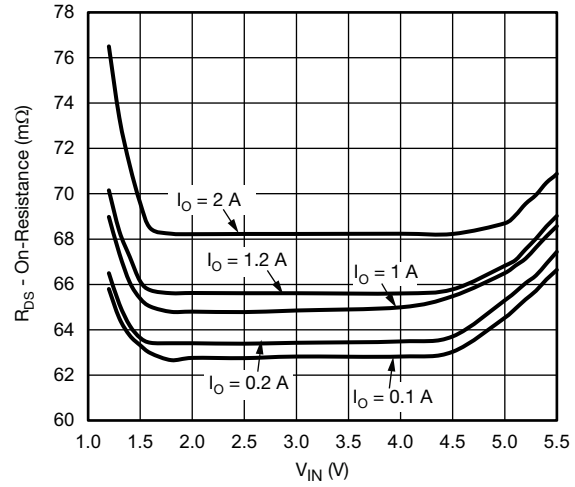



**Fig. 8 - $R_{DS(on)}$ vs. $V_{IN}$**

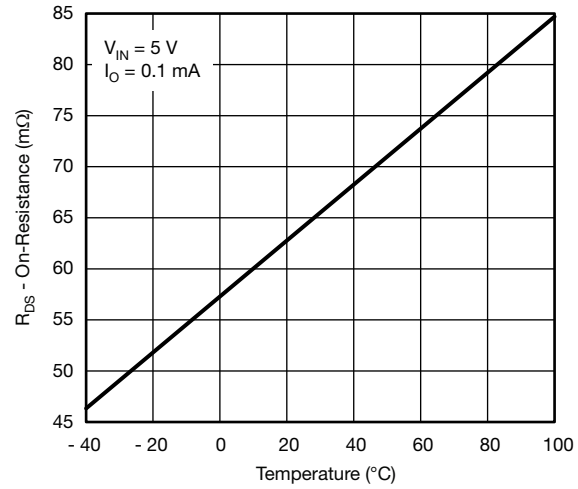



**Fig. 11 - $R_{DS(on)}$ vs. Temperature**

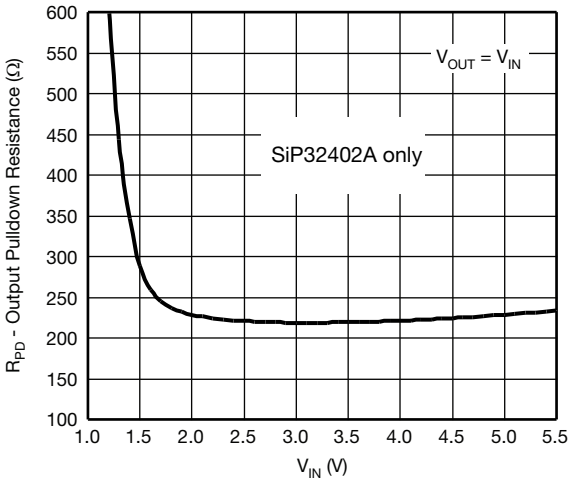



**Fig. 9 - Output Pull Down vs. Input Voltage**

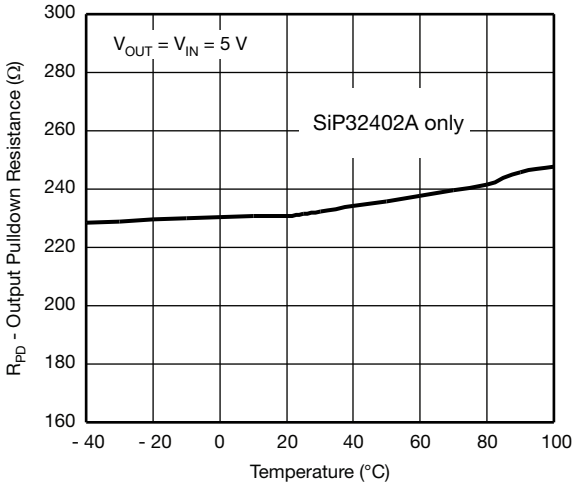



**Fig. 12 - Output Pull Down vs. Temperature**

**TYPICAL CHARACTERISTICS** (internally regulated, 25 °C, unless otherwise noted)

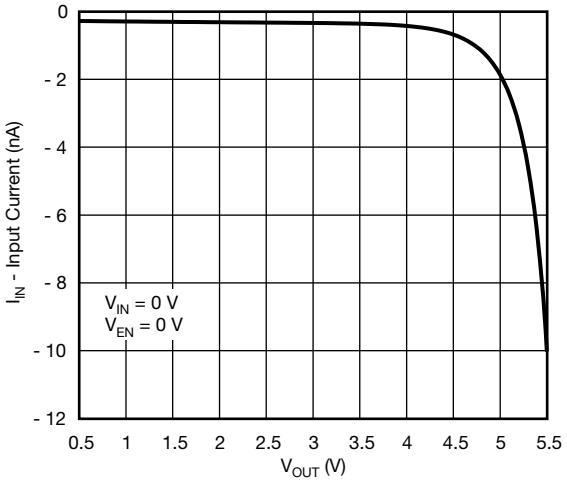



**Fig. 13 - Reverse Blocking Current vs. Output Voltage**

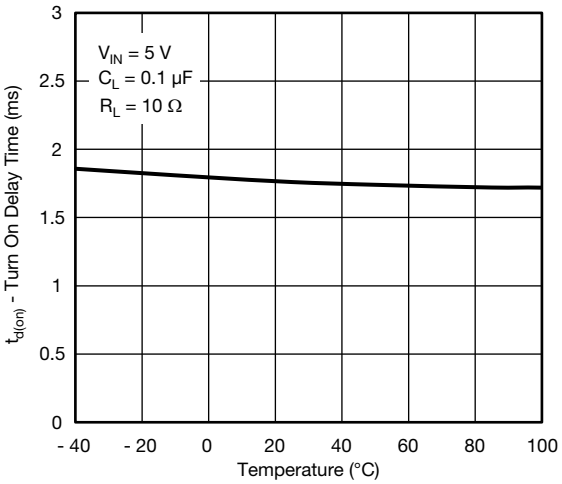



**Fig. 16 - Turn-on Delay Time vs. Temperature**

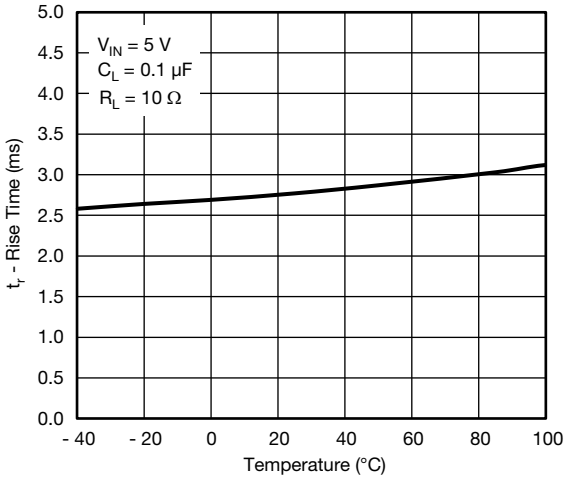



**Fig. 14 - Rise Time vs. Temperature**

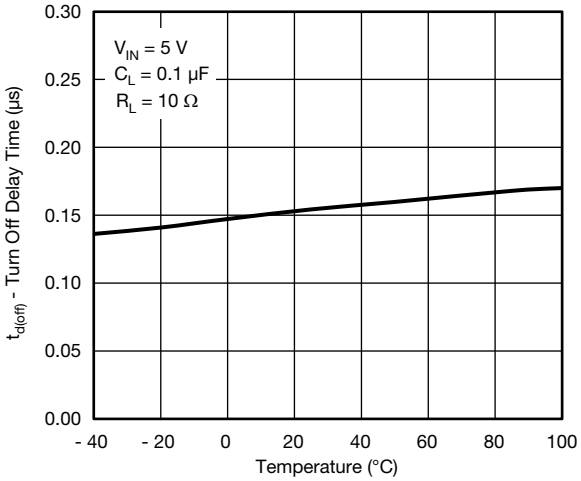



**Fig. 17 - Turn-Off Delay Time vs. Temperature**

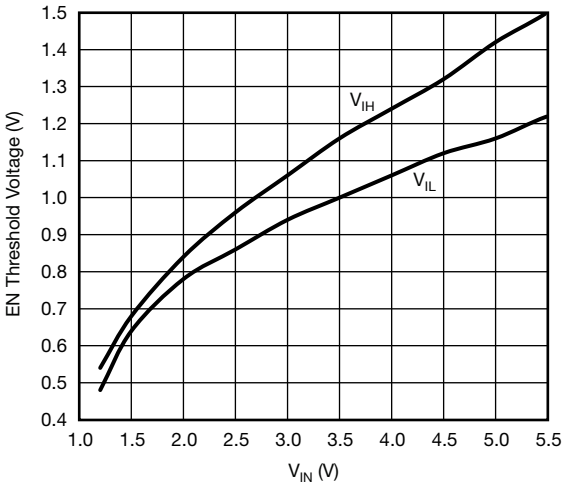



**Fig. 15 - EN Threshold Voltage vs. Input Voltage**

**TYPICAL CHARACTERISTICS** (internally regulated, 25 °C, unless otherwise noted)

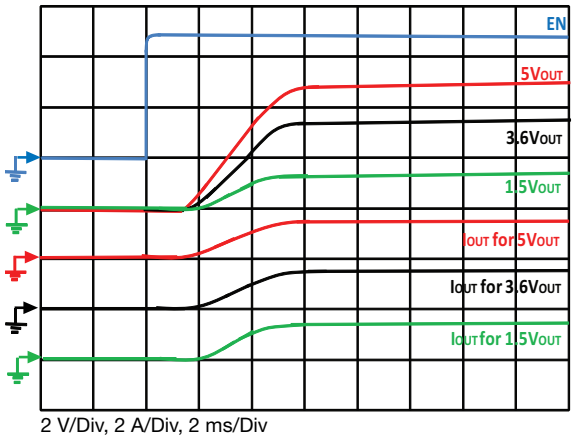



**Fig. 18 - Typical Turn-on Delay, Rise Time**
**$C_{OUT}$ = 0.1 µF, $C_{IN}$ = 4.7 µF, $I_{OUT}$ = 1.5 A**

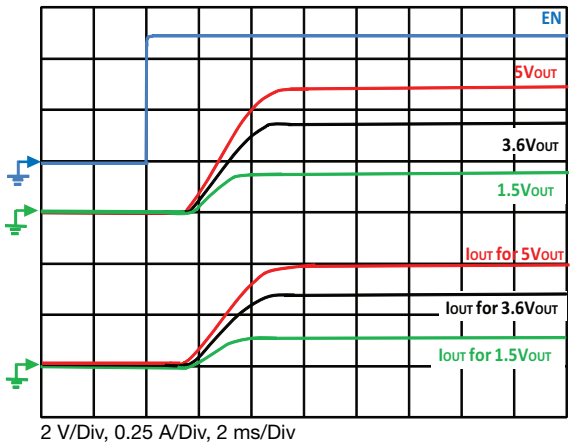



**Fig. 19 - Typical Turn-on Delay, Rise Time**
**$C_{OUT}$ = 0.1 µF, $C_{IN}$ = 4.7 µF, $R_{OUT}$ = 10 Ω**

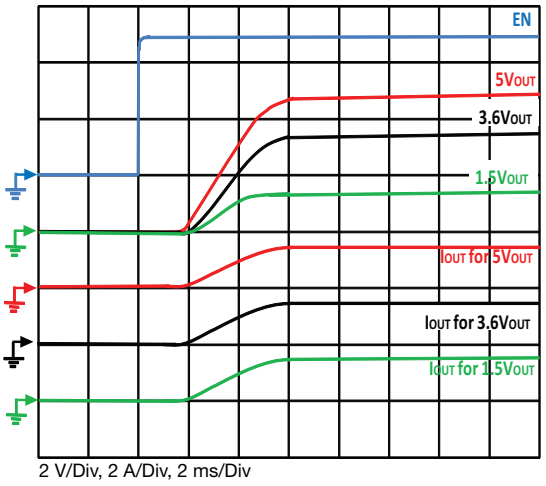



**Fig. 20 - Typical Turn-on Delay, Rise Time**
**$C_{OUT}$ = 200 µF, $C_{IN}$ = 4.7 µF, $I_{OUT}$ = 1.5 A**

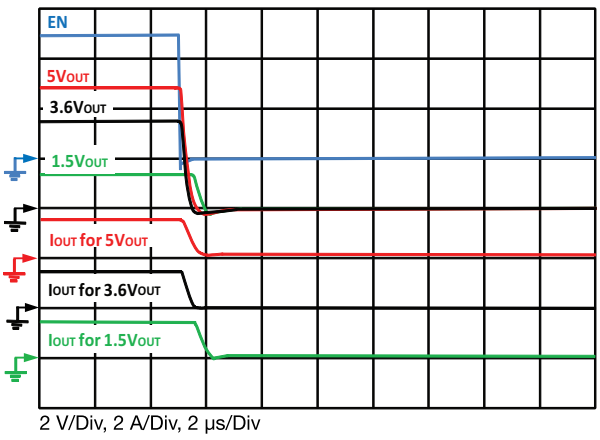



**Fig. 21 - Typical Fall Time**
**$C_{OUT}$ = 0.1 µF, $C_{IN}$ = 4.7 µF, $I_{OUT}$ = 1.5 A**

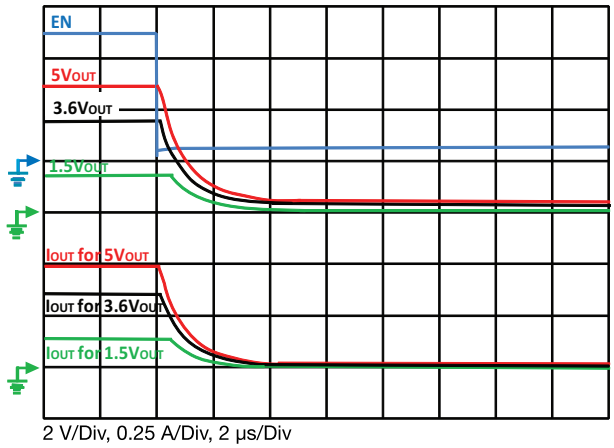



**Fig. 22 - Typical Fall Time**
**$C_{OUT}$ = 0.1 µF, $C_{IN}$ = 4.7 µF, $R_{OUT}$ = 10 Ω**

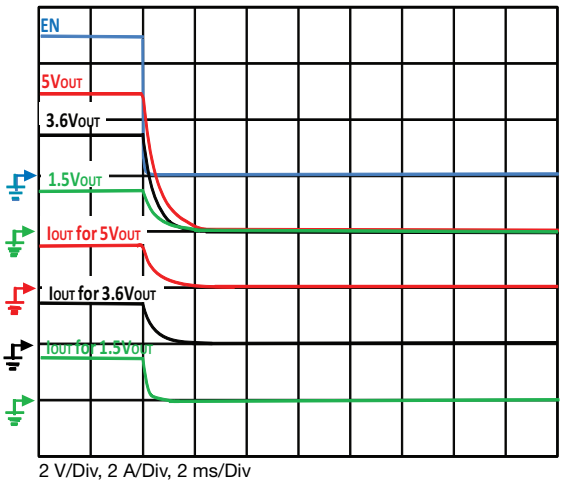



**Fig. 23 - Typical Fall Time**
**$C_{OUT}$ = 200 µF, $C_{IN}$ = 4.7 µF, $I_{OUT}$ = 1.5 A**

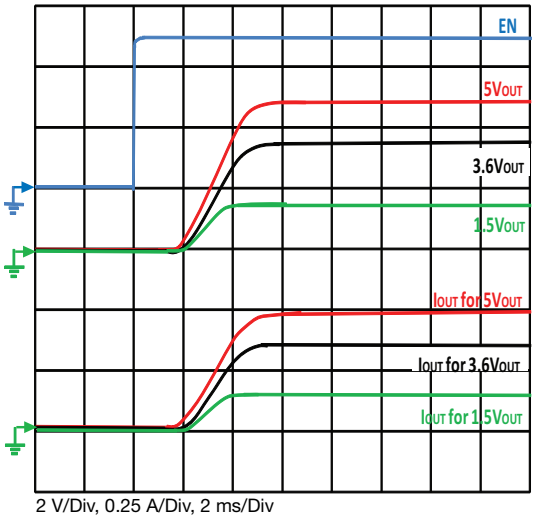



**Fig. 24 - Typical Turn-on Delay, Rise Time**
**$C_{OUT}$ = 200 µF, $C_{IN}$ = 4.7 µF, $R_{OUT}$ = 10 Ω**

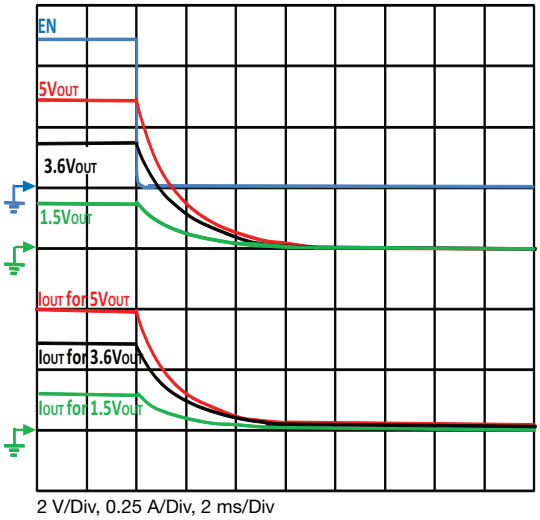



**Fig. 25 - Typical Fall Time**
**$C_{OUT}$ = 200 µF, $C_{IN}$ = 4.7 µF, ROUT = 10 Ω**

## BLOCK DIAGRAM

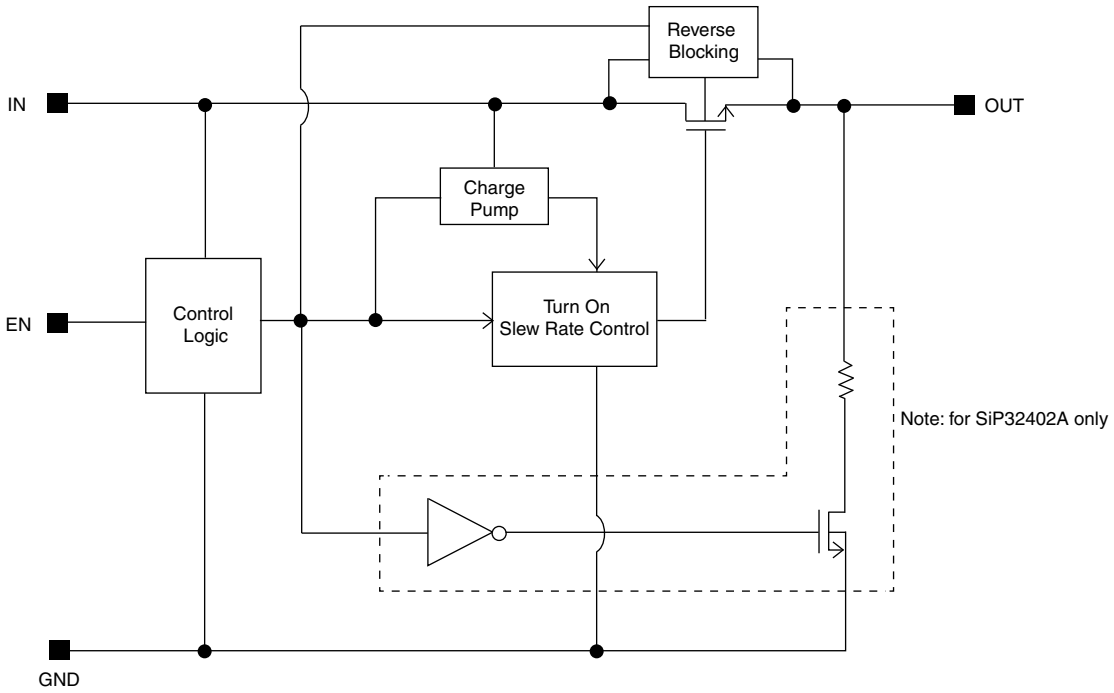
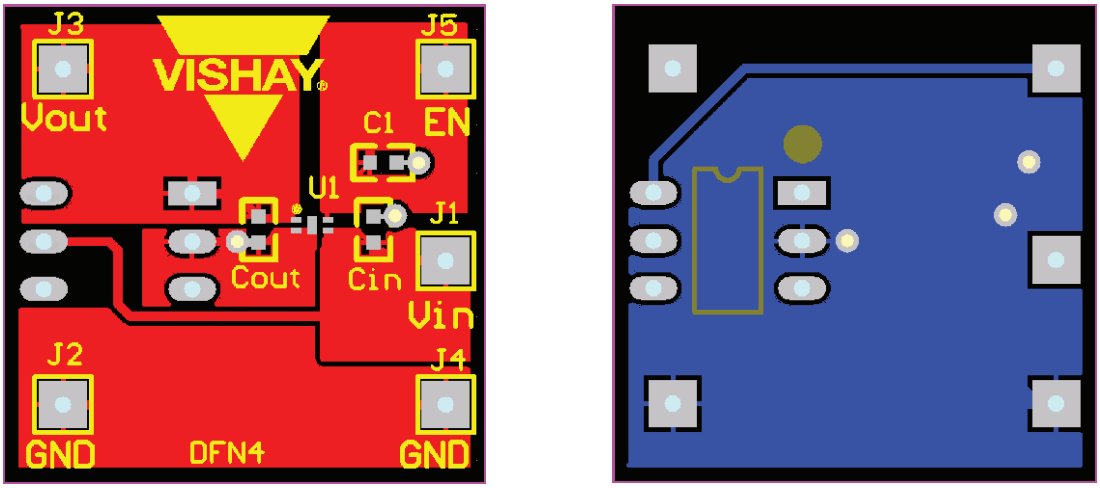



**Fig. 26 - Functional Block Diagram**

## PCB LAYOUT




Top Bottom

**Fig. 27 - PCB Layout for TDFN4 1.2 mm x 1.6 mm (type: FR4, size: 1" x 1", thickness: 0.062", copper thickness: 2 oz.)**

## DETAILED DESCRIPTION

SiP32401A and SiP32402A are advanced slew rate controlled high side load switch consisted of a n-channel power switch. When the device is enable the gate of the power switch is turned on at a controlled rate to avoid excessive in-rush current. Once fully on the gate to source voltage of the power switch is biased at a constant level. The design gives a flat on resistance throughout the operating voltages. When the device is off, the reverse blocking circuitry prevents current from flowing back to input if output is raised higher than input. The reverse blocking mechanism also works in case of no input applied. The SiP32402A also integrates an output discharge switch which allows fast output discharge.

## APPLICATION INFORMATION

### Input Capacitor

The SiP32401A and SiP32402A do not require an input capacitor. To limit the voltage drop on the input supply caused by transient inrush currents, an input bypass capacitor is recommended. A 2.2 µF ceramic capacitor placed as close to the $V_{IN}$ and GND should be enough. Higher values capacitor can help to further reduce the voltage drop. Ceramic capacitors are recommended for their ability to withstand input current surge from low impedance sources such as batteries in portable devices.

### Output Capacitor

While these devices works without an output capacitor, an 0.1 µF or larger capacitor across $V_{OUT}$ and GND is recommended to accommodate load transient condition. It also help to prevent parasitic inductance forces $V_{OUT}$ below GND when switching off. Output capacitor has minimal affect on device's turn on slew rate time. There is no requirement on capacitor type and its ESR.

### Enable

The EN pin is compatible with both TTL and CMOS logic voltage levels.

### Protection Against Reverse Voltage Condition

Both SiP32401A and SiP32402A contain reverse blocking circuitry to protect the current from going to the input from the output in case where the output voltage is higher than the input voltage when the main switch is off. Reverse blocking works for input voltage as low as 0 V.

### Thermal Considerations

SiP32401A and SiP32402A are designed to maintain a constant output load current. Due to physical limitations of the layout and assembly of the device the maximum switch current is 2.8 A, as stated in the Absolute Maximum Ratings table. However, another limiting characteristic for the safe operating load current is the thermal power dissipation of the package. To obtain the highest power dissipation (and a thermal resistance of 170 °C/W) the power pad of the device should be connected to a heat sink on the printed circuit board. Figure 23 shows a typical PCB layout. All copper traces and vias for the IN and OUT pins should be sized adequately to carry the maximum continuous current.

The maximum power dissipation in any application is dependant on the maximum junction temperature, $T_J$ (max.) = 125 °C, the junction-to-ambient thermal resistance for the TDFN4 1.2 mm x 1.6 mm package, $\theta_{J-A}$ = 170 °C/W, and the ambient temperature, $T_A$, which may be formulaically expressed as:

$$P\ (max.) = \frac{T_J\ (max.) - T_A}{\theta_{J-A}} = \frac{125 - T_A}{170}$$

It then follows that, assuming an ambient temperature of 70 °C, the maximum power dissipation will be limited to about 324 mW.

So long as the load current is below the 2.8 A limit, the maximum continuous switch current becomes a function of two things: the package power dissipation and the $R_{DS(on)}$ at the ambient temperature.

As an example let us calculate the worst case maximum load current at $T_A$ = 70 °C. The worst case $R_{DS(on)}$ at 25 °C occurs at an input voltage of 1.2 V and is equal to 76 mΩ. The $R_{DS(on)}$ at 70 °C can be extrapolated from this data using the following formula:

$R_{DS(on)}$ (at 70 °C) = $R_{DS(on)}$ (at 25 °C) x (1 + $T_C$ x DT)

Where $T_C$ is 4250 ppm/°C. Continuing with the calculation we have

$R_{DS(on)}$ (at 70 °C) = 76 mΩ x (1 + 0.00425 x (70 °C - 25 °C)) = 90.5 mΩ

The maximum current limit is then determined by

$$I_{LOAD}\,(max.) < \sqrt{\frac{P\,(max.)}{R_{DS(on)}}}$$

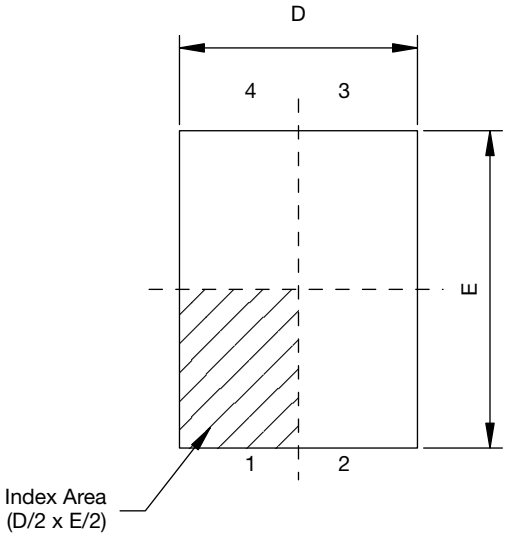
which in case is 1.9 A. Under the stated input voltage condition, if the 1.9 A current limit is exceeded the internal die temperature will rise and eventually, possibly damage the device.

**Recommended Board Layout**

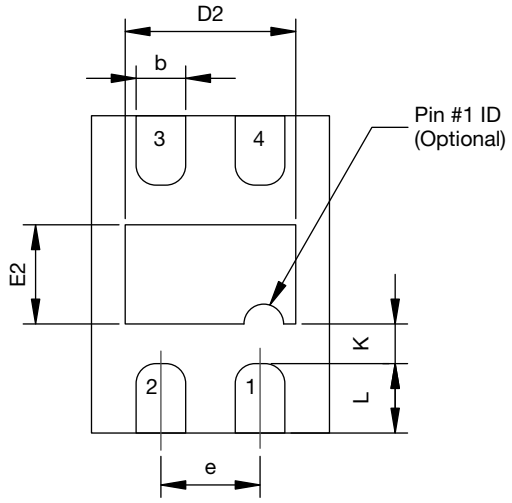
For the best performance, all traces should be as short as possible to minimize the inductance and parasitic effects. The input and output capacitors should be kept as close as possible to the input and output pins respectively. Connecting the central exposed pad to GND, using wide traces for input, output, and GND help reducing the case to ambient thermal impedance.

*Vishay Siliconix maintains worldwide manufacturing capability. Products may be manufactured at one of several qualified locations. Reliability data for Silicon Technology and Package Reliability represent a composite of all qualified locations. For related documents such as package/tape drawings, part marking, and reliability data, see www.vishay.com/ppg?63705.*

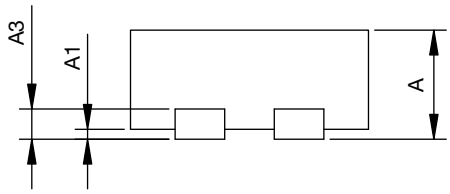
# TDFN4 1.2 x 1.6 Case Outline




Top View




Bottom View



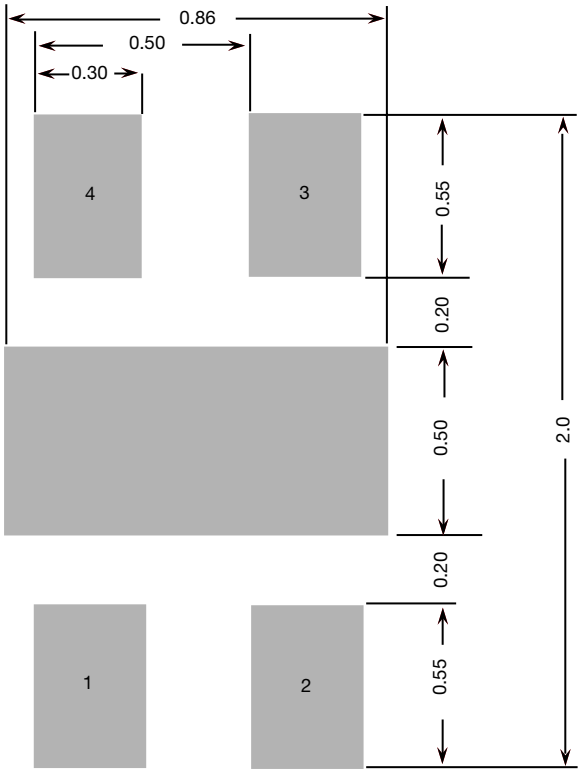

Side View

| DIM. | MILLIMETERS | | | INCHES | | |
|---|---|---|---|---|---|---|
| | MIN. | NOM. | MAX. | MIN. | NOM. | MAX. |
| A | 0.45 | 0.55 | 0.60 | 0.017 | 0.022 | 0.024 |
| A1 | 0.00 | - | 0.05 | 0.00 | - | 0.002 |
| A3 | 0.15 REF. or 0.127 REF. (1) | | | 0.006 or 0.005 (1) | | |
| b | 0.20 | 0.25 | 0.30 | 0.008 | 0.010 | 0.012 |
| D | 1.15 | 1.20 | 1.25 | 0.045 | 0.047 | 0.049 |
| D2 | 0.81 | 0.86 | 0.91 | 0.032 | 0.034 | 0.036 |
| e | 0.50 BSC | | | 0.020 | | |
| E | 1.55 | 1.60 | 1.65 | 0.061 | 0.063 | 0.065 |
| E2 | 0.45 | 0.50 | 0.55 | 0.018 | 0.020 | 0.022 |
| K | 0.25 typ. | | | 0.010 typ. | | |
| L | 0.25 | 0.30 | 0.35 | 0.010 | 0.012 | 0.014 |
| ECN: T16-0143-Rev. C, 18-Apr-16<br>DWG: 5995 | | | | | | |

**Note**

(1) The dimension depends on the leadframe that assembly house used.

## RECOMMENDED MINIMUM PADS FOR TDFN4 1.2 x 1.6




Recommended Minimum Pads
Dimensions in mm

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