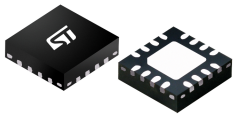
STEC01

Datasheet

Ground path safety switch with programmable timers



Features

- Input voltage range from 2.2 to 5 V
- 12 mΩ typ. N-channel FET $R_{DS(on)}$
- 7 A continuous current capability
- PWM control signal from 4 Hz to 5 kHz, with 30% to 100% duty cycle
- 30 µA battery supply current
- 2 programmable timers: T1, T3
- 1 fixed timer T2
- Input undervoltage lockout
- VFQFPN 3x3x0.9 16L, 0.5 mm pitch package

Applications

- Electronic cigarettes
- Timing/reset circuitry
- Ground path protection circuitry

Description

The STEC01 is an integrated programmable 12 mΩ power switch managed by the timer based circuitry.

The device has 3 timers designed to interrupt the ground path of a power application after a maximum on-time and inhibits the restart of the platform during a cooling window. The maximum on-time can be set from few seconds to hundreds of seconds, while the cooling window can be programmed to 69, 345 and 1380 seconds.

3 multi-level input pins, combined with a programmable oscillator and a fixed oscillator, are used to set the timing.

An input continuous or pulsed signal applied to the PWM pin starts the internal logic and counters. In case of a normal operation, as soon as the activity on the PWM pin stops, the device automatically enters idle mode, waiting for a new valid PWM signal to be applied. If the device detects a fault condition, a reset pulse is generated and the safety MOSFET is turned off and managed according to a predefined state machine.

The STEC01 has a continuous current capability up to 7 A through the internal power MOSFET. A higher current can be supported by using an external power transistor driven through GDRV pin.

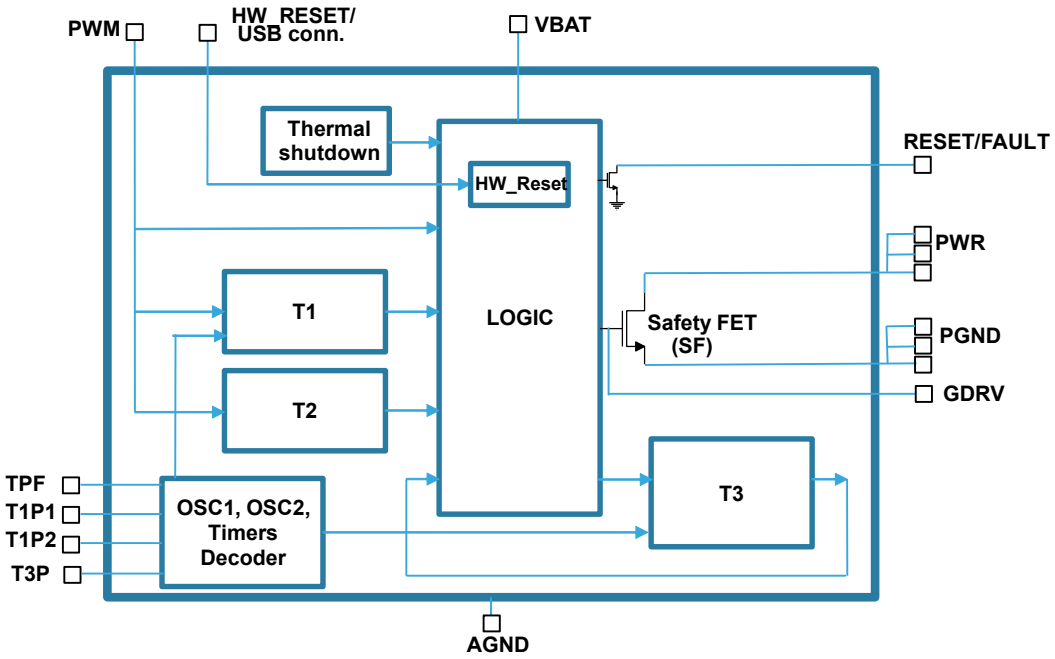
A rising edge on the HW_RESET input pin generates a 57 ms pulse on the RESET_FAULT pin. This function can be used to notify the connection of an external power source (e.g. USB).

Product status link
STEC01

Product summary	
Order code	STEC01PUR
Package	VFQFPN 3x3x0.9 16L

1 Block diagram

Figure 1. Block diagram



2 Pin configuration

Figure 2. **Pin configuration**

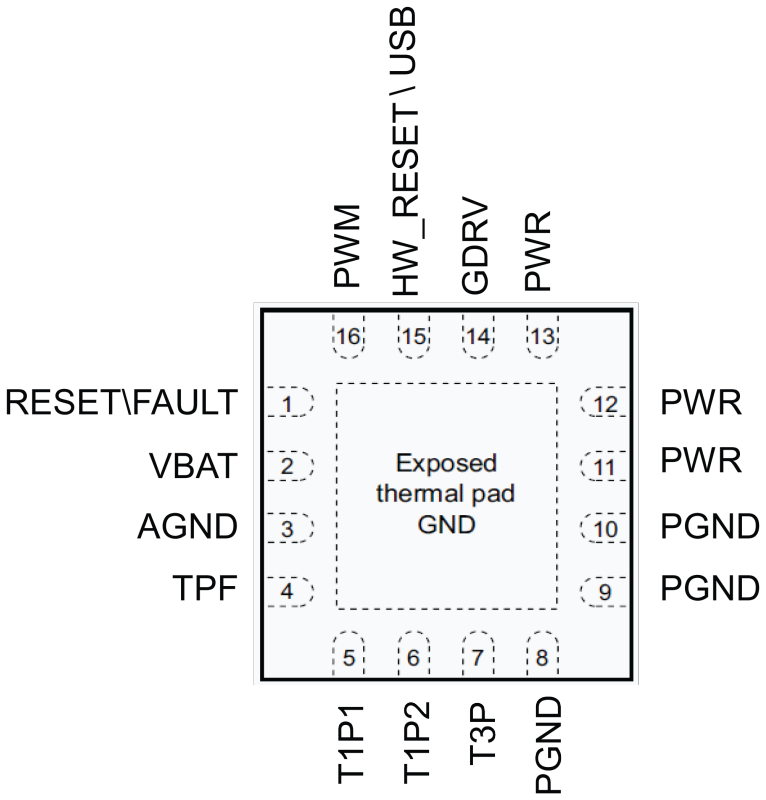


Table 1. **Pin configuration**

Symbol	Pin	Description
RESET\FAULT	1	Open drain output, active low. It generates a 57 ms pulse if a fault condition is detected or when HW_RESET\USB is pulled high
VBAT	2	Battery supply voltage. Bypass this pin to GND with a 1 µF ceramic capacitor
AGND	3	Analog GND. Connect it to a dedicated ground path
TPF	4	T1 oscillator programming pin. Connect a resistor to GND, to achieve a frequency ranging from 100 kHz to 400 kHz
T1P1	5	T1 timer programming pin. Connect to VBAT, GND or floating to select T1 prescaler (hard wired). See Figure 5. Timer configuration truth table
T1P2	6	
T3P	7	T3 timer programming pin. Connect to VBAT, GND or floating (hard wired). See Figure 5. Timer configuration truth table
PGND	8, 9, 10	Power ground (internal N-channel power MOS source terminal)
PWR	11, 12, 13	Input power voltage (internal N-channel power MOS drain terminal)
GDRV	14	Gate driver output. Leave floating if it is not used
HW_RESET\USB	15	Input hardware reset. Do not leave floating. If it is not used, put to GND
PWM	16	Input control signal, 4 Hz to 5 kHz, 30%-100% duty cycle
GND	EXP	Exposed pad, connect to thermal ground plane

3 Typical application diagram

Figure 3. Typical application diagram, I_{load} up to 7 A

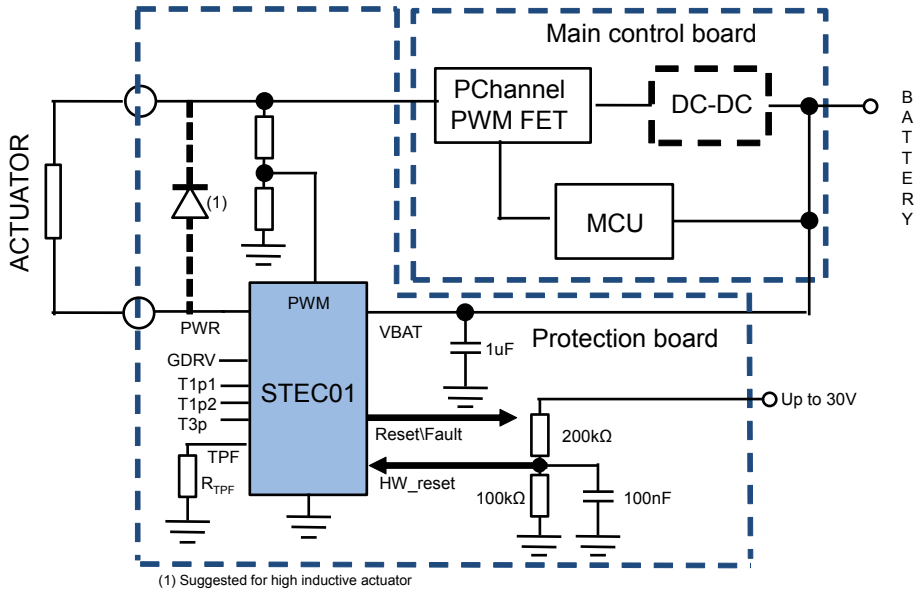
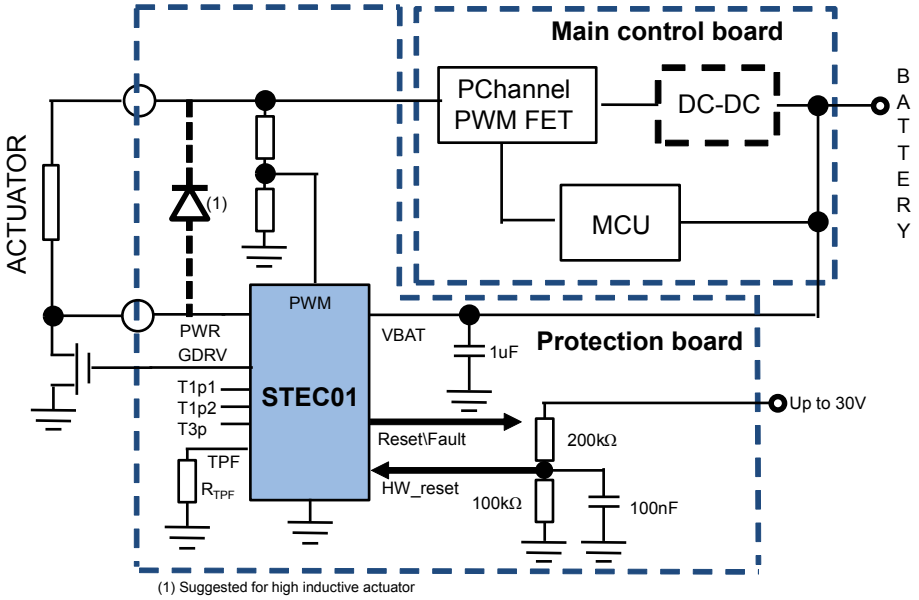


Figure 4. Typical application diagram, I_{load} > 7 A, external MOSFET



4 Maximum ratings

Table 2. Absolute maximum ratings

Symbol	Parameter	Value	Unit
VBAT	Supply voltage pin to AGND	-0.3 to 6	V
PWM	PWM input signal to AGND	-0.3 to 11.5	V
T1P1,T1P2 ,T3P	Timing setting pins to AGND	-0.3 to VBAT+0.3	V
TPF	T1 oscillator programming pin to AGND	-0.3 to 1.8	V
HW_RESET	Hardware reset pin to AGND	-0.3 to 11.5	V
RESET/FAULT	Open drain pin to PGND	-0.3 to 6	V
GDRV	Gate driver pin to PGND	-0.3 to VBAT+0.3	V
PWR	Input power voltage pin to PGND	-0.3 to 11.5	V
IPWR	DC N-channel power MOSFET current	7	A
$T_{J\text{-}MAX}$	Maximum junction temperature	150	°C
T_{STG}	Storage temperature	-55 to 150	°C

Table 3. Thermal data

Symbol	Parameter	Value	Unit
R_{thja}	Thermal resistance, junction-to-ambient	42	°C/W
R_{thjc}	Thermal resistance, junction-to-case	5	°C/W

Note: thermal test board JESD51-7, 4-layer PCB (2s2p)

5 Electrical characteristics

T_A = 25 °C, VBAT = 3.7 V, C_{BAT} = 1 µF, T1P1=T1P2=GND, R_{TPF} = 100 kΩ, T3P = GND, unless otherwise specified.

Table 4. Electrical characteristics

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
VBAT	Supply voltage range		2.2		5	V
V_{UVLO}	Undervoltage lockout	Turn-on, voltage rising, T_A from -40 to 85 °C	1.7	1.9	2.2	V
V_{Hyst}	UVLO hysteresis	VBAT falling		0.05		V
t_{BATT_PWM}	VBAT valid to PWM time	VBAT rising above UVLO then PWM rising		1	3.5	ms
V_{PWM}	PWM input voltage range	T_A from -40 to 85 °C	1		10	V
V_{IL_MAX}	PWM threshold	T_A from -40 to 85 °C			0.3	V
V_{IH_MIN}			0.9			
PWM_HysT	PWM hysteresis			0.006	0.05	
F_{PWM}	PWM operating frequency	(1)	4		5000	Hz
t_{PWM_HI}	PWM minimum high time		40			µs
$R_{DS(on)}$	Internal power MOSFET on-resistance	VBAT = 2.5 V, I_{PWR}=1 A		12		mΩ
		VBAT = 3 V, I_{PWR}=1 A		11.3		
		T_A from -40 to 85 °C, VBAT=>2.5 V I_{PWR}=1 A			20	
I_{L_PWR}	NFET leakage current	PWR=10 V, fault condition			1.5	µA
I_{BATT}	Battery supply current	VBAT from 2.2 to 5 V, active mode		30		µA
I_{BATT_IDLE}	Idle battery current	IC in idle-mode		2	4	µA
		IC in idle-mode, T_A from -40 to 85 °C			10	
R_{GDRV_H}	Gate drive high resistance	IGDRV=5 mA, PWM=high, T1 and T2 not expired		30		Ω
R_{GDRV_L}	Gate drive low resistance	IGDRV=-5 mA, IC idle or in fault mode		8		
V_{HW_RESET}	Hardware reset threshold	T_A from -40 to 85 °C	0.3		0.9	V
I_{HW_RESET}	Hardware reset leakage	T_A from -40 to 85 °C, V_{HW_RESET}=10 V			1	µA
$t_{HW\_RESET\_dl}$	Hardware reset deglitch time			10		ms
$V_{RESET/FAULT}$	VOL_MAX	I_{RESET}=2 mA, fault condition, T_A from -40 to 85 °C			0.2	V
$I_{RESET/FAULT}$	Reset leakage current	$V_{RESET/FAULT}$=5 V, T_A from -40 to 85 °C			1	µA
t_{PW_RESET}	Reset pulse width		50	57	66	ms
V_{PT}	Programming threshold pins VIL, input logic low	Applies to T1P1, T1P2, T3P			0.2	V

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
V_{PT}	Programming threshold pins VIH, input logic high	Applies to T1P1, T1P2, T3P	1.9			V
I_{PT}	Programming input pins leakage current	Applies to T1P1, T1P2, T3P. VPT=5 V			1	µA
T1	Timer accuracy	T1P1,T1P2=GND, R_{TPF} =91 kΩ	4	5	6	s
T2			0.250	0.285	0.330	
T3		T3P=GND	60	69	80	
OTP	Overtemperature protection	PWR OFF		160		°C
OTP_HYST	OTP hysteresis	PWR ON		20		

1. *Guaranteed by design.*

Figure 5. Timer configuration truth table

T1p1	T1P2	Prescaler	T1 [s]
0	0	x1	5 - 20
Floating	0	x4	20 - 80
1	0	x16	80 - 320
0	1	x64	320 - 1280
Floating	1	x256	1280 - 5120
1	1	x1024	5120 - 20480
0	Floating	Do not use	
Floating	Floating		
1	Floating		

T2 [ms]
250

T3p	T3[s]
0	60
Floating	345
1	1380

Connect 100 kΩ 1% tolerance between R_{TPF} and GND to obtain minimum values
Connect 400 kΩ 1% tolerance between R_{TPF} and GND to obtain maximum values

Note: See Section 6.1 T1 timer settings for more details.

6 General description

The STEC01 is an integrated low-side 12 mΩ N-channel power MOSFET used to protect applications where a big amount of current flows from the battery to an actuator such as the heater inside an e-cigarette. The maximum on-time can be configured for the actuator with a range from 5 s to 20480 s. Once the set time expires, the actuator is disconnected from the GND path.

The device monitors the PWM activity and as soon as a rising edge is detected it exits the idle mode, turns the N-channel power MOSFET on to connect the actuator to the GND path and starts the setting on-time timer (T1). As soon as a falling edge on PWM is detected, a 285 ms timer (T2) is started and, if within such time no further PWM activity is recognized, the N-channel MOSFET is turned off and the device enters idle mode till a new PWM signal is detected (Figure 6. T1 vs R_{TPF}- prescaler x1). Depending on the user's application, the device works with a continuous or pulsed PWM signal.

If, for any reason, the PWM duration is longer than the value set for timer T1, a fault event is detected, the N-channel MOSFET is turned off and a fault signal is generated. In order to exit fault mode, a stable low voltage level on the PWM pin is required. Once the PWM goes low, T2 starts counting about 250 ms to make sure the fault has been removed and as soon as it expires, the T3 timer is started. Timer T3 sets the cooling window during which any new activity on the PWM pin is ignored and the internal N-channel power MOSFET is kept OFF (T3 can be programmed to 69 s, 345 s or 1380 s). Once T3 expires, a new power cycle can be started by a valid PWM signal.

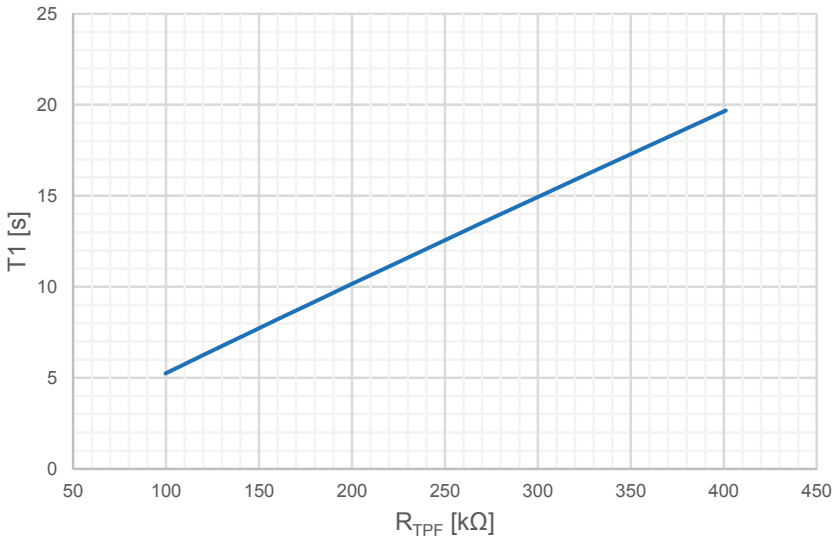
The STEC01 is able to manage a continuous current up to 7 A through the internal power MOSFET. A higher current can be supported by using an external N-channel power MOSFET driven through GDRV pin.

A rising edge on the HW_RESET input pin generates a 57 ms pulse on the RESET_FAULT pin that can be detected by a dedicated MCU GPIO. This function can be used to notify the connection of an external power source (e.g. USB).

6.1 T1 timer settings

Figure 6. T1 vs R_{TPF}- prescaler x1 reports the typical T1 curve vs setting resistor R_{TPF} when the prescaler x1 is selected. It allows the user to set T1 from 5 s to 20 s as reported in Figure 5. Timer configuration truth table.

Figure 6. T1 vs R_{TPF}- prescaler x1



For a longer setting time, please refer to the example below:

The typical example of R_{TPF} calculation to obtain T1=6 minutes (3600 s): select the x256 pre-scaler (according to the ranges reported in Figure 5. Timer configuration truth table, by keeping T1P1 floating and T1P2=1. Divide 3600 s by selected pre-scaler value (256) and obtain 14.06 s that in the graph above corresponds to R_{TPF} = 280 kΩ.

6.2 Timer expiration: normal mode

Figure 7. Normal power cycle shows a typical power cycle not triggering a fault condition. In this example a PWM signal with duty cycle lower than 100% is applied to also show T2 timer functionality but a 100% duty cycle can be used as well.

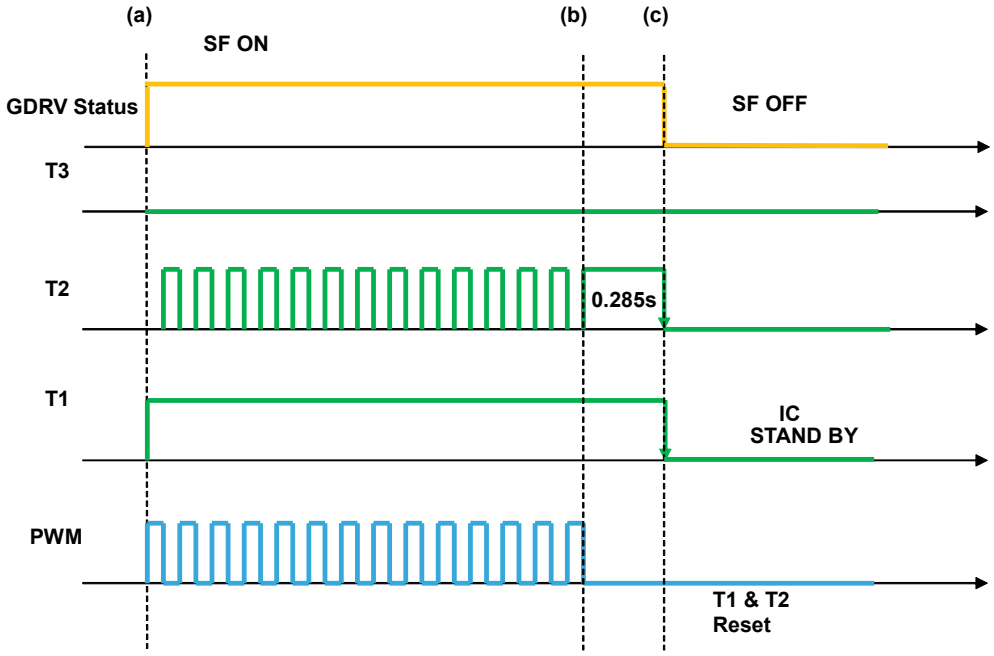
When a rising edge on the PWM input pin is detected (a), T1 is started, the internal power MOSFET is turned on and the external gate drive pin is activated. As soon as a falling edge of the PWM signal is detected, T2 is started. The purpose of T2 is to detect the end of the power cycle. After the power cycle starts, every high level of the PWM signal resets T2.

If the PWM signal is in line with requirements (4 Hz < f_{PWM} <5 kHz, duty cycle >30%), its low time is always lower than 285 ms (typ., T2 fixed value) and T2 never expires till the end of the power cycle (b). T2 is started and reset at each PWM period.

After the power cycles ends, the voltage at PWM input remains low for more than 285 ms causing the expiration of T2 (c). When T2 expires, the internal N-channel power MOSFET is turned off, the GDRV output is deactivated and the device enters idle mode (low power consumption mode) during which it keeps monitoring the PWM line waiting for a new cycle to start.

In this example the time duration of the full power cycle (a to c) is lower than the maximum on-time programmed for T1.

Figure 7. Normal power cycle



a) Start on first PWM rising edge. Global reset

b) 8 s elapsed, PWM stops toggling

c) T2 expires, T1/T2 are reset, IC goes to idle mode, ready for next PWM cycle

6.3 T1 timer expiration: fault mode

Figure 8. T1 expiration, fault mode shows an example of platform failure triggering the protection function of the IC. In this case, the power control unit keeps generating the power PWM signal for a time longer than expected.

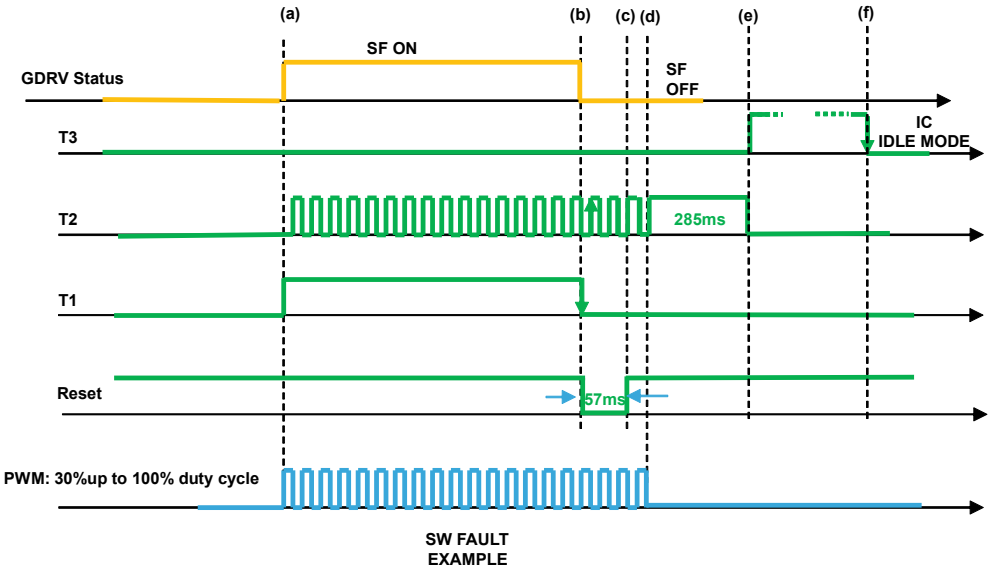
As per previous case, the device exits idle mode, starts T1, turns on the internal N-channel power MOSFET and activates the GDRV output as soon as a rising edge on PWM is detected (a).

The PWM signal keeps commutating for more than the maximum programmed on-time causing T1 to expire and making the device enter fault mode (b).

In fault mode, the internal power MOSFET is turned off, the GDRV output is deactivated, a reset pulse on the RESET/FAULT pin is generated and the device starts waiting for the fault condition to be removed. The condition to exit fault mode is a low voltage level at the PWM pin for more than T2 ((d) to (e), 285 ms typ.). When the fault removal is detected (e), T3 timer is started. During T3 (cooling window), any activity on the PWM line is ignored and the power MOSFETs (both internal or external if used) are kept off to let the application cool down.

After T3 expires, the device enters again idle mode and is ready for a new cycle.

Figure 8. T1 expiration, fault mode



a) Global reset on first PWM rising edge, T1 starts, SF ON

b) T1 expires, SF is turned OFF and 57 ms reset pulse is generated

c) 57 ms reset pulse ends

d) PWM stops toggling (or goes stable low) and T2 starts 285 ms timer

e) T2 expires and T3 starts

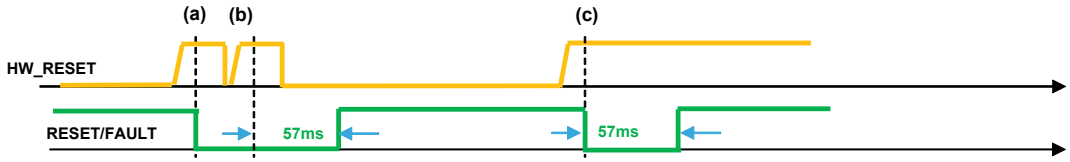
f) T3 expires, the device goes to idle mode and SF can be turned ON again if needed (by PWM rising edge)

6.4 HW_RESET functionality

The HW_RESET input can be used to monitor an input power line (e.g. USB) to notify the connection to the platform control unit.

When the signal on the HW_REST pin is more than V_{HW_RESET} threshold, after a deglitch time of the 10 ms (typ.), a 57 ms (typ.) pulse is generated on the RESET/FAULT output pin. If several pulses longer than the deglitch time are detected, during the RESET/FAULT low time, the pulse duration is extended (see events (a) and (b) in the example below).

Figure 9. HW_RESET input functionality



a) HW_RESET is higher than V_{HW_RESET} threshold for more than the deglitch time of 10 ms (typ.), a 57 ms reset fault pulse is generated

b) HW_RESET goes down and rises again above the V_{HW_RESET} threshold for more than the deglitch time, a new 50 ms reset fault signal is generated overlapping the previous one

c) HW_RESET is higher than V_{HW_RESET} threshold for more than deglitch time on rising edge and remains high

Note: A Schmitt trigger is used in the input stage of HW_RESET. If the HW_RESET is used for USB V_{Bus} line monitoring, during USB disconnection, in case of voltage bouncing, a reset might be generated.

7 Typical performance characteristics

Figure 10. $R_{DS(on)}$ vs VBAT, room temperature

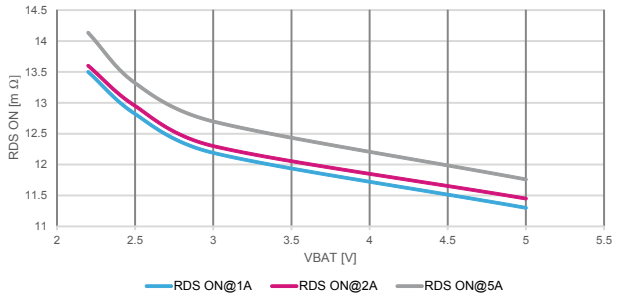


Figure 11. $R_{DS(on)}$ vs VBAT@-40 °C

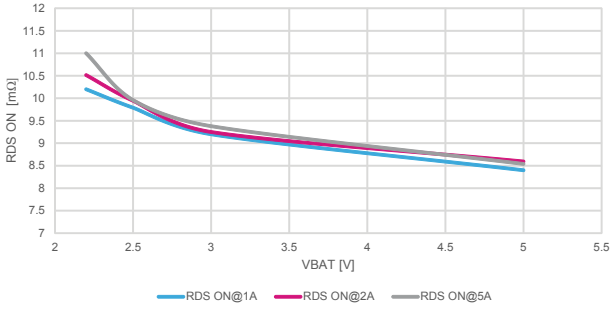


Figure 12. $R_{DS(on)}$ vs VBAT@-85 °C

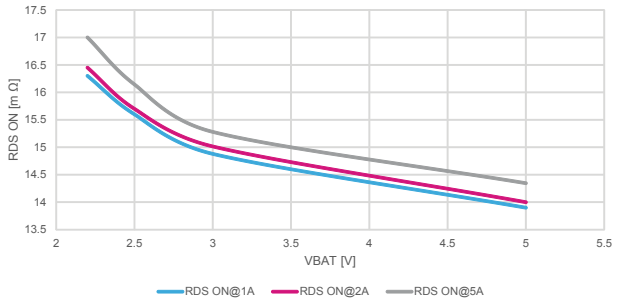


Figure 13. Reset pulse width: VBAT=3.7 V T1P1=T1P2=T3P=GND, ROSC=100 kΩ

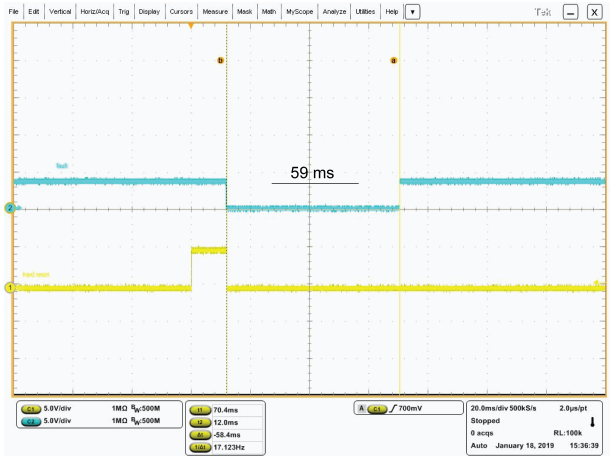


Figure 14. PWM V_{IH_MIN}: VBAT=3.7 V

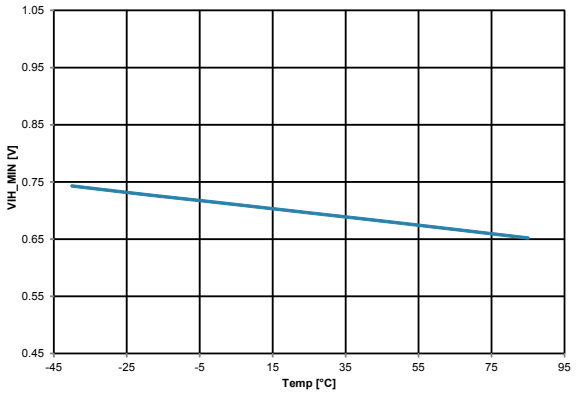


Figure 15. PWM V_{IL_MAX}: VBAT=3.7 V

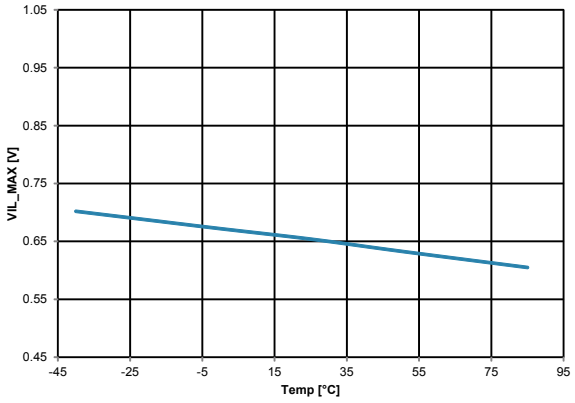


Figure 16. HW_RESET V_{IH_MIN}: VBAT=3.7 V

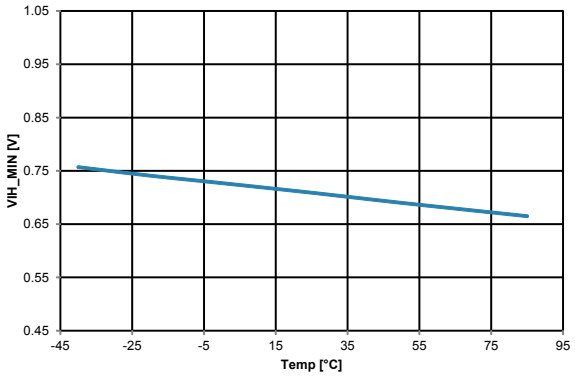


Figure 17. HW_RESET V_{IL_MAX}: VBAT=3.7 V

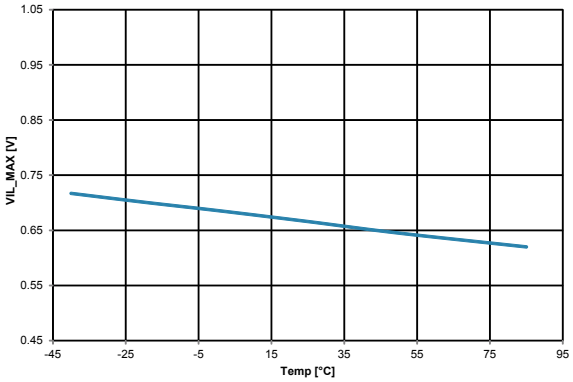


Figure 18. IBATT_ACTIVE: VBAT=3.7 V

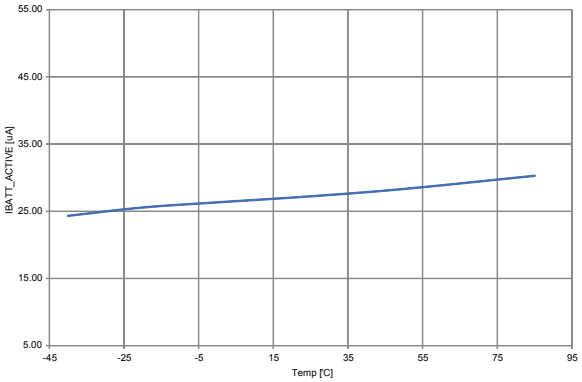


Figure 19. IBATT_IDLE: VBAT=3.7V

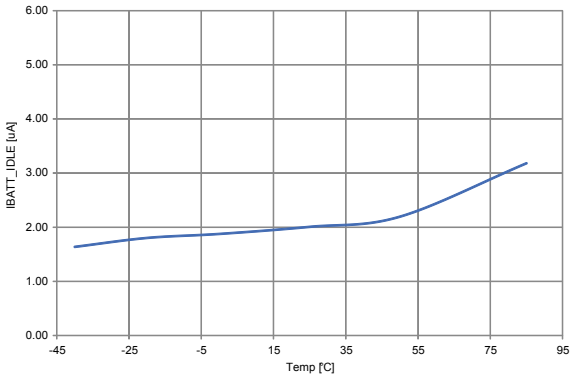


Figure 20. Leakage TxPy pin: V_{TxPY}@5 V

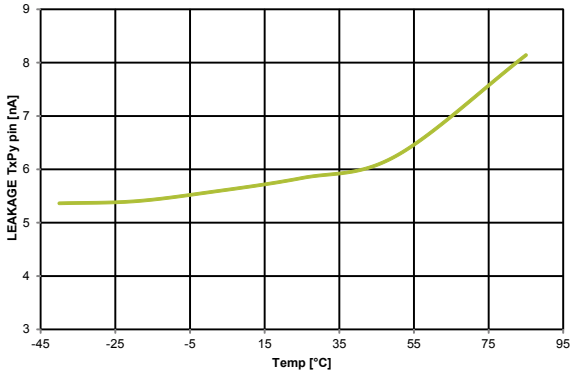
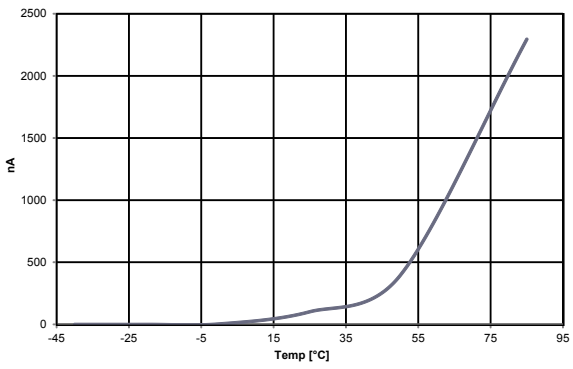


Figure 21. Leakage PWR: V_{PWR}@10 V



8 Package information

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK packages, depending on their level of environmental compliance. ECOPACK specifications, grade definitions and product status are available at: www.st.com. ECOPACK is an ST trademark.

8.1 VFQFPN 3x3x0.9 16L package information

Figure 22. **VFQFPN 3x3x0.9 package outline**

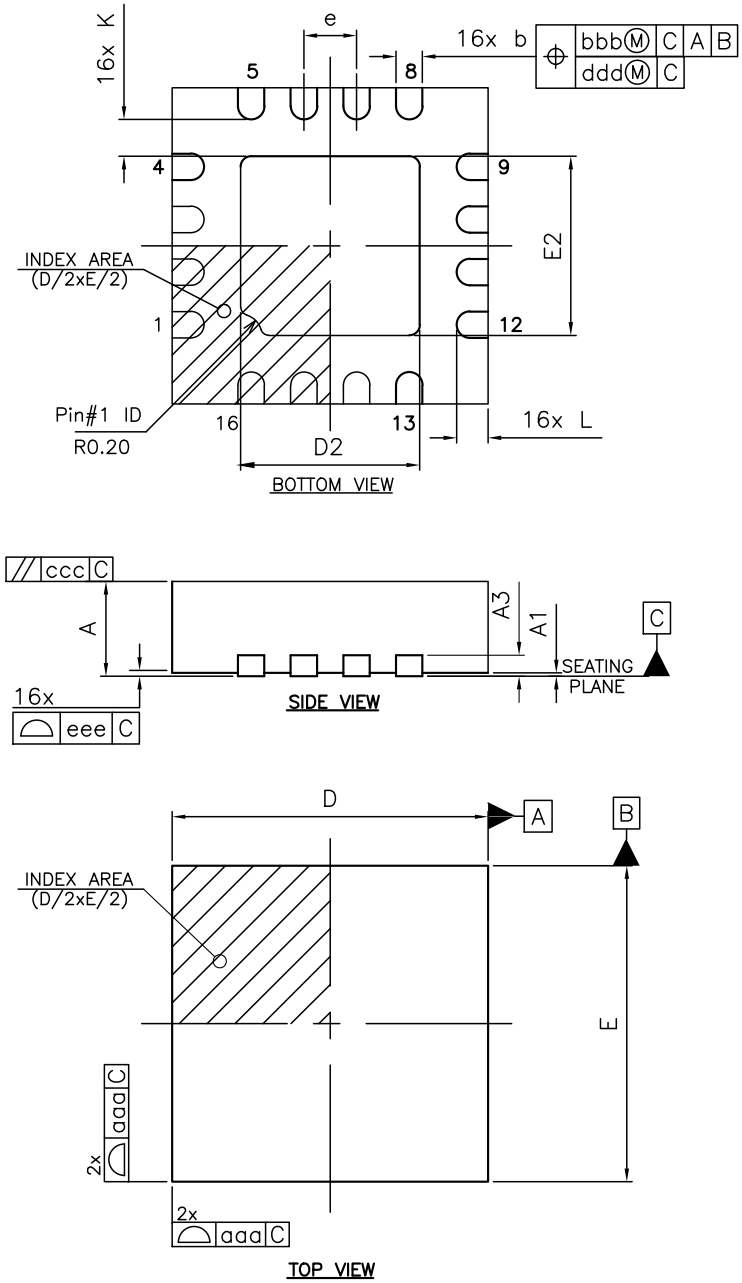
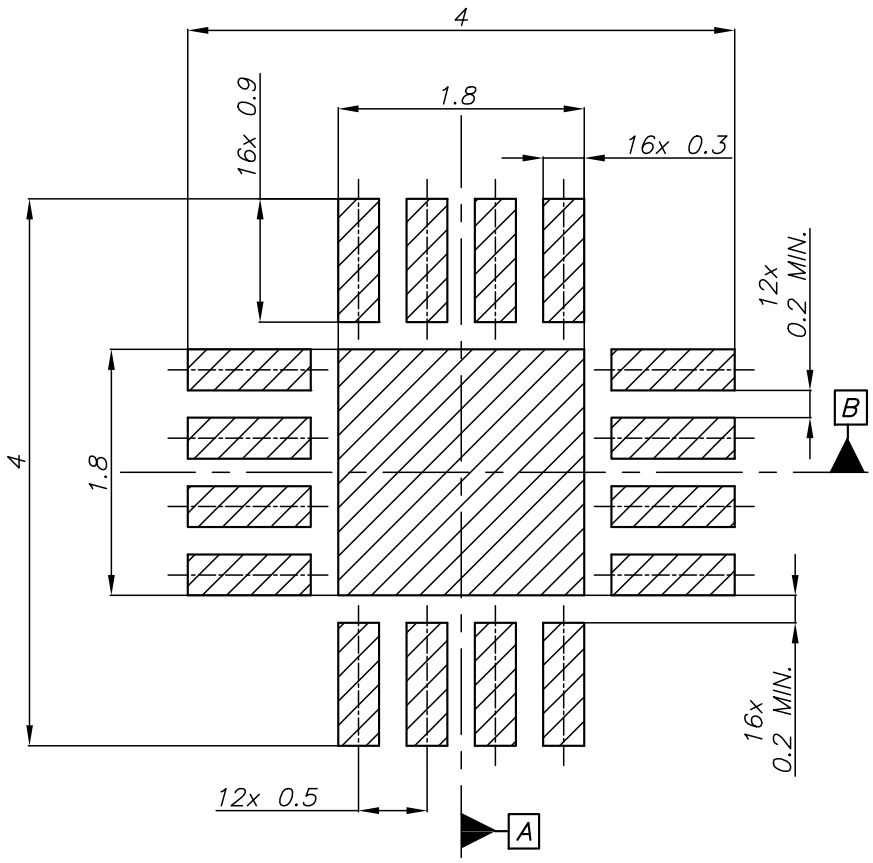


Table 5. VFQFPN 3x3x0.9 mechanical data

Symbol	Milimeters		
	Min	Typ	Max
A	0.80	0.90	1.00
A1	0	0.02	0.05
A3		0.20	
b	0.18	0.25	0.30
D		3.00	
D2	1.55	1.70	1.80
E		3.00	
E2	1.55	1.70	1.80
e		0.50	
L	0.20	0.30	0.40
K	0.20		
aaa		0.05	
bbb		0.10	
ccc		0.10	
ddd		0.05	
eee		0.08	

Note: VFQFPN - standard for thermally enhanced very thin fine pitch quad flat package no leads. The leads size is comprehensive of the thickness of the leads finishing material. Dimensions do not include mold protrusion, not to exceed 0,15 mm. Package outline exclusive of metal burr dimensions.

Figure 23. **VFQFPN 3x3x0.9 recommended footprint**



Revision history

Table 6. **Document revision history**

Date	Version	Changes
14-Jan-2020	1	Initial release.
20-Oct-2020	2	Updated Section 3 Typical application diagram and Table 2. Absolute maximum ratings.

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