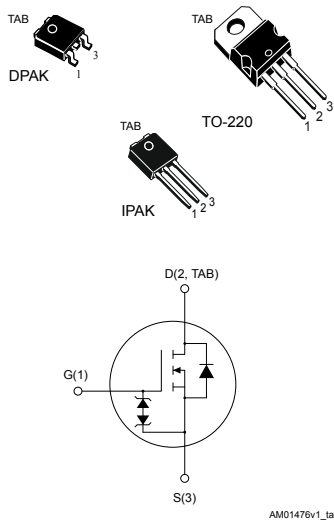


## N-channel 800 V, 0.95 $\Omega$ typ., 6 A MDmesh K5 Power MOSFETs in DPAK, TO-220 and IPAK packages



### Features

Order code	$V_{DS}$	$R_{DS(on) \text{ max}}$	$I_D$
STD7N80K5	800 V	1.2 $\Omega$	6 A
STP7N80K5			
STU7N80K5			

- Industry's lowest  $R_{DS(on)}$  x area
- Industry's best FoM (figure of merit)
- Ultra-low gate charge
- 100% avalanche tested
- Zener-protected

### Applications

- Switching applications

### Description

These very high voltage N-channel Power MOSFETs are designed using MDmesh K5 technology based on an innovative proprietary vertical structure. The result is a dramatic reduction in on-resistance and ultra-low gate charge for applications requiring superior power density and high efficiency.



#### Product status link

[STD7N80K5](#)
[STP7N80K5](#)
[STU7N80K5](#)

# 1 Electrical ratings

**Table 1. Absolute maximum ratings**

Symbol	Parameter	Value	Unit
$V_{GS}$	Gate- source voltage	$\pm 30$	V
$I_D$	Drain current (continuous) at $T_C = 25\text{ }^\circ\text{C}$	6	A
$I_D$	Drain current (continuous) at $T_C = 100\text{ }^\circ\text{C}$	3.8	A
$I_{DM}^{(1)}$	Drain current (pulsed)	24	A
$P_{TOT}$	Total power dissipation at $T_C = 25\text{ }^\circ\text{C}$	110	W
$I_{AR}$	Max current during repetitive or single pulse avalanche (pulse width limited by $T_{jmax}$ )	2	A
$E_{AS}$	Single pulse avalanche energy (starting $T_J = 25\text{ }^\circ\text{C}$ , $I_D = I_{AS}$ , $V_{DD} = 50\text{ V}$ )	88	mJ
$dv/dt^{(2)}$	Peak diode recovery voltage slope	4.5	V/ns
$di/dt^{(2)}$	Peak diode recovery current slope	100	A/ $\mu\text{s}$
$dv/dt^{(3)}$	MOSFET $dv/dt$ ruggedness	50	V/ns
$T_j$	Operating junction temperature range	-55 to 150	$^\circ\text{C}$
$T_{stg}$	Storage temperature range		$^\circ\text{C}$

1. Pulse width limited by safe operating area.
2.  $I_{SD} \leq 6\text{ A}$ ,  $V_{DS(peak)} \leq V_{(BR)DSS}$
3.  $V_{DS} \leq 640\text{ V}$

**Table 2. Thermal data**

Symbol	Parameter	Value			Unit
		DPAK	TO-220	IPAK	
$R_{thj-case}$	Thermal resistance junction-case	1.14			$^\circ\text{C/W}$
$R_{thj-amb}$	Thermal resistance junction-amb		62.5	100	$^\circ\text{C/W}$
$R_{thj-pcb}^{(1)}$	Thermal resistance junction-pcb	50			$^\circ\text{C/W}$

1. When mounted on 1 inch<sup>2</sup> FR-4, 2 Oz copper board.

## 2 Electrical characteristics

( $T_{CASE} = 25\text{ °C}$  unless otherwise specified).

**Table 3. On/off states**

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{(BR)DSS}$	Drain-source breakdown voltage	$V_{GS} = 0\text{ V}; I_D = 1\text{ mA}$	800			V
$I_{DSS}$	Zero gate voltage drain current	$V_{GS} = 0\text{ V}; V_{DS} = 800\text{ V}$			1	$\mu\text{A}$
		$V_{GS} = 0\text{ V}; V_{DS} = 800\text{ V}; T_c = 125\text{ °C}^{(1)}$			50	$\mu\text{A}$
$I_{GSS}$	Gate body leakage current	$V_{DS} = 0\text{ V}; V_{GS} = \pm 20\text{ V}$			$\pm 10$	$\mu\text{A}$
$V_{GS(th)}$	Gate threshold voltage	$V_{DS} = V_{GS}; I_D = 100\text{ }\mu\text{A}$	3	4	5	V
$R_{DS(on)}$	Static drain-source on-resistance	$V_{GS} = 10\text{ V}; I_D = 3\text{ A}$		0.95	1.2	$\Omega$

1. Defined by design, not subject to production test.

**Table 4. Dynamic**

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$C_{iss}$	Input capacitance	$V_{DS} = 100\text{ V}; f = 1\text{ MHz}; V_{GS} = 0\text{ V}$	-	360	-	pF
$C_{oss}$	Output capacitance		-	30	-	pF
$C_{riss}$	Reverse transfer capacitance		-	1	-	pF
$C_{o(tr)}^{(1)}$	Equivalent capacitance time related	$V_{GS} = 0\text{ V}; V_{DS} = 0\text{ to }640\text{ V}$	-	47	-	pF
$C_{o(er)}^{(2)}$	Equivalent capacitance energy related		-	20	-	pF
$R_G$	Intrinsic gate resistance	$f = 1\text{ MHz}; I_D = 0\text{ A}$	-	6	-	$\Omega$
$Q_g$	Total gate charge	$V_{DD} = 640\text{ V}; I_D = 6\text{ A}$	-	13.4	-	nC
$Q_{gs}$	Gate-source charge	$V_{GS} = 0\text{ to }10\text{ V}$	-	3.7	-	nC
$Q_{gd}$	Gate-drain charge	(see Figure 17. Test circuit for gate charge behavior)	-	7.5	-	nC

1. Time related is defined as a constant equivalent capacitance giving the same charging time as  $C_{oss}$  when  $V_{DS}$  increases from 0 to 80%  $V_{DSS}$

2. Energy related is defined as a constant equivalent capacitance giving the same stored energy as  $C_{oss}$  when  $V_{DS}$  increases from 0 to 80%  $V_{DSS}$

**Table 5. Switching times**

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$t_{d(on)}$	Turn-on delay time	$V_{DD} = 400\text{ V}$ , $I_D = 3\text{ A}$ , $R_G = 4.7\ \Omega$ , $V_{GS} = 10\text{ V}$ (see Figure 16. Test circuit for resistive load switching times and Figure 21. Switching time waveform)	-	11.3	-	ns
$t_r$	Rise time		-	8.3	-	ns
$t_{d(off)}$	Turn-off delay time		-	23.7	-	ns
$t_f$	Fall time		-	20.2	-	ns

**Table 6. Source drain diode**

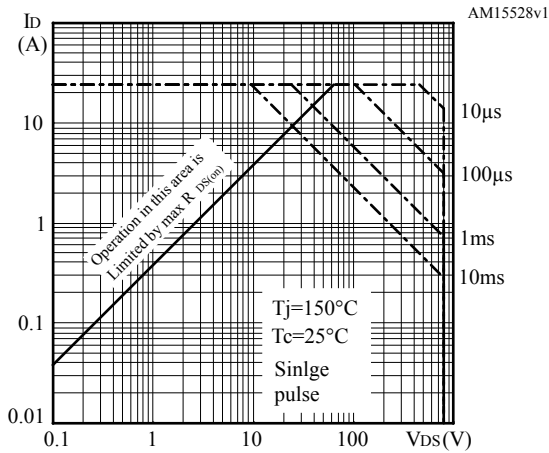
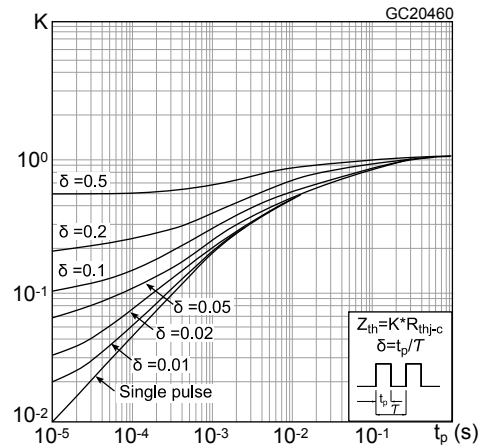
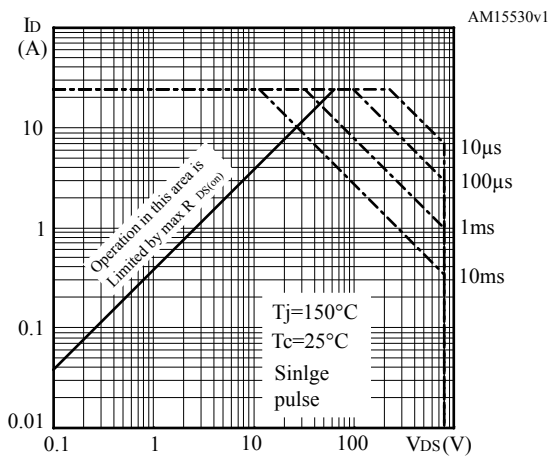
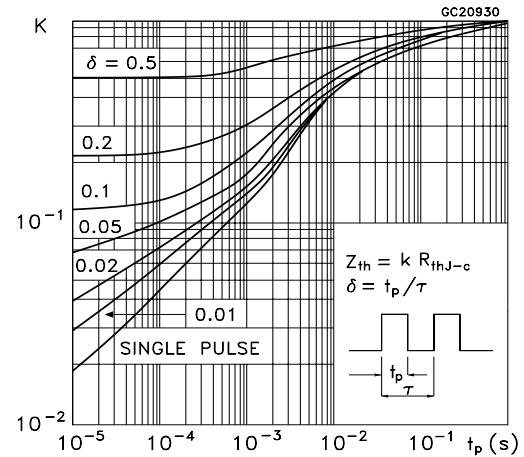
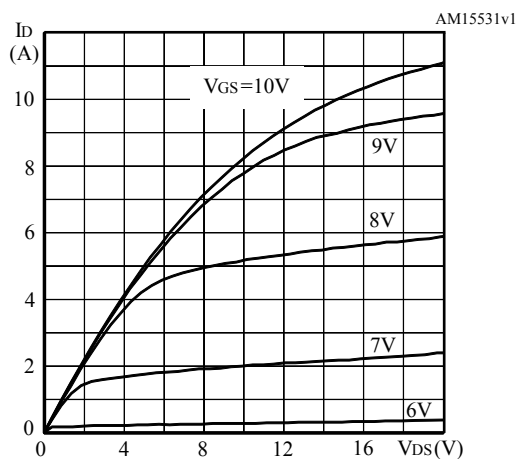
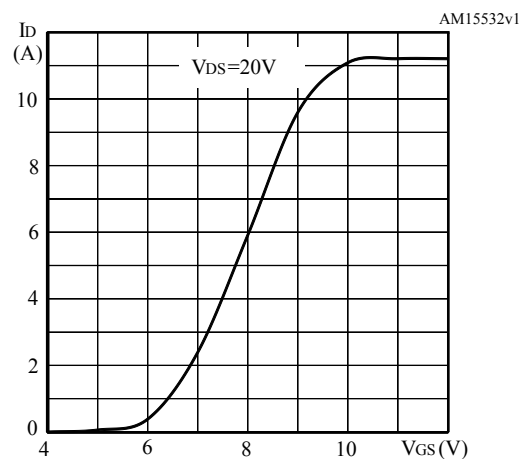
Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$I_{SD}$	Source-drain current		-		6	A
$I_{SDM}$	Source-drain current (pulsed)		-		24	A
$V_{SD}^{(1)}$	Forward on voltage	$I_{SD} = 6\text{ A}$ , $V_{GS} = 0\text{ V}$	-		1.5	V
$t_{rr}$	Reverse recovery time	$I_{SD} = 6\text{ A}$ , $V_{DD} = 60\text{ V}$ $di/dt = 100\text{ A}/\mu\text{s}$ , (see Figure 18. Test circuit for inductive load switching and diode recovery times)	-	315		ns
$Q_{rr}$	Reverse recovery charge		-	2.8		$\mu\text{C}$
$I_{RRM}$	Reverse recovery current		-	17.5		A
$t_{rr}$	Reverse recovery time	$I_{SD} = 6\text{ A}$ , $V_{DD} = 60\text{ V}$ $di/dt = 100\text{ A}/\mu\text{s}$ , $T_j = 150\text{ }^\circ\text{C}$ (see Figure 18. Test circuit for inductive load switching and diode recovery times)	-	480		ns
$Q_{rr}$	Reverse recovery charge		-	3.8		$\mu\text{C}$
$I_{RRM}$	Reverse recovery current		-	16		A

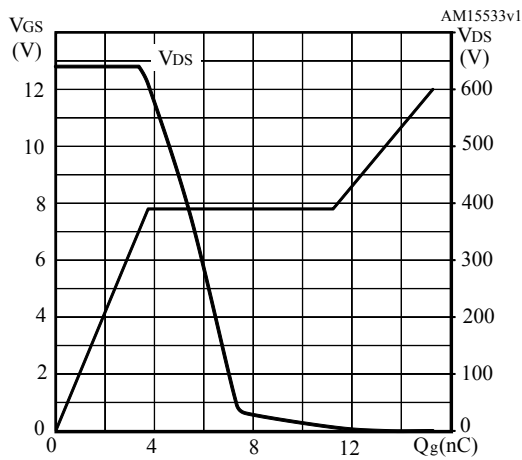
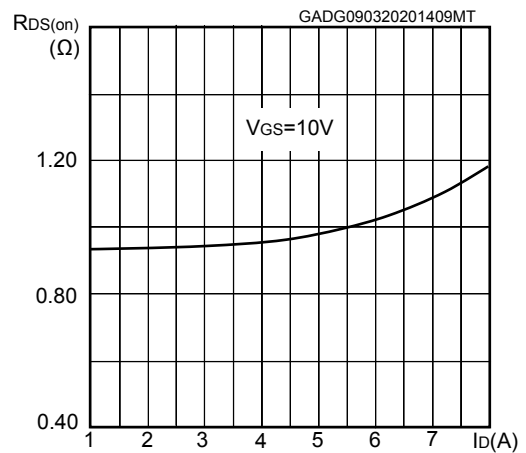
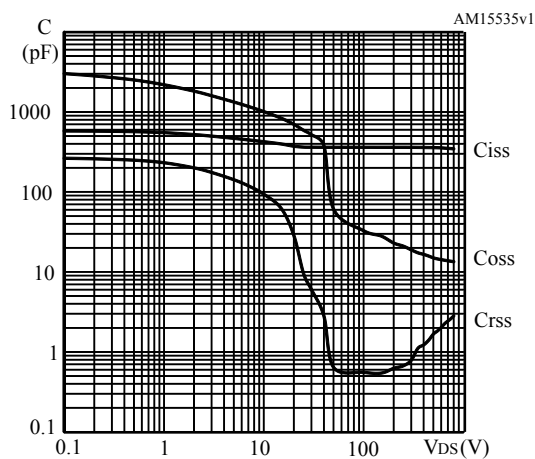
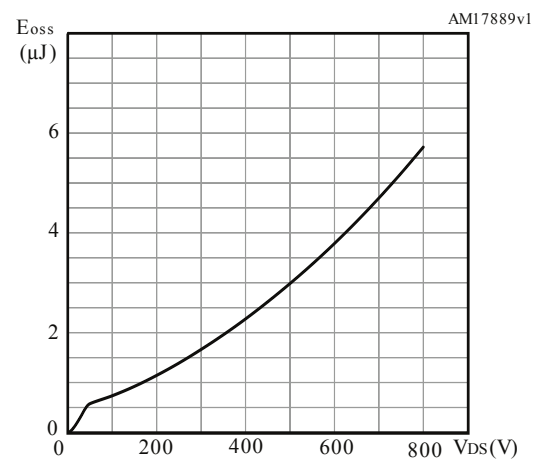
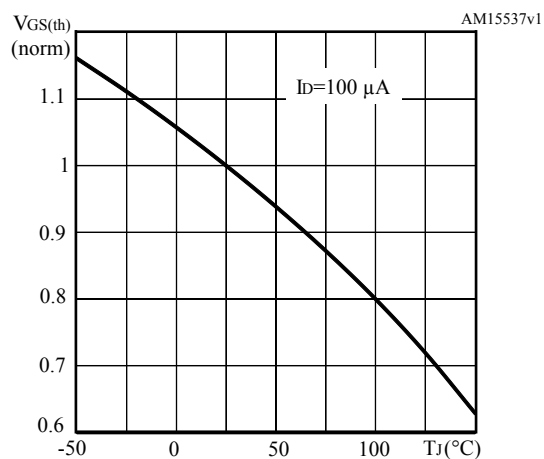
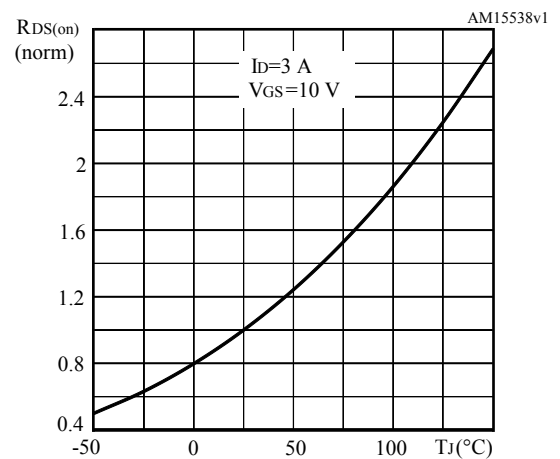
1. Pulsed: pulse duration = 300 $\mu\text{s}$ , duty cycle 1.5%

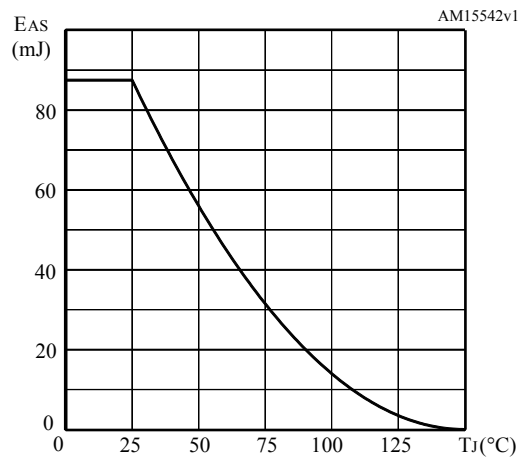
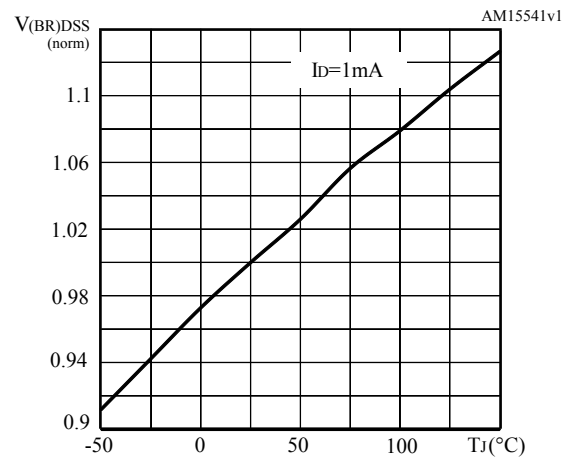
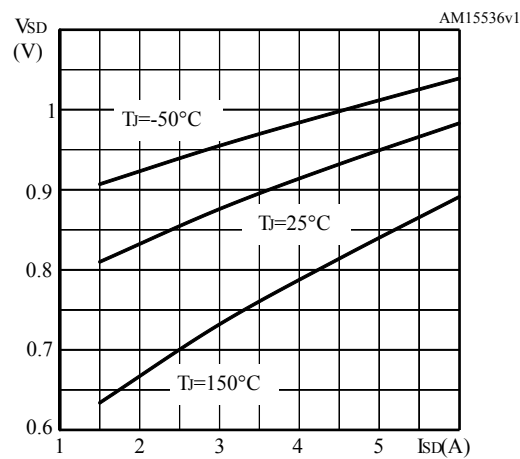
**Table 7. Gate-source Zener diode**

Symbol	Parameter	Test conditions	Min	Typ.	Max	Unit
$V_{(BR)GSO}$	Gate-source breakdown voltage	$I_{GS} = \pm 1\text{ mA}$ , $I_D = 0\text{ A}$	$\pm 30$	-	-	V

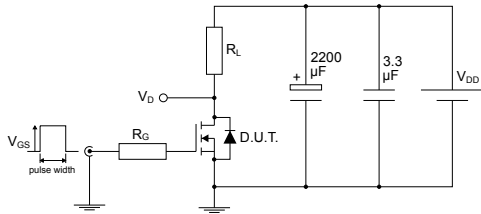
The built-in back-to-back Zener diodes are specifically designed to enhance the ESD performance of the device. The Zener voltage facilitates efficient and cost-effective device integrity protection, thus eliminating the need for additional external componentry.

**2.1 Electrical characteristics (curves)**
**Figure 1. Safe operating area for DPAK and IPAK**

**Figure 2. Thermal impedance for DPAK and IPAK**

**Figure 3. Safe operating area for TO-220**

**Figure 4. Thermal impedance for TO-220**

**Figure 5. Output characteristics**

**Figure 6. Transfer characteristics**


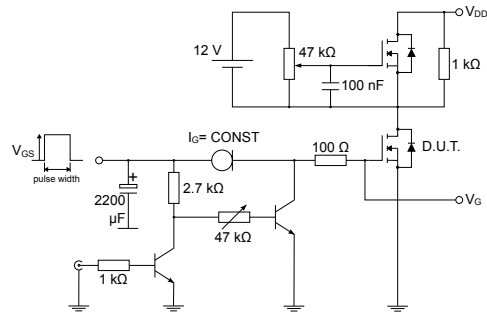
**Figure 7. Gate charge vs gate-source voltage**

**Figure 8. Static drain-source on-resistance**

**Figure 9. Capacitance variations**

**Figure 10. Output capacitance stored energy**

**Figure 11. Normalized gate threshold voltage vs temperature**

**Figure 12. Normalized on-resistance vs temperature**


**Figure 13. Maximum avalanche energy vs starting  $T_J$** 

**Figure 14. Normalized  $V_{(BR)DSS}$  vs temperature**

**Figure 15. Source-drain diode forward characteristics**


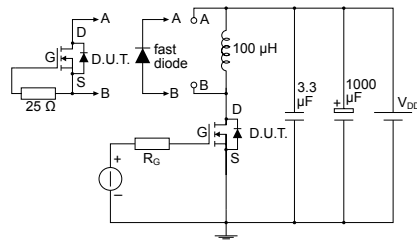
### 3 Test circuits

**Figure 16. Test circuit for resistive load switching times**


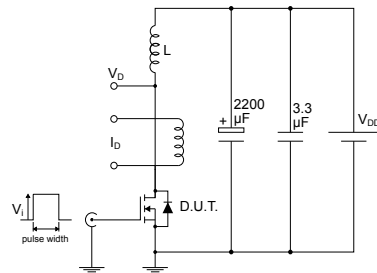
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**Figure 17. Test circuit for gate charge behavior**


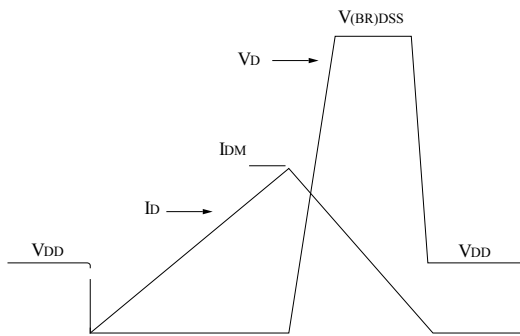
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**Figure 18. Test circuit for inductive load switching and diode recovery times**


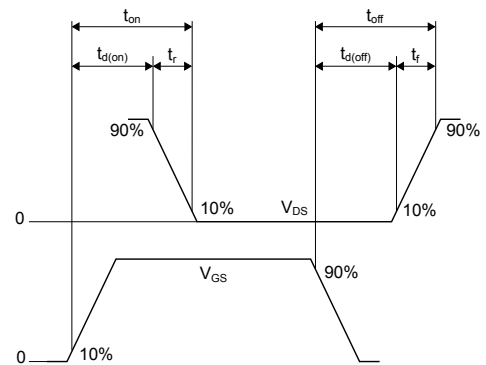
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**Figure 19. Unclamped inductive load test circuit**


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**Figure 20. Unclamped inductive waveform**


AM01472v1

**Figure 21. Switching time waveform**


AM01473v1

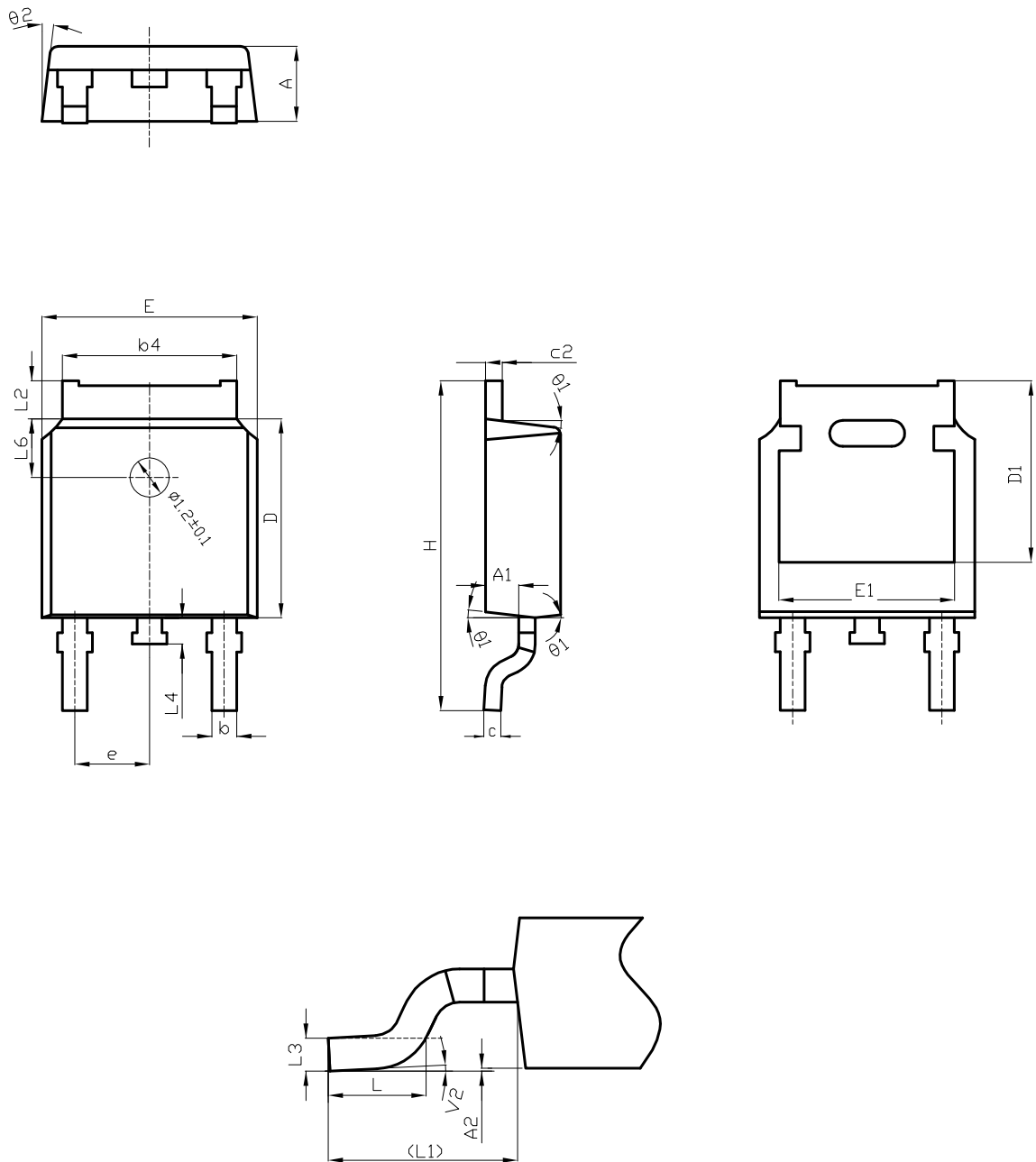


## 4 Package information

In order to meet environmental requirements, ST offers these devices in different grades of **ECOPACK** packages, depending on their level of environmental compliance. ECOPACK specifications, grade definitions and product status are available at: [www.st.com](http://www.st.com). ECOPACK is an ST trademark.

### 4.1 DPAK (TO-252) type C2 package information

Figure 22. DPAK (TO-252) type C2 package outline



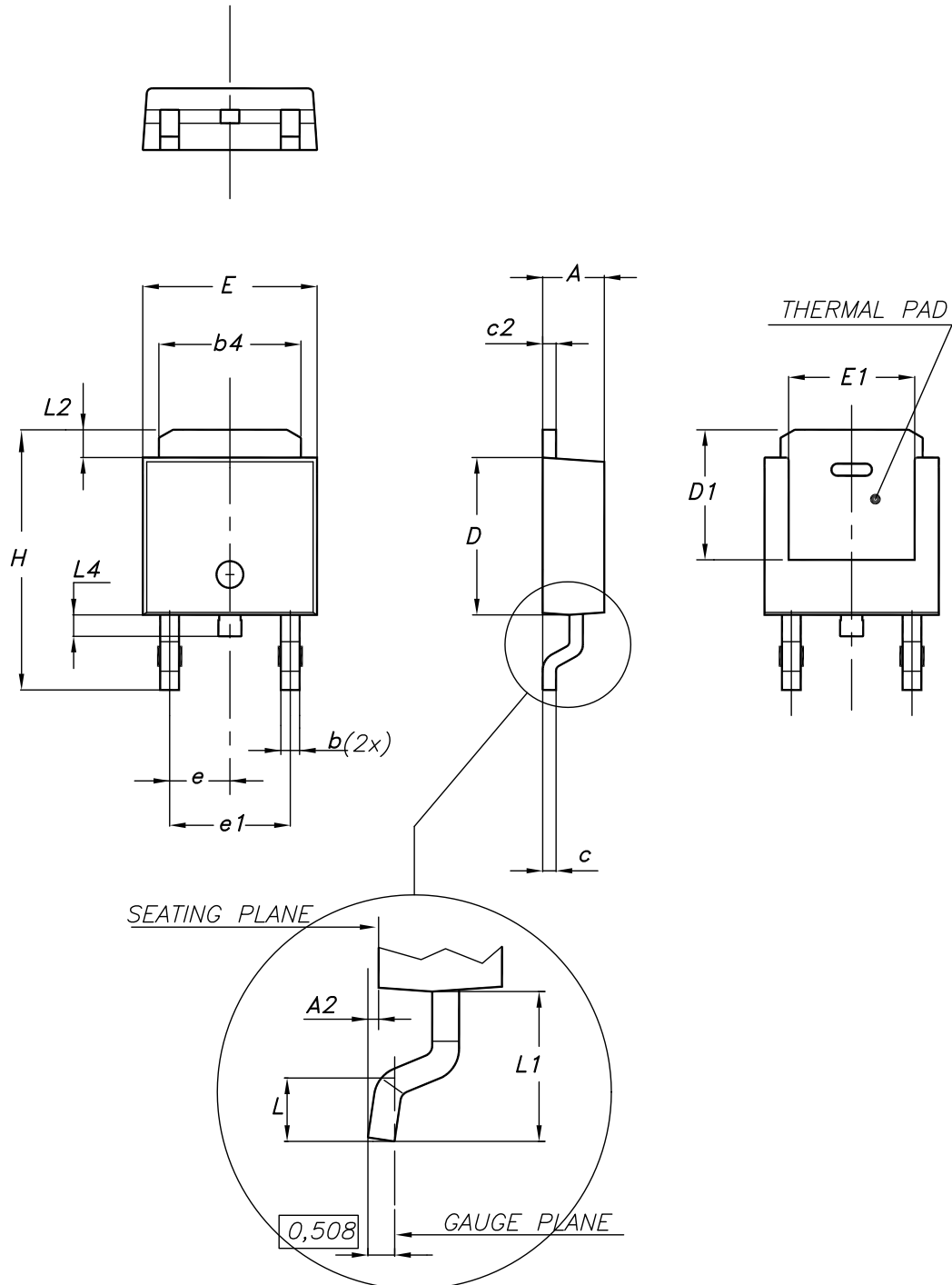
0068772\_type-C2\_rev29

**Table 8. DPAK (TO-252) type C2 mechanical data**

Dim.	mm		
	Min.	Typ.	Max.
A	2.20	2.30	2.38
A1	0.90	1.01	1.10
A2	0.00		0.10
b	0.72		0.85
b4	5.13	5.33	5.46
c	0.47		0.60
c2	0.47		0.60
D	6.00	6.10	6.20
D1	5.10		5.60
E	6.50	6.60	6.70
E1	5.20		5.50
e	2.186	2.286	2.386
H	9.80	10.10	10.40
L	1.40	1.50	1.70
L1	2.90 REF		
L2	0.90		1.25
L3	0.51 BSC		
L4	0.60	0.80	1.00
L6	1.80 BSC		
θ1	5°	7°	9°
θ2	5°	7°	9°
V2	0°		8°

## 4.2 DPAK (TO-252) type E package information

Figure 23. DPAK (TO-252) type E package outline

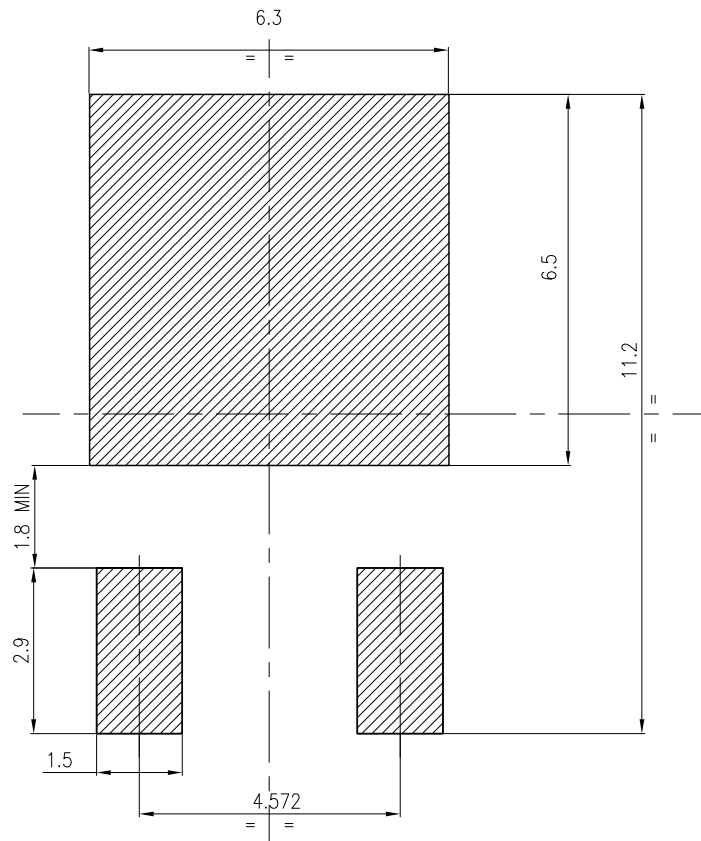


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**Table 9. DPAK (TO-252) type E mechanical data**

Dim.	mm		
	Min.	Typ.	Max.
A	2.18		2.39
A2			0.13
b	0.65		0.884
b4	4.95		5.46
c	0.46		0.61
c2	0.46		0.60
D	5.97		6.22
D1	5.21		
E	6.35		6.73
E1	4.32		
e		2.286	
e1		4.572	
H	9.94		10.34
L	1.50		1.78
L1		2.74	
L2	0.89		1.27
L4			1.02

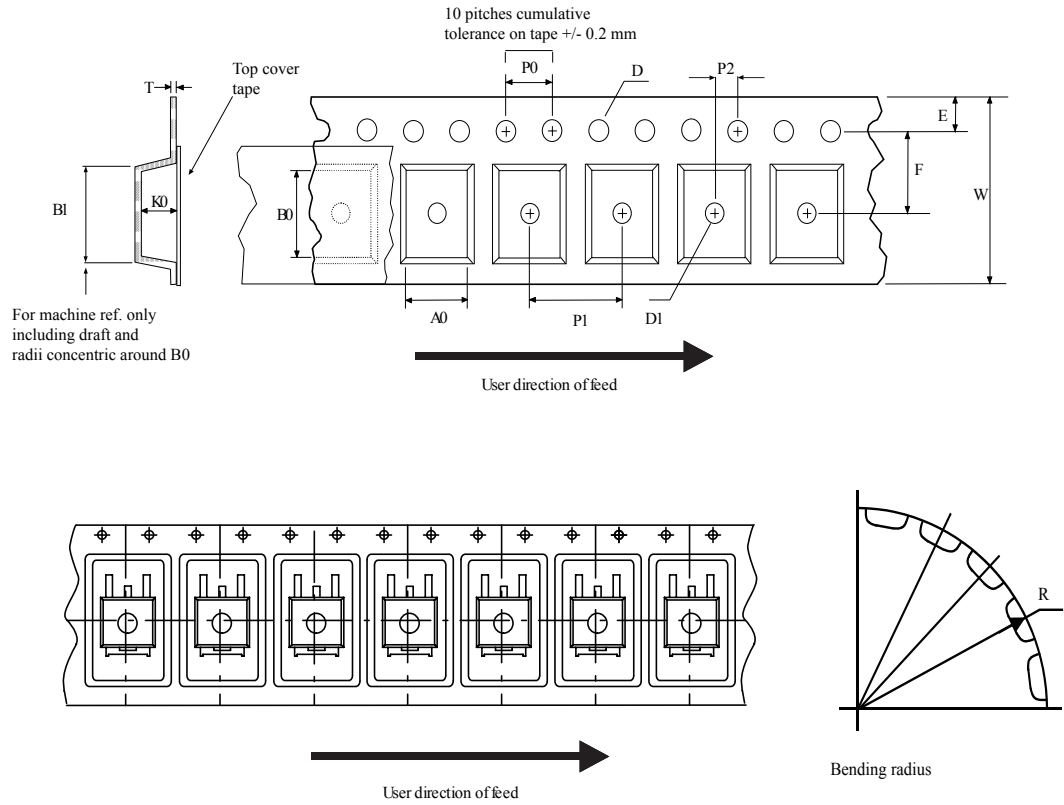
Figure 24. DPAK (TO-252) recommended footprint (dimensions are in mm)



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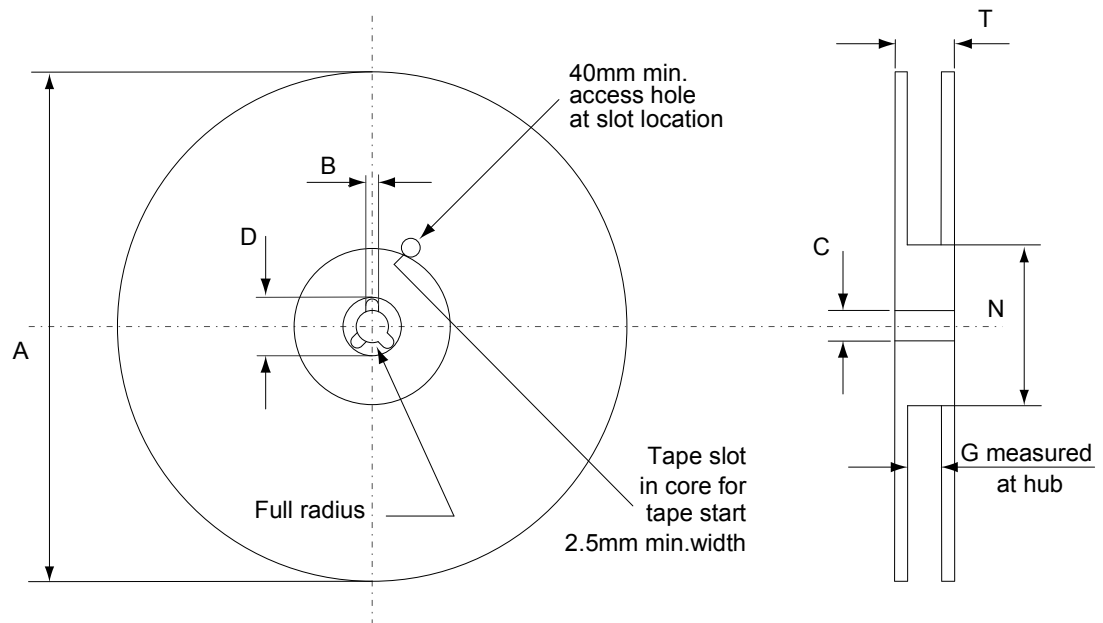
### 4.3 DPAK (TO-252) packing information

Figure 25. DPAK (TO-252) tape outline



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Figure 26. DPAK (TO-252) reel outline



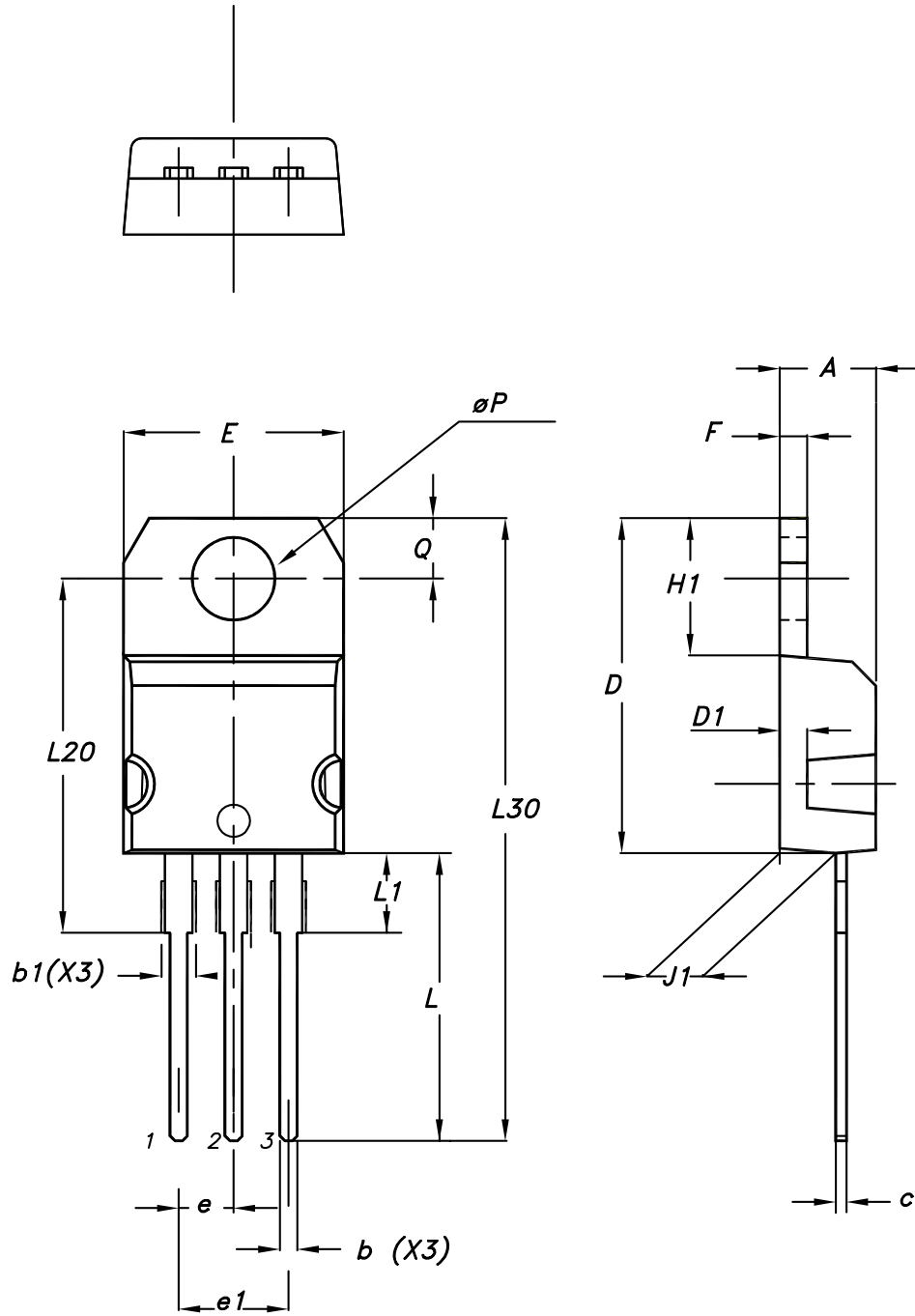
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Table 10. DPAK (TO-252) tape and reel mechanical data

Dim.	Tape		Dim.	Reel	
	mm			mm	
	Min.	Max.		Min.	Max.
A0	6.8	7	A		330
B0	10.4	10.6	B	1.5	
B1		12.1	C	12.8	13.2
D	1.5	1.6	D	20.2	
D1	1.5		G	16.4	18.4
E	1.65	1.85	N	50	
F	7.4	7.6	T		22.4
K0	2.55	2.75			
P0	3.9	4.1	Base qty.		2500
P1	7.9	8.1	Bulk qty.		2500
P2	1.9	2.1			
R	40				
T	0.25	0.35			
W	15.7	16.3			

#### 4.4 TO-220 type A package information

Figure 27. TO-220 type A package outline



0015988\_typeA\_Rev\_23

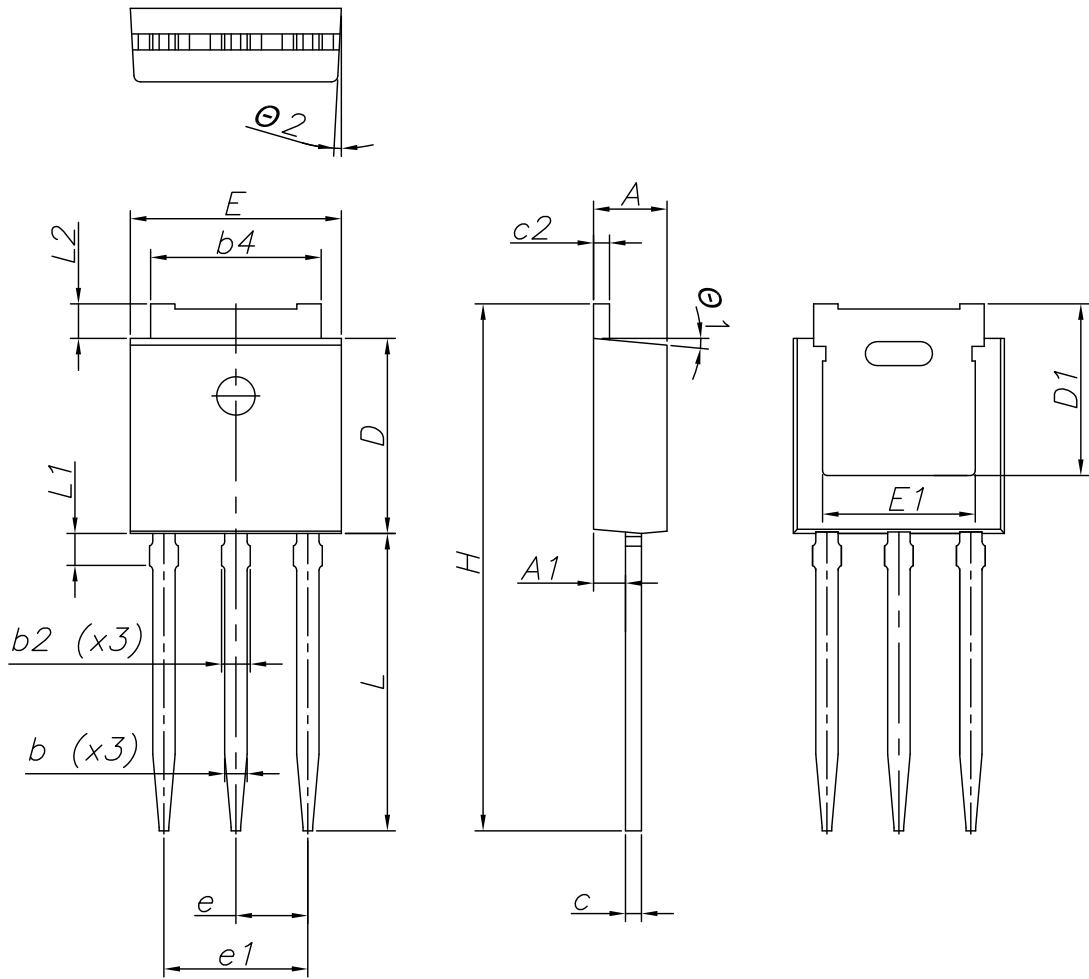


Table 11. TO-220 type A package mechanical data

Dim.	mm		
	Min.	Typ.	Max.
A	4.40		4.60
b	0.61		0.88
b1	1.14		1.55
c	0.48		0.70
D	15.25		15.75
D1		1.27	
E	10.00		10.40
e	2.40		2.70
e1	4.95		5.15
F	1.23		1.32
H1	6.20		6.60
J1	2.40		2.72
L	13.00		14.00
L1	3.50		3.93
L20		16.40	
L30		28.90	
øP	3.75		3.85
Q	2.65		2.95
Slug flatness		0.03	0.10

#### 4.5 IPAK (TO-251) type C package information

Figure 28. IPAK (TO-251) type C package outline



0068771\_IK\_typeC\_rev15

**Table 12. IPAK (TO-251) type C package mechanical data**

Dim.	mm		
	Min.	Typ.	Max.
A	2.20	2.30	2.35
A1	0.90	1.00	1.10
b	0.66		0.79
b2			0.90
b4	5.23	5.33	5.43
c	0.46		0.59
c2	0.46		0.59
D	6.00	6.10	6.20
D1	5.20	5.37	5.55
E	6.50	6.60	6.70
E1	4.60	4.78	4.95
e	2.20	2.25	2.30
e1	4.40	4.50	4.60
H	16.18	16.48	16.78
L	9.00	9.30	9.60
L1	0.80	1.00	1.20
L2	0.90	1.08	1.25
θ1	3°	5°	7°
θ2	1°	3°	5°

## 5 Ordering information

**Table 13. Ordering information**

Order code	Marking	Package	Packing
STD7N80K5	7N80K5	DPAK	Tape and reel
STP7N80K5		TO-220	Tube
STU7N80K5		IPAK	

## Revision history

**Table 14. Document revision history**

Date	Revision	Changes
17-Jul-2012	1	First release.
17-Oct-2012	2	Minor text changes in cover page Modified: title and I <sub>D</sub> value in cover page
19-Dec-2012	3	Minor text changes Added: IPAK package Updated: Section 4: Package mechanical data for IPAK
18-Mar-2013	4	Modified: I <sub>AR</sub> value on Table 2 Updated: Section 4: Package mechanical data only for DPAK package
09-Oct-2013	5	The part number STF7N80K5 has been moved to a separate datasheet Minor text changes
19-May-2017	6	Updated title, description and features in cover page. Updated <i>Table 2: "Absolute maximum ratings"</i> and <i>Table 4: "On/off states"</i> . Updated <i>Section 4: "Package information"</i> . Minor text changes.
09-Sep-2020	7	The DPAK type A2 and IPAK type A package information have been removed from the datasheet. Minor text changes.

## Contents

<b>1</b>	<b>Electrical ratings</b> .....	<b>2</b>
<b>2</b>	<b>Electrical characteristics</b> .....	<b>3</b>
<b>2.1</b>	Electrical characteristics (curves) .....	5
<b>3</b>	<b>Test circuits</b> .....	<b>8</b>
<b>4</b>	<b>Package information</b> .....	<b>9</b>
<b>4.1</b>	DPAK (TO-252) type C2 package information .....	9
<b>4.2</b>	DPAK (TO-252) type E package information .....	11
<b>4.3</b>	DPAK (TO-252) packing information .....	14
<b>4.4</b>	TO-220 type A package information .....	16
<b>4.5</b>	IPAK (TO-251) type C package information .....	18
<b>5</b>	<b>Ordering information</b> .....	<b>20</b>
	<b>Revision history</b> .....	<b>21</b>

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