



STD60NF55L STD60NF55L-1

N-channel 55V - 0.012Ω - 60A - DPAK/IPAK
STripFET™ II Power MOSFET

General features

Type	V _{DSS}	R _{DS(on)}	I _D
STD60NF55L-1	55V	<0.015Ω	60A
STD60NF55L	55V	<0.015Ω	60A

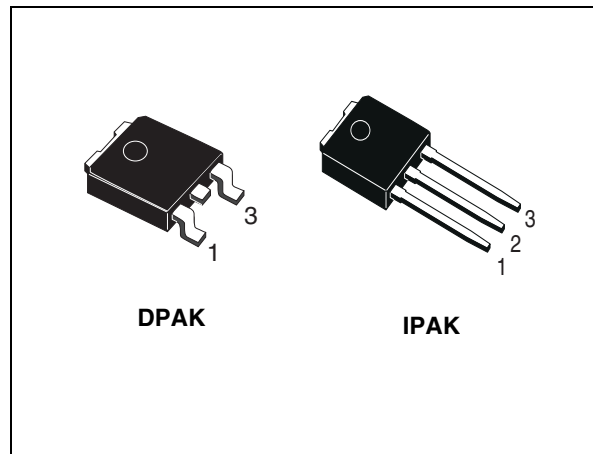
- Low threshold drive

Description

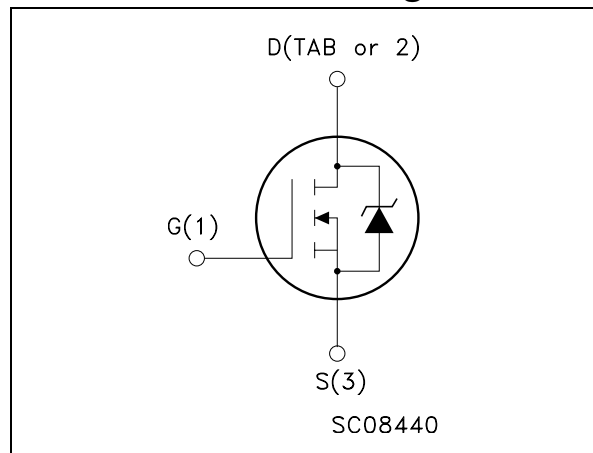
This MOSFET is the latest development of STMicroelectronics unique “Single Feature Size™” strip-based process. The resulting transistor shows extremely high packing density for low on-resistance, rugged avalanche characteristics and less critical alignment steps therefore a remarkable manufacturing reproducibility.

Applications

- Switching application



Internal schematic diagram



Order codes

Part number	Marking	Package	Packaging
STD60NF55LT4	D60NF55L	DPAK	Tape & reel
STD60NF55L-1	D60NF55L	IPAK	Tube

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1 Electrical ratings

Table 1. Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_{DS}	Drain-source voltage ($V_{GS} = 0$)	55	V
V_{GS}	Gate- source voltage	± 15	V
I_D	Drain current (continuous) at $T_C = 25^\circ\text{C}$	60	A
I_D	Drain current (continuous) at $T_C = 100^\circ\text{C}$	42	A
$I_{DM}^{(1)}$	Drain current (pulsed)	240	A
P_{tot}	Total dissipation at $T_C = 25^\circ\text{C}$	110	W
	Derating Factor	0.73	W/°C
$dv/dt^{(2)}$	Peak diode recovery voltage slope	16	V/ns
$E_{AS}^{(3)}$	Single pulse avalanche energy	400	mJ
T_{stg}	Storage temperature	-55 to 175	°C
T_j	Max. operating junction temperature		

1. Pulse width limited by safe operating area.
2. $I_{SD} \leq 40\text{A}$, $di/dt \leq 350\text{A}/\mu\text{s}$, $V_{DD} \leq V_{(BR)DSS}$, $T_j \leq T_{JMAX}$.
3. Starting $T_j = 25^\circ\text{C}$, $I_D = 17.5\text{A}$, $V_{DD} = 24\text{V}$

Table 2. Thermal data

$R_{thj-case}$	Thermal resistance junction-case max	1.36	°C/W
$R_{thj-amb}$	Thermal resistance junction-to ambient max	62.5	°C/W
T_J	Maximum lead temperature for soldering purpose	275	°C

2 Electrical characteristics

($T_{CASE}=25^{\circ}C$ unless otherwise specified)

Table 3. On/off states

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{(BR)DSS}$	Drain-source breakdown voltage	$I_D = 250\mu A, V_{GS} = 0$	55			V
I_{DSS}	Zero gate voltage drain current ($V_{GS} = 0$)	$V_{DS} = \text{Max rating}$ $V_{DS} = \text{Max rating},$ $T_C = 125^{\circ}C$			1 10	μA μA
I_{GSS}	Gate-body leakage current ($V_{DS} = 0$)	$V_{GS} = \pm 15V$			± 100	nA
$V_{GS(th)}$	Gate threshold voltage	$V_{DS} = V_{GS}, I_D = 250\mu A$	1		2	V
$R_{DS(on)}$	Static drain-source on resistance	$V_{GS} = 10V, I_D = 30A$ $V_{GS} = 4.5V, I_D = 30A$		0.012 0.014	0.015 0.017	Ω Ω

Table 4. Dynamic

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$g_{fs}^{(1)}$	Forward transconductance	$V_{DS} = 10V, I_D = 30A$		35		S
C_{iss}	Input capacitance	$V_{DS} = 25V, f = 1MHz,$ $V_{GS} = 0$		1950		pF
C_{oss}	Output capacitance			390		pF
C_{rss}	Reverse transfer capacitance			130		pF
$t_{d(on)}$	Turn-on delay time	$V_{DD} = 25V, I_D = 30A$ $R_G = 4.7\Omega, V_{GS} = 4.5V$ (see Figure 12)		30		ns
t_r	Rise time			180		ns
$t_{d(off)}$	Turn-off delay time			80		ns
t_f	Fall time			35		ns
Q_g	Total gate charge	$V_{DD} = 40V, I_D = 60A,$ $V_{GS} = 5V, R_G = 4.7\Omega$ (see Figure 13)		40	56	nC
Q_{gs}	Gate-source charge			10		nC
Q_{gd}	Gate-drain charge			20		nC

1. Pulsed: Pulse duration = 300 μs , duty cycle 1.5 %.

Table 5. Source drain diode

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
I_{SD} $I_{SDM}^{(1)}$	Source-drain current Source-drain current (pulsed)				60 240	A A
$V_{SD}^{(2)}$	Forward on voltage	$I_{SD} = 60A, V_{GS} = 0$			1.3	V
t_{rr} Q_{rr} I_{RRM}	Reverse recovery time Reverse recovery charge Reverse recovery current	$I_{SD} = 40A, di/dt = 100A/\mu s,$ $V_{DD} = 25V, T_j = 150^\circ C$ (see Figure 14)		65 130 4		ns nC A

1. Pulse width limited by safe operating area.
2. Pulsed: Pulse duration = 300 μs , duty cycle 1.5 %

2.1 Electrical characteristics (curves)

Figure 1. Safe operating area

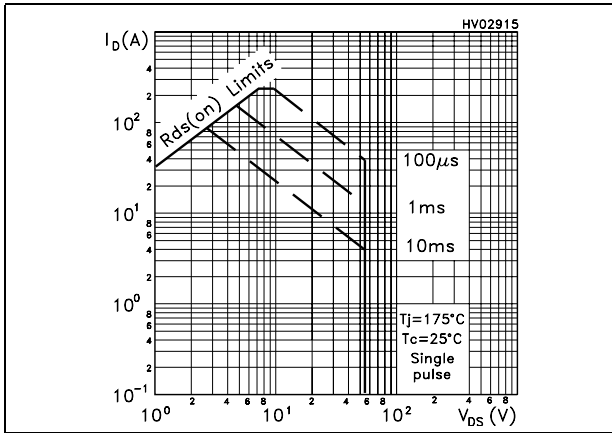


Figure 2. Thermal impedance

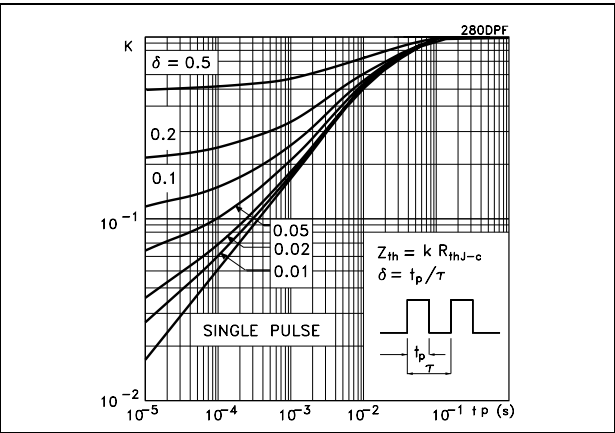


Figure 3. Output characteristics

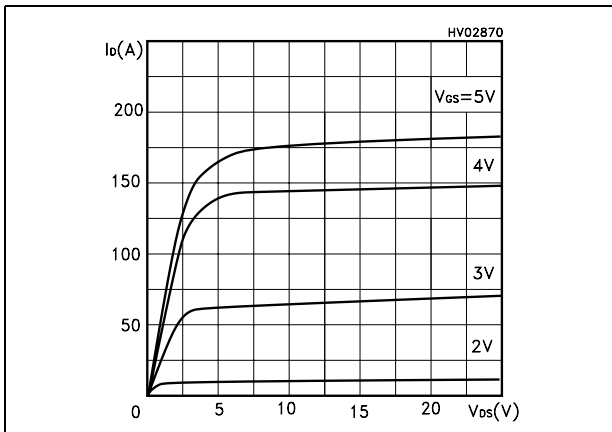


Figure 4. Transfer characteristics

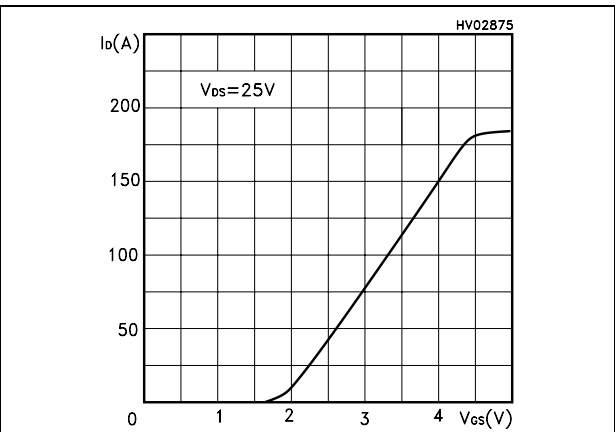


Figure 5. Transconductance

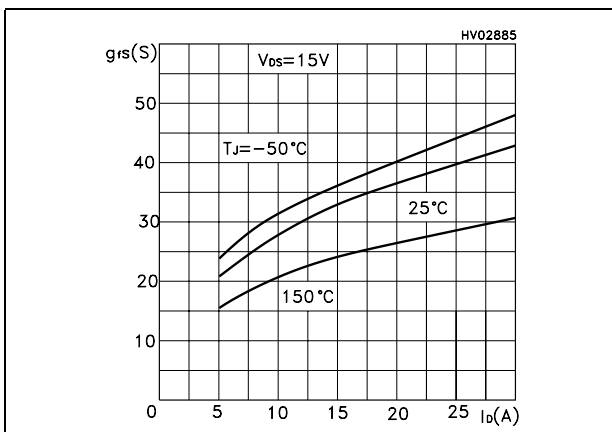


Figure 6. Static drain-source on resistance

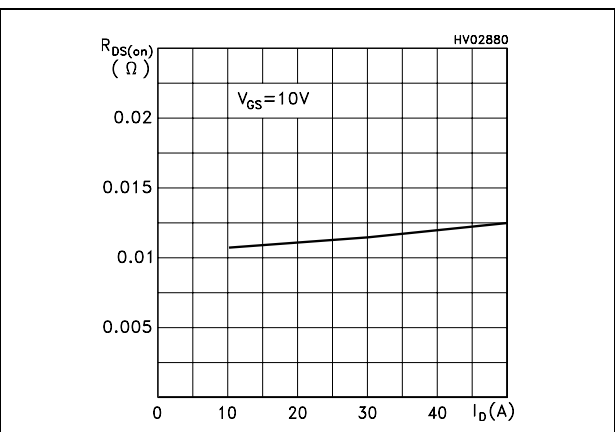


Figure 7. Gate charge vs gate-source voltage Figure 8. Capacitance variations

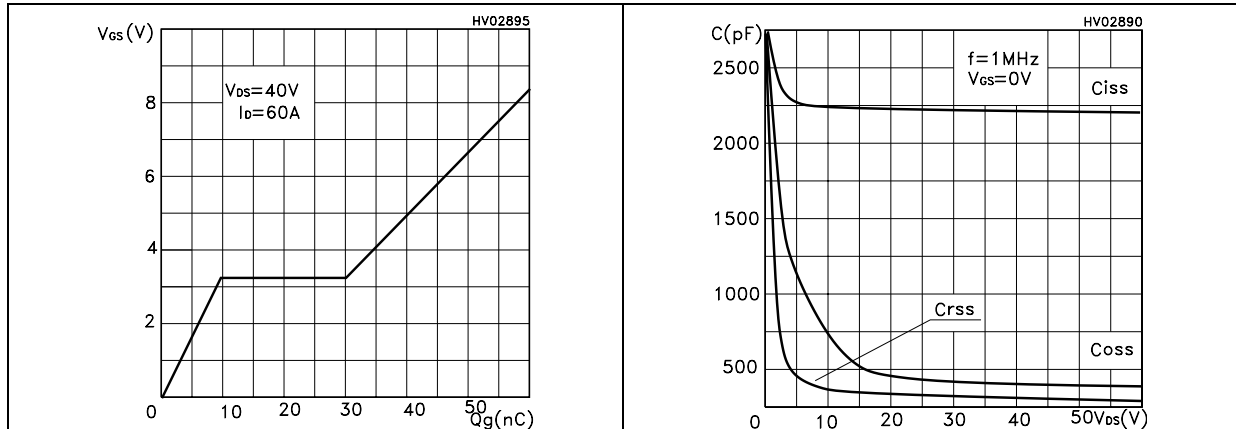


Figure 9. Normalized gate threshold voltage vs temperature Figure 10. Normalized on resistance vs temperature

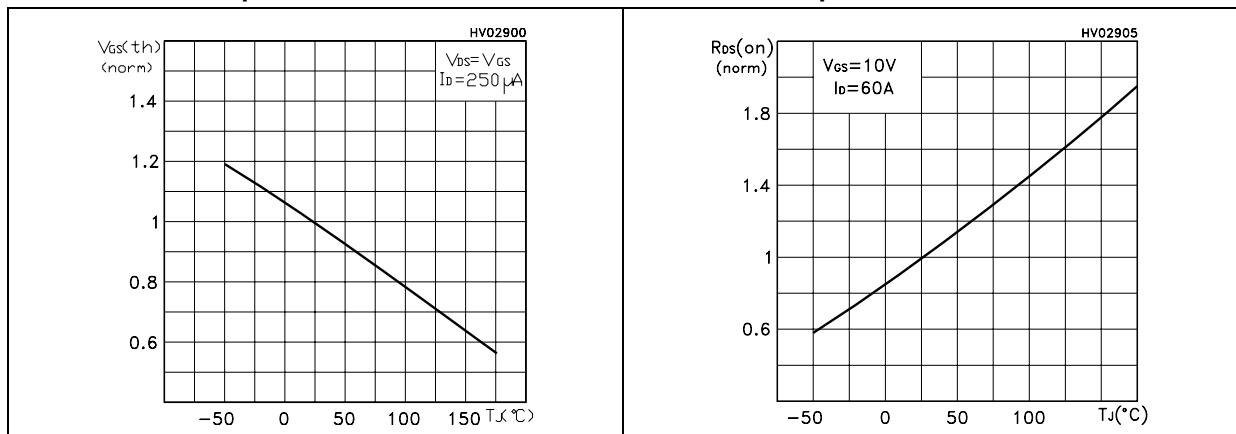
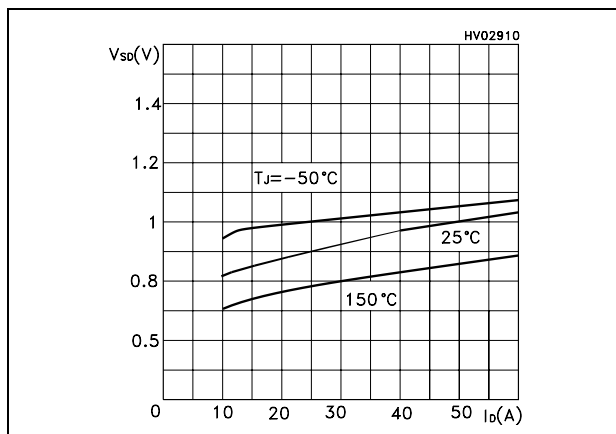


Figure 11. Source-drain diode forward characteristics



3 Test circuit

Figure 12. Switching times test circuit for resistive load

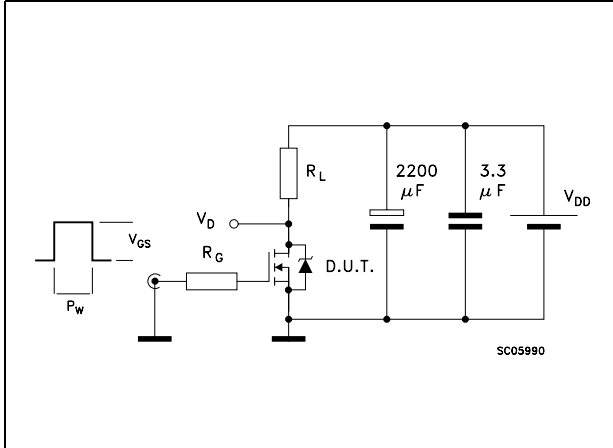


Figure 13. Gate charge test circuit

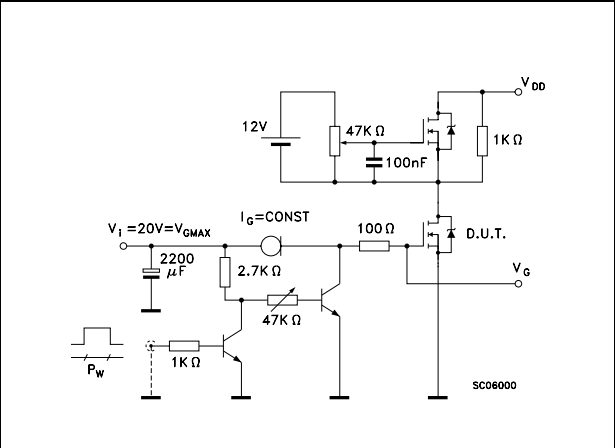


Figure 14. Test circuit for inductive load switching and diode recovery times

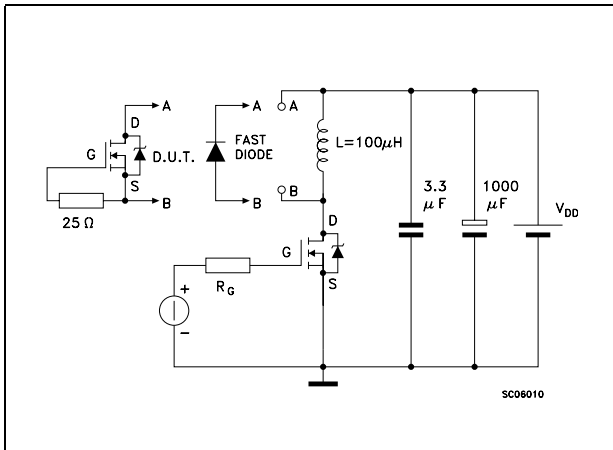


Figure 15. Unclamped Inductive load test circuit

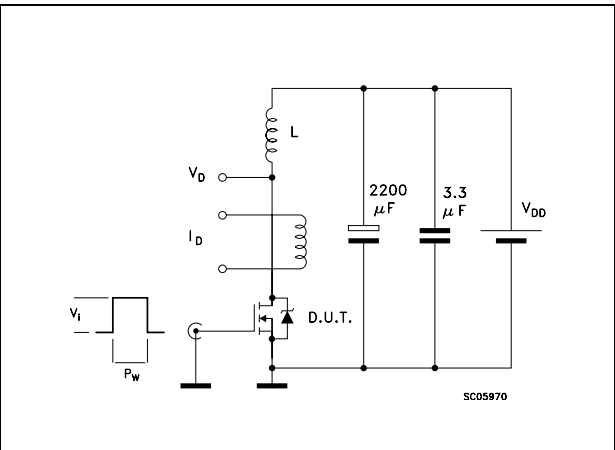


Figure 16. Unclamped inductive waveform

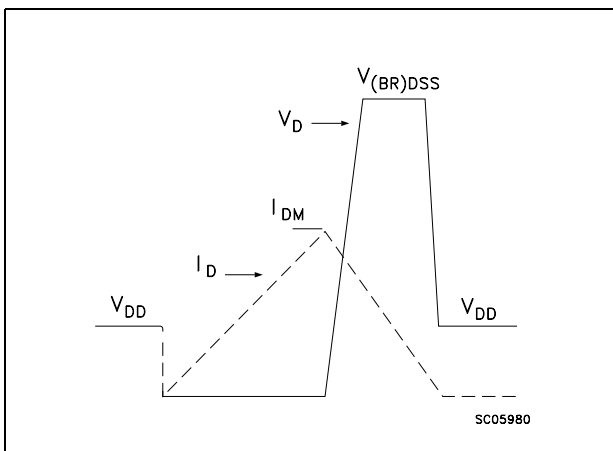
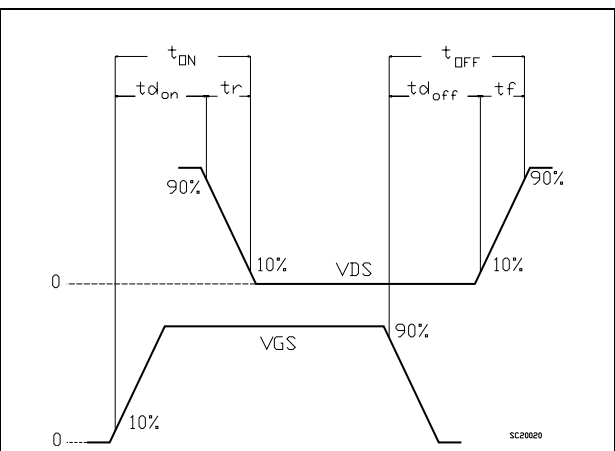


Figure 17. Switching time waveform

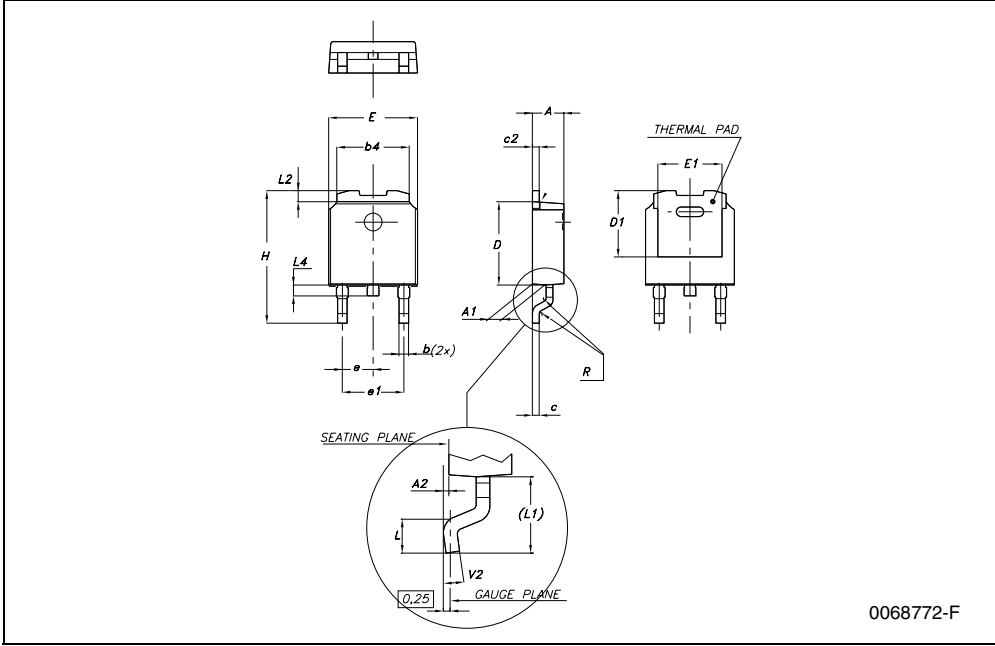


4 Package mechanical data

In order to meet environmental requirements, ST offers these devices in ECOPACK® packages. These packages have a Lead-free second level interconnect . The category of second level interconnect is marked on the package and on the inner box label, in compliance with JEDEC Standard JESD97. The maximum ratings related to soldering conditions are also marked on the inner box label. ECOPACK is an ST trademark. ECOPACK specifications are available at: www.st.com

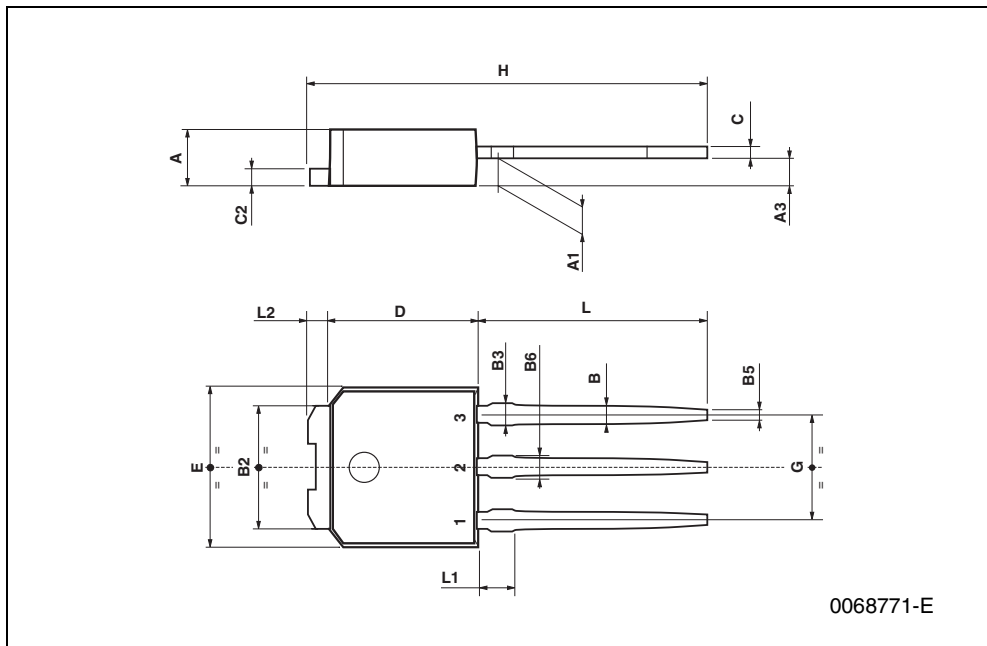
DPAK MECHANICAL DATA

DIM.	mm.			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A	2.2		2.4	0.086		0.094
A1	0.9		1.1	0.035		0.043
A2	0.03		0.23	0.001		0.009
B	0.64		0.9	0.025		0.035
b4	5.2		5.4	0.204		0.212
C	0.45		0.6	0.017		0.023
C2	0.48		0.6	0.019		0.023
D	6		6.2	0.236		0.244
D1		5.1			0.200	
E	6.4		6.6	0.252		0.260
E1		4.7			0.185	
e		2.28			0.090	
e1	4.4		4.6	0.173		0.181
H	9.35		10.1	0.368		0.397
L	1			0.039		
(L1)		2.8			0.110	
L2		0.8			0.031	
L4	0.6		1	0.023		0.039
R		0.2			0.008	
V2	0°		8°	0°		8°



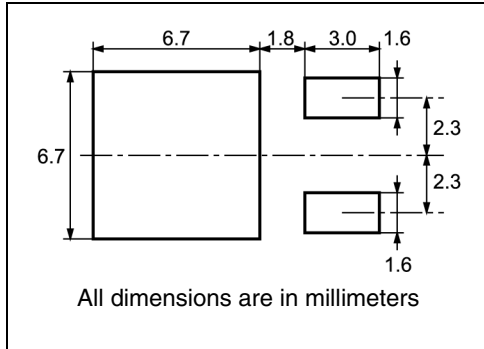
TO-251 (IPAK) MECHANICAL DATA

DIM.	mm			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A	2.2		2.4	0.086		0.094
A1	0.9		1.1	0.035		0.043
A3	0.7		1.3	0.027		0.051
B	0.64		0.9	0.025		0.031
B2	5.2		5.4	0.204		0.212
B3			0.85			0.033
B5		0.3			0.012	
B6			0.95			0.037
C	0.45		0.6	0.017		0.023
C2	0.48		0.6	0.019		0.023
D	6		6.2	0.236		0.244
E	6.4		6.6	0.252		0.260
G	4.4		4.6	0.173		0.181
H	15.9		16.3	0.626		0.641
L	9		9.4	0.354		0.370
L1	0.8		1.2	0.031		0.047
L2		0.8	1		0.031	0.039



5 Packing mechanical data

DPAK FOOTPRINT



TAPE AND REEL SHIPMENT

40 mm min. Access hole at slot location

Full radius

Tape slot in core for tape start 2.5mm min. width

G measured at hub

REEL MECHANICAL DATA

DIM.	mm		inch	
	MIN.	MAX.	MIN.	MAX.
A		330		12.992
B	1.5		0.059	
C	12.8	13.2	0.504	0.520
D	20.2		0.795	
G	16.4	18.4	0.645	0.724
N	50		1.968	
T		22.4		0.881

TAPE MECHANICAL DATA

DIM.	mm		inch	
	MIN.	MAX.	MIN.	MAX.
A0	6.8	7	0.267	0.275
B0	10.4	10.6	0.409	0.417
B1		12.1		0.476
D	1.5	1.6	0.059	0.063
D1	1.5		0.059	
E	1.65	1.85	0.065	0.073
F	7.4	7.6	0.291	0.299
K0	2.55	2.75	0.100	0.108
P0	3.9	4.1	0.153	0.161
P1	7.9	8.1	0.311	0.319
P2	1.9	2.1	0.075	0.082
R	40		1.574	
W	15.7	16.3	0.618	0.641

TOP COVER TAPE

User Direction of Feed

Center line of cavity

Bending radius R min.

FEED DIRECTION

TRL

For machine ref. only including draft and radii concentric around B0

10 pitches cumulative tolerance on tape +/- 0.2 mm

6 Revision history

Table 6. Revision history

Date	Revision	Changes
14-Mar-2005	3	Preliminary version
18-May-2005	4	New package inserted: IPAK
18-Nov-2005	5	Changed value in Table 4 (Rise Time from 18 to 180ns)
19-Jul-2006	6	New template, no content change

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