NTE40182B
Integrated Circuit
CMOS, Look–Ahead Carry Generator
16–Lead DIP Type Package

Description:

The NTE40182B is a high–speed look–ahead carry generator capable of anticipating a carry across four binary adders or groups of adders. This device is cascadable to perform full look–ahead across n–bit adders. Carry, propagate–carry, and generate–carry functions are provided as enumerated in the Pin Connection Diagram.

Features:

- Generates High–Speed Carry Across Four Adders of Adders Groups
- High–Speed Operational: $t_{PHL} = t_{PLH} = 100ns$ (Typ) at $V_{DD} = 10V$
- Cascadable for Fast Carries over N–Bits
- Standardized, Symmetrical Output Characteristics
- Quiescent Current Specified at 20V
- 5V, 10V, and 15V Parametric Ratings
- Input Current of 100nA at 18V and +25°C

Absolute Maximum Ratings: (Note 1)

Supply Voltage (Voltages Referenced to V_{SS}), V_{DD} . . . . –0.5 to +20V
Input Voltage, V_I . . . . –0.5 to V_{DD}+0.5V
DC Input Current (Any One Input), I_I . . . . ±10mA
Total Power Dissipation (Per Package), P_{tot} 200mW
Device Dissipation (Per Output Transistor)
      For T_{opr} = Full package Temperature Range 100mW
Operating Temperature Range, T_{opr} . . . . –55° to +125°C
Storage Temperature Range, T_{stg} . . . . –65° to +150°C

Note 1. Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for external periods may affect device reliability.

Recommended Operating Conditions:

Supply Voltage, V_{DD} . . . . 3 to 18V
Input Voltage, V_I . . . . 0 to V_{DD} V
Operating Temperature Range, T_{opr} . . . . –55° to +125°C

Static Electrical Characteristics:

Characteristic	Conditions				Limits at Indicated Temperature (°C)							Units
	V_I (V)	V_O (V)	$|I_O|$ (µA)	V_{DD} (V)	−55°C		+25°C			+125°C		
					Min	Max	Min.	Typ.	Max.	Min	Max	
Quiescent Device, I_L	0,5	–	–	5	–	5	–	0.04	5.0	–	150	µA
	0,10	–	–	10	–	10	–	0.04	10	–	300	µA
	0,15	–	–	15	–	20	–	0.04	20	–	600	µA
	0,20	–	–	20	–	100	–	0.08	100	–	3000	µA
Output High Voltage, V_{OH}	0,5	–	< 1	5	4.95	–	4.95	5.0	–	4.95	–	V
	0,10	–	< 1	10	9.95	–	9.95	10	–	9.95	–	V
	0,15	–	< 1	15	14.95	–	14.95	15	–	14.95	–	V
Output Low Voltage, V_{OL}	5,0	–	< 1	5	–	0.05	–	–	0.05	–	0.05	V
	10,0	–	< 1	10	–	0.05	–	–	0.05	–	0.05	V
	15,0	–	< 1	15	–	0.05	–	–	0.05	–	0.05	V
Input High Voltage, V_{IH}	–	0.5,4.5	< 1	5	3.5	–	3.5	–	–	3.5	–	V
	–	1,9	< 1	10	7.0	–	7.0	–	–	7.0	–	V
	–	1.5,13.5	< 1	15	11.0	–	11.0	–	–	11.0	–	V
Input Low Voltage, V_{IL}	–	0.5,4.5	< 1	5	–	1.5	–	–	1.5	–	1.5	V
	–	9,1	< 1	10	–	3.0	–	–	3.0	–	3.0	V
	–	1.5,13.5	< 1	15	–	4.0	–	–	4.0	–	4.0	V
Output Drive Current, I_{OH}	0,5	2.5	–	5	−2.0	–	−1.6	−3.2	–	−1.15	–	mA
	0.5	4.6	–	5	−0.64	–	−0.51	−1.0	–	−0.36	–	mA
	0,10	9.5	–	10	−1.6	–	−1.3	−2.6	–	−0.9	–	mA
	0,15	13.5	–	15	−4.2	–	−3.4	−6.8	–	−2.4	–	mA
Output Sink Current, I_{OL}	0,5	0.4	–	5	0.64	–	0.51	1.0	–	0.36	–	mA
	0,10	0.5	–	10	1.6	–	1.3	2.6	–	0.9	–	mA
	0,15	1.5	–	15	4.2	–	3.4	6.8	–	2.4	–	mA
Input Current, I_{IH}, I_{IL}	0,18	Any Input		18	–	±0.1	–	$±10^{-5}$	±0.1	–	±1.0	µA
Input Capacitance, C_I	–	Any Input		–	–	–	–	5.0	7.5	–	–	pF

Dynamic Electrical Characteristics:

(T_A = +25°C, C_L = 50pF, R_L = 200kΩ, t_r and t_f = 20ns, Note 2 unless otherwise specified)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Propagation Delay Time P, G, in to P G out and Carry Outs	t_{PHL} or t_{PLH}	V_{DD} = 5V	–	200	400	ns
		V_{DD} = 10V	–	100	200	ns
		V_{DD} = 15V	–	75	150	ns
C_n to Carry Outs		V_{DD} = 5V	–	240	480	ns
		V_{DD} = 10V	–	120	240	ns
		V_{DD} = 15V	–	90	180	ns
Transition Time	t_{THL} or t_{TLH}	V_{DD} = 5V	–	100	200	ns
		V_{DD} = 10V	–	50	100	ns
		V_{DD} = 15V	–	40	80	ns

Note 2. Typical temperature coefficient for all V_{DD} values is 0.3%/°C.

Functional Diagram

Pin	Signal		Pin	Signal
3	$\overline{G0}$		12	$C_n \cdot x$
1	$\overline{G1}$		11	$C_n \cdot y$
14	$\overline{G2}$		9	$C_n \cdot z$
5	$\overline{G3}$			

$\overline{G}$ { $\overline{G0}$ (3), $\overline{G1}$ (1), $\overline{G2}$ (14), $\overline{G3}$ (5) }

$\overline{P}$ { $\overline{P0}$ (4), $\overline{P1}$ (2), $\overline{P2}$ (15), $\overline{P3}$ (6) }

C_n — 13

Outputs:
- 12 — $C_n \cdot x$
- 11 — $C_n \cdot y$
- 9 — $C_n \cdot z$
- 7 — $\overline{P}$
- 10 — $\overline{G}$
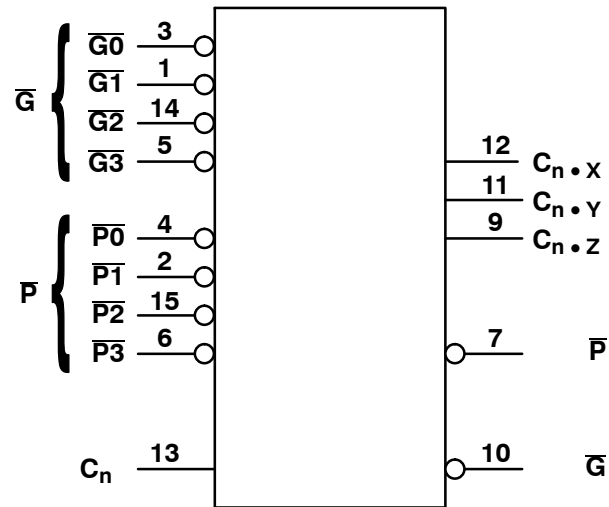
V_{DD} = Pin16
V_{SS} = Pin8

Pin Connection Diagram

Left	Pin		Pin	Right
$\overline{G1}$	1		16	V_{DD}
$\overline{P1}$	2		15	$\overline{P2}$
$\overline{G0}$	3		14	$\overline{G2}$
$\overline{P0}$	4		13	C_n
$\overline{G3}$	5		12	C_{n+x}
$\overline{P3}$	6		11	C_{n+y}
$\overline{P}$	7		10	$\overline{G}$
V_{SS}	8		9	C_{n+x}

16   9

1   8

.870 (22.0) Max

.200
(5.08)
Max

.099 (2.5) Min

.100 (2.54)

.700 (17.78)

.260 (6.6)
Max