Features

- Power-On Reset Generator with Adjustable Delay Time: 1.25ms to 10s.
- Very Low Quiescent Current: 2.8µA Typical
- High Threshold Accuracy: 0.5% Typ.
- Fixed Threshold Voltages for Standard Voltage Rails from 0.9V to 5V and Adjustable Voltage Down to 0.4V are available.
- Manual Reset ($\overline{MR}$) Input.
- Open-Drain $\overline{RESET}$ Output.
- Temperature Range: -40°C to +125°C
- Package: TDFN2.0x2.0-6L and SOT23-6L

Applications

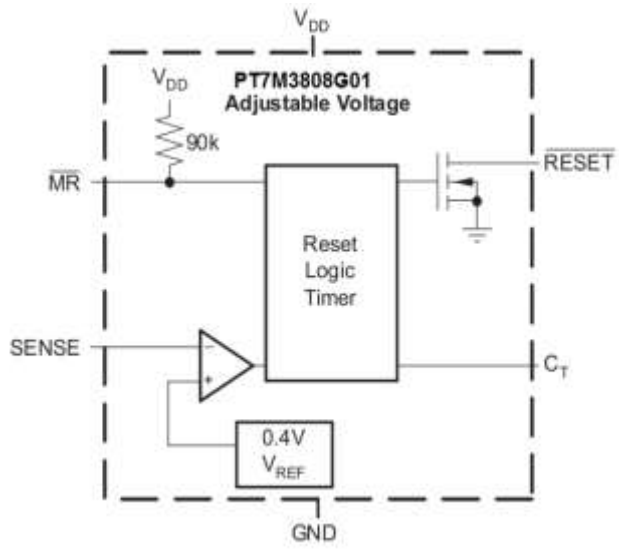
- DSP or Microcontroller Applications capacitor.
- Notebook/Desktop Computers
- PDAs/Hand-Held Products battery-powered applications.
- Portable/Battery-Powered Products
- FPGA/ASIC Applications

Description

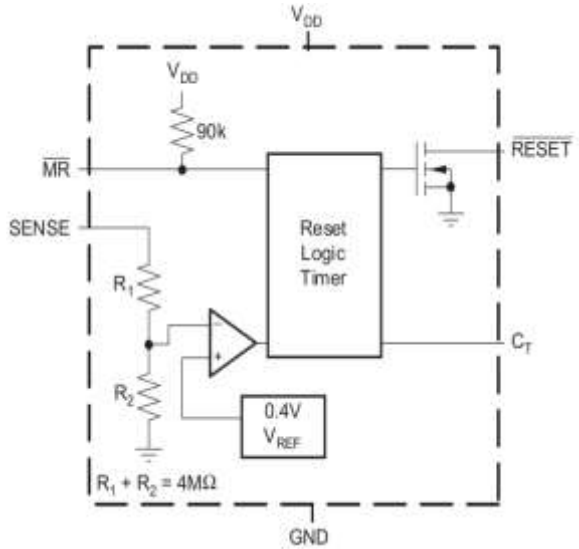
The PT7M3808G family of microprocessor supervisory circuits monitor system voltage form 0.4V to 5.0V, asserting an open-drain $\overline{RESET}$ signal when the SENSE voltage drops below a preset threshold or when the manual reset ($\overline{MR}$) pin drops to a logic low. The $\overline{RESET}$ output remains low for the user-adjustable delay time after the SENSE voltage and manual reset ($\overline{MR}$) return above the respective thresholds.

The PT7M3808G series use a precision reference to achieve 0.5% threshold accuracy for VIT ≤ 3.3 V. The reset delay time can be set to 20ms by disconnecting the C_T pin, 300ms by connecting the C_T pin to V_{DD} using a resister, or can be user-adjusted between 1.25ms and 10s by connecting the C_T pin to an external capacitor. The PT7M3808 has a very low typical quiescent current of 2.8uA so it is well-suited to battery-powered applications. It is available in a small SOT23 and an ultra-small 2.0x2.0 TDFN package, and is fully specified over a temperature range of -40°C to +125°C.

Block Diagram

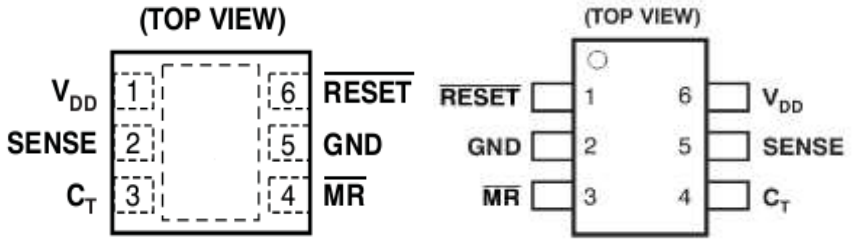


Adjustable Voltage Diagram(PT7M3808G01)



Fixed Voltage Diagram

Pin Configuration



TDFN2.0x2.0-6L SOT23-6L

Pin Description

Pin No		Pin Name	Description
SOT23	TDFN		
1	6	$\overline{\text{RESET}}$	An open-drain output that is driven to a low impedance state when $\overline{\text{RESET}}$ is asserted. $\overline{\text{RESET}}$ will remain low (asserted) for the reset period after both SENSE is above V_{IT} and $\overline{\text{MR}}$ is set to a logic high. A pull-up resistor from 10kΩ to 1Mohm should be used on this pin, and allows the reset pin to attain voltages higher than V_{DD}.
2	5	GND	Ground.
3	4	$\overline{\text{MR}}$	Driving the manual reset pin ($\overline{\text{MR}}$) low asserts $\overline{\text{RESET}}$. MR is internally tied to V_{DD} by a 90kohm pull-up resistor.
4	3	C_T	Reset period programming pin. Connection this pin to VDD through a 40kΩ to 200kΩ resistor for 300ms or leaving it open results in fixed delay times 20ms. And connecting this pin with a cap ≥ 100pF to ground a user-programmable delay time.
5	2	SENSE	This pin is connected to the voltage to be monitored. If the voltage at this terminal drops below the threshold voltage VIT, then RESET is asserted.
6	1	V_{DD}	Supply Voltage. Place a 0.1uF ceramic capacitor close to this pin.

Maximum Ratings

Storage Temperature ..... -65°C to +150°C
Operating Junction Temperature, T_J ..... -40°C to +125°C
Input Voltage Range, V_{DD} ..... -0.3V to +7.0V
C_T Voltage Range, V_{CT} ..... -0.3V to V_{DD} +0.5V
Other Voltage Range, $V_{\overline{RESET}}$, $V_{\overline{MR}}$, V_{SENSE} ..... -0.3V to +7.0V
RESET pin Current 5mA
ESD rating, HBM 2kV
ESD rating, CDM 500V

Note:
Stresses greater than those listed under MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

Recommended Operation Conditions

Sym.	Description	Test Conditions	Min.	Typ.	Max.	Unit
VDD	Supply Voltage	-	1.7	--	6.5	V
V_{IH}	Input High Voltage $\overline{\text{MR}}$	-	--	-	VDD	V
	Input High Voltage for Open-drain RESET, SENSE		0	--	6.5	V
V_{IL}	Input Low Voltage $\overline{\text{MR}}$.	-	-	-	0.3VDD	V
T_A	Operating Temperature	-	-40	-	125	°C

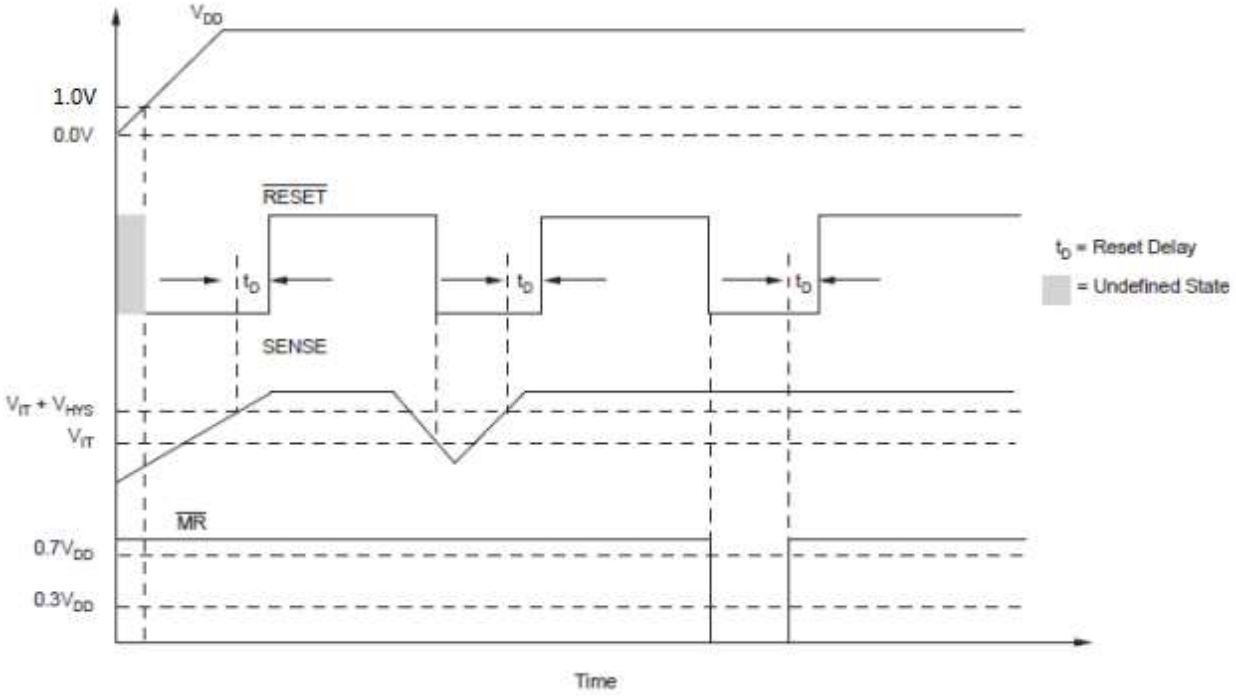
Electrical Characteristics

Unless otherwise specified, -40°C≤T_A≤125°C, 1.7V≤V_{DD}≤6.5V, R_{RESET}=100kΩ, C_{RESET}=50Pf, Typical values are at T_A=+25°C.

Symbol	Parameter	Test Conditions		Min.	Typ.	Max.	Unit
V_{DD}	Supply voltage			1.7	-	6.5	V
I_{DD}	Supply current	V_{DD}=3.3V, $\overline{RESET}$ not asserted, $\overline{MR}$, $\overline{RESET}$, C_T open.		-	2.8	5.0	μA
		V_{DD}=6.5V, $\overline{RESET}$ not asserted, $\overline{MR}$, $\overline{RESET}$, C_T open.		-	3.0	6.0	uA
V_{OL}	Low level output voltage	1.3V≤V_{DD}<1.8V, I_{OL}=0.4mA		-	-	0.3	V
		1.8V≤V_{DD}≤6.5V, I_{OL}=1.0mA		-	-	0.4	
V_{POR}	Power-up reset voltage *	V_{OL}=0.2V, $I_{\overline{RESET}}$=15μA		-	-	1.0	V
V_{IT}	Negative-going input threshold accuracy	PT7M3808G01		-2.0	±1.0	+2.0	%
		V_{IT} ⩽ 3.3 V		-1.5	±0.5	+1.5	
		3.3 V < V_{IT} ⩽ 5.0 V		-2.0	±1.0	+2.0	
V_{HYS}	Hysteresis on V_{IT} pin	PT7M3808G01		-	1.5	3.0	$\%V_{IT}$
		Fixed versions			1	2.5	
$R_{\overline{MR}}$	$\overline{MR}$ Internal pull-up resistance			70	90	-	kΩ
I_{SENSE}	Input current at SENSE pin	PT7M3808G01	V_{SENSE}=V_{IT}	-25		25	nA
		Fixed versions	V_{SENSE}=6.5V	-	1.8	-	μA
I_{OH}	$\overline{RESET}$ Leakage Current	$V_{\overline{RESET}}$=6.5V, $\overline{RESET}$ not asserted		-		300	nA
C_{IN}	Input capacitance, any pin	C_T pin	V_{IN}=0V to V_{DD}	-	5	-	pF
		Other pins	V_{IN}=0V to 6.5V	-	5	-	
V_{IL}	$\overline{MR}$ logic low input	-		0		$0.3V_{DD}$	V
V_{IH}	$\overline{MR}$ logic High input	-		$0.7V_{DD}$		VDD	V
t_W	Input pulse width to $\overline{RESET}$	SENSE	V_{IH}=1.05V_{IT}, V_{IL}=0.95V_{IT}	-	20	-	μs
		$\overline{MR}$	V_{IH}=0.7V_{DD}, V_{IL}=0.3V_{DD}	-	0.001	-	μs
t_D	$\overline{RESET}$ delay time	C_T=open		12	20	28	ms
		C_T=VDD		180	300	420	ms
		C_T=100pF		0.75	1.25	1.75	ms
		C_T=180nF		0.7	1.2	1.7	s
t_{pHL}	Propagation delay	$\overline{MR}$ to $\overline{RESET}$	V_{IH}=0.7V_{DD}, V_{IL}=0.3V_{DD}	-	150	-	ns
	High to low level $\overline{RESET}$ delay	SENSE to $\overline{RESET}$	V_{IH}=1.05V_{IT}, V_{IL}=0.95V_{IT}	-	20	-	us

Note: The lowest supply voltage (V_{DD}) at which $\overline{RESET}$ becomes active. Trise(V_{DD})⩾15us/V.

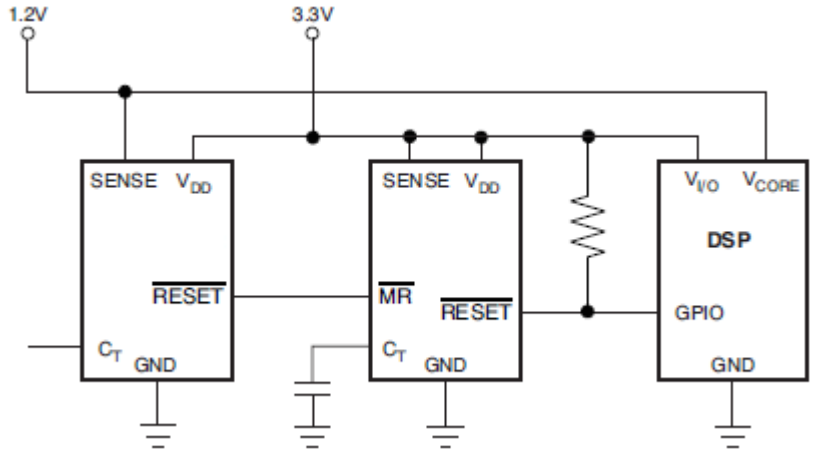
Timing Diagram



Truth Table

$\overline{MR}$	SENSE>VIT	$\overline{RESET}$
L	0	L
L	1	L
H	0	L
H	1	H

Typical application circuit



PT7M3808G12 **PT7M3808G33**

Functional Description

The PT7M3808 microprocessor supervisory product family is designed to assert a $\overline{\text{RESET}}$ signal when either the SENSE pin voltage drops below V_{IT} or the manual reset ($\overline{\text{MR}}$) is driven low. The $\overline{\text{RESET}}$ output remains asserted for a user-adjustable time after both the manual reset ($\overline{\text{MR}}$) and SENSE voltages return above the respective thresholds. A broad range of the voltage threshold and reset delay time adjustments are available, allowing these devices to be used in a wide array of applications. Reset threshold voltages can be factory-set from 0.82V to 3.3V or from 4.4V to 5.0V, while the PT7M3808G01 can be set to any voltage above 0.405V using an external resistor divider. Two preset delay times are also user-selectable: connecting the C_T pin to V_{DD} results in a 300ms reset delay, while leaving the C_T pin open yields a 20ms reset delay. In addition, connecting a capacitor between C_T and GND allows the designer to select any reset delay period from 1.25ms to 10s.

RESET Output

The open-drain $\overline{\text{RESET}}$ output is typically connected to the $\overline{\text{RESET}}$ input of a microprocessor. A pull-up resistor must be used to hold this line high when $\overline{\text{RESET}}$ is not asserted. The $\overline{\text{RESET}}$ output is undefined for voltage below 1.0V, but this is normally not a problem since most microprocessors do not function below this voltage. $\overline{\text{RESET}}$ remains high (unasserted) as long as SENSE is above its threshold(V_{IT}) and the manual reset ($\overline{\text{MR}}$) is logic high. If either SENSE falls below V_{IT} or $\overline{\text{MR}}$ is driven low, $\overline{\text{RESET}}$ is asserted, driving the $\overline{\text{RESET}}$ pin to low impedance.

Once $\overline{\text{MR}}$ is again logic high and SENSE is above V_{IT} + VHYS (the threshold hysteresis), a delay circuit is enabled which holds $\overline{\text{RESET}}$ low for a specified reset delay period. Once the reset delay has expired, the $\overline{\text{RESET}}$ pin goes to a high impedance state. The pull-up resistor from the open-drain $\overline{\text{RESET}}$ to the supply line can be used to allow the reset signal for the microprocessor to have a voltage higher than V_{DD} (up to 6.5V). The pull-up resistor should be no smaller than 10kΩ as a result of the finite impedance of the $\overline{\text{RESET}}$ line.

SENSE Input

The SENSE input provides a pin at which any system voltage can be monitored. If the voltage on this pin drops below V_{IT}, then $\overline{\text{RESET}}$ is asserted. The comparator has a built-in hysteresis to ensure smooth $\overline{\text{RESET}}$ assertions and de-assertions. It is good analog design practice to put a 1nF to 10nF bypass capacitor on the SENSE input to reduce sensitivity to transients and layout parasitic.
The PT7M3808G01 can be used to monitor any voltage rail down to 0.405V by resister divider.

Manual Reset ($\overline{\text{MR}}$) Input

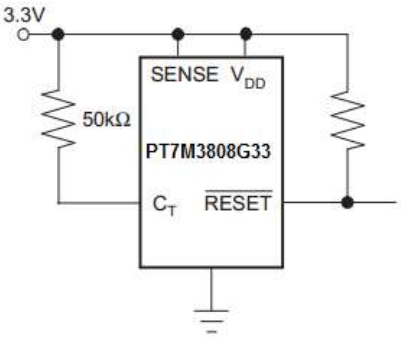
The manual reset ($\overline{\text{MR}}$) input allows a processor or other logic circuits to initiate a reset. A logic low ($0.3V_{DD}$) on $\overline{\text{MR}}$ will cause $\overline{\text{RESET}}$ to assert. After $\overline{\text{MR}}$ returns to a logic high and SENSE is above its reset threshold, $\overline{\text{RESET}}$ is de-asserted after the user defined reset delay expires. Note that $\overline{\text{MR}}$ is internally tied to V_{DD} using a 90kohm resistor so this pin can be left unconnected if $\overline{\text{MR}}$ will not be used. Do not apply voltage level over VDD.

Selecting the RESET Delay Time

The PT7M3808 has three options for setting the $\overline{\text{RESET}}$ delay time.

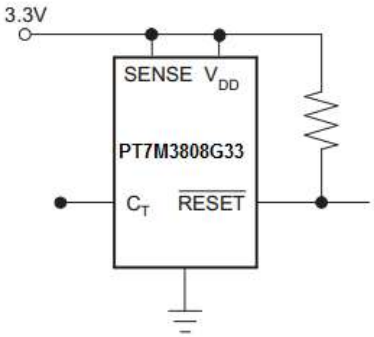
1. A fixed 300ms typical delay time by tying C_T to V_{DD} through a resistor from 40kΩ to 200kΩ. As below Figure (a) shown.
2. A fixed 20ms delay time by leaving the C_T pin open. As below Figure (b) shown.
3. A ground referenced capacitor connected to C_T for a user-defined program time between 1.25ms and 10s. The capacitor C_T should be ≥ 100pF nominal value in order for the PT7M3808xxx to recognize that the capacitor is present. The capacitor value for a given delay time can be calculated using the following equation: $C_T(nF)=[t_D(s)-0.5x10^{-3}(s)]x175$. As below Figure (c) shown.

The reset delay time is determined by the time it takes an on-chip precision 220nA current source to charge the external capacitor to 1.23V. When a $\overline{\text{RESET}}$ is asserted the capacitor is discharged. When the $\overline{\text{RESET}}$ conditions are cleared, the internal current source is enabled and begins to charge the external capacitor. When the voltage on this capacitor reaches 1.23V, $\overline{\text{RESET}}$ is de-asserted. Note that a low leakage type capacitor such as a ceramic should be used and the stray capacitance around this pin may cause errors in the reset delay time.



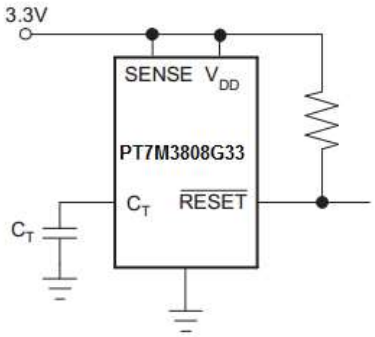
300ms Delay

(a)



20ms Delay

(b)

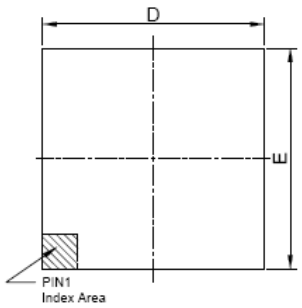


$$\text{Delay (s)} = \frac{C_T\ (nF)}{175} + 0.5 \times 10^{-3}\ (s)$$

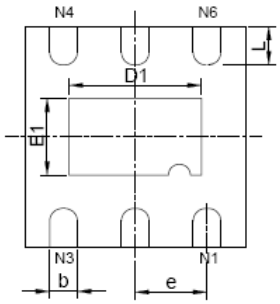
(c)

Mechanical Information

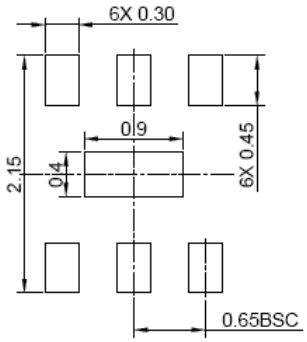
TDFN2.0x2.0-6L



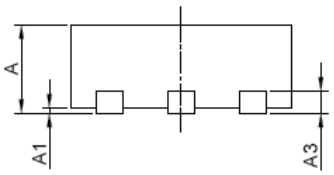
TOP VIEW



BOTTOM VIEW



RECOMMENDED LAND PATTERN(unit:mm)



SIDE VIEW

PKG. DIMENSIONS(MM)		
SYMBOL	Min	Max
A	0.70	0.80
A1	0.00	0.05
A3	0.20 REF	
D	2.00 BSC	
E	2.00 BSC	
D1	1.10	1.30
E1	0.60	0.80
b	0.20	0.30
L	0.27	0.43
e	0.65 BSC	

Note:
1. Ref: JEDEC MO-287A

PERICOM Enabling Serial Connectivity

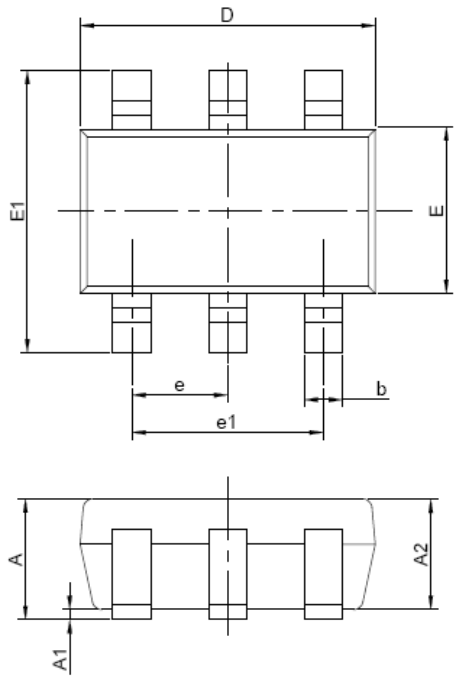
DATE: 12/09/13

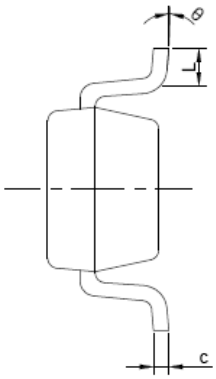
DESCRIPTION: 6-Pin, TDFN, 2X2

PACKAGE CODE: ZC (ZC6)

DOCUMENT CONTROL #: PD-2178 REVISION: --

SOT23-6L





PKG. DIMENSIONS(MM)		
SYMBOL	Min	Max
A	1.05	1.25
A1	0.00	0.10
A2	1.05	1.15
b	0.30	0.50
c	0.10	0.20
D	2.82	3.02
E	1.50	1.70
E1	2.65	2.95
e	0.95 BSC	
e1	1.80	2.00
L	0.30	0.60
θ	0°	8°

Note:
1. Ref: JEDEC MO-178C/AB

PERICOM Enabling Serial Connectivity

DATE: 06/18/13

DESCRIPTION: 6-Pin, Small Outline Transistor Plastic Package (SOT23)

PACKAGE CODE: TA (TA6)

DOCUMENT CONTROL #: PD-2145 REVISION:--

Ordering Information

Part No.	Package Code	Package
PT7M3808GxxxZCE	ZC	6-pin, 2.0x2.0 (TDFN)
PT7M3808GxxxZCEX	ZC	6-pin, 2.0x2.0 (TDFN), Tape & Reel
PT7M3808Gxxx TAE	TA	6-pin, Small Outline Transistor Plastic Package (SOT23)
PT7M3808Gxxx TAEX	TA	6-pin, Small Outline Transistor Plastic Package (SOT23), Tape & Reel

Note:

- E = Pb-free and Green
- Adding X Suffix= Tape/Reel
- xxx shows different function, see below ***Function Comparison Table***.

Function Comparison Table

Product	Nominal Supply Voltage	SENSE Threshold Voltage(V_{IT})
PT7M3808G01	adjustable	0.405V
PT7M3808G09	0.9V	0.84V
PT7M3808G12	1.2V	1.12V
PT7M3808G125	1.25V	1.16V
PT7M3808G15	1.5V	1.40V
PT7M3808G18	1.8V	1.67V
PT7M3808G19	1.9V	1.77V
PT7M3808G25	2.5V	2.33V
PT7M3808G30	3.0V	2.79V
PT7M3808G33	3.3V	3.07V
PT7M3808G50	5.0V	4.65V

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