

## DESCRIPTION

The MPM3814C is synchronous, step-down power module with an integrated inductor. The MPM3814C achieves 1A of continuous output current ( $I_{OUT}$ ) from a 2.75V to 6V input voltage ( $V_{IN}$ ) range, with excellent load and line regulation. The MPM3814C works in forced continuous conduction mode (FCCM) and has a small output voltage ( $V_{OUT}$ ) ripple with one output capacitor. This makes the device well-suited for optical modules, FPGA, ASIC, and other applications requiring low ripple noise and a small PCB area.

$V_{OUT}$  can be regulated to be as low as 0.6V. Only FB resistors, input capacitors, and output capacitors are required to complete the design. Constant-on-time control (COT) provides fast transient response, high efficiency, and easy loop stabilization.

Full protection features include cycle-by-cycle current limiting, short-circuit protection (SCP) with hiccup mode, and thermal shutdown.

The MPM3814C requires a minimal number of readily available, standard external components. It is available in an ultra-small ECLGA-14 (2.5mmx2.5mmx1.2mm) package.

## FEATURES

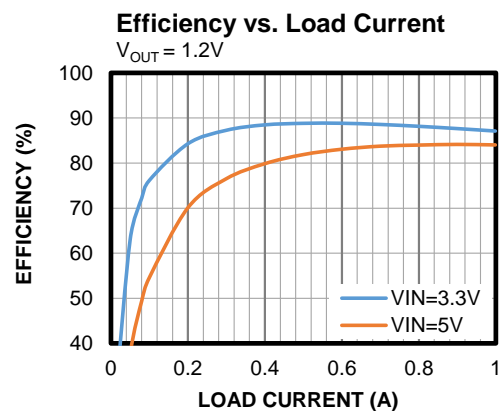
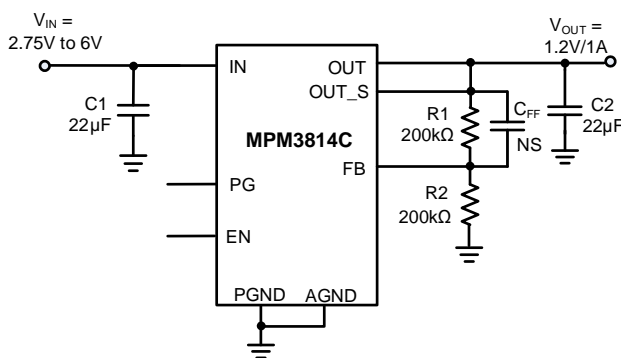
- Wide 2.75V to 6V Operating Input Voltage ( $V_{IN}$ ) Range
- Adjustable Output Voltage ( $V_{OUT}$ ) from 0.6V
- Up to 1A Continuous Output Current ( $I_{OUT}$ )
- 100% Duty Cycle in Dropout
- Up to 92.3% Efficiency with 3.3V to 1.8V
- Forced Continuous Conduction Mode (FCCM)
- Enable (EN) and Power Good (PG) for Power Sequencing
- Cycle-by-Cycle Over-Current Protection (OCP)
- Short-Circuit Protection (SCP) with Hiccup Mode
- Only Four External Components Required
- Available in an ECLGA-14 (2.5mmx2.5mmx1.2mm) Package

## APPLICATIONS

- FPGA, ASIC, DSP Power
- Optical Modules
- LDO Replacements
- Power for Portable Products
- Storage (Solid-State Drives and Hard-Disk Drives)
- Space-Constrained Applications

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## TYPICAL APPLICATION



### ORDERING INFORMATION

| Part Number* | Package                   | Top Marking | MSL Rating |
|--------------|---------------------------|-------------|------------|
| MPM3814CGPA  | ECLGA-14<br>(2.5mmx2.5mm) | See Below   | 3          |

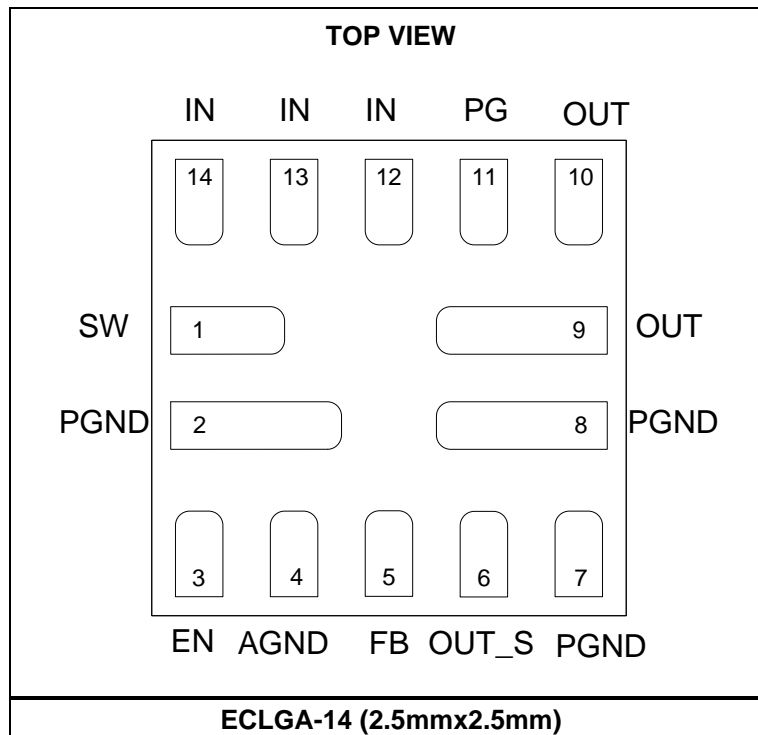
\* For Tape & Reel, add suffix -Z (e.g. MPM3814CGPA-Z).

### TOP MARKING

**BTK**  
**YWW**  
**LLL**

BTK: Product code of MPM3814CGPA  
Y: Year code  
WW: Week code  
LLL: Lot number

### PACKAGE REFERENCE



## PIN FUNCTIONS

| Pin #      | Name  | Description  |
|------------|-------|--|
| 1          | SW    | <b>SW test pin.</b> Float the SW pin.  |
| 2, 7, 8    | PGND  | <b>Power ground.</b>   |
| 3          | EN    | <b>On/off control.</b>   |
| 4          | AGND  | <b>Analog ground for the internal control circuit.</b> The AGND pin is not connected to PGND internally. Connect AGND to the PGND on the PCB layout.   |
| 5          | FB    | <b>Feedback.</b> Use an external resistor divider from the output to AGND, tapped to the FB pin, to set the output voltage ( $V_{OUT}$ ).  |
| 6          | OUT_S | <b>Output voltage sense.</b>   |
| 9, 10      | OUT   | <b>Power output.</b>   |
| 11         | PG    | <b>Power good indicator.</b> The output of the PG pin is an open drain with an internal pull-up resistor connected to the IN pin. PG is pulled up to IN when the FB voltage is within 10% of the regulation level; otherwise, PG is low. |
| 12, 13, 14 | IN    | <b>Power input.</b>  |

### ABSOLUTE MAXIMUM RATINGS <sup>(1)</sup>

$V_{SW}$  .....  
 -0.3V (-5V for <10ns) to +6.5V (10V for <10ns)  
 All other pins ..... -0.3V to +6.5V  
 Continuous power dissipation ( $T_A = 25^\circ\text{C}$ )<sup>(5)</sup>  
 ECLGA-14 (2.5mmx2.5mm) ..... 2.2W  
 Junction temperature ..... 150°C  
 Lead temperature ..... 260°C  
 Storage temperature ..... -65°C to +150°C

### ESD Ratings

Human body model (HBM) ..... 2000V  
 Charged device model (CDM) ..... 2000V

### Recommended Operating Conditions <sup>(2)</sup>

Operation input voltage range ..... 2.75V to 6V  
 Operating junction temp ( $T_J$ ).... -40°C to +125°C

### Thermal Resistance <sup>(3) (4) (5) (6) (7)</sup>

ECLGA-14 (2.5mmx2.5mm)

$\theta_{JA}$  ..... 56.7°C/W

$\theta_{JC\_TOP}$  ..... 6.85°C/W

$\theta_{JB}$  ..... 25.5°C/W

#### Notes:

- Exceeding these ratings may damage the device.
- The device is not guaranteed to function outside of its operating conditions.
- $\theta_{JA}$  is the junction-to-ambient thermal resistance,  $\theta_{JC\_TOP}$  is the junction-to-case top thermal characterization parameter, and  $\theta_{JB}$  is the junction-to-board thermal characterization parameter.
- The thermal parameter is based on the test on the MPS evaluation board (T-EVM3814C-PA-00A) under a no airflow cooling condition in a standard enclosure. The board size is 5.1cmx5.1cm, 2-layer, of which top and bottom layer Cu thickness is 2oz.
- The maximum allowable power dissipation is a function of the maximum junction temperature,  $T_J$  (MAX), the junction-to-ambient thermal resistance,  $\theta_{JA}$ , and the ambient temperature,  $T_A$ . The maximum allowable continuous power dissipation at any ambient temperature is calculated by  $P_D$  (MAX) =  $(T_J$  (MAX) -  $T_A$ ) /  $\theta_{JA}$ . Exceeding the maximum allowable power dissipation produces an excessive die temperature.
- The junction-to-case top thermal characterization parameter,  $\theta_{JC\_TOP}$ , estimates the junction temperature in the real system, based on equation  $T_J = \theta_{JC\_TOP} \times P_{LOSS} + T_{CASE\_TOP}$ . Where  $P_{LOSS}$  is the entire loss of the module in real applications, and  $T_{CASE\_TOP}$  is case top temperature
- The junction-to-board thermal characterization parameter,  $\theta_{JB}$ , estimating the junction temperature in the real system, based on equation  $T_J = \theta_{JB} \times P_{LOSS} + T_{BOARD}$ . Where  $P_{LOSS}$  is the entire power loss of the module in real applications, and  $T_{BOARD}$  is board temperature.

## ELECTRICAL CHARACTERISTICS

$V_{IN} = 3.6V$ ,  $T_J = -40^{\circ}C$  to  $+125^{\circ}C$  <sup>(8)</sup>, typical value is tested at  $T_J = 25^{\circ}C$ , the over-temperature limit is guaranteed by characterization, unless otherwise noted.

| Parameter  | Symbol        | Condition  | Min | Typ  | Max  | Units      |
|--|---------------|--|-----|------|------|------------|
| Feedback (FB) voltage                                | $V_{FB}$      | $2.75V \leq V_{IN} \leq 6V$  | 591 | 600  | 609  | mV         |
| FB current   | $I_{FB}$      | $V_{FB} = 0.6V$  |     | 10   |      | nA         |
| Dropout resistance                                   | $R_{DR}$      | 100% on duty cycle   |     | 105  |      | m $\Omega$ |
| Switch leakage                                       |               | $V_{EN} = 0V$ , $V_{IN} = 6V$ , $V_{SW} = 0V$ and $6V$ , $T_J = 25^{\circ}C$ |     | 0    | 2    | $\mu A$    |
| P-channel MOSFET peak current limit                  |               | $T_J = 25^{\circ}C$  | 1.6 | 2    |      | A          |
| N-channel MOSFET valley current limit <sup>(8)</sup> |               |  |     | 1.5  |      | A          |
| On time  |               | $V_{IN} = 3.6V$ , $V_{OUT} = 1.2V$   |     | 130  |      | ns         |
| Switching frequency                                  | $f_{SW}$      | $V_{OUT} = 1.2V$ , $I_{LOAD} = 1A$   |     | 2200 |      | kHz        |
| Minimum off time <sup>(9)</sup>                      | $t_{MIN-OFF}$ |  |     | 100  |      | ns         |
| Minimum on time <sup>(9)</sup>                       | $t_{MIN-ON}$  |  |     | 80   |      | ns         |
| Soft-start time <sup>(9)</sup>                       | $t_{SS-ON}$   |  |     | 1.7  |      | ms         |
| Soft-stop time                                       | $t_{SS-OFF}$  |  |     | 2    |      | ms         |
| Power good (PG) upper trip threshold                 | $PG_{OV}$     | FB voltage in respect to the regulation                                      |     | 7    |      | %          |
| PG lower trip threshold                              | $PG_{UV}$     |  |     | -12  |      | %          |
| PG delay   |               |  |     | 100  |      | $\mu s$    |
| PG sink current capability                           | $V_{PG\_LO}$  | Sink 1mA   |     |      | 0.4  | V          |
| PG logic high voltage                                | $V_{PG\_HI}$  | $V_{IN} = 5V$ , $V_{FB} = 0.6V$  | 4   |      |      | V          |
| PG internal pull-up resistor                         | $R_{PG}$      |  |     | 440  |      | k $\Omega$ |
| Under-voltage lockout (UVLO) rising threshold        |               |  | 2.3 | 2.5  | 2.75 | V          |
| UVLO threshold hysteresis                            |               |  |     | 400  |      | mV         |
| EN input logic low voltage                           |               |  |     |      | 0.3  | V          |
| EN input logic high voltage                          |               |  | 1.2 |      |      | V          |
| EN input current                                     |               | $V_{EN} = 2V$  |     | 2    |      | $\mu A$    |
|  |               | $V_{EN} = 0V$  |     | 0    |      | $\mu A$    |
| Supply current (shutdown)                            |               | $V_{EN} = 0V$ , $T_J = 25^{\circ}C$  |     | 0    | 1    | $\mu A$    |
| Supply current (quiescent)                           |               | $V_{EN} = 2V$ , $V_{FB} = 0.63V$ , $V_{IN} = 3.6V$                           |     | 500  |      | $\mu A$    |

**ELECTRICAL CHARACTERISTICS (continued)**

$V_{IN} = 3.6V$ ,  $T_J = -40^{\circ}C$  to  $+125^{\circ}C$  <sup>(8)</sup>, typical value is tested at  $T_J = 25^{\circ}C$ , the over-temperature limit is guaranteed by characterization, unless otherwise noted.

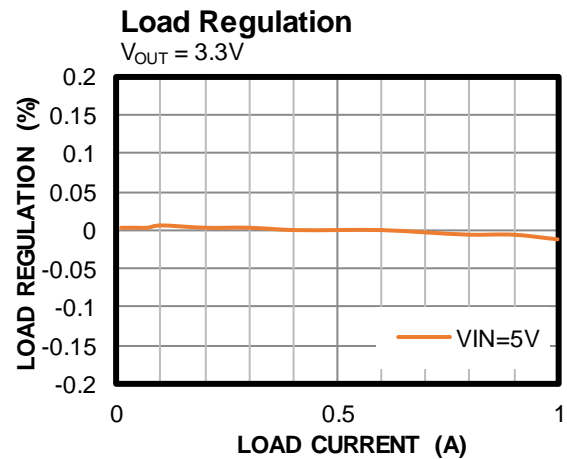
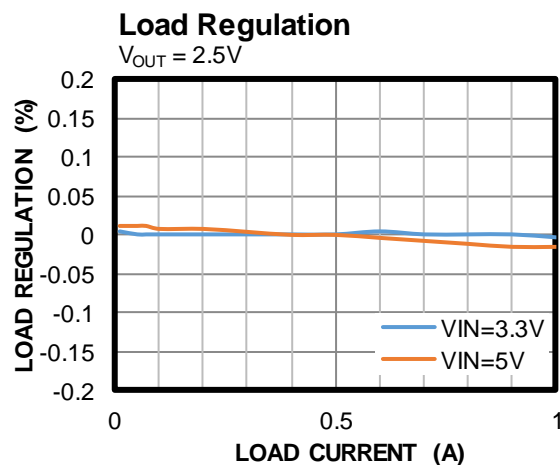
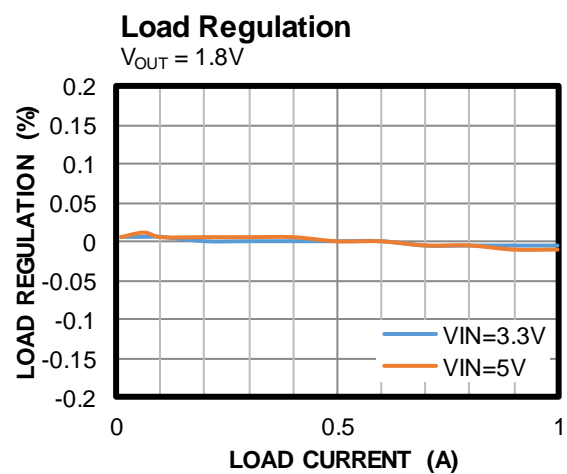
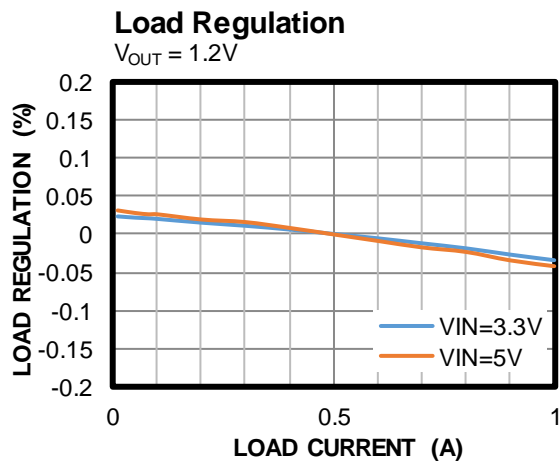
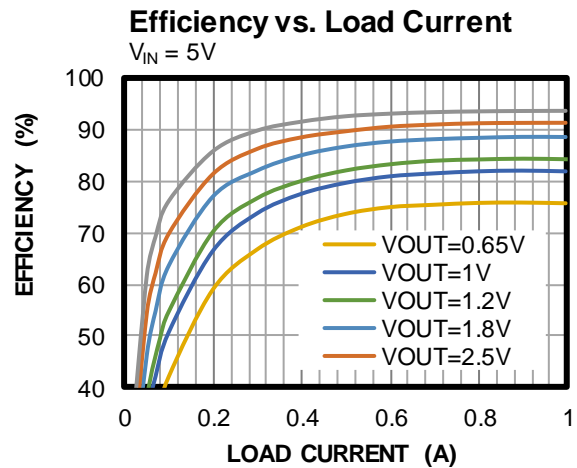
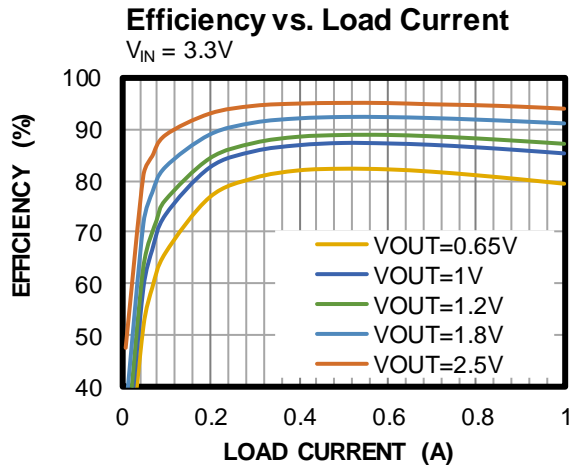
| Parameter  | Symbol     | Condition   | Min | Typ | Max | Units       |
|--|------------|---|-----|-----|-----|-------------|
| <b>Converter System</b> <sup>(9)</sup>             |            |   |     |     |     |             |
| Output voltage range <sup>(9)</sup>                |            |   | 0.6 |     | 6   | V           |
| Recommended input capacitance <sup>(9)</sup>       | $C_{IN1}$  | $V_{IN} = 3.6V$ , $V_{OUT} = 1.2V$ , $I_{OUT} = 1A$   | 4.7 | 22  |     | $\mu F$     |
| Output capacitance <sup>(9)</sup>                  | $C_{OUT1}$ | $V_{IN} = 3.6V$ , $V_{OUT} = 1.2V$ , $I_{OUT} = 1A$   | 10  | 22  |     | $\mu F$     |
| Output ripple <sup>(9)</sup>                       |            | $V_{IN} = 3.6V$ , $V_{OUT} = 1.2V$ ,<br>$C_{OUT} = 22\mu F$ , $I_{OUT} = 1A$                          |     | 5   |     | mV          |
| Efficiency <sup>(9)</sup>                          |            | $V_{IN} = 3.6V$ , $V_{OUT} = 1.2V$ , $I_{OUT} = 1A$   |     | 87  |     | %           |
| Load transient peak-to-peak voltage <sup>(9)</sup> | $V_{P2P1}$ | $V_{IN} = 3.6V$ , $V_{OUT} = 1.2V$ ,<br>$C_{OUT} = 22\mu F$ , $I_{OUT} = 0A$ to $1A$ at<br>$1A/\mu s$ |     |     | 36  | mV          |
| Thermal shutdown <sup>(9)</sup>                    |            |   |     | 150 |     | $^{\circ}C$ |
| Thermal hysteresis <sup>(9)</sup>                  |            |   |     | 30  |     | $^{\circ}C$ |

**Notes:**

- 8) Not tested in production. Guaranteed by over-temperature correlation.  
 9) Guaranteed by engineering sample characterization.

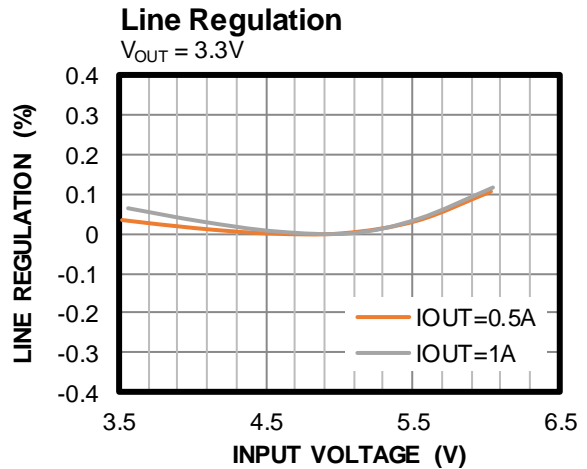
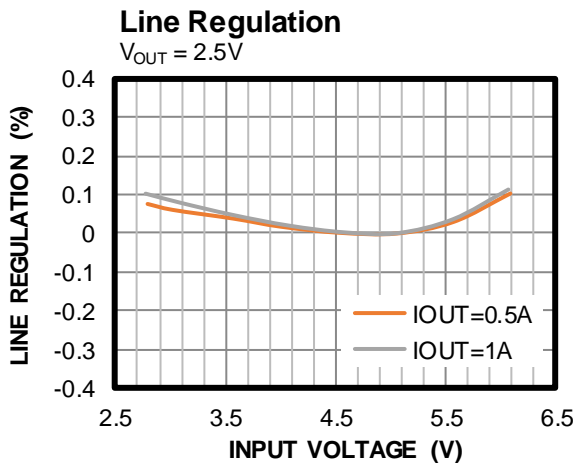
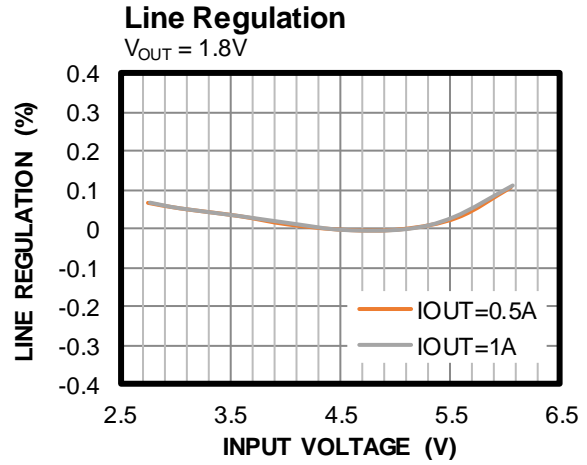
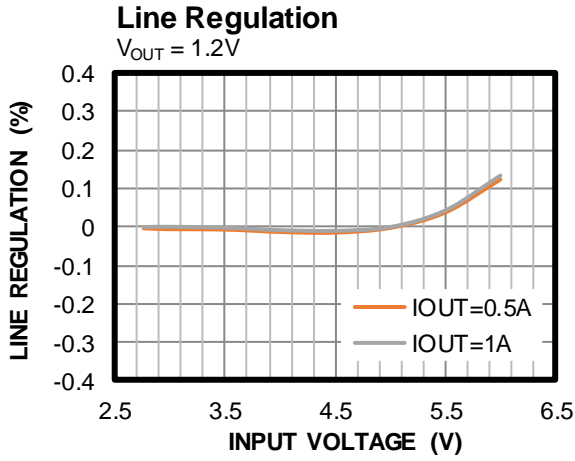
## TYPICAL CHARACTERISTICS

Performance curves are tested on the evaluation board.  $V_{IN} = 5V$ ,  $V_{OUT} = 1.2V$ ,  $C_{IN} = 22\mu F$ ,  $C_{OUT} = 22\mu F$ ,  $T_A = 25^\circ C$ , unless otherwise noted.

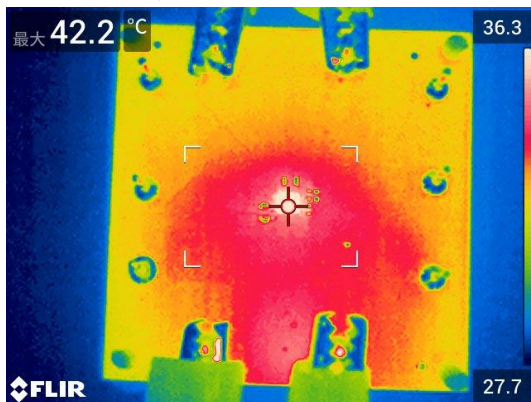


### TYPICAL CHARACTERISTICS (continued)

Performance curves are tested on the evaluation board.  $V_{IN} = 5V$ ,  $V_{OUT} = 1.2V$ ,  $C_{IN} = 22\mu F$ ,  $C_{OUT} = 22\mu F$ ,  $T_A = 25^\circ C$ , unless otherwise noted.



**Thermal Result**  
 $I_{OUT} = 1A$ , 4-layer PCB

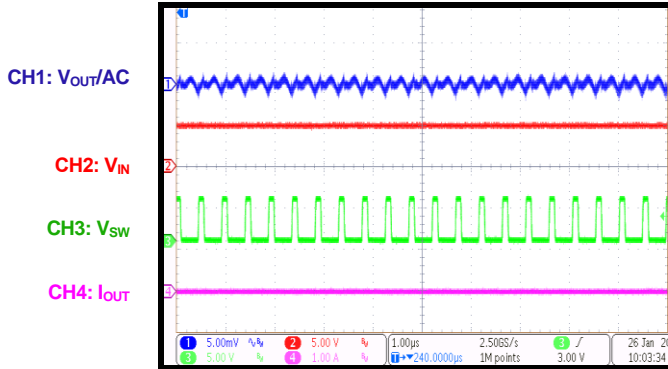


## TYPICAL PERFORMANCE CHARACTERISTICS

Performance waveforms are tested on the evaluation board.  $V_{IN} = 5V$ ,  $V_{OUT} = 1.2V$ ,  $C_{IN} = 22\mu F$ ,  $C_{OUT} = 22\mu F$ ,  $T_A = 25^\circ C$ , unless otherwise noted.

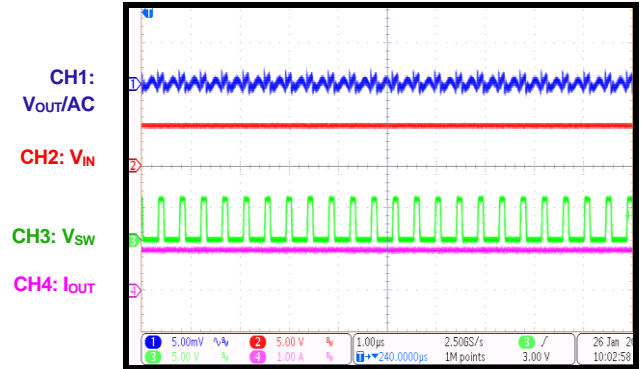
### Steady State

$V_{IN} = 5V$ ,  $V_{OUT} = 1.2V$ ,  $I_{OUT} = 0A$



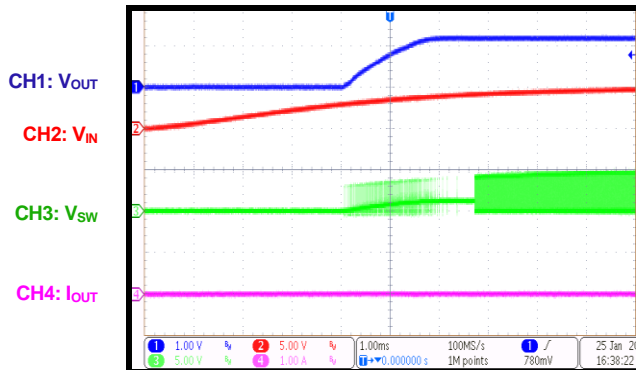
### Steady State

$V_{IN} = 5V$ ,  $V_{OUT} = 1.2V$ ,  $I_{OUT} = 1A$



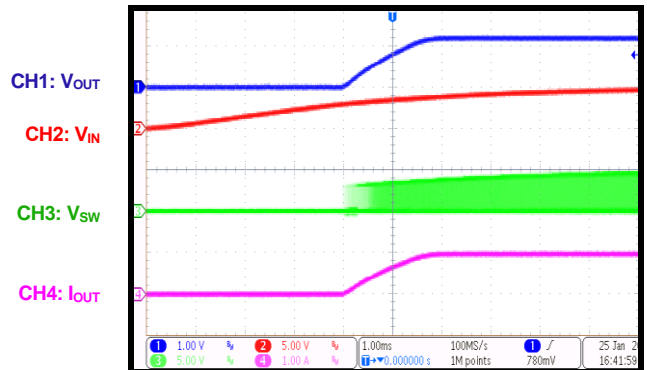
### Start-Up through $V_{IN}$

$V_{IN} = 5V$ ,  $V_{OUT} = 1.2V$ ,  $I_{OUT} = 0A$



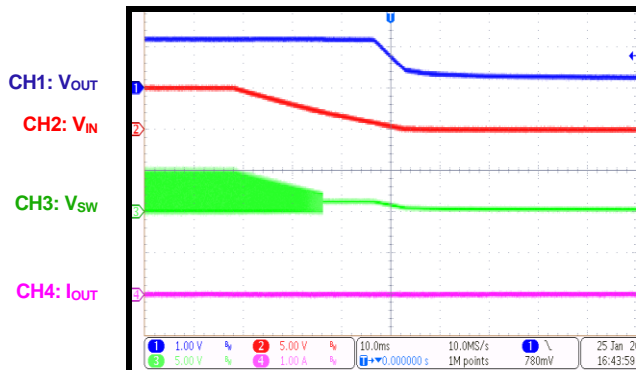
### Start-Up through $V_{IN}$

$V_{IN} = 5V$ ,  $V_{OUT} = 1.2V$ ,  $I_{OUT} = 1A$



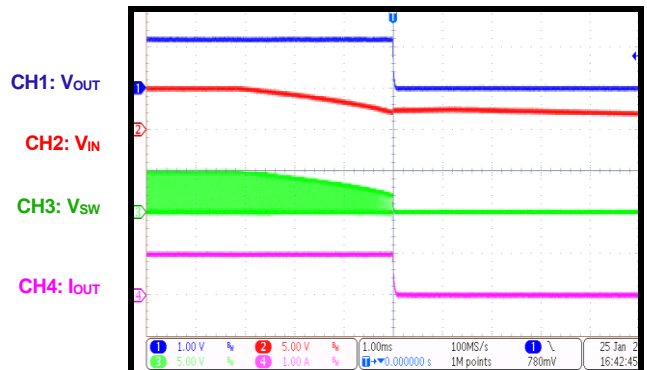
### Shutdown through $V_{IN}$

$V_{IN} = 5V$ ,  $V_{OUT} = 1.2V$ ,  $I_{OUT} = 0A$



### Shutdown through $V_{IN}$

$V_{IN} = 5V$ ,  $V_{OUT} = 1.2V$ ,  $I_{OUT} = 1A$



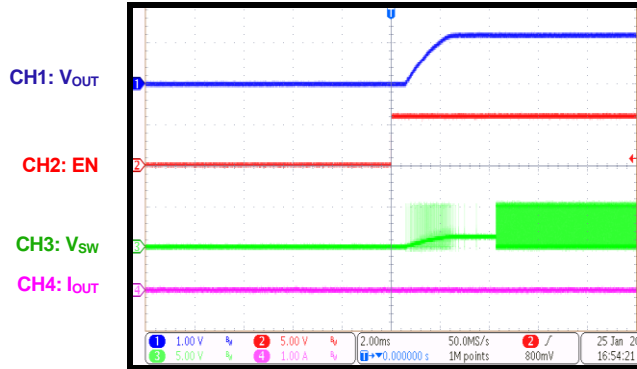


## TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

Performance waveforms are tested on the evaluation board.  $V_{IN} = 5V$ ,  $V_{OUT} = 1.2V$ ,  $C_{IN} = 22\mu F$ ,  $C_{OUT} = 22\mu F$ ,  $T_A = 25^\circ C$ , unless otherwise noted.

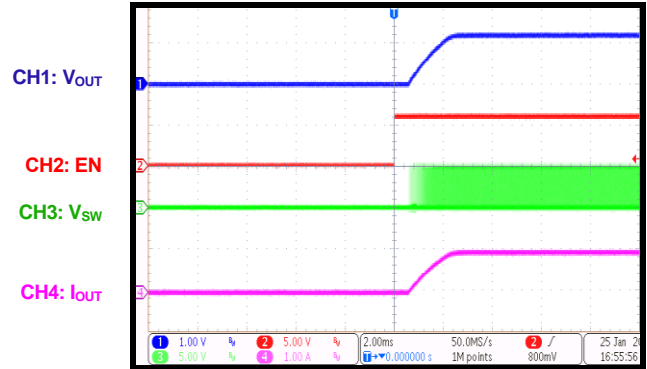
### Start-Up through EN

$V_{IN} = 5V$ ,  $V_{OUT} = 1.2V$ ,  $I_{OUT} = 0A$



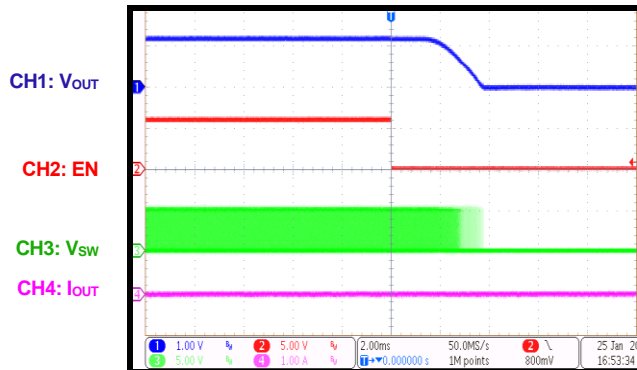
### Start-Up through EN

$V_{IN} = 5V$ ,  $V_{OUT} = 1.2V$ ,  $I_{OUT} = 1A$



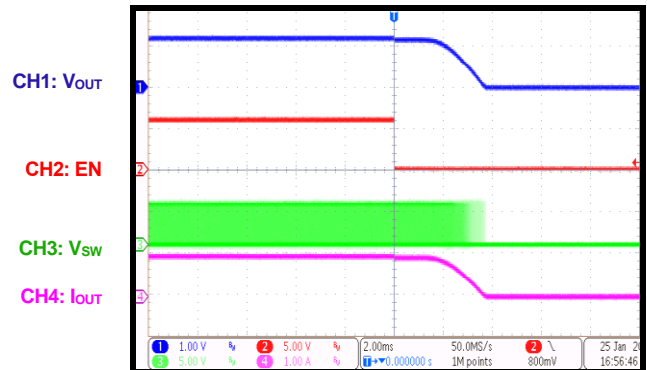
### Shutdown through EN

$V_{IN} = 5V$ ,  $V_{OUT} = 1.2V$ ,  $I_{OUT} = 0A$



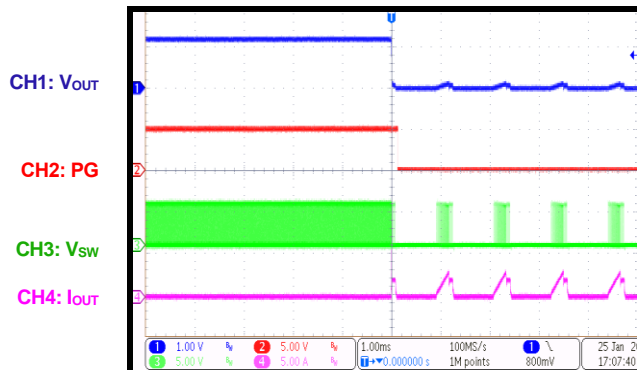
### Shutdown through EN

$V_{IN} = 5V$ ,  $V_{OUT} = 1.2V$ ,  $I_{OUT} = 1A$



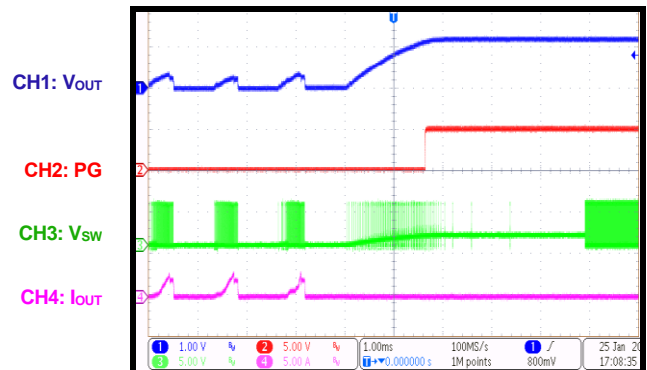
### SCP Entry

$V_{IN} = 5V$ ,  $V_{OUT} = 1.2V$ ,  $I_{OUT} = 0A$



### SCP Recovery

$V_{IN} = 5V$ ,  $V_{OUT} = 1.2V$ ,  $I_{OUT} = 0A$

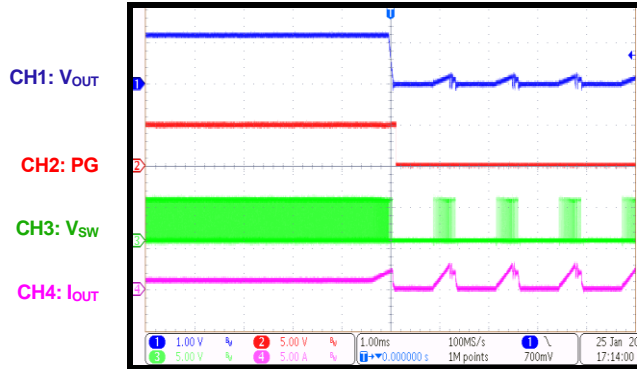


### TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

Performance waveforms are tested on the evaluation board.  $V_{IN} = 5V$ ,  $V_{OUT} = 1.2V$ ,  $C_{IN} = 22\mu F$ ,  $C_{OUT} = 22\mu F$ ,  $T_A = 25^\circ C$ , unless otherwise noted.

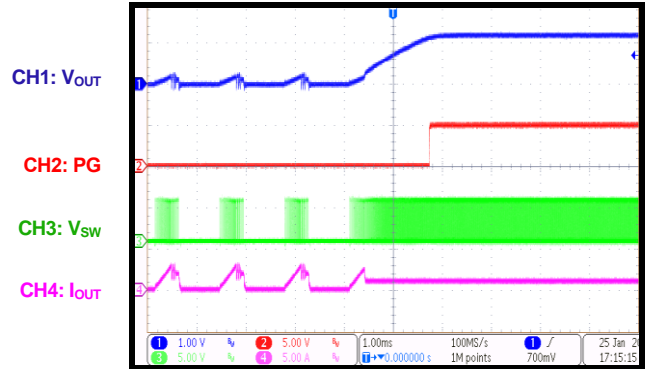
#### SCP Entry

$V_{IN} = 5V$ ,  $V_{OUT} = 1.2V$ ,  $I_{OUT} = 1A$



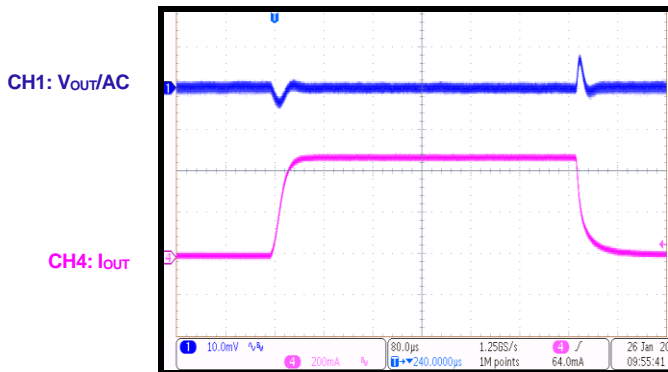
#### SCP Recovery

$V_{IN} = 5V$ ,  $V_{OUT} = 1.2V$ ,  $I_{OUT} = 1A$



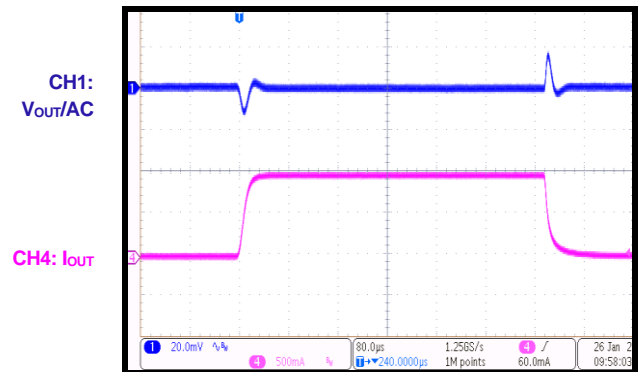
#### Load Transient

$V_{IN} = 5V$ ,  $V_{OUT} = 1.2V$ ,  $I_{OUT} = 0A$  to  $0.5A$ ,  $2.5A/\mu s$  e-load



#### Load Transient

$V_{IN} = 5V$ ,  $V_{OUT} = 1.2V$ ,  $I_{OUT} = 0A$  to  $1A$ ,  $2.5A/\mu s$  e-load



## FUNCTIONAL BLOCK DIAGRAM

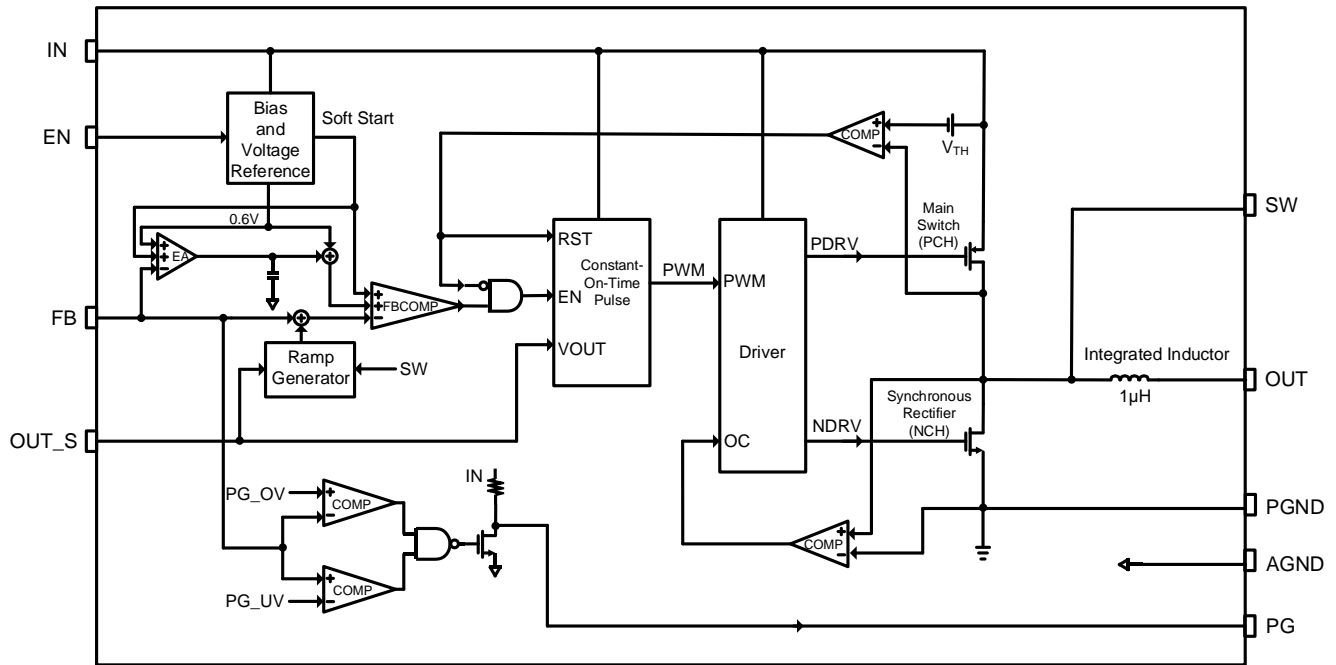


Figure 1: Functional Block Diagram

## OPERATION

The MPM3814C comes in a small surface-mounted ECLGA-14 (2.5mmx2.5mmx1.2mm) package. The MPM3814C's integrated inductor simplifies the schematic and layout design. Only FB resistors, input capacitors, and output capacitors are required to complete the design. The MPM3814C uses constant-on-time (COT) control with input voltage feed-forward to stabilize the switching frequency ( $f_{sw}$ ) across the full input range.

### Constant-On-Time Control (COT)

Compared to fixed-frequency pulse-width modulation (PWM) control, COT control offers the advantage of a simpler control loop and faster transient response. By using input voltage feed-forward, the MPM3814C maintains a nearly constant  $f_{sw}$  across the input and output voltage ranges. The on time of the switching pulse can be estimated with Equation (1):

$$t_{ON} = \frac{V_{OUT}}{V_{IN}} \times \frac{1}{f_{sw}} \quad (1)$$

To prevent inductor current runaway during the load transition, the MPM3814C fixes the minimum off time. This minimum off time limit does not affect operation during steady state.

### Forced PWM Operation

The MPM3814C works in continuous conduction mode (CCM) to achieve a smaller output voltage ripple, load regulation, and load transient response across the full load range.

### Enable (EN)

If the input voltage ( $V_{IN}$ ) exceeds the under-voltage lockout (UVLO) threshold (typically 2.5V), the MPM3814C can be enabled by pulling EN above 1.2V. Leave EN floating or pull EN down to ground to disable the MPM3814C. There is an internal pull-down resistor connected from EN to ground.

### Soft Start and Soft Shutdown

The MPM3821C has a built-in soft start that ramps up  $V_{OUT}$  at a controlled slew rate to prevent overshoot during start-up. The soft-start time is  $t_{SS-ON}$ .

When disabled, the MPM3824C ramps down the internal reference, so the load can discharge the output linearly. The soft-shutdown time is  $t_{SS-OFF}$ .

### Power Good (PG) Indicator

The MPM3814C has an open-drain power good (PG) indication pin with a pull-up resistor ( $R_{PG}$ ). When FB is within PG\_OV and PG\_UV, PG is pulled up to IN by the internal resistor. If the FB voltage is out of this window, PG is pulled down to ground by an internal MOSFET. The MOSFET has a maximum  $R_{DS(ON)}$  of 100Ω.

### Current Limit

The MPM3814C's high-side MOSFET (HS-FET) has a typical peak current limit, and the low-side MOSFET (LS-FET) has a valley current limit. When the HS-FET reaches its current limit, the HS-FET turns off, and the LS-FET turns on. When the current drops to the valley current limit threshold, the MPM3814C turns on the HS-FET again.

If the HS-FET reaches the peak current limit or the LS-FET reaches the valley current limit in every cycle for about 64 cycles, the MPM3814C initiates hiccup mode. It remains in hiccup mode until the current decreases. This prevents the inductor current from continuously rising and damaging components.

### Short-Circuit Protection (SCP) and Recovery

If the output is shorted to GND, the current limit is triggered. If the current limit is triggered every cycle for about 64 cycles, the MPM3814C enters hiccup mode and disables the output power stage. The MPM3814C discharges the soft-start capacitor, then automatically attempts to soft start again. If the short-circuit condition remains after soft start ends, the MPM3814C repeats this operation until the short circuit is removed and the output rises back to the regulation level.

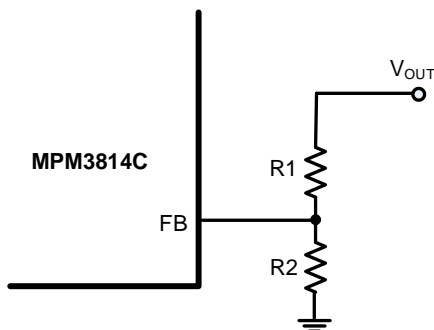
## APPLICATION INFORMATION

### Setting the Output Voltage

The external resistor divider sets the output voltage ( $V_{OUT}$ ). Consider the tradeoff between stability and dynamics to choose a feedback resistor ( $R1$ ) that is not too large or too small. There is no strict requirement for the feedback resistor.  $R2$  can be calculated with Equation (2):

$$R2 = \frac{R1}{\frac{V_{OUT}}{0.6} - 1} \quad (2)$$

Figure 2 shows the feedback circuit.



**Figure 2: Feedback Network**

Table 1 lists the recommended resistor values for common output voltages.

**Table 1: Resistor Values for Common Output Voltages**

| $V_{OUT}$ (V) | $R1$ (k $\Omega$ ) | $R2$ (k $\Omega$ ) |
|---------------|--------------------|--------------------|
| 1.0           | 200 (1%)           | 300 (1%)           |
| 1.2           | 200 (1%)           | 200 (1%)           |
| 1.8           | 200 (1%)           | 100 (1%)           |
| 2.5           | 200 (1%)           | 63.2 (1%)          |
| 3.3           | 200 (1%)           | 44.2 (1%)          |

### Selecting the Input Capacitor

The step-down converter has a discontinuous input current, and requires a capacitor to supply AC current while maintaining the DC input voltage. For optimal performance, use low-ESR capacitors. Ceramic capacitors with X5R or X7R dielectrics are highly recommended because of their low ESR and small temperature coefficients. For most applications, a 22 $\mu$ F capacitor is sufficient.

Since the input capacitor absorbs the input switching current, it requires an adequate ripple current rating. The RMS current in the input capacitor can be estimated with Equation (3):

$$I_{C1} = I_{LOAD} \times \sqrt{\frac{V_{OUT}}{V_{IN}} \times \left(1 - \frac{V_{OUT}}{V_{IN}}\right)} \quad (3)$$

The worst-case condition occurs at  $V_{IN} = 2 \times V_{OUT}$ , estimated with Equation (4):

$$I_{C1} = \frac{I_{LOAD}}{2} \quad (4)$$

For simplification, choose an input capacitor with an RMS current rating greater than half of the maximum load current.

The input capacitor can be electrolytic, tantalum, or ceramic. When using electrolytic or tantalum capacitors, add a small, high-quality ceramic capacitor (i.e. 0.1 $\mu$ F) as close to the IC as possible. When using ceramic capacitors, ensure that they have enough capacitance to provide a sufficient charge to prevent an excessive voltage ripple at the input. The input voltage ripple caused by the capacitance can be calculated with Equation (5):

$$\Delta V_{IN} = \frac{I_{LOAD}}{f_{SW} \times C1} \times \frac{V_{OUT}}{V_{IN}} \times \left(1 - \frac{V_{OUT}}{V_{IN}}\right) \quad (5)$$

### Selecting the Output Capacitor

An output capacitor ( $C2$ ) is required to maintain the DC output voltage.

Low-ESR ceramic capacitors can be used to keep the output voltage ripple low. Generally, a 22 $\mu$ F output ceramic capacitor is sufficient for most applications. If  $V_{OUT}$  is higher, a 47 $\mu$ F capacitor may be required to stabilize the system.

When using ceramic capacitors, the capacitance dominates the impedance at the switching frequency and causes the majority of the output voltage ripple. For simplification, the output voltage ripple can be estimated with Equation (6):

$$\Delta V_{OUT} = \frac{V_{OUT}}{8 \times f_{SW}^2 \times L_1 \times C2} \times \left(1 - \frac{V_{OUT}}{V_{IN}}\right) \quad (6)$$

When using tantalum or electrolytic capacitors, the ESR dominates the impedance at the switching frequency. For simplification, the output ripple can be calculated with Equation (7):

$$\Delta V_{OUT} = \frac{V_{OUT}}{f_{SW} \times L_1} \times \left(1 - \frac{V_{OUT}}{V_{IN}}\right) \times R_{ESR} \quad (7)$$

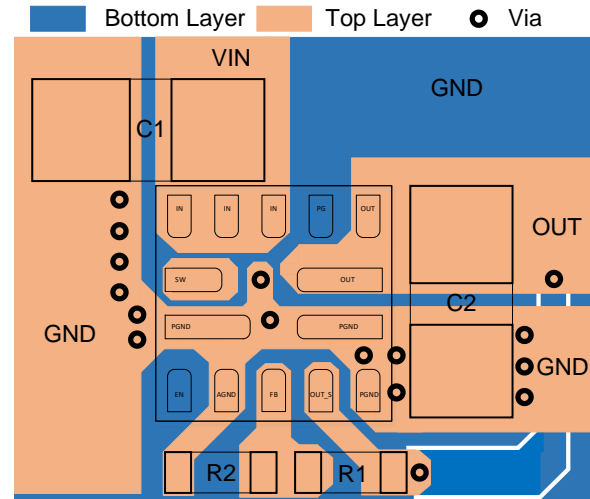
Where L1 is the 1μH integrated inductor.

The output capacitor's characteristics affect the stability of the regulation system.

### PCB Layout Guidelines

An efficient layout for the switching power supplies is critical for stable operation, especially for the high switching frequency converter. A poorly optimized layout can result in poor line for the regulator or load regulation or stability issues. For the best results, refer to Figure 3 and follow the guidelines below:

1. Place a 0805-sized ceramic input capacitor as close to the IC pins as possible.
2. Place a 0402-sized capacitor place at the bottom of the IC (optional).
3. Connect the two ends of the ceramic capacitor directly to IN and PGND.
4. Place the external feedback resistor next to FB.
5. Connect AGND and PGND at a single point.



**Figure 3: Recommended PCB layout**

## TYPICAL APPLICATION CIRCUIT

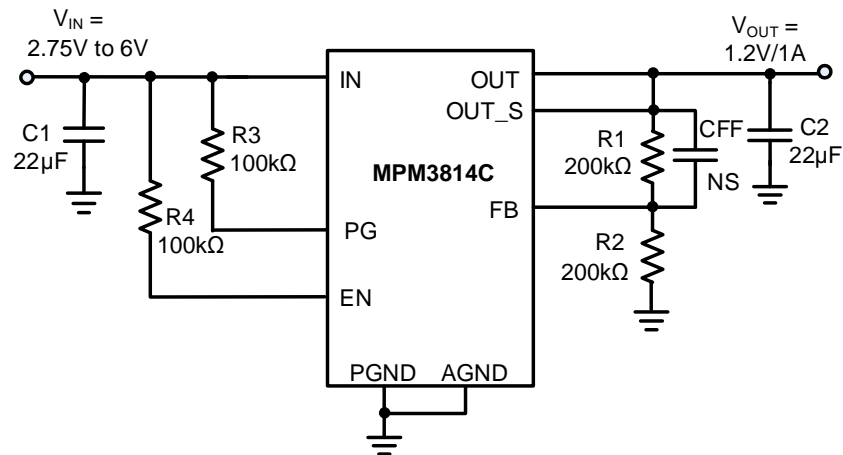


Figure 4: Typical Application Circuits <sup>(10)</sup>

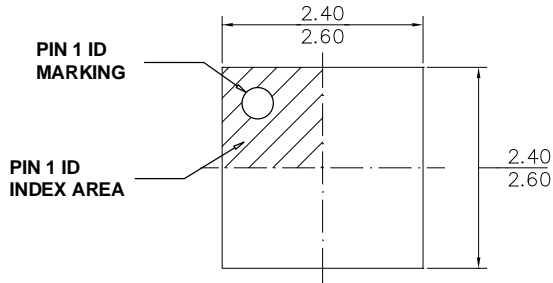
**Note:**

10) Additional input capacitors may be required for applications where  $V_{IN} < 3.3V$ .

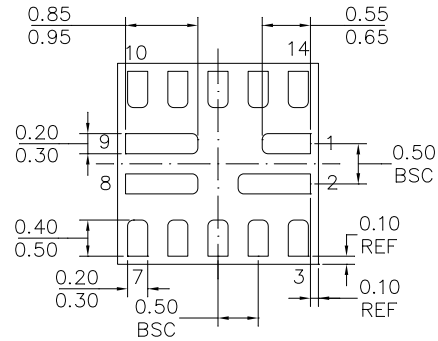


**PACKAGE INFORMATION**

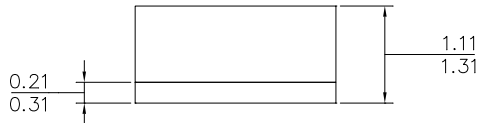
**ECLGA-14 (2.5mmx2.5mm)**



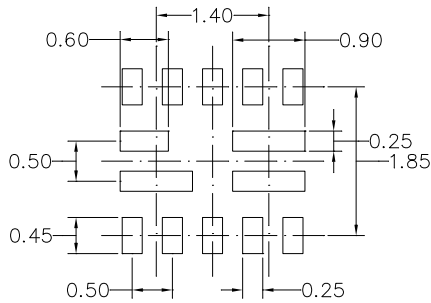
**TOP VIEW**



**BOTTOM VIEW**



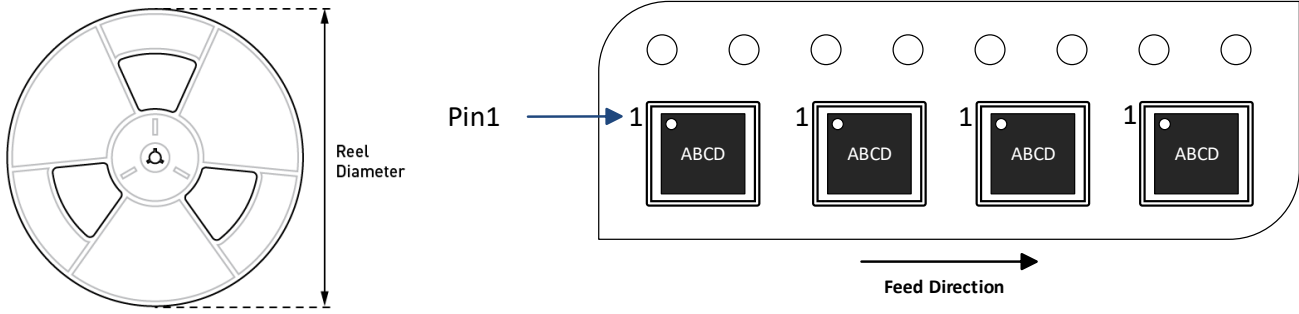
**SIDE VIEW**



**RECOMMENDED LAND PATTERN**

**NOTE:**

- 1) ALL DIMENSIONS ARE IN MILLIMETERS.
- 2) LEAD COPLANARITY SHALL BE 0.10 MILLIMETERS MAX.
- 3) JEDEC REFERENCE IS MO-303.
- 4) DRAWING IS NOT TO SCALE.

**CARRIER INFORMATION**


| Part Number   | Package Description       | Quantity/ Reel | Quantity/ Tray | Quantity/ Tube | Reel Diameter | Carrier Tape Width | Carrier Tape Pitch |
|---------------|---------------------------|----------------|----------------|----------------|---------------|--------------------|--------------------|
| MPM3814CGPA-Z | ECLGA-14<br>(2.5mmx2.5mm) | 2500           | N/A            | N/A            | 13in          | 12mm               | 8mm                |

## REVISION HISTORY

| Revision # | Revision Date | Description     | Pages Updated |
|------------|---------------|-----------------|---------------|
| 1.0        | 4/15/2022     | Initial Release | -             |

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