FSA4480

USB Type-C Analog Audio Switch with Protection Function

FSA4480 is a high performance USB Type−C port multimedia switch which supports analog audio headsets. FSA4480 allows the sharing of a common USB Type−C port to pass USB2.0 signal, analog audio, sideband use wires and analog microphone signal. FSA4480 also supports high voltage on SBU port and USB port on USB Type−C receptacle side.

Features

- Power Supply: V_{CC}, 2.7 V to 5.5 V
- USB High Speed (480 Mbps) Switch:
  - SDD_{21} −3dB bandwidth: 950 MHz
  - 3 Ω R_{ON} Typical
- Audio Switch
  - Negative Rail Capability: −3 V to +3 V
  - THD+N = −110 dB; 1 V_{RMS}, f = 20 Hz ∼ 20 kHz, 32 W Load
  - 1 Ω R_{ON} Typical
- High Voltage Protection
  - 20 V DC Tolerance on Connector Side Pins
  - Over Voltage Protection: V_{TH} = 5 V (Typ)
- OMTP and CTIA Pinout Support
- Support Audio Sense Path
- 25−Ball WLCSP Package (2.24 mm x 2.28 mm)

Applications

- Mobile Phone, Tablet, Notebook PC, Media Player

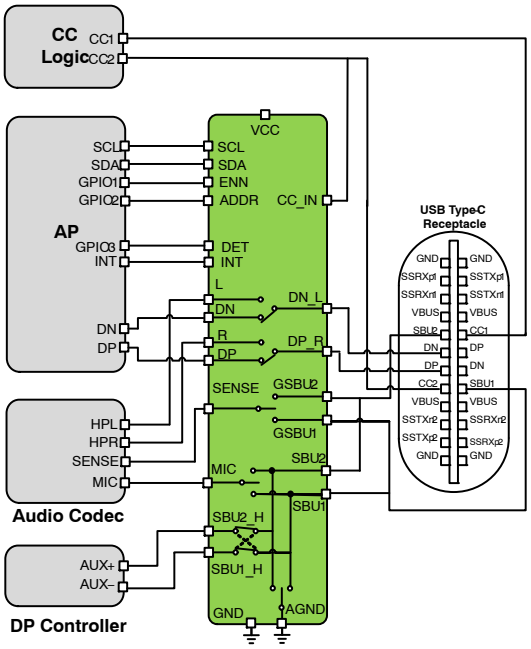

Figure 1. Application Block Diagram

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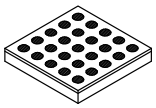


WLCSP25
CASE 567UZ

ORDERING INFORMATION

Part Number	Package	Marking
FSA4480UCX	WLCSP25 (Pb−Free)	6D

PIN CONFIGURATION

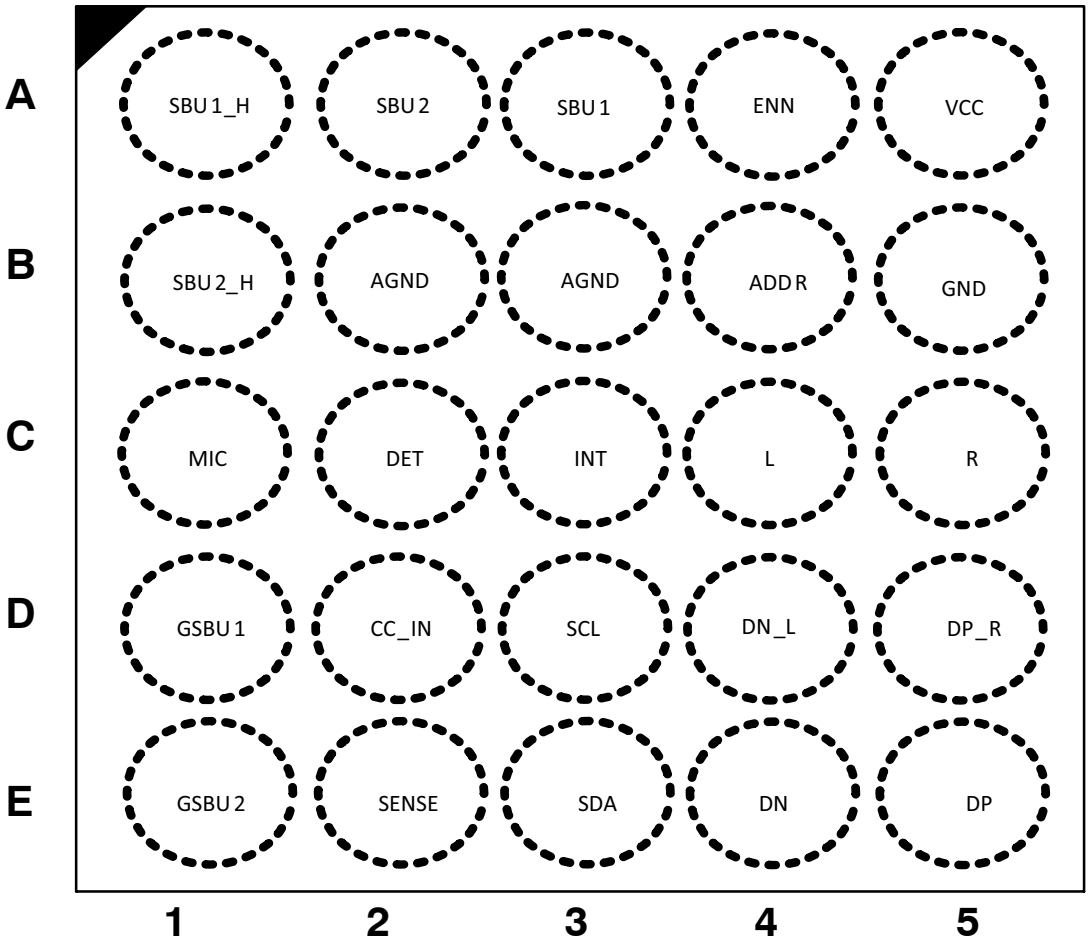


Figure 2. Pin Assignment (Top Through View)

Table 1. PIN DESCRIPTIONS

No.	Pin	Name	Description
1	A5	VCC	Power Supply (2.7 to 5.5 V)
2	B5	GND	Chip ground
3	D5	DP_R	USB/Audio Common Connector
4	D4	DN_L	USB/Audio Common Connector
5	E5	DP	USB Data (Differential +)
6	E4	DN	USB Data (Differential −)
7	C5	R	Audio − Right Channel
8	C4	L	Audio − Left Channel
9	A3	SBU1	Sideband use wire 1
10	A2	SBU2	Sideband use wire 2
11	C1	MIC	Microphone signal
12	B2	AGND	Audio signal ground
13	B3	AGND	Audio signal ground
14	E2	SENSE	Audio ground reference output
15	C3	INT	I^2C Interrupt output, active low (open drain)
16	D2	CC_IN	Audio accessory attachment detection input
17	D1	GSBU1	Audio sense path 1 to headset jack GND
18	E1	GSBU2	Audio sense path 2 to headset jack GND
19	C2	DET	Push−pull output. When CC_IN > 1.5 V, DET is low and CC_IN < 1.2 V, DET is high
20	D3	SCL	I^2C clock
21	E3	SDA	I^2C data
22	B1	SBU2_H	Host Side Sideband Use Wire 2
23	A1	SBU1_H	Host Side Sideband Use Wire 1
24	A4	ENN	Chip Enable, active low, internal pull−down by 470 kΩ
25	B4	ADDR	I^2C slave address pin

Table 2. ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter		Min.	Max.	Unit
V_{CC}	Supply Voltage from VCC		−0.5	6.5	V
V_{CC_IN}	V_{CC_IN}, to GND		−0.5	20	V
V_{SW_C}	V_{DP_R} to GND, V_{DN_L} to GND		−3.5	20	V
V_{SW_USB}	V_{DP} to GND, V_{DN} to GND		−0.5	6.5	V
V_{SW_Audio}	V_L to GND, V_R to GND		−3.6	6.5	V
$V_{V\_SBU/GSBU}$	V_{SBU1} to GND, V_{SBU2} to GND, V_{GSBU1} to GND, V_{GSBU1} to GND		−0.5	20	V
V_{VSBU_H}	V_{SBU1_H} to GND, V_{SBU2_H} to GND		−0.5	6.5	V
$V_{I/O}$	SENSE, MIC, DET, INT, to GND		−0.5	6.5	V
V_{CNTRL}	Control Input Voltage	SDA, SCL, ENN, ADDR	−0.5	6.5	V
I_{SW_Audio}	Switch I/O Current, Audio Path		−250	250	mA
I_{SW_USB}	Switch I/O Current, USB Path		–	100	mA
I_{SW_MIC}	Switch I/O Current, MIC to SBU1 or SBU2		–	50	mA
I_{SW_SBU}	Switch I/O Current, SBUx to SBUx_H		–	50	mA
I_{SW_SENSE}	Switch I/O Current, SENSE to GSBU1 or GSBU2		–	100	mA
I_{SW_AGND}	Switch I/O Current, AGND to SBU1 or SBU2		–	500	mA
I_{IK}	DC Input Diode Current		−50	–	mA
ESD	Human Body Model, ANSI/ESDA/JEDEC JS−001−2012	Connector side and power pins: VCC, SBU1, SBU2, DP_R, DN_L, GSBU1, GSBU2, CC_IN	4	–	kV
ESD	Human Body Model, ANSI/ESDA/JEDEC JS−001−2012	Host side pins: the rest pins	2	–	kV
ESD	Charged Device Model, JEDEC: JESD22−C101		1	–	kV
T_A	Absolute Maximum Operating Temperature		−40	85	°C
T_{STG}	Storage Temperature		−65	150	°C

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

Table 3. RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Min.	Typ.	Max.	Unit
POWER					
V_{CC}	Supply Voltage	2.7	–	5.5	V
USB SWITCH					
V_{SW_USB}	V_{DP} to GND, V_{DN} to GND, V_{DP_R} to GND, V_{DN_L} to GND	0	–	3.6	V
AUDIO SWITCH					
V_{SW_Audio}	V_{DP_R} to GND, V_{DN_L} to GND, V_L to GND, V_R to GND	−3.6	–	3.6	V
MIC SWITCH					
V_{VSBU_MIC}	V_{SBU1} to GND, V_{SBU2} to GND, V_{MIC} to GND	0	–	3.6	V
SENSE SWITCH					
V_{VGSBU_SEN}	V_{GSBU1} to GND, V_{GSBU2} to GND, V_{SENSE} to GND	0	–	3.6	V
SBU TO SBUX_H SWITCH					
V_{VGSBU}	V_{SBU1} to GND, V_{SBU2} to GND, V_{SBU1_H} to GND, V_{SBU2_H} to GND	0	–	3.6	V
CC_IN PIN					
V_{CC_IN}	V_{CC_IN}, to GND	0	–	5.5	V
CONTROL VOLTAGE (ENN/SDA/SCL)					
V_{IH}	Input Voltage High	1.3	–	V_{CC}	V
V_{IL}	Input Voltage Low	–	–	0.5	V
OPERATING TEMPERATURE					
T_A	Ambient Operating Temperature	−40	25	+85	°C

Functional operation above the stresses listed in the Recommended Operating Ranges is not implied. Extended exposure to stresses beyond the Recommended Operating Ranges limits may affect device reliability.

Table 4. DC ELECTRICAL CHARACTERISTICS

(V_{CC} = 2.7 V to 5.5 V, V_{CC} (Typ.) = 3.3 V, T_A = −40°C to 85°C, and T_A (Typ.) = 25°C, unless otherwise specified.)

Symbol	Parameter	Condition	Power	Min.	Typ.	Max.	Unit
I_{CC}	Supply Current	USB switches on, SBUx to SBUx_H switches on	V_{CC}: 2.7 V to 5.5 V	–	–	65	μA
		Audio switches on, MIC switch on and Audio GND switch on		–	–	60	μA
I_{CCZ}	Quiescent Current	ENN = L, 04H'b7 = 0		-	–	5	μA
USB/AUDIO COMMON PINS: DP/R, DN_L							
I_{OZ}	Off Leakage Current of DP_R and DN_L	DN_L, DP_R = −3 V to 3.6 V	V_{CC}: 2.7 V to 5.5 V	−3.0	–	3.0	μA
I_{OFF}	Power−Off Leakage Current of DP_R and DN_L	DN_L, DP_R = 0 V to 3.6 V	Power off	−3.0	–	3.0	μA
V_{OV_TRIP}	Input OVP Lockout	Rising edge	V_{CC}: 2.7 V to 5.5 V	4.5	5	5.3	V
V_{OV_HYS}	Input OVP Hysteresis			–	0.3	–	V
AUDIO SWITCH							
I_{ON}	On Leakage Current of Audio Switch	DN_L, DP_R = −3 V to 3.0 V, DP, DN, R, L = Float	V_{CC}: 2.7 V to 5.5 V	−2.5	–	2.5	μA
I_{OFF}	Power−Off Leakage Current of L and R	L, R = 0 V to 3 V; DP_R, DN_L = Float	Power off	−1.0	–	1.0	μA
R_{ON}	Switch On Resistance	I_{SW} = 100 mA, V_{SW} = −3 V to 3 V	V_{CC}: 2.7 V to 5.5 V	–	1	–	Ω
R_{SHUNT}	Pull Down Resistor on R/L Pin when Audio Switch is Off	L = R = 3 V		6	10	14	kΩ
USB SWITCH							
I_{ON}	On Leakage Current of USB Switch	DN_L, DP_R = 0 V to 3.6 V, DP, DN, R, L = Float	V_{CC}: 2.7 V to 5.5 V	−3.0	–	3.0	μA
I_{OZ}	Off Leakage Current of DP and DN	DN, DP = 0 V to 3.6 V		−3.0	–	3.0	μA
I_{OFF}	Power−Off Leakage Current of DP and DN	DN, DP = 0 V to 3.6 V	Power off	−3.0	–	3.0	μA
R_{ON_USB}	USB Switch On Resistance	I_{SW} = 8 mA, V_{SW} = 0.4 V	V_{CC}: 2.7 V to 5.5 V	–	3	–	Ω
SENSE SWITCH							
I_{ON}	Sense Path Leakage Current	GSBUx = 0 V to 1 V, SENSE is floating	V_{CC}: 2.7 V to 5.5 V	−2.0	–	2.0	μA
R_{ON}	SENSE Switch On Resistance	I_{OUT} = 100 mA, V_{SW} = 1 V	V_{CC}: 2.7 V to 5.5 V	–	300	–	mΩ
I_{OZ}	Off Leakage Current of SENSE	Sense = 0 V to 1.0 V		−2.0	–	2.0	μA
	Off Leakage Current of GSBUx	GSBUx = 0 V to 1.0 V		−2.0	–	2.0	μA
		GSBUx = 1 V to 3.6 V		−3.0	–	3.0	
I_{OFF}	Power−Off Leakage Current of SENSE	Sense = 0 V to 1.0 V	Power off	−2.0	–	2.0	μA
	Power−Off Leakage Current of GSBUx	GSBUx = 0 V to 3.6 V		−3.0	–	3.0	

Table 4. DC ELECTRICAL CHARACTERISTICS (continued)
(V_{CC} = 2.7 V to 5.5 V, V_{CC} (Typ.) = 3.3 V, T_A = −40°C to 85°C, and T_A (Typ.) = 25°C, unless otherwise specified.)

Symbol	Parameter	Condition	Power	Min.	Typ.	Max.	Unit
SENSE SWITCH							
V_{OV_TRIP}	Input OVP Lockout on GSBUx	Rising edge	V_{CC}: 2.7 V to 5.5 V	4.5	5	5.3	V
V_{OV_HYS}	Input OVP Hysteresis of GSBUx			–	0.3	–	V
SBUX PINS							
I_{OZ}	Off Leakage Current of SBUx	SBUx = 0 V to 3.6 V	V_{CC}: 2.7 V to 5.5 V	−3.0	–	3.0	μA
I_{OFF}	Power−Off Leakage Current Port SBUx	SBUx = 0 V to 3.6 V	Power off	−3.0	–	3.0	μA
V_{OV_TRIP}	Input OVP Lockout	Rising edge	V_{CC}: 2.7 V to 5.5 V	4.5	5	5.3	V
V_{OV_HYS}	Input OVP Hysteresis			–	0.3	–	V
MIC SWITCH							
I_{ON}	On Leakage Current of MIC Switch	SBUx = 0 V to 3.6 V, MIC is floating	V_{CC}: 2.7 V to 5.5 V	−3.0	–	3.0	μA
I_{OZ}	Off Leakage Current of MIC	MIC = 0 V to 3.6 V		−1.0	–	1.0	μA
I_{OFF}	Power Off Leakage Current of MIC	MIC = 0 V to 3.6 V	Power off	−1.0	–	1.0	μA
R_{ON}	MIC Switch On Resistance	V_{SW} = 3.6 V, Isw = 30 mA	V_{CC}: 2.7 V to 5.5 V	–	3	–	Ω
SBUX_H SWITCH							
I_{ON}	On Leakage Current of SBUx_H Switch	SBUx = 0 V to 3.6 V, SBUx_H is floating	V_{CC}: 2.7 V to 5.5 V	−3.0	–	3.0	μA
I_{OZ}	Off Leakage of SBUx_H	SBUx_H =0 V to 3.6 V		−1	–	1	μA
I_{OFF}	Power Off Leakage Current of SBUx_H	SBUx_H = 0 V to 3.6 V	Power off	−1.0	–	1.0	μA
R_{ON}	SBUx_H Switch On Resistance	V_{SW} = 0 V to 3.6 V, Isw = 30 mA	V_{CC}: 2.7 V to 5.5 V	–	3	–	Ω
AUDIO GROUND SWITCH: PIN: AGND TO SBUX							
R_{ON}	AGND Switch On Resistance	I_{SOURCE} = 100 mA on SBUx	V_{CC}: 2.7 V to 5.5 V	–	50	90	mΩ
CC_IN PIN							
V_{TH_L}	Input Low Threshold		V_{CC}: 2.7 V to 5.5 V	–	1.2	–	V
V_{TH_H}	Input High Threshold			–	1.5	–	V
I_{IN}	Input Leakage of CC_IN	CC_IN = 0 V to 5.5 V		–	–	1.0	μA
INT, DET PINS							
V_{OH}	Output High for DET	Io = −2 mA	V_{CC}: 2.7 V to 5.5 V	1.5	1.8	2	V
V_{OL}	Output Low for DET and INT	Io = 2 mA		–	–	0.4	V

Table 4. DC ELECTRICAL CHARACTERISTICS (continued)
(V_{CC} = 2.7 V to 5.5 V, V_{CC} (Typ.) = 3.3 V, T_A = −40°C to 85°C, and T_A (Typ.) = 25°C, unless otherwise specified.)

Symbol	Parameter	Condition	Power	Min.	Typ.	Max.	Unit
ADDR PIN							
V_{IH}	Input voltage High		V_{CC}: 2.7 V to 5.5 V	1.3	–	–	V
V_{IL}	Input voltage Low			–	–	0.45	V
I_{IN}	Control Input Leakage	ADDR = 0 V to V_{CC}		−1	–	1	μA
ENN PIN							
V_{IH}	Input Voltage High		V_{CC}: 2.7 V to 5.5 V	1.3	–	–	V
V_{IL}	Input Voltage Low			–	–	0.45	V
R_{PD}	Internal Pull Down Resistor			–	470	–	kΩ
SDS, SCL PINS							
V_{ILI2C}	Low−Level Input Voltage		V_{CC}: 2.7 V to 5.5 V	–	–	0.4	V
V_{IHI2C}	High−Level Input Voltage			1.2	–	–	V
I_{I2C}	Input Current of SDA and SCL Pins	SCL/SDA = 0 V to 3.6 V		−2	–	2	μA
V_{OLSDA}	Low−Level Output Voltage	I_{OL} = 2 mA		–	–	0.3	V
I_{OLSDA}	Low−Level Output Current	V_{OLSDA} = 0.2 V		10	–	–	mA

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

Table 5. AC ELECTRICAL CHARACTERISTICS

(V_{CC} = 2.7 V to 5.5 V, V_{CC} (Typ.) = 3.3 V, T_A = −40°C to 85°C, and T_A (Typ.) = 25°C, unless otherwise specified.)

Symbol	Parameter	Condition	Power	Min.	Typ.	Max.	Unit
AUDIO SWITCH							
t_{delay}	Audio Switch Turn On Delay Time	DP_R = DN_L = 1 V, R_L = 32 Ω	V_{CC} = 3.3 V	–	65	–	μs
t_{rise}	Audio Switch Turn On Rising Time (Note 1)	DP_R = DN_L = 1 V, R_L = 32 Ω		–	240	–	μs
t_{OFF}	Audio Switch Turn Off Time	DP_R = DN_L = 1 V, R_L = 32 Ω		–	15	–	μs
X_{TALK}	Cross Talk (Adjacent)	f = 1 kHz, R_L = 50 Ω, V_{SW} = 1 V_{RMS}		–	−100	–	dB
BW	−3 dB Bandwidth	R_L = 50 Ω		–	600	–	MHz
O_{IRR}	Off Isolation	F = 1 kHz, R_L = 50 Ω, C_L = 0 pF, V_{SW} = 1 V_{RMS}		–	−100	–	dB
THD+N	Total Harmonic Distortion + Noise Performance with A−weighting Filter	R_L = 600 Ω, f = 20 Hz~20 kHz, V_{SW} = 2 V_{RMS}		–	−110	–	dB
		R_L = 32 Ω, f = 20 Hz~20 kHz, V_{SW} = 1 V_{RMS}		–	−110	–	dB
		R_L = 16 Ω, f = 20 Hz~20 kHz, V_{SW} = 0.5 V_{RMS}		–	−108	–	dB
USB SWITCH							
t_{ON}	USB Switch Turn−on Time	DP_R = DN_L = 1.5 V, R_L = 50 Ω	V_{CC} = 3.3 V	–	60	–	μs
t_{OFF}	USB Switch Turn −off Time	DP_R = DN_L = 1.5 V, R_L = 50 Ω		–	15	–	μs
BW	−3 dB Bandwidth	R_L = 50 Ω		–	850	–	MHz
	SDD_{21} −3 dB Bandwidth			–	950	–	
O_{IRR}	Off Isolation between DP, DN and Common Node Pins	f = 1 kHz, R_L = 50 Ω, C_L = 0 pF, V_{SW} = 1 V_{RMS}		–	−100	–	dB
t_{OVP}	DP_R and DN_L pins OVP Response Time	Vsw = 3.5 V to 5.5 V		–	1	1.5	μs
MIC/AUDIO GROUND SWITCH							
t_{delay_MIC}	MIC Switch Turn On Delay Time	SBUx = 1 V, R_L = 50 Ω	V_{CC} = 3.3 V	–	100	–	μs
t_{rise_MIC}	MIC Switch Turn On Rising Time (Note 1)			–	250	–	
t_{delay_AGND}	AGND Switch Turn On Time	SBUx pulled up to 0.5 V by 16 Ω, AGND connect to GND		–	100	–	μs
t_{rise_AGND}	AGND Switch Turn On Rising Time (Note 1)			–	1500	–	
t_{OFF_MIC}	MIC Switch Turn Off Time	SBUx = 2.5 V, R_L = 50 Ω		–	15	–	
$t_{OFF\_Audio\ GND}$	AGND Switch Turn Off Time	SBUx: Isource = 10 mA, clamp to 2.5 V		–	15	–	
BW	MIC Switch Bandwidth	R_L = 50 Ω		–	50	–	MHz

Table 5. AC ELECTRICAL CHARACTERISTICS (continued)
(V_{CC} = 2.7 V to 5.5 V, V_{CC} (Typ.) = 3.3 V, T_A = −40°C to 85°C, and T_A (Typ.) = 25°C, unless otherwise specified.)

Symbol	Parameter	Condition	Power	Min.	Typ.	Max.	Unit
SBUX_H SWITCH							
t_{ON}	SBUx_H Switch Turn On Time	SBUx = 2.5 V, R_L = 50 Ω	V_{CC} = 3.3 V	–	35	–	μs
t_{OFF}	SBUx_H Switch Turn Off Time			–	15	–	
BW	Bandwidth	R_L = 50 Ω		–	50		MHz
t_{OVP}	SBUx Pins OVP Response Time	Vsw = 3.5 V to 5.5 V		–	0.5	1	μs
SENSE SWITCH							
t_{delay}	Sense Switch Turn On Delay Time	GSBUx = 1 V, R_L = 50 Ω	V_{CC} = 3.3 V	–	65	–	μs
t_{rise}	Sense Switch Turn On Rising Time (Note 1)			–	260	–	μs
t_{OFF}	Sense Switch Turn Off Time			–	15	–	μs
t_{OVP}	GSBUx Pins OVP Response Time	V_{SW}: 3.5 V to 5.5 V		–	0.7	1.5	μs
BW	Bandwidth	R_L = 50 Ω		–	150	–	MHz
DET DELAY							
t_{DELAY_DET}	DET Response Delay	Transition from 0 to 1.8 V	V_{CC} = 3.3 V	–	1	–	μs
		Transition from 1.8 to 0 V		–	5	–	

1. Turn on timing can be controlled by I^2C register.

Table 6. I²C SPECIFICATION

(V_{CC} = 2.7 V to 5.5, V_{CC} (Typ.) = 3.3 V ,T_A = −40°C to 85°C. T_A (Typ.) = 25°C, unless otherwise specified)

Symbol	Parameter	Fast Mode		
		Min.	Max.	Unit
f_{SCL}	I²C_SCL Clock Frequency		400	kHz
$t_{HD;\ STA}$	Hold Time (Repeated) START Condition	0.6		μs
t_{LOW}	Low Period of I²C_SCL Clock	1.3		μs
t_{HIGH}	High Period of I²C_SCL Clock	0.6		μs
$t_{SU;\ STA}$	Set−up Time for Repeated START Condition	0.6		μs
$t_{HD;\ DAT}$	Data Hold Time (Note 2)	0	0.9	μs
$t_{SU;\ DAT}$	Data Set−up Time (Note 3)	100		ns
t_r	Rise Time of I²C_SDA and I²C_SCL Signals (Note 3)	20 + 0.1C_b	300	ns
t_f	Fall Time of I²C_SDA and I²C_SCL Signals (Note 3)	20 + 0.1C_b	300	ns
$t_{SU;\ STO}$	Set−up Time for STOP Condition	0.6		μs
t_{BUF}	Bus−Free Time between STOP and START Conditions	1.3		μs
t_{SP}	Pulse Width of Spikes that Must Be Suppressed by the Input Filter	0	50	ns

2. Guaranteed by design, not production tested.
3. A fast−mode I²C−bus device can be used in a standard−mode I²C−bus system, but the requirement $t_{SU;DAT} \geq \pm 250$ ns must be met. This is automatically the case if the device does not stretch the LOW period of the I2C_SCL signal. If such a device does stretch the LOW period of the I²C_SCL signal, it must output the next data bit to the I²C_SDA line $t_{r\_max} + t_{SU;DAT}$ = 1000 + 250 = 1250 ns (according to the standard−mode I²C bus specification) before the I²C_SCL line is released.

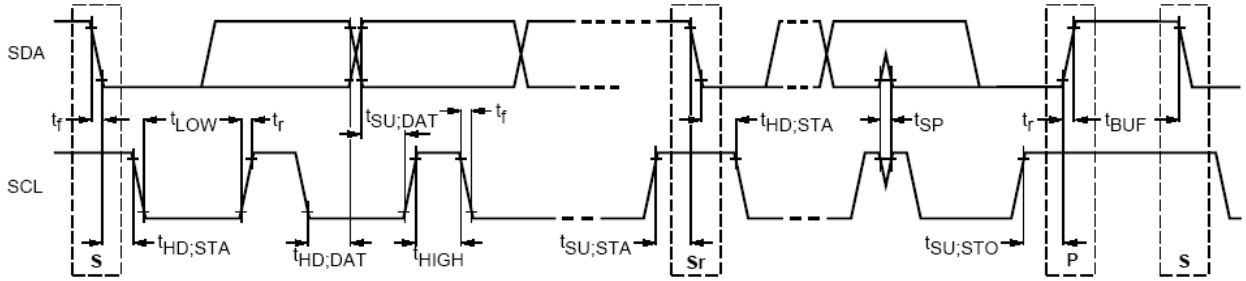


Figure 3. Definition of Timing for Full−Speed Mode Devices on the I²C Bus

Table 7. CAPACITANCE

(V_{CC}= 2.7 V to 5.5 V, V_{CC} (Typ.) = 3.3 V, T_A = −40°C to 85°C, and T_A (Typ.) = 25°C)

Symbol	Parameter	Condition		Power	T_A =− 40°C to +85°C			Unit
					Min.	Typ.	Max.	
$C_{ON\_USB/Audio}$	On Capacitance (6) (Common Port)	f = 1 MHz, 100 mV_{PK-PK}, 100 mV DC bias		VCC = 3.3 V		9		pF
$C_{OFF\_USB/Audio}$	Off Capacitance(6) (Common Port)	f = 1 MHz, 100 mV_{PK-PK}, 100 mV DC bias				7.5		pF
C_{OFF_USB}	Off Capacitance (Non−Common Ports) (6)	f = 1 MHz, 100 mV_{PK-PK}, 100 mV DC bias				3		pF
$C_{ON\_SENSE\_SW}$	On Capacitance – (Common Ports) (6)	f = 1 MHz, 100 mV_{PK-PK}, 100 mV DC bias				55		pF
$C_{OFF\_SENSE\_SW}$	Off Capacitance – (Common Ports) (6)	f = 1 MHz, 100 mV_{PK-PK}, 100 mV DC bias				88		pF
$C_{ON\_MIC\_SW}$	On Capacitance – (Common Ports) (6)	f = 1 MHz, 100 mV_{PK-PK}, 100 mV DC bias				170		pF
$C_{OFF\_MIC\_SW}$	Off Capacitance – (Common Ports) (6)	f = 1 MHz, 100 mV_{PK-PK}, 100 mV DC bias				10		pF
$C_{ON\_AGND\_SW}$	On Capacitance (6) (Common Port)	f = 1 MHz, 100 mV_{PK-PK}, 100 mV DC bias				125		pF
$C_{ON\_SBUx\_H\_SW}$	On Capacitance (6) (Common Port)	f = 1 MHz, 100 mV_{PK-PK}, 100 mV DC bias				160		pF
C_{CNTRL}	Control Input Pin Capacitance (6)	f = 1 MHz, 100 mV_{PP}, 100 mV DC bias	ENN			3		pF

Table 8. REGISTER MAPS

ADDR	Register Name	Type	Reset Value	BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0
00H	Device ID	R	0x09	0	0	0	0	1	0	0	1
01H	OVP Interrupt Mask	R/W	0x00	Reserved	Mask OVP interrupt	Mask OVP /DP_R	Mask OVP /DN_L	Mask OVP /SBU1	Mask OVP /SBU2	Mask OVP /GSBU1	Mask OVP /GSBU2
02H	OVP interrupt flag	R/C	0x00	Reserved		DP_R	DN_L	SBU1	SBU2	GSBU	GSBU2
03H	OVP status	R	0x00	Reserved		OVP/ DP_R	OVP/ DN_L	OVP/SB U1	OVP/SB U2	OVP/ GSBU1	OVP/ GSBU2
04H	Switch settings Enable	R/W	0x98	Device control	SBU1_H to SBUx	SBU2_H to SBUx	DN_L to DN or L	DP_R to DP or R	Sense to GSBUx	MIC to SBUx	Audio Ground to SBUx
05H	Switch select	R/W	0x18	Reserved	SBU1_H to SBUx	SBU2_H to SBUx	DN_L to DN or L	DP_R to DP or R	Sense to GSBUx	MIC to SBUx	Audio Ground to SBUx
06H	Switch Status0	R	0x00	Reserved		Sense Switch Status		DP_R Switch Status		DN_L Switch Status	
07H	Switch Status1	R	0x00	Reserved		SBU2 Switch Status			SBU1 Switch Status		
08H	Audio Switch Left Channel turn on Control	R/W	0x01	Audio switch left channel slow control [7:0]							
09H	Audio Switch Right Channel turn on Control	R/W	0x01	Audio switch right channel slow control [7:0]							
0AH	MIC switch turn on control	R/W	0x01	MIC switch right channel slow control [7:0]							
0BH	Sense switch turn on control	R/W	0x01	Sense switch right channel slow control [7:0]							
0CH	Audio Ground Switch turn on Control	R/W	0x01	Audio ground switch right channel slow control [7:0]							

Table 8. REGISTER MAPS

ADDR	Register Name	Type	Reset Value	BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0
0DH	Timing Delay between R switch enable and L switch enable	R/W	0x00	Timing Delay between R switch enable and L switch enable control [7:0]							
0EH	Timing Delay between MIC switch enable and L switch enable	R/W	0x00	Timing Delay between MIC switch enable and L switch enable control [7:0]							
0FH	Timing Delay between Sense switch enable and L switch enable	R/W	0x00	Timing Delay between Sense switch enable and L switch enable control [7:0]							
10H	Timing Delay between Audio ground switch enable and L switch enable	R/W	0x00	Timing Delay between Audio ground switch enable and L switch enable control [7:0]							
11H	Audio accessory status	R	0x02	Reserved						CC_IN	DET
12H	Function enable	R/W	0x08	Reserved	DET I/O Control	RES detection range setting	GIPO control	SLOW TURN−ON CONTROLL	MIC auto control	RES detection : auto clear	Audio jack detection : auto clear
13H	RES detection pin setting	R/W	0x00	Reserved					Detection pin select [2:0]		
14H	RES detection value	R	0xFF	R detection value [7:0]							
15H	RES detection interrupt threshold	R/W	0x16	R detection Interrupt resistance threshold [7:0]							
16H	RES detection interval	R/W	0X00	Reserved						Detection interval [1:0]	
17H	Audio jack Status	RO	0x01	Reserved				4pole,SBU2 MIC	4pole,SBU1 MIC	3pole	No audio
18H	Detection interrupt	R/C	0x00	Reserved					Audio detection done	RES detection occurred	RES detection done
19H	Detection interrupt Mask	R/W	0x00	Reserved					Audio detection done mask	RES detection occurred mask	RES detection done mask
1AH	Audio detection RGE1	RO	0xFF	audio detection value REG1 [7:0]							
1BH	Audio detection RGE2	RO	0xFF	audio detection value REG2 [7:0]							
1CH	MIC Threshold DATA0	R/W	0x20	MIC Threshold value DATA0 [7:0]							
1DH	MIC Threshold DATA1	R/W	0xFF	MIC Threshold value DATA1 [7:0]							
1EH	I2C Reset	W/C	0x00	Reserved							I2C reset
1FH	Current Source Setting	R/W	0x07	Reserved				Current Source setting [3:0]			

Table 9. I²C SLAVE ADDRESS

ADDR	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
ADDR = L	1	0	0	0	0	1	0	R/W
ADDR = H	1	0	0	0	0	1	1	R/W

DEVICE ID
Address: 00h
Reset Value: 8'b 0000_1001
Type: Read

Bits	Name	Size	Description
7:6	Vendor ID	2	Vendor ID
5:3	Version ID	3	Device Version ID
2:0	Revision ID	3	Revision History ID

OVP INTERRUPT MASK
Address: 01h
Reset Value: 8'b 0000_0000
Type: Read/Write

Bits	Name	Size	Description
7	Reserved	1	Do Not Use
6	OVP Interrupt mask control	1	OVP Interrupt function Enable/Disable 0: Controlled by [5:0] bit 1: Mask all connector side pins OVP interrupt
5	DP_R OVP Interrupt mask control	1	0: Do not mask OVP interrupt 1: Mask OVP interrupt
4	DN_L OVP Interrupt mask control	1	0: Do not mask OVP interrupt 1: Mask OVP interrupt
3	SBU1 OVP Interrupt mask control	1	0: Do not mask OVP interrupt 1: Mask OVP interrupt
2	SBU2 OVP Interrupt mask control	1	0: Do not mask OVP interrupt 1: Mask OVP interrupt
1	GSBU1 OVP Interrupt mask control	1	0: Do not mask OVP interrupt 1: Mask OVP interrupt
0	GSBU2 OVP Interrupt mask control	1	0: Do not mask OVP interrupt 1: Mask OVP interrupt

OVP INTERRUPT FLAG
Address: 02h
Reset Value: 8'b 0000_0000
Type: Read Clear

Bits	Name	Size	Description
[7:6]	Reserved	2	Do Not Use
5	DP_R OVP	1	0: OVP event has not occurred 1: OVP event has occurred
4	DN_L OVP	1	0: OVP event has not occurred 1: OVP event has occurred
3	SBU1 OVP	1	0: OVP event has not occurred 1: OVP event has occurred
2	SBU2 OVP	1	0: OVP event has not occurred 1: OVP event has occurred
1	GSBU1 OVP	1	0: OVP event has not occurred 1: OVP event has occurred
0	GSBU2 OVP	1	0: OVP event has not occurred 1: OVP event has occurred

OVP STATUS

Address: 03h
Reset Value: 8'b 0000_0000
Type: Read

Bits	Name	Size	Description
[7:6]	Reserved	2	Do Not Use
5	OVP on DP_R PIN	1	0: OVP event has not occurred 1: OVP event has occurred
4	OVP on DN_L PIN	1	0: OVP event has not occurred 1: OVP event has occurred
3	OVP on SBU1 PIN	1	0: OVP event has not occurred 1: OVP event has occurred
2	OVP on SBU2 PIN	1	0: OVP event has not occurred 1: OVP event has occurred
1	OVP on GSBU1 PIN	1	0: OVP event has not occurred 1: OVP event has occurred
0	OVP on GSBU2 PIN	1	0: OVP event has not occurred 1: OVP event has occurred

SWITCHING SETTING ENABLE

Address: 04h
Reset Value: 8'b 1001_1000
Type: Read/Write

Bits	Name	Size	Description
7	Device Enable	1	0: Device Disable; L, R pull down by 10 k and other switch nodes will be high−Z for positive input. 1: Device Enable. Device Enable = 1 Device enable = 0 ENN = 1 Device Disable Device Disable ENN = 0 Device Enable Device Disable
6	SBU1_H to SBUx switches	1	0: Switch Disable; SBU1_H will be high−Z for positive input 1: Switch Enable
5	SBU2_H to SBUx switches	1	0: Switch Disable; SBU2_H will be high−Z for positive input 1: Switch Enable
4	DN_L to DN or L switches	1	0: Switch Disable; DN_L,DN will be high−Z for positive input. L pull down by 10 kohm 1: Switch Enable
3	DP_R to DP or R switches	1	0: Switch Disable; DP_R,DP will be high−Z for positive input. R pull down by 10 kohm 1: Switch Enable
2	Sense to GSBUx switches	1	0: Switch Disable; Sense,GSBU1 and GSBU2 will be high−Z for positive input 1: Switch Enable
1	MIC to SBUx switches	1	0: Switch Disable: MIC will be high−Z for positive input. 1: Switch Enable
0	AGND to SBUx switches	1	0: Switch Disable: AGND will be high−Z for positive input. 1: Switch Enable

SWITCH SELECT

Address: 05h
Reset Value: 8'b 0001_1000
Type: Read/Write

Bits	Name	Size	Description
7	Reserved	1	Do Not Use
6	SBU1_H switches	1	0: SBU1_H to SBU1 switch ON 1: SBU1_H to SBU2 switch ON
5	SBU2_H switches	1	0: SBU2_H to SBU2 switch ON 1: SBU2_H to SBU1 switch ON
4	DN_L to DN or L switches	1	0: DN_L to L switch ON 1: DN_L to DN switch ON
3	DP_R to DP or R switches	1	0: DP_R to R switch ON 1: DP_R to DP switch ON
2	Sense to GSBUx switches	1	0: Sense to GSBU1 switch ON 1: Sense to GSBU2 switch ON
1	MIC to SBUx switches	1	0: MIC to SBU2 switch ON 1: MIC to SBU1 switch ON
0	AGND to SBUx switches	1	0: AGND to SBU1 switch ON 1: AGND to SBU2 switch ON

SWITCH STATUS0

Address: 06h
Reset Value: 8'b 0000_0000
Type: Read Only

Bits	Name	Size	Description
[7:6]	Reserved	2	Do not use
[5:2]	Sense Switch Status	2	00: Sense switch is Open/Not Connected 01: Sense connected to GSBU1 10: Sense connected to GSBU2 11: Not Valid
[3:2]	DP_RSwitch Status	2	00: DP_R Switch Open/Not Connected 01: DP_Rconnected to DP 10: DP_Rconnected to R 11: Not Valid
[1:0]	DN_L switch Status	2	00: DN_L Switch Open/Not Connected 01: DN_L connected to DN 10: DN_L connected to L 11: Not Valid

SWITCH STATUS1

Address: 07h
Reset Value: 8'b 0000_0000
Type: Read Only

Bits	Name	Size	Description
[7:6]	Reserved	2	Do not use
[5:3]	SBU2 Switch Status	3	000: SBU2 switch is Open/Not Connected 001: SBU2 connected to MIC 010: SBU2 connected to AGND 011: SBU2 connected to SBU1_H 100: SBU2 connected to SBU2_H 101: SBU2 connected both SBU1_H and SBU2_H 110…111: Do not use
[2:0]	SBU1 Switch Status	3	000: SBU1 switch is Open/Not Connected 001: SBU1 connected to MIC 010: SBU1 connected to AGND 011: SBU1 connected to SBU1_H 100: SBU1 connected to SBU2_H 101: SBU1 connected both SBU1_H and SBU2_H 110…111: Do not use

AUDIO SWITCH LEFT CHANNEL SLOW TURN−ON

Address: 08h
Reset Value: 8'b 0000_0001
Type: Read/Write

Bits	Name	Size	Description
[7:0]	Switch turn on rising time setting	8	11111111: 25600 μS
			…
			00000001: 200 μS
			00000000: 100 μS

AUDIO SWITCH RIGHT CHANNEL SLOW TURN−ON

Address: 09h
Reset Value: 8'b 0000_0001
Type: Read/Write

Bits	Name	Size	Description
[7:0]	Switch turn on rising time setting	8	11111111: 25600 μS
			…
			00000001: 200 μS
			00000000: 100 μS

MIC SWITCH SLOW TURN−ON

Address: 0Ah
Reset Value: 8'b 0000_0001
Type: Read/Write

Bits	Name	Size	Description
[7:0]	Switch turn on rising time setting	8	11111111: 25700 μS
			…
			00000010: 350 μS
			00000001: 250 μS
			00000000: Not Valid

SENSE SWITCH SLOW TURN−ON

Address: 0Bh
Reset Value: 8'b 0000_0001
Type: Read/Write

Bits	Name	Size	Description
[7:0]	Switch turn on rising time setting	8	11111111: 25600 μS
			…
			00000001: 200 μS
			00000000: 100 μS

AUDIO GROUND SWITCH SLOW TURN−ON

Address: 0Ch
Reset Value: 8'b 0000_0001
Type: Read/Write

Bits	Name	Size	Description
[7:0]	Switch turn on rising time setting	8	11111111: 179000 μS
			…
			00000001: 1400 μS
			00000000: 700 μS

TIMING DELAY BETWEEN R SWITCH ENABLE AND L SWITCH ENABLE

Address: 0Dh
Reset Value: 8'b 0000_0000
Type: Read/Write

Bits	Name	Size	Description
[7:0]	Delay timing setting	8	11111111: 25500 μS
			11111110: 25400 μS
			…
			00000001: 100 μS
			00000000: 0 μS

TIMING DELAY BETWEEN MIC SWITCH ENABLE AND L SWITCH ENABLE

Address: 0Eh
Reset Value: 8'b 0000_0000
Type: Read/Write

Bits	Name	Size	Description
[7:0]	Delay timing setting	8	11111111: 25500 μS
			11111110: 25400 μS
			…
			00000001: 100 μS
			00000000: 0 μS

TIMING DELAY BETWEEN SENSE SWITCH ENABLE AND L SWITCH ENABLE

Address: 0Fh
Reset Value: 8'b 0000_0000
Type: Read/Write

Bits	Name	Size	Description
[7:0]	Delay timing setting	8	11111111: 25500 μS
			11111110: 25400 μS
			…
			00000001: 100 μS
			00000000: 0 μS

TIMING DELAY BETWEEN AUDIO GROUND SWITCH ENABLE AND L SWITCH ENABLE

Address: 10h
Reset Value: 8'b 0000_0000
Type: Read/Write

Bits	Name	Size	Description
[7:0]	Delay timing setting	8	11111111: 25500 μS
			11111110: 25400 μS
			…
			00000001: 100 μS
			00000000: 0 μS

AUDIO ACCESSORY STATUS

Address: 11h
Reset Value: 8'b 0000_0010
Type: Read

Bits	Name	Size	Description
[7:2]	Reserved	6	Do not use
1	CC_IN	1	0: CC_IN < 1.2 V 1: CC_IN > 1.5 V
0	DET	1	0: DET output is low 1: DET is output is high

FUNCTION ENABLE
Address: 12h
Reset Value: 8'b 0000_1000
Type: Read/Write

Bits	Name	Size	Description
7	Reserved	1	Do not use
6	DET I/O Control	1	1: DET pin is in Open/Drain Configuration 0: DET pin is in Push/Pull Configuration
5	RES detection range setting	1	1: 10k to 2560 k 0: 1k to 256 k
4	GPIO control enable	1	1: enable 0: disable
3	Slow turn on control enable	1	1: enable 0: disable
2	MIC auto break out control enable	1	1: enable 0: disable
1	RES detection enable	1	1: enable; will be changed to '0' after low resistance detection 0: disable
0	Audio jack detection and configuration enable	1	1: enable; will be changed to '0' after audio jack detection and configuration 0: disable

When GPIO control mode (manual switch control) is enable. '**Switch control'** register is changed to read only. It will reflect switch status. I^2C slave address is

RES DETECTION PIN SETTING
Address: 13h
Reset Value: 8'b 0000_0000
Type: Read

Bits	Name	Size	Description
[7:3]	Reserved	5	Do not use
[2:0]	Pin selection	3	000: CC_IN 001: DP/R 010: DN_L 011: SBU1 100: SBU2 101: Do not use … 111: Do not use

If RES detection pin is enable before setting PIN selection it will always do the CC_IN first. Recommend user to select the pin first before setting the RES detection pin enable.

RES VALUE
Address: 14h
Reset Value: 8'b 1111_1111
Type: Read

Bits	Name	Size	Description
[7:0]	Detected resistance value	8	0000_0000 : R < 1 k … 1111_1111: R > 300 K

RES DETECTION THRESHOLD

Address: 15h
Reset Value: 8'b 0001_0110
Type: Read

Bits	Name	Size	Description
[7:0]	RES detection threshold	8	Selection by 1 KΩ per step if Reg 12h [5] = 0 Selection by 10 KΩ per step if Reg 12h [5] = 0 Default Value = 22 KΩ 0000_0000: 1 KΩ /10 KΩ … 1111_1111: 256 KΩ / 2560 KΩ

RES DETECTION INTERVAL

Address: 16h
Reset Value: 8'b 0000_0000
Type: Read

Bits	Name	Size	Description
[7:2]	Reserved	6	Do not use
[1:0]	RES detection interval	2	00: Single 01: 100 mS 10: 1 S 11: 10 S

AUDIO JACK STATUS

Address: 17h
Reset Value: 8'b 0000_0001
Type: Read

Bits	Name	Size	Description
[7:3]	Reserved	4	Do not use
3	4pole	1	1: 4 Pole SBU2 to MIC, SBU1 to audio ground 0: others
2	4pole	1	1: 4 Pole SBU1 to MIC, SBU2 to audio ground 0: others
1	3 pole	1	1: 3 pole 0: others
0	No audio accessory	1	1: No audio accessory 0: Audio accessory attached

RES DETECTION /AUDIO JACK DETECTION INTERRUPT FLAG

Address: 18h
Reset Value: 8'b 0000_0000
Type: Read Clear

Bits	Name	Size	Description
[7:3]	Reserved	5	Do Not Use
2	Audio jack detection and configuration	1	0: Audio jack detection and configuration has not occurred 1: Audio jack detection and configuration has occurred
1	Low resistance occurred	1	0: Low resistance has not occurred 1: Low resistance has occurred
0	Low resistance detection	1	0: Low resistance has not occurred 1: Low resistance has occurred

RES /AUDIO JACK DETECTION INTERRUPT MASK

Address: 19h
Reset Value: 8'b 0000_0000
Type: Read Clear

Bits	Name	Size	Description
[7:3]	Reserved	5	Do Not Use
2	Audio jack detection and configuration	1	1: Mask Audio jack detection and configuration has occurred interrupt
1	Low resistance occurred	1	1: Low resistance has occurred interrupt
0	Low resistance detection	1	1: Low resistance detection has occurred interrupt

AUDIO JACK DETECTION REG1 VALUE

Address: 1Ah
Reset Value: 8'b 1111_1111
Type: Read

Bits	Name	Size	Description
[7:0]	Audio jack detection value	8	Resistance between SBU1 to SBU2

AUDIO JACK DETECTION REG2 VALUE

Address: 1Bh
Reset Value: 8'b 1111_1111
Type: Read

Bits	Name	Size	Description
[7:0]	Audio jack detection value	8	Resistance between SBU2 to SBU1

MIC DETECTION THRESHOLD DATA0

Address: 1Ch
Reset Value: 8'b 0010_0000
Type: Read/Write

Bits	Name	Size	Description
[7:0]	MIC detection threshold DATA0	8	MIC detection threshold DATA0 0010_0000: 300 mV

MIC DETECTION THRESHOLD DATA1

Address: 1Dh
Reset Value: 8'b 1111_1111
Type: Read/Write

Bits	Name	Size	Description
[7:0]	MIC detection threshold DATA1	8	MIC detection threshold DATA1 1111_1111: 2.4 V

I2C RESET

Address: 1Eh
Reset Value: 8'b 0000_0000
Type: W/C

Bits	Name	Size	Description
[7:1]	Reserved	7	Reserved
0	I2C reset	1	0: default 1: I^2C reset

CURRENT SOURCE SETTING

Address: 1Fh
Reset Value: 8'b 0000_0111
Type: Write

Bits	Name	Size	Description
[7:4]	Reserved	4	Reserved
[3:0]	Current Source Setting	4	1111: 1500 μA 0111: 700 μA 0001: 100 μA 0000: invalid

APPLICATION INFORMATION

Over−Voltage Protection

FSA4480 features over−voltage protection (OVP) on receptacle side pins that switches off the internal signal routing path if the input voltage exceeds the OVP threshold.

If OVP is occurred, interrupt signal can be send by INT signal and FLAG data will provide information that which pin had OVP event.

Headset Detection

FSA4480 integrates headset unplug detection function by detecting the CC_IN voltage. The function is always active when device is enabling. DET will be high when CC_IN is low (CC_IN < 1.2 V). When CC_IN = High (CC_IN > 1.5 V), DET will be released to low.

	Device Disable	Device Enable
CC_IN < V_{TH_L} = 1.2 V	DET = 0	DET = 1
CC_IN > V_{TH_H} = 1.5 V	DET = 0	DET = 0

MIC Switch Auto−off Function

The function is active during control bit 0x12h bit[2] = 1. When CC_IN is high (CC_IN > 1.5 V) and L,R, Audio ground switches are under on status, MIC switch will be off and receptacle side pin will be connected to ground for 50 μS first. Then it shows high−Z status under MIC switch is set on status.

Audio Ground Detection and Configuration

The function is active when control bit 0x12h bit[0] = 1 and R, L AGND switches are set to be on status. For type−C interface analog headset, the audio ground could be SBU1 pin or SBU2 pin. The function will provide autonomous detection and configuration to route MIC and audio ground signal accordingly.

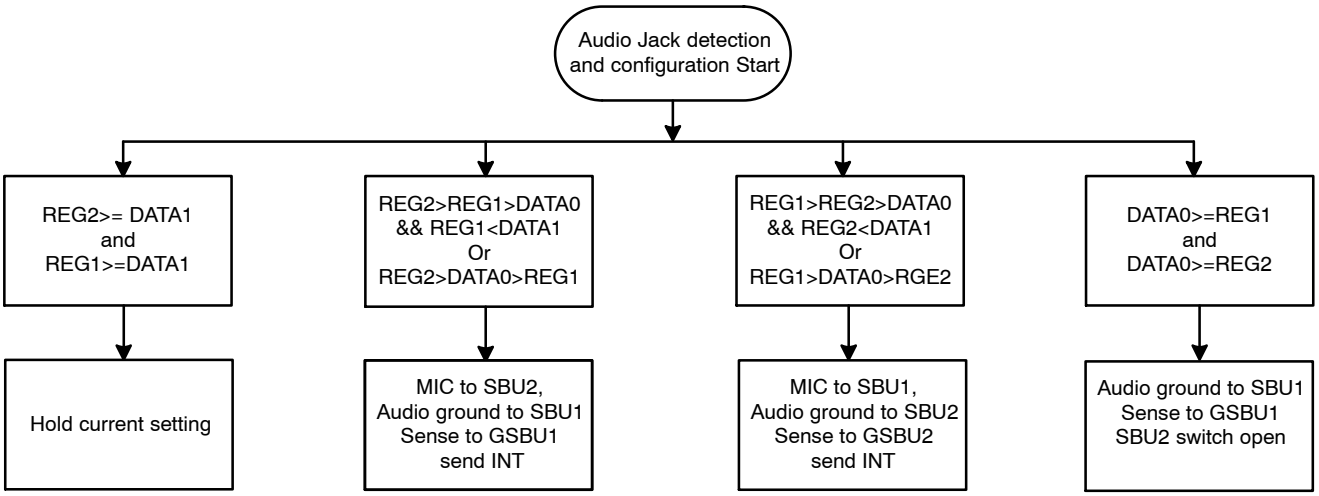


Figure 4.

During detection and configuration, the R, L, Sense, MIC and Audio ground switch will be off. After detection and configuration, R and L switches will turn on according to switch configuration and timing setting. MIC, Sense and Audio ground will turn on according to detection results and timing control setting.

Resistance Detection

The function is active during control bit 0x12h bit[1] = 1. It will monitor the resistance between receptacle side pins and ground. During resistance detection, the switch which is monitored will be off. The detection result will be saved in the resistance flag register. The measurement could be from 1 kΩ to 2.56 MΩ which is controlled by internal register. The detection interval can be set at 100 ms, 1 s or 10 s by register 0x16h.

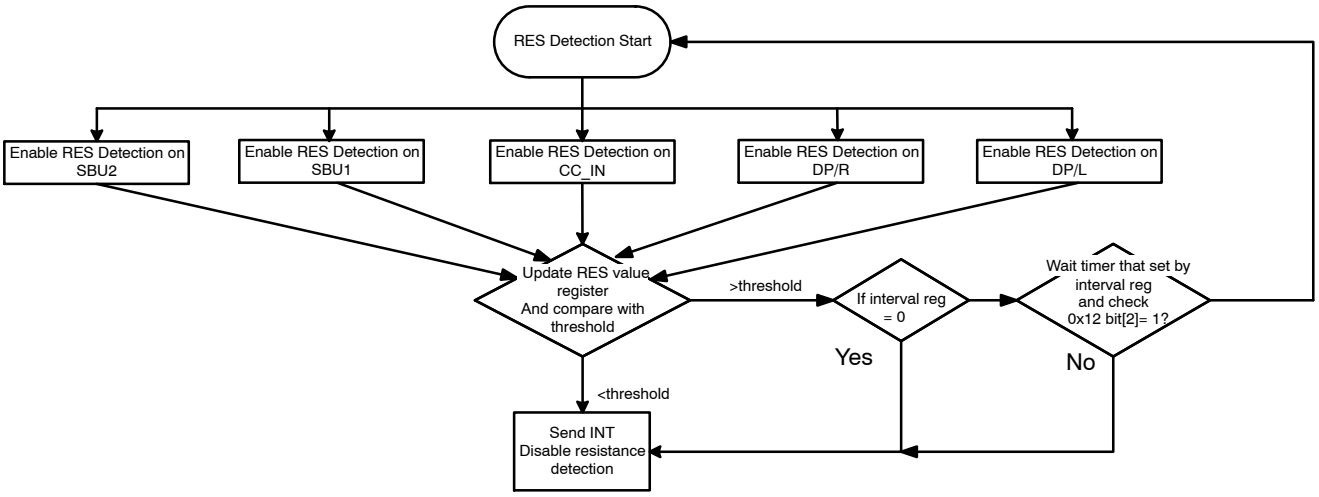


Figure 5.

Manual Switch Control

The function is active during control bit 0x12h bit[4] = 1 and 0x04h = FF. It will provide manual control for device. During this configuration, ADDR and INT pins will be set as logic control input.

MANUAL SWITCH CONTROL

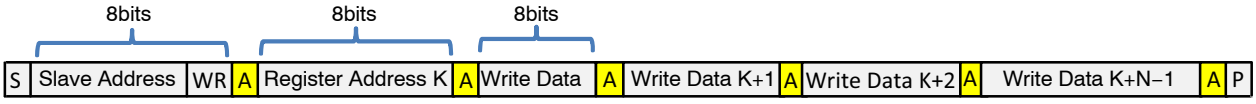
(The function is active during control bit 0x12h bit[4] = 1 and 0x04h = FF. It will provide manual control for device. During this configuration, ADDR and INT pins will be set as logic control input.)

Power	ENN	ADDR	INT	SENSE Switch	Headset Detection	USB Switch	Audio Switch	MIC/ Audio GND Switch	SBU by Pass Switch
OFF	X	X	X	OFF	OFF	OFF	OFF	OFF	OFF
ON	H	X	X	OFF	OFF	OFF	OFF	OFF	OFF
ON	L	0	0	OFF	OFF	ON: DP_R to DP DN_L to DN	OFF	OFF	ON: SBU1 to SBU1_H SBU2 to SBU2_H
ON	L	0	1	OFF	OFF	ON: DP_R to DP DN_L to DN	OFF	OFF	ON: SBU1 to SBU2_H SBU2 to SBU1_H
ON	L	1	0	ON GSBU2 to SESNE	ON	OFF	ON: DP_R to R DN_L to L	ON: SBU1 to MIC SBU2 to Audio GND	OFF
ON	L	1	1	ON GSBU1 to SESNE	ON	OFF	ON: DP_R to R DN_L to L	ON: SBU2 to MIC SBU1 to Audio GND	OFF

I²C INTERFACE

The FSA4480 includes a full I²C slave controller. The I²C slave fully complies with the I²C specification version 2.1 requirements. This block is designed for fast mode, 400 kHz, signals.

Examples of an I²C write and read sequence are shown in below figures respectively.



NOTE: Single Byte read is initiated by Master with P immediately following first data byte.

Figure 6. I²C Write Example

NOTE: If Register is not specified Master will begin read from current register. In this case only sequence showing in Red bracket is needed

	From Master to Slave	**S**	Start Condition	**NA**	NOT Acknowledge (SDA High)	**RD**	Read =1
	From Slave to Master	**A**	Acknowledge (SDA Low)	**WR**	Write = 0	**P**	Stop Condition

Figure 7. I²C Read Example

TEST DIAGRAMS

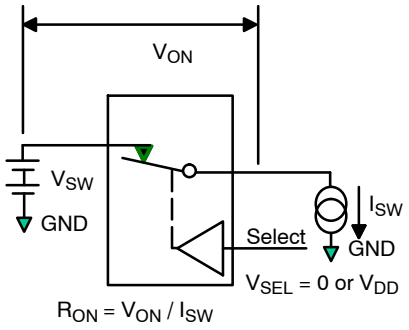
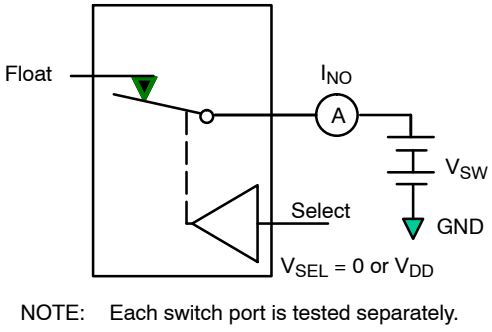


Figure 8. On Resistance



NOTE: Each switch port is tested separately.

Figure 9. Off Leakage (Ioz)

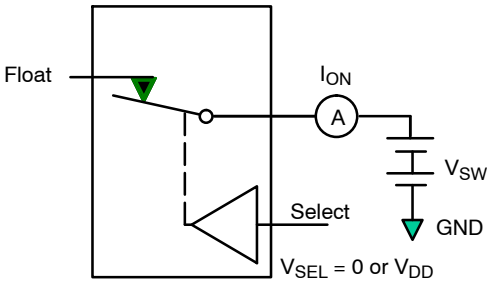
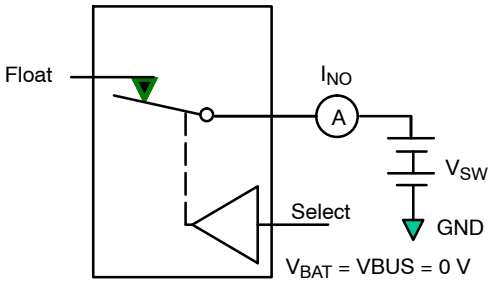


Figure 10. On Leakage



NOTE: Each switch port is tested separately.

Figure 11. Power Off Leakage (Ioff)

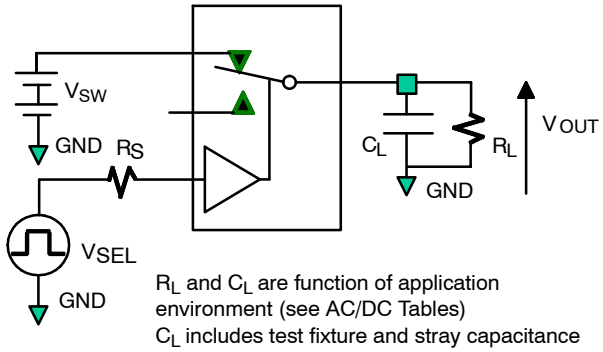


Figure 12. Test Circuit Load

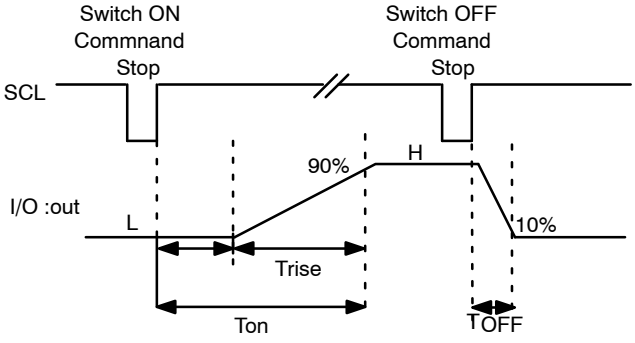
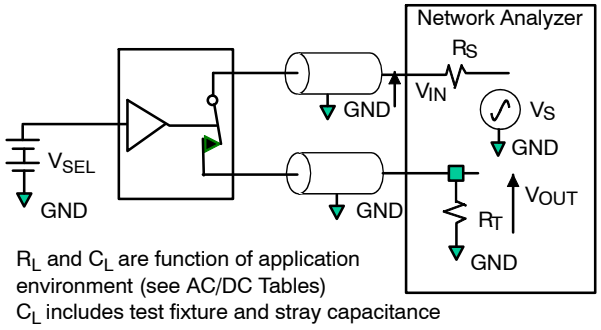
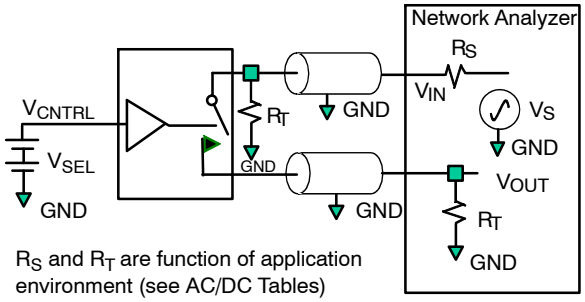


Figure 13. Turn On/Off Waveforms under Manual Mode



R_L and C_L are function of application environment (see AC/DC Tables)
C_L includes test fixture and stray capacitance

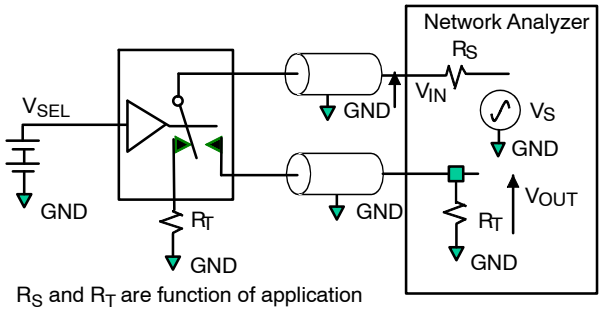
Figure 14. Bandwidth



R_S and R_T are function of application environment (see AC/DC Tables)

OFF − Isolation = 20 Log (V_{OUT}/V_{IN})

Figure 15. Channel Off Isolation



R_S and R_T are function of application environment (see AC/DC Tables)

CROSSTALK = 20 Log (V_{OUT}/V_{IN})

Figure 16. Adjacent Channel Crosstalk

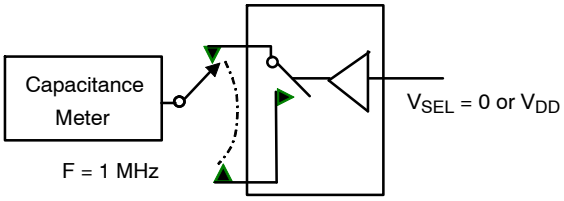


Figure 17. Channel Off Capacitance

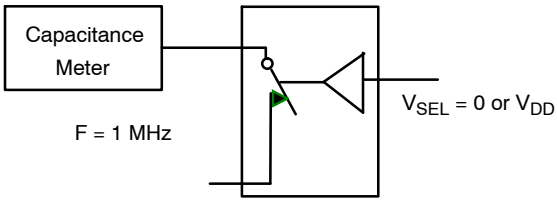
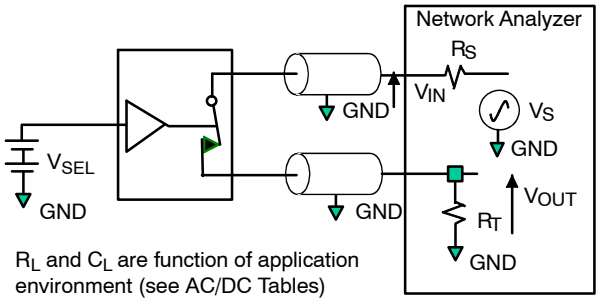


Figure 18. Channel On Capacitance



R_L and C_L are function of application environment (see AC/DC Tables)
C_L includes test fixture and stray capacitance

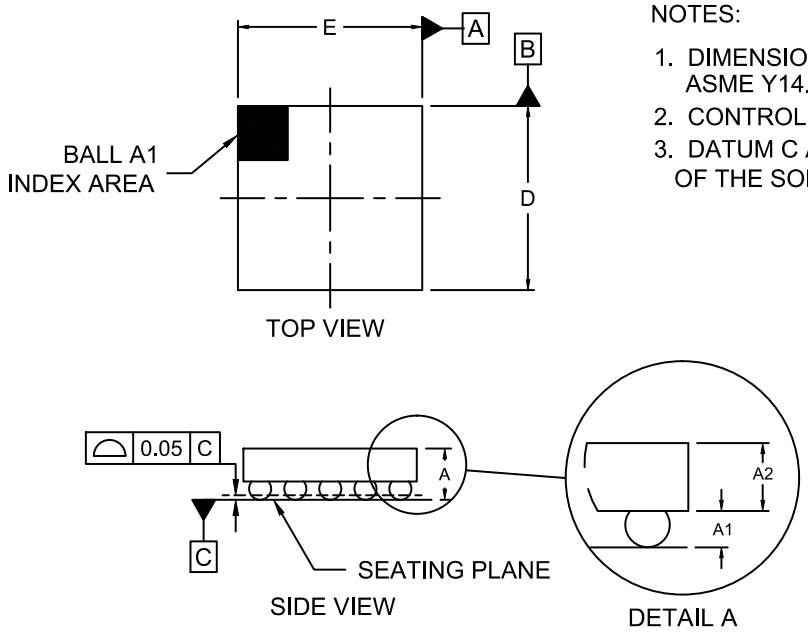
Figure 19. Total Harmonic Distortion (THD + N)

ORDERING INFORMATION

Part Number	Top Mark	Package	D	E	X	Y
FSA4480UCX	6D	25−Ball WLCSP	2.24mm	2.28mm	0.32mm	0.34mm

PACKAGE DIMENSIONS

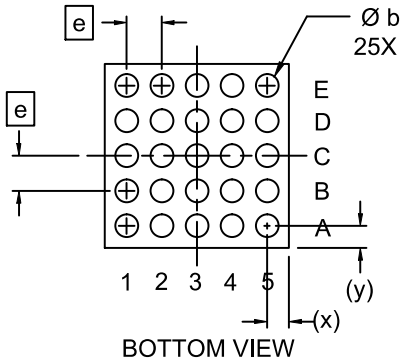
WLCSP25 2.24x2.28x0.586
CASE 567UZ
ISSUE B

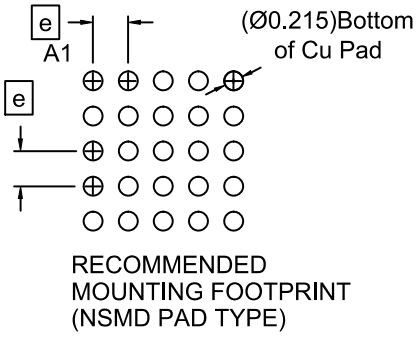


NOTES:

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 2009.
2. CONTROLLING DIMENSION: MILLIMETERS
3. DATUM C APPLIES TO THE SPHERICAL CROWN OF THE SOLDER BALLS

DIM	MILLIMETERS		
	MIN.	NOM.	MAX.
A	0.547	0.586	0.625
A1	0.178	0.208	0.238
A2	0.360	0.378	0.396
b	0.24	0.26	0.28
D	2.250	2.280	2.310
E	2.210	2.240	2.270
e	0.40 BSC		
x	0.305	0.320	0.335
y	0.325	0.340	0.355





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