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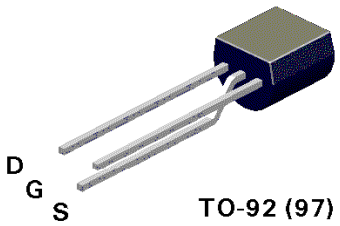
BS270
N-Channel Enhancement Mode Field Effect Transistor

General Description

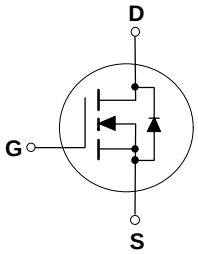
These N-Channel enhancement mode field effect transistors are produced using ON Semiconductor's proprietary, high cell density, DMOS technology. These products have been designed to minimize on-state resistance while provide rugged, reliable, and fast switching performance. They can be used in most applications requiring up to 500mA DC. These products are particularly suited for low voltage, low current applications such as small servo motor control, power MOSFET gate drivers, and other switching applications.

Features

- 400mA, 60V. $R_{DS(ON)}$ = 2Ω @ V_{GS} = 10V.
- High density cell design for low $R_{DS(ON)}$.
- Voltage controlled small signal switch.
- Rugged and reliable.
- High saturation current capability.



TO-92 (97)



Absolute Maximum Ratings

T_A = 25°C unless otherwise noted

Symbol	Parameter	BS270	Units
V_{DSS}	Drain-Source Voltage	60	V
V_{DGR}	Drain-Gate Voltage ($R_{GS} \leq 1M\Omega$)	60	V
V_{GSS}	Gate-Source Voltage - Continuous	±20	V
	- Non Repetitive (tp < 50µs)	±40	
I_D	Drain Current - Continuous	400	mA
	- Pulsed	2000	
P_D	Maximum Power Dissipation	625	mW
	Derate Above 25°C	5	mW/°C
T_J,T_{STG}	Operating and Storage Temperature Range	-55 to 150	°C
T_L	Maximum Lead Temperature for Soldering Purposes, 1/16" from Case for 10 Seconds	300	°C
THERMAL CHARACTERISTICS			
$R_{\theta JA}$	Thermal Resistacne, Junction-to-Ambient	200	°C/W

September-2017, Rev. 2

Publication Order Number:
BS270/D

Electrical Characteristics (T_A = 25°C unless otherwise noted)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
OFF CHARACTERISTICS						
BV_{DSS}	Drain-Source Breakdown Voltage	V_{GS} = 0 V, I_D = 10 µA	60			V
I_{DSS}	Zero Gate Voltage Drain Current	V_{DS} = 60 V, V_{GS} = 0 V			1	µA
		T_J = 125°C			500	µA
I_{GSSF}	Gate - Body Leakage, Forward	V_{GS} = 20 V, V_{DS} = 0 V			10	nA
I_{GSSF}	Gate - Body Leakage, Reverse	V_{GS} = -20 V, V_{DS} = 0 V			-10	nA
ON CHARACTERISTICS (Note 1)						
$V_{GS(th)}$	Gate Threshold Voltage	V_{DS} = V_{GS}, I_D = 250 µA	1	2.1	2.5	V
$R_{DS(ON)}$	Static Drain-Source On-Resistance	V_{GS} = 10 V, I_D = 500 mA		1.2	2	Ω
		T_J = 125°C		2	3.5	
		V_{GS} = 4.5 V, I_D = 75 mA		1.8	3	
$V_{DS(ON)}$	Drain-Source On-Voltage	V_{GS} = 10 V, I_D = 500 mA		0.6	1	V
		V_{GS} = 4.5 V, I_D = 75 mA		0.14	0.225	
$I_{D(ON)}$	On-State Drain Current	V_{GS} = 10 V, V_{DS} ≥ 2 $V_{DS(on)}$	2000	2700		mA
		V_{GS} = 4.5 V, V_{DS} ≥ 2 $V_{DS(on)}$	400	600		
g_{FS}	Forward Transconductance	V_{DS} ≥ 2 $V_{DS(on)}$, I_D = 200 mA	100	320		mS
DYNAMIC CHARACTERISTICS						
C_{iss}	Input Capacitance	V_{DS} = 25 V, V_{GS} = 0 V, f = 1.0 MHz		20	50	pF
C_{oss}	Output Capacitance			11	25	pF
C_{rss}	Reverse Transfer Capacitance			4	5	pF
SWITCHING CHARACTERISTICS (Note 1)						
t_{on}	Turn-On Time	V_{DD} = 30 V, I_D = 500 m A, V_{GS} = 10 V, R_{GEN} = 25 Ω			10	ns
t_{off}	Turn-Off Time				10	ns
DRAIN-SOURCE DIODE CHARACTERISTICS AND MAXIMUM RATINGS						
I_S	Maximum Continuous Drain-Source Diode Forward Current				400	mA
I_{SM}	Maximum Pulsed Drain-Source Diode Forward Current				2000	mA
V_{SD}	Drain-Source Diode Forward Voltage	V_{GS} = 0 V, I_S = 400 mA (Note 1)		0.88	1.2	V

Note:
1. Pulse Test: Pulse Width ≤ 300µs, Duty Cycle ≤ 2.0%.

Typical Electrical Characteristics

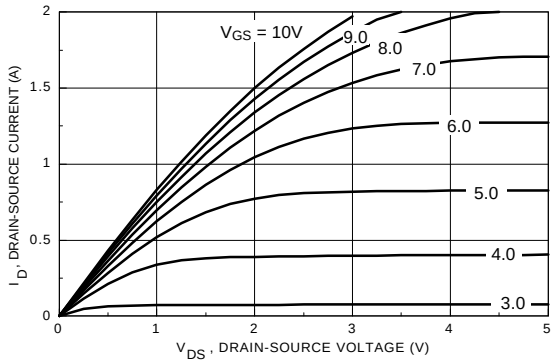


Figure 1. On-Region Characteristics.

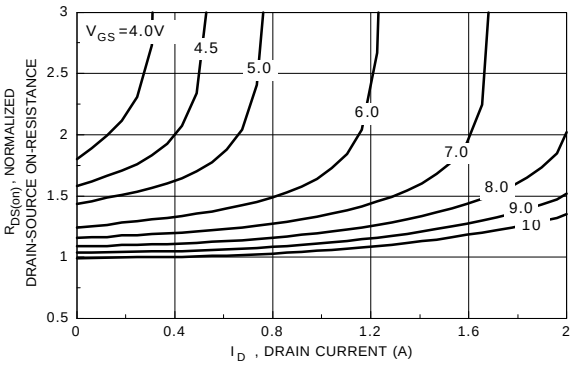


Figure 2. On-Resistance Variation with Gate Voltage and Drain Current.

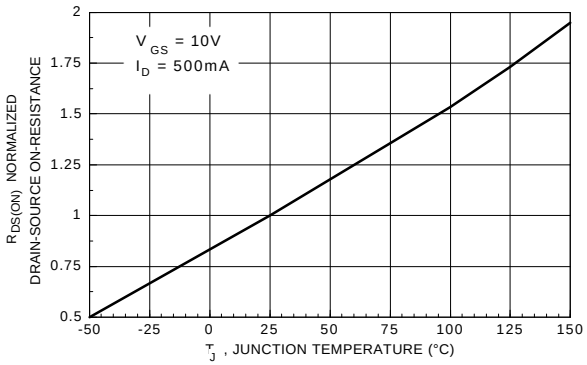


Figure 3. On-Resistance Variation with Temperature.

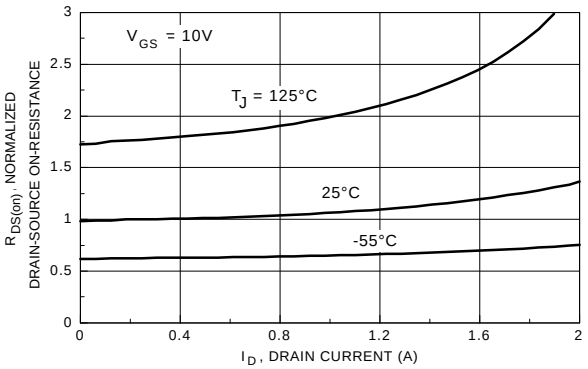


Figure 4. On-Resistance Variation with Drain Current and Temperature.

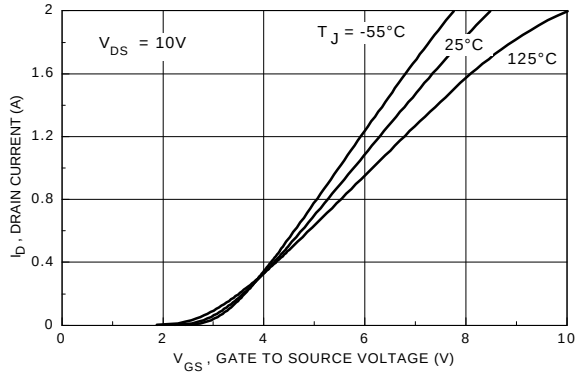


Figure 5. Transfer Characteristics.

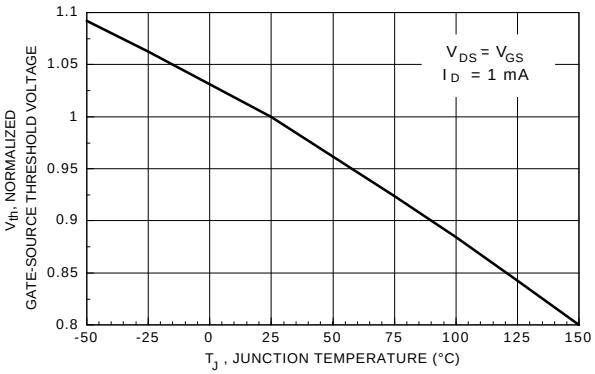


Figure 6. Gate Threshold Variation with Temperature.

Typical Electrical Characteristics (continued)

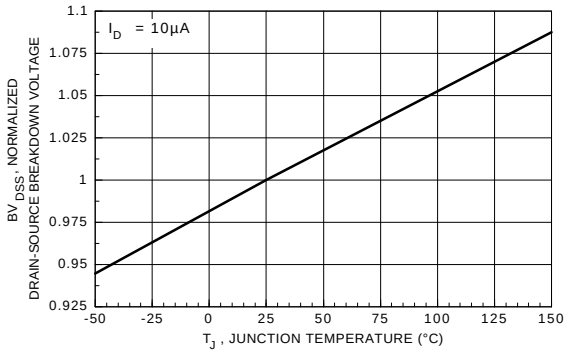


Figure 7. Breakdown Voltage Variation with Temperature.

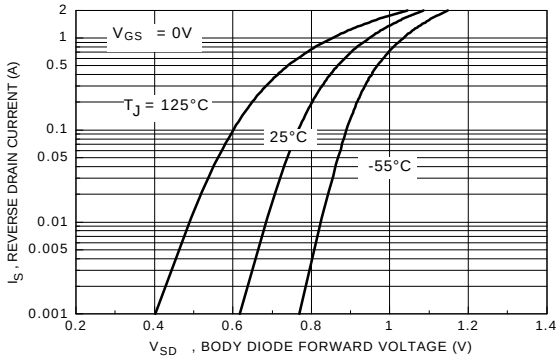


Figure 8. Body Diode Forward Voltage Variation with Current and Temperature.

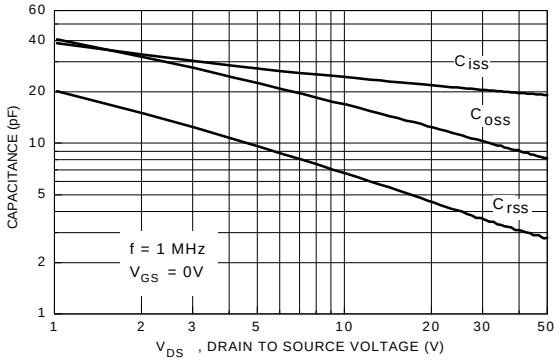


Figure 9. Capacitance Characteristics.

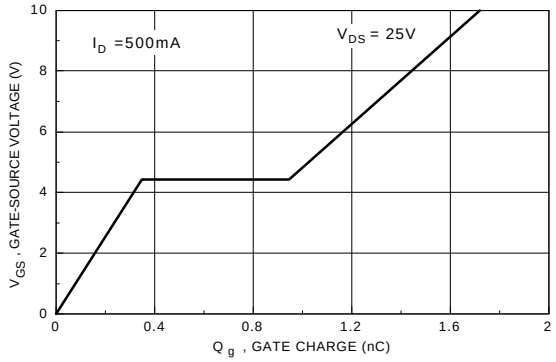


Figure 10. Gate Charge Characteristics.

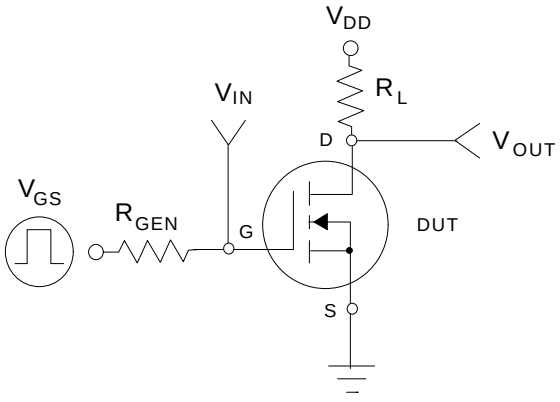


Figure 11. Switching Test Circuit.

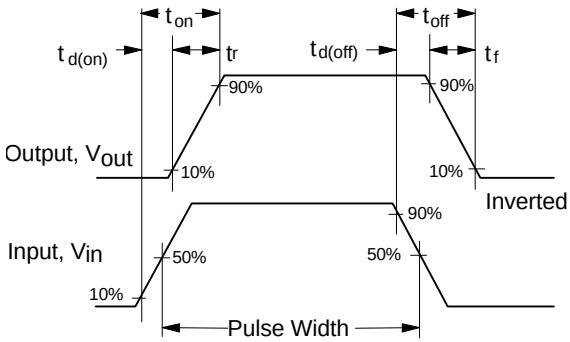


Figure 12. Switching Waveforms.

Typical Electrical Characteristics (continued)

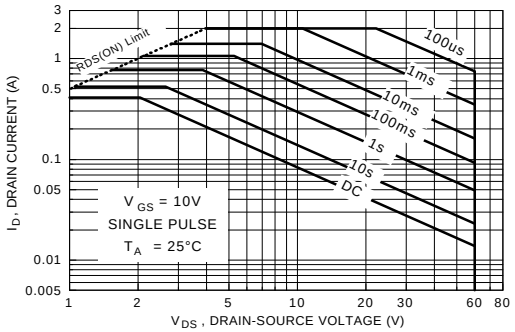


Figure 13. Maximum Safe Operating Area.

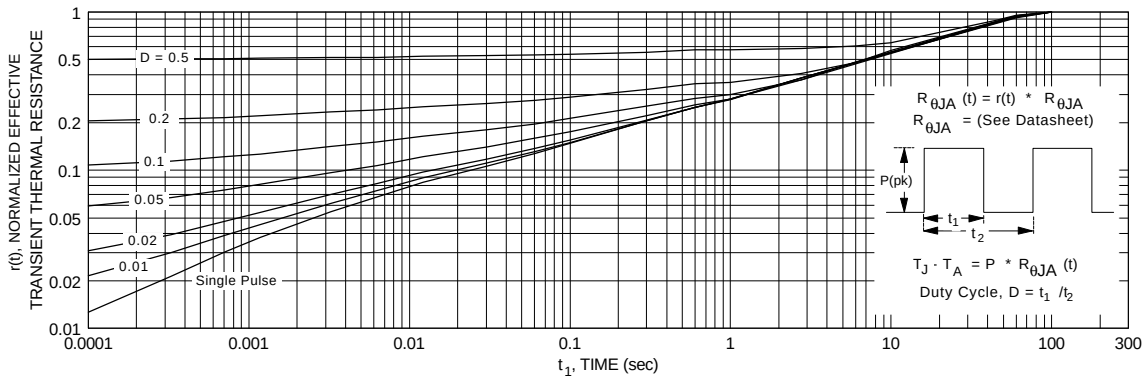
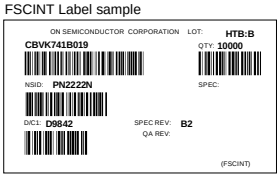


Figure 14. Transient Thermal Response Curve.

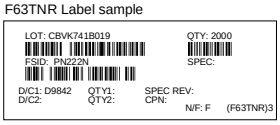
TO-92 Tape and Reel Data

TO-92 Packaging Configuration: Figure 1.0

FSCINT Label sample

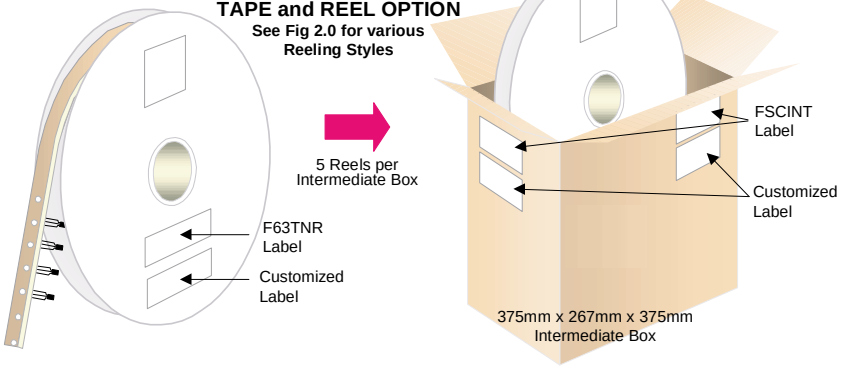


F63TNR Label sample



TAPE and REEL OPTION

See Fig 2.0 for various Reeling Styles



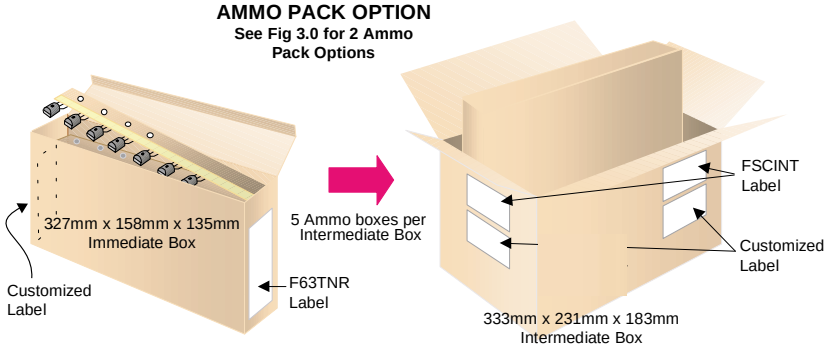
TO-92 TNR/AMMO PACKING INFROMATION

Packing	Style	Quantity	EOL code
Reel	A	2,000	D26Z
	E	2,000	D27Z
Ammo	M	2,000	D74Z
	P	2,000	D75Z

Unit weight = 0.22 gm
Reel weight with components = 1.04 kg
Ammo weight with components = 1.02 kg
Max quantity per intermediate box = 10,000 units

AMMO PACK OPTION

See Fig 3.0 for 2 Ammo Pack Options

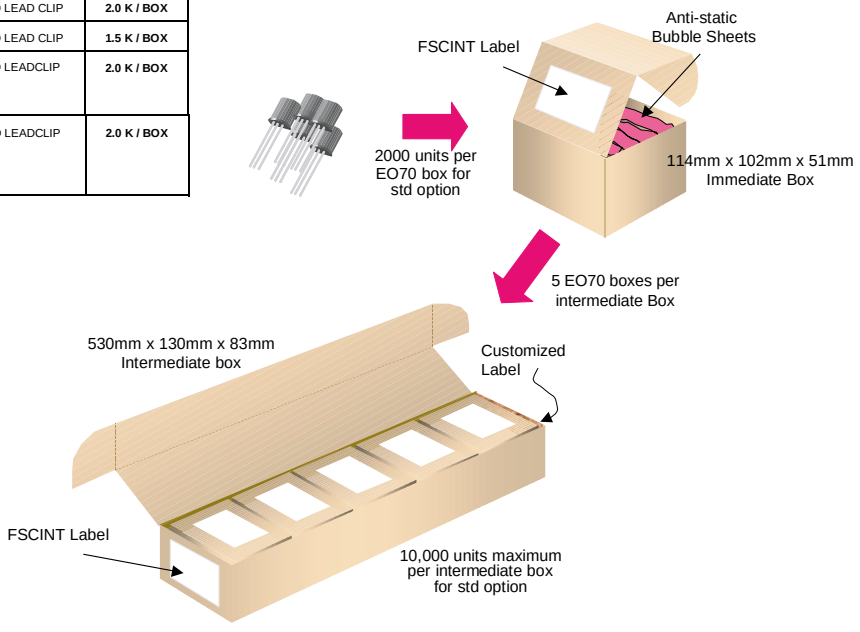


(TO-92) BULK PACKING INFORMATION

EOL CODE	DESCRIPTION	LEADCLIP DIMENSION	QUANTITY
J18Z	TO-18 OPTION STD	NO LEAD CLIP	2.0 K / BOX
J05Z	TO-5 OPTION STD	NO LEAD CLIP	1.5 K / BOX
NO EOL CODE	TO-92 STANDARD STRAIGHT FOR: PKG 92, 94 (NON PROELECTRON SERIES), 96	NO LEADCLIP	2.0 K / BOX
L34Z	TO-92 STANDARD STRAIGHT FOR: PKG 94 (PROELECTRON SERIES BCXXX, BFXXX, BSRXXX), 97, 98	NO LEADCLIP	2.0 K / BOX

BULK OPTION

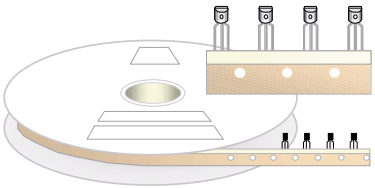
See Bulk Packing Information table



TO-92 Tape and Reel Data, continued

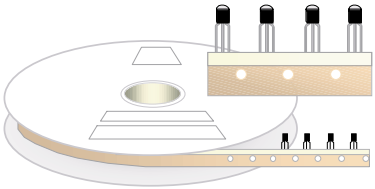
TO-92 Reeling Style
Configuration: Figure 2.0

Machine Option “A” (H)



Style “A”, D26Z, D70Z (s/h)

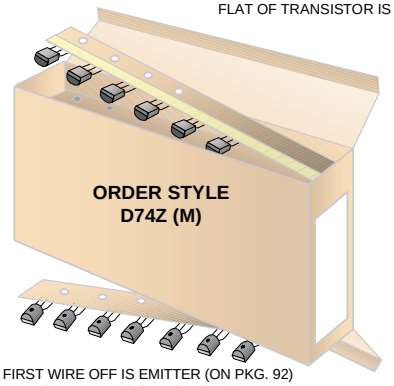
Machine Option “E” (J)



Style “E”, D27Z, D71Z (s/h)

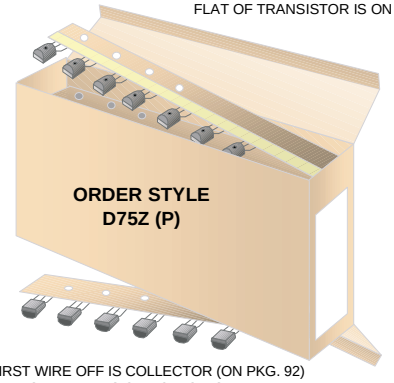
TO-92 Radial Ammo Packaging
Configuration: Figure 3.0

FIRST WIRE OFF IS COLLECTOR
ADHESIVE TAPE IS ON THE TOP SIDE
FLAT OF TRANSISTOR IS ON TOP



FIRST WIRE OFF IS EMITTER (ON PKG. 92)
ADHESIVE TAPE IS ON BOTTOM SIDE
FLAT OF TRANSISTOR IS ON BOTTOM

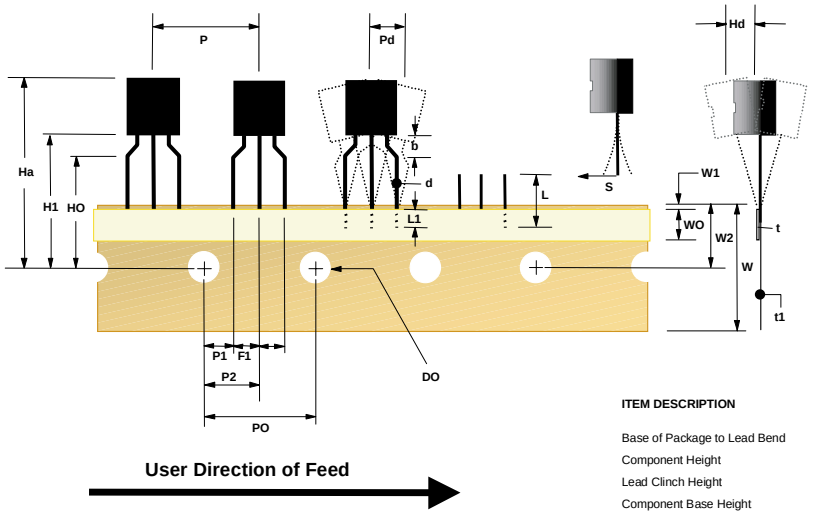
FIRST WIRE OFF IS EMITTER
ADHESIVE TAPE IS ON THE TOP SIDE
FLAT OF TRANSISTOR IS ON BOTTOM



FIRST WIRE OFF IS COLLECTOR (ON PKG. 92)
ADHESIVE TAPE IS ON BOTTOM SIDE
FLAT OF TRANSISTOR IS ON TOP

TO-92 Tape and Reel Data, continued

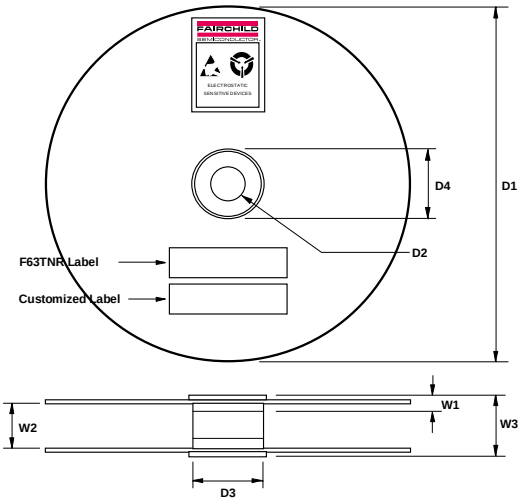
TO-92 Tape and Reel Taping
Dimension Configuration: Figure 4.0



ITEM DESCRIPTION	SYMBOL	DIMENSION
Base of Package to Lead Bend	b	0.098 (max)
Component Height	Ha	0.928 (+/- 0.025)
Lead Clinch Height	HO	0.630 (+/- 0.020)
Component Base Height	H1	0.748 (+/- 0.020)
Component Alignment (side/side)	Pd	0.040 (max)
Component Alignment (front/back)	Hd	0.031 (max)
Component Pitch	P	0.500 (+/- 0.020)
Feed Hole Pitch	PO	0.500 (+/- 0.008)
Hole Center to First Lead	P1	0.150 (+0.009, -0.010)
Hole Center to Component Center	P2	0.247 (+/- 0.007)
Lead Spread	F1/F2	0.104 (+/- 0 .010)
Lead Thickness	d	0.018 (+0.002, -0.003)
Cut Lead Length	L	0.429 (max)
Taped Lead Length	L1	0.209 (+0.051, -0.052)
Taped Lead Thickness	t	0.032 (+/- 0.006)
Carrier Tape Thickness	t1	0.021 (+/- 0.006)
Carrier Tape Width	W	0.708 (+0.020, -0.019)
Hold - down Tape Width	WO	0.236 (+/- 0.012)
Hold - down Tape position	W1	0.035 (max)
Feed Hole Position	W2	0.360 (+/- 0.025)
Sprocket Hole Diameter	DO	0.157 (+0.008, -0.007)
Lead Spring Out	S	0.004 (max)

Note : All dimensions are in inches.

TO-92 Reel
Configuration: Figure 5.0

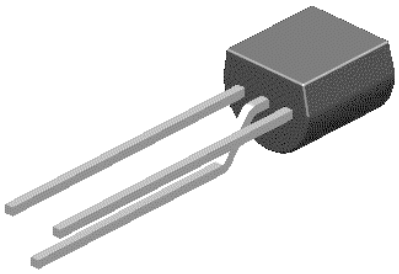


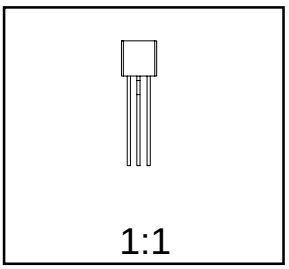
ITEM DESCRIPTION	SYSMBOL	MINIMUM	MAXIMUM
Reel Diameter	D1	13.975	14.025
Arbor Hole Diameter (Standard)	D2	1.160	1.200
(Small Hole)	D2	0.650	0.700
Core Diameter	D3	3.100	3.300
Hub Recess Inner Diameter	D4	2.700	3.100
Hub Recess Depth	W1	0.370	0.570
Flange to Flange Inner Width	W2	1.630	1.690
Hub to Hub Center Width	W3		2.090

Note: All dimensions are inches

TO-92 Package Dimensions

TO-92; TO-18 Reverse Lead Form (J35Z Option) (FS PKG Code 92, 94, 96)

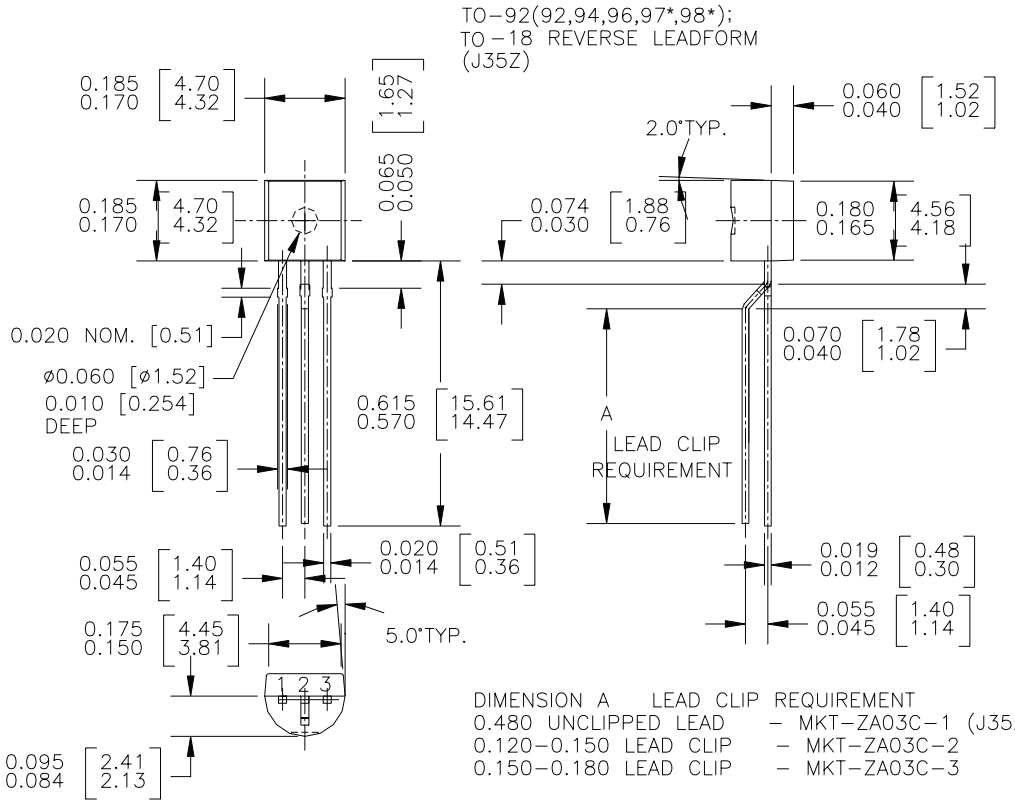




Scale 1:1 on letter size paper

Dimensions shown below are in:
inches [millimeters]

Part Weight per unit (gram): 0.22



DIMENSION A LEAD CLIP REQUIREMENT
0.480 UNCLIPPED LEAD − MKT−ZA03C−1 (J35Z)
0.120−0.150 LEAD CLIP − MKT−ZA03C−2
0.150−0.180 LEAD CLIP − MKT−ZA03C−3

Note: All package 97 or 98 transistors are leadformed to this configuration prior to bulk shipment. Order L34Z option if in-line leads are preferred on package 97 or 98.

***** Standard Option on 97 & 98 package code

PUBLICATION ORDERING INFORMATION

LITERATURE FULFILLMENT:
Literature Distribution Center for ON Semiconductor
19521 E. 32nd Pkwy, Aurora, Colorado 80011 USA
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Email: orderlit@onsemi.com

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