High-Speed, Closed-Loop Buffer

FEATURES

- **Wide Bandwidth: 1000MHz**
- **High Slew Rate: 8000V/μs**
- **Flexible Supply Range:**
  ±1.4V to ±6.3V Dual Supplies
  +2.8V to +12.6V Single Supply
- **Output Current: 60mA (continuous)**
- **Peak Output Current: 350mA**
- **Low Quiescent Current: 5.8mA**
- **Standard Buffer Pinout**
- **Optional Mid-Supply Reference Buffer**

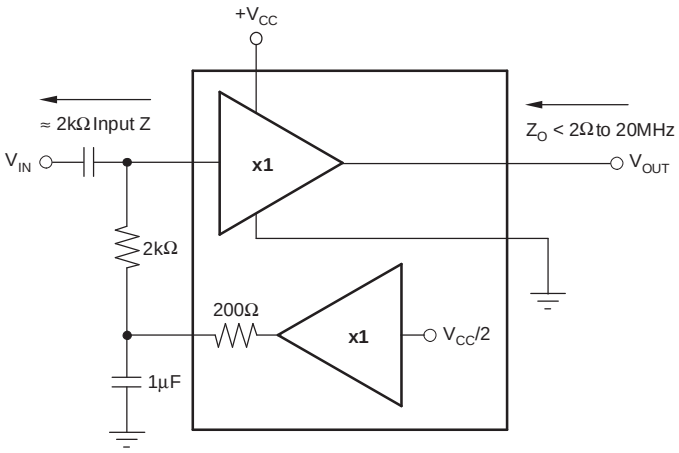
APPLICATIONS

- **Low Impedance Reference Buffers**
- **Clock Distribution Circuits**
- **Video/Broadcast Equipment**
- **Communications Equipment**
- **High-Speed Data Acquisition**
- **Test Equipment and Instrumentation**

DESCRIPTION

The BUF602 is a closed-loop buffer recommended for a wide range of applications. Its wide bandwidth (1000MHz) and high slew rate (8000V/μs) make it ideal for buffering very high-frequency signals. For AC-coupled applications, an optional mid-point reference (V_{REF}) is provided, reducing the number of external components required and the necessary supply current to provide that reference.

The BUF602 is available in a standard SO-8 surface-mount package and in an SOT23-5 where a smaller footprint is needed.



Self-Referenced, AC-Coupled, Single-Supply Buffer

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

ORDERING INFORMATION(1)

PRODUCT	PACKAGE	PACKAGE DESIGNATOR	SPECIFIED TEMPERATURE RANGE	PACKAGE MARKING	ORDERING NUMBER	TRANSPORT MEDIA, QUANTITY
BUF602	SO-8	D	–45°C to +85°C	BUF602	BUF602ID	Rails, 75
					BUF602IDR	Tape and Reel, 2500
BUF602	SOT23-5	DBV	–45°C to +85°C	AWO	BUF602IDBVT	Tape and Reel, 250
					BUF602IDBVR	Tape and Reel, 3000

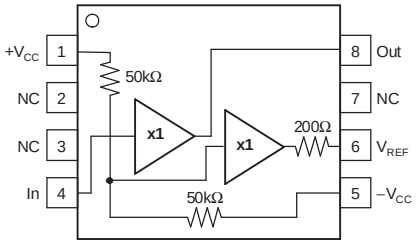
(1) For the most current package and ordering information, see the Package Option Addendum at the end of this document or see the TI web site at www.ti.com.

ABSOLUTE MAXIMUM RATINGS(1)

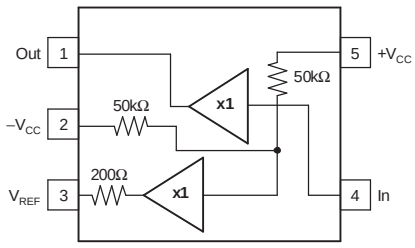
Power Supply	±6.5V_{DC}
Internal Power Dissipation	See Thermal Information
Input Common-Mode Voltage Range	±V_S
Storage Temperature Range: D, DBV	–65°C to +125°C
Lead Temperature (soldering, 10s)	+300°C
Junction Temperature (T_J)	+150°C
ESD Rating:	
Human Body Model (HBM)	2000V
Charge Device Model (CDM)	1000V
Machine Model (MM)	200V

(1) Stresses above these ratings may cause permanent damage. Exposure to absolute maximum conditions for extended periods may degrade device reliability. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those specified is not supported.

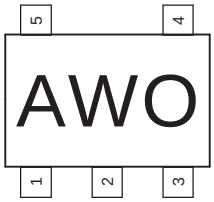
Top View



SO–8
NC = No Connection



SOT23–5



Pin Orientation/Package Marking

ELECTRICAL CHARACTERISTICS: V_S = ±5V

Boldface limits are tested at **+25°C.**
At R_L = 100Ω, unless otherwise noted.

PARAMETER	CONDITIONS	BUF602ID, IDBV				UNITS	MIN/ MAX	TEST LEVEL(1)
		TYP	MIN/MAX OVER TEMPERATURE					
		+25°C	+25°C(2)	0°C to 70°C(3)	–40°C to +85°C(3)			
AC PERFORMANCE	(See figure 30)							
Bandwidth	V_O = 500mV$_{PP}$	1000	560	550	540	MHz	min	B
	V_O = 1V$_{PP}$	920				MHz	typ	C
Full Power Bandwidth	V_O = 5V$_{PP}$	880				MHz	typ	C
Bandwidth for 0.1dB Flatness	V_O = 500mV$_{PP}$	240				MHz	typ	C
Slew Rate	V_O = 5V Step	8000	7000	6000	5000	V/µs	min	B
Rise Time and Fall Time	V_O = 0.2V Step	350	625	640	650	ps	max	B
Settling Time to 0.05%	V_O = 1V Step	6				ns	typ	C
Harmonic Distortion	V_O = 2V$_{PP}$, 5MHz							
2nd-Harmonic	R_L = 100Ω	–57	–44	–44	–42	dBc	max	B
	R_L = 500Ω	–76	–63	–62	–60	dBc	max	B
3rd-Harmonic	R_L = 100Ω	–68	–63	–63	–63	dBc	max	B
	R_L = 500Ω	–98	–85	–84	–82	dBc	max	B
Input Voltage Noise	f > 100kHz	4.8	5.1	5.6	6.0	nV/√Hz	max	B
Input Current Noise	f > 100kHz	2.1	2.6	2.7	2.8	pA/√Hz	max	B
Differential Gain	NTSC, R_L = 150Ω to 0V	0.15				%	typ	C
Differential Phase	NTSC, R_L = 150Ω to 0V	0.04				°	typ	C
BUFFER DC PERFORMANCE(4)								
Maximum Gain	R_L = 500Ω	0.99	**1**	1	1	V/V	max	A
Minimum Gain	R_L = 500Ω	0.99	**0.98**	0.98	0.98	V/V	min	A
Input Offset Voltage		±16	**±30**	±36	±38	mV	max	A
Average Input Offset Voltage Drift				±125	±125	µV/°C	max	B
Input Bias Current		±3	**±7**	±8	±8.5	µA	max	A
Average Input Bias Current Drift				±20	±20	nA/°C	max	B
BUFFER INPUT								
Input Impedance		1.0 || 2.1				MΩ || pF	typ	C
BUFFER OUTPUT								
Output Voltage Swing	R_L = 100Ω	±3.8	±3.7	±3.7	±3.7	V	min	B
	R_L = 500Ω	±4.0	**±3.8**	±3.8	±3.8	V	min	A
Output Current (Continuous)	V_O = 0V	±60	**±50**	±49	±48	mA	min	A
Peak Output Current	V_O = 0V	±350				mA	typ	C
Closed-Loop Output Impedance	f ≤ 10MHz	1.4				Ω	typ	C
POWER SUPPLY								
Specified Operating Voltage		±5				V	typ	C
Maximum Operating Voltage			**±6.3**	±6.3	±6.3	V	max	A
Minimum Operating Voltage			**±1.4**	±1.4	±1.4	V	min	B
Maximum Quiescent Current	V_S = ±5V	5.8	**6.3**	6.9	7.2	mA	max	A
Minimum Quiescent Current	V_S = ±5V	5.8	**5.3**	4.9	4.3	mA	min	A
Power-Supply Rejection Ratio (+PSRR)		54	**48**	46	45	dB	min	A
THERMAL CHARACTERISTICS								
Specification: ID		–40 to +85				°C	typ	C
Thermal Resistance θ_{JA}								
D SO-8	Junction-to-Ambient	125				°C/W	typ	C
DBV SOT23-5	Junction-to-Ambient	150				°C/W	typ	C

(1) Test levels: (A) 100% tested at +25°C. Over temperature limits set by characterization and simulation. (B) Limits set by characterization and simulation. (C) Typical value only for information.
(2) Junction temperature = ambient for +25°C specifications.
(3) Junction temperature = ambient at low temperature limit; junction temperature = ambient +8°C at high temperature limit for over temperature specifications.
(4) Current is considered positive out of node.

ELECTRICAL CHARACTERISTICS: V_S = +5V

Boldface limits are tested at **+25°C.**
At R_L = 100Ω to V_S/2, unless otherwise noted.

PARAMETER	CONDITIONS	BUF602ID, IDBV				UNITS	MIN/ MAX	TEST LEVEL(1)
		TYP	MIN/MAX OVER TEMPERATURE					
		+25°C	+25°C(2)	0°C to 70°C(3)	–40°C to +85°C(3)			
AC PERFORMANCE	(See figure 31)							
Bandwidth	V_O = 500mV$_{PP}$	780	400	400	390	MHz	min	B
	V_O = 1V$_{PP}$	700				MHz	typ	C
Full-Power Bandwidth	V_O = 3V$_{PP}$	420				MHz	typ	C
Bandwidth for 0.1dB Flatness	V_O = 500mV$_{PP}$	130				MHz	typ	C
Slew Rate	V_O = 3V Step	2500	1800	1600	1400	V/µs	min	B
Rise Time and Fall Time	V_O = 0.2V Step	450	875	875	900	ps	max	B
Settling Time to 0.05%	V_O = 1V Step	6				ns	typ	C
Harmonic Distortion	V_O = 2V$_{PP}$, 5MHz							
2nd-Harmonic	R_L = 100Ω	–50	–45	–44	–43	dBc	max	B
	R_L = 500Ω	–73	–62	–61	–60	dBc	max	B
3rd-Harmonic	R_L = 100Ω	–70	–64	–64	–63	dBc	max	B
	R_L = 500Ω	–73	–72	–72	–71	dBc	max	B
Input Voltage Noise	f > 100kHz	4.9	5.2	5.7	6.1	nV/√Hz	max	B
Input Current Noise	f > 100kHz	2.2	2.7	2.8	2.9	pA/√Hz	max	B
Differential Gain	NTSC, R_L = 100Ω to V_S/2	0.16				%	typ	C
Differential Phase	NTSC, R_L = 100Ω to V_S/2	0.05				°	typ	C
BUFFER DC PERFORMANCE(4)								
Maximum Gain	R_L = 500Ω	0.99	**1**	1	1	V/V	max	A
Minimum Gain	R_L = 500Ω	0.99	**0.98**	0.98	0.98	V/V	min	A
Input Offset Voltage		±16	**±30**	±36	±38	mV	max	A
Average Input Offset Voltage Drift				±125	±125	µV/°C	max	B
Input Bias Current		±3	**±7**	±8	±8.5	µA	max	A
Average Input Bias Current Drift				±20	±20	nA/°C	max	B
BUFFER INPUT								
Input Impedance		1.0 || 2.1				MΩ || pF	typ	C
BUFFER OUTPUT								
Most Positive Output Voltage	R_L = 100Ω	+3.9	+3.7	+3.7	+3.7	V	min	B
	R_L = 500Ω	+4.1	**+3.8**	+3.8	+3.8	V	min	A
Least Positive Output Voltage	R_L = 100Ω	+1.1	+1.3	+1.3	+1.3	V	max	B
	R_L = 500Ω	+0.9	**+1.2**	+1.2	+1.2	V	max	A
Output Current (Continuous)	V_O = 0V	±60	**±50**	±49	±48	mA	min	A
Peak Output Current	V_O = 0V	±160				mA	typ	C
Closed-Loop Output Impedance	f ≤ 10MHz	1.4				Ω	typ	C
MID-POINT REFERENCE OUTPUT								
Maximum Mid-Supply Reference Voltage		2.5	**2.6**	2.6	2.6	V	max	A
Minimum Mid-Supply Reference Voltage		2.5	**2.4**	2.4	2.4	V	min	A
Mid-Supply Output Current, Sourcing		800				µA	typ	C
Mid-Supply Output Current, Sinking		70				µA	typ	C
Mid-Supply Output Impedance		200				Ω	typ	C

(1) Test levels: (A) 100% tested at +25°C. Over temperature limits set by characterization and simulation. (B) Limits set by characterization and simulation. (C) Typical value only for information.
(2) Junction temperature = ambient for +25°C specifications.
(3) Junction temperature = ambient at low temperature limit; junction temperature = ambient +4°C at high temperature limit for over temperature specifications.
(4) Current is considered positive out of node.

ELECTRICAL CHARACTERISTICS: V_S = +5V (continued)

Boldface limits are tested at **+25°C.**
At R_L = 100Ω to V_S/2, unless otherwise noted.

PARAMETER	CONDITIONS	BUF602ID, IDBV				UNITS	MIN/ MAX	TEST LEVEL[1]
		TYP	MIN/MAX OVER TEMPERATURE					
		+25°C	+25°C[2]	0°C to 70°C[3]	–40°C to +85°C[3]			
POWER SUPPLY								
Specified Operating Voltage		+5				V	typ	C
Maximum Operating Voltage			**+12.6**	+12.6	+12.6	V	max	A
Minimum Operating Voltage			**+2.8**	+2.8	+2.8	V	min	B
Maximum Quiescent Current	V_S = +5V	5.3	**5.8**	6.3	6.5	mA	max	A
Minimum Quiescent Current	V_S = +5V	5.3	**4.8**	4.5	3.9	mA	min	A
Power-Supply Rejection Ratio (+PSRR)		52	**46**	44	43	dB	min	A
THERMAL CHARACTERISTICS								
Specification: ID		–40 to +85				°C	typ	C
Thermal Resistance θ_{JA}								
D SO-8	Junction-to-Ambient	125				°C/W	typ	C
DBV SOT23-5	Junction-to-Ambient	150				°C/W	typ	C

ELECTRICAL CHARACTERISTICS: V_S = +3.3V

Boldface limits are tested at **+25°C.**
At R_L = 100Ω, unless otherwise noted.

PARAMETER	CONDITIONS	BUF602ID, IDBV				UNITS	MIN/MAX	TEST LEVEL(1)
		TYP	MIN/MAX OVER TEMPERATURE					
		+25°C	+25°C(2)	0°C to 70°C(3)	–40°C to +85°C(3)			
AC PERFORMANCE								
Bandwidth	V_O = 500mV$_{PP}$	600	320	320	310	MHz	min	B
Full Power Bandwidth	V_O = 1V$_{PP}$	520				MHz	typ	C
Bandwidth for 0.1dB Flatness	V_O = 500mV$_{PP}$	110				MHz	typ	C
Slew Rate	V_O = 1.4V Step	800	650	600	600	V/µs	min	B
Rise Time and Fall Time	V_O = 0.2V Step	580	1100	1100	1150	ps	max	B
Settling Time to 0.05%	V_O = 1V Step	6.5				ns	typ	C
Harmonic Distortion	V_O = 1V$_{PP}$, 5MHz							
2nd-Harmonic	R_L = 100Ω	–59	–49	–49	–48	dBc	max	B
	R_L = 500Ω	–76	–61	–57	–53	dBc	max	B
3rd-Harmonic	R_L = 100Ω	–70	–51	–48	–44	dBc	max	B
	R_L = 500Ω	–63	–51	–48	–44	dBc	max	B
Input Voltage Noise	f > 100kHz	4.9	5.2	5.7	6.1	nV/√Hz	max	B
Input Current Noise	f > 100kHz	2.2	2.7	2.8	2.9	pA/√Hz	max	B
BUFFER DC PERFORMANCE(4)								
Maximum Gain	R_L = 500Ω	0.99	**1**	1	1	V/V	max	A
Minimum Gain	R_L = 500Ω	0.99	**0.98**	0.98	0.98	V/V	min	A
Input Offset Voltage		±16	**±30**	±36	±38	mV	max	A
Average Input Offset Voltage Drift				±125	±125	µV/°C	max	B
Input Bias Current		±3	**±7**	±8	±8.5	µA	max	A
Average Input Bias Current Drift				±20	±20	nA/°C	max	B
BUFFER INPUT								
Input Impedance		1.0 || 2.1				MΩ || pF	typ	C
BUFFER OUTPUT								
Most Positive Output Voltage	R_L = 100Ω	+2.1	+2.0	+2.0	+2.0	V	min	B
	R_L = 500Ω	+2.3	**+2.2**	+2.2	+2.2	V	min	A
Least Positive Output Voltage	R_L = 100Ω	+1.2	+1.3	+1.3	+1.3	V	max	B
	R_L = 500Ω	+1.0	**+1.1**	+1.1	+1.1	V	max	A
Output Current (Continuous)	V_O = 0	±60	**±50**	±49	±48	mA	min	A
Peak Output Current		±100				mA	typ	C
Closed-Loop Output Impedance	f ≤ 10MHz	1.4				Ω	typ	C
MID-POINT REFERENCE OUTPUT								
Maximum Mid-Supply Reference Voltage		1.65	**1.72**	1.72	1.72	V	max	A
Minimum Mid-Supply Reference Voltage		1.65	**1.58**	1.58	1.58	V	min	A
Mid-Supply Output Current, Sourcing		500				µA	typ	C
Mid-Supply Output Current, Sinking		60				µA	typ	C
Mid-Supply Output Impedance		200				Ω	typ	C
POWER SUPPLY								
Specified Operating Voltage		+3.3				V	typ	C
Maximum Operating Voltage			**+12.6**	+12.6	+12.6	V	max	A
Minimum Operating Voltage			**+2.8**	+2.8	+2.8	V	min	B
Maximum Quiescent Current	V_S = +3.3V	5.0	**5.5**	6.0	6.3	mA	max	A
Minimum Quiescent Current	V_S = +3.3V	5.0	**4.5**	4.2	3.8	mA	min	A
Power-Supply Rejection Ratio (+PSRR)		50	**44**	42	41	dB	min	A

(1) Test levels: (A) 100% tested at +25°C. Over temperature limits set by characterization and simulation. (B) Limits set by characterization and simulation. (C) Typical value only for information.
(2) Junction temperature = ambient for +25°C specifications.
(3) Junction temperature = ambient at low temperature limit; junction temperature = ambient +2°C at high temperature limit for over temperature specifications.
(4) Current is considered positive out of node.

ELECTRICAL CHARACTERISTICS: V_S = +3.3V (continued)

Boldface limits are tested at **+25°C.**
At R_L = 100Ω, unless otherwise noted.

PARAMETER	CONDITIONS	BUF602ID, IDBV				UNITS	MIN/ MAX	TEST LEVEL(1)
		TYP	MIN/MAX OVER TEMPERATURE					
		+25°C	+25°C(2)	0°C to 70°C(3)	–40°C to +85°C(3)			
THERMAL CHARACTERISTICS								
Specification: ID		–40 to +85				°C	typ	C
Thermal Resistance θ_{JA}								
D SO-8	Junction-to-Ambient	125				°C/W	typ	C
DBV SOT23-5	Junction-to-Ambient	150				°C/W	typ	C

TYPICAL CHARACTERISTICS: V_S = ±5V

At T_A = +25°C and R_L = 100Ω, unless otherwise noted.

BUFFER BANDWIDTH vs OUTPUT VOLTAGE

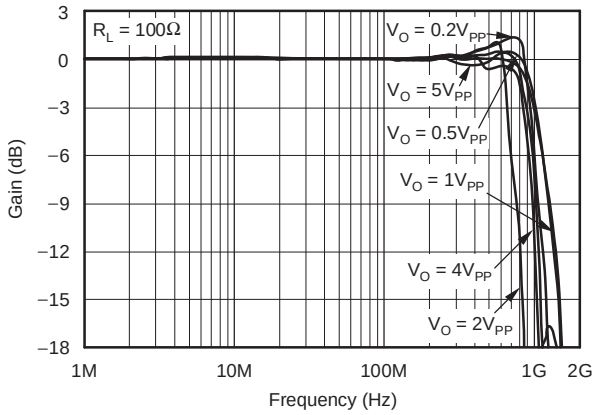


Figure 1.

BUFFER BANDWIDTH vs LOAD RESISTANCE

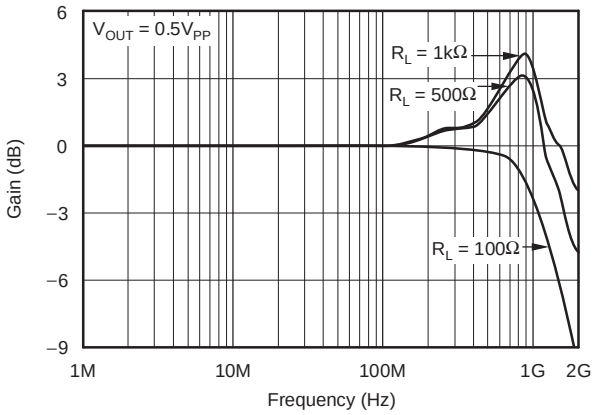


Figure 2.

BUFFER GAIN FLATNESS

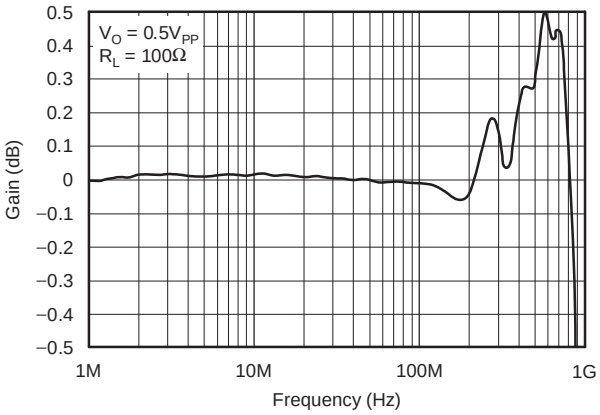


Figure 3.

INPUT VOLTAGE AND CURRENT NOISE DENSITY

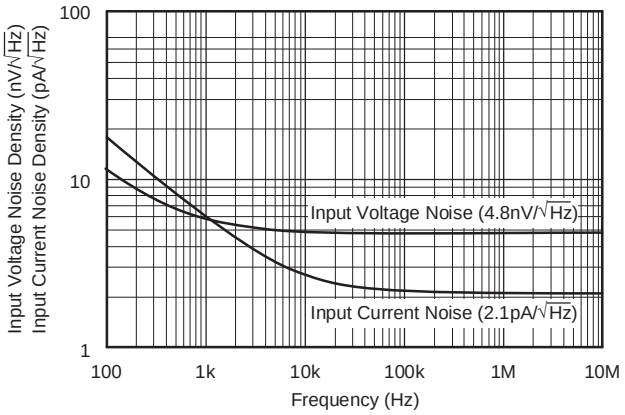


Figure 4.

BUFFER SMALL-SIGNAL PULSE RESPONSE

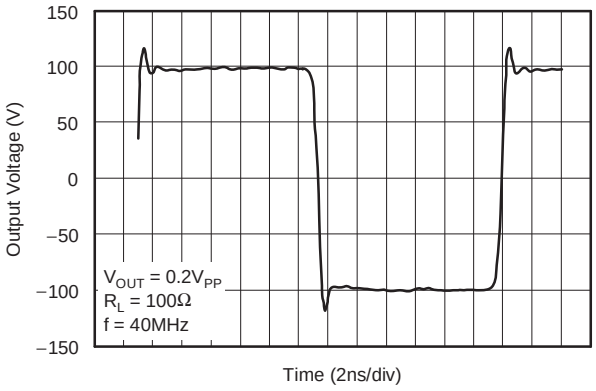


Figure 5.

BUFFER LARGE-SIGNAL PULSE RESPONSE

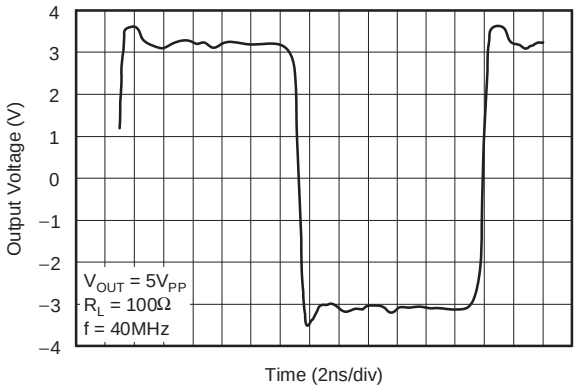


Figure 6.

TYPICAL CHARACTERISTICS: V_S = ±5V (continued)

At T_A = +25°C and R_L = 100Ω, unless otherwise noted.

HARMONIC DISTORTION vs FREQUENCY

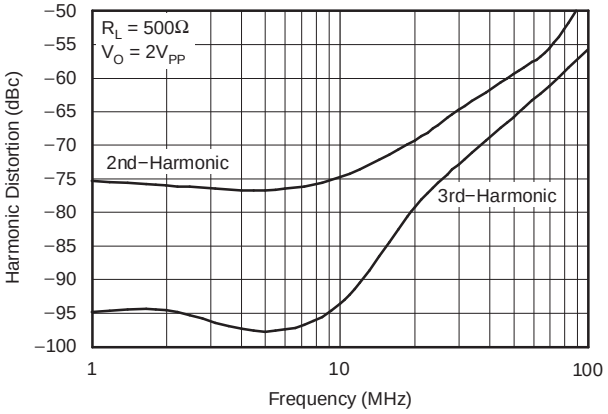


Figure 7.

5MHz HARMONIC DISTORTION vs LOAD RESISTANCE

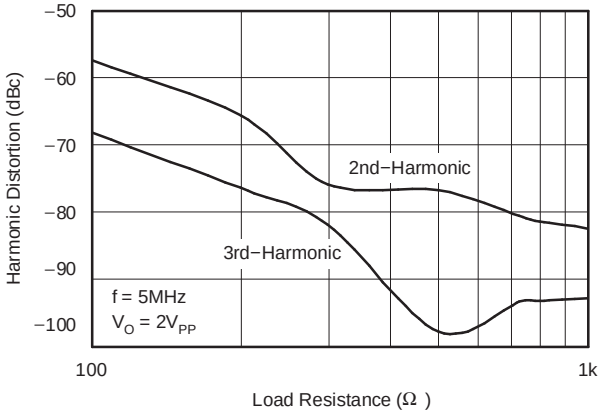


Figure 8.

HARMONIC DISTORTION vs OUTPUT VOLTAGE

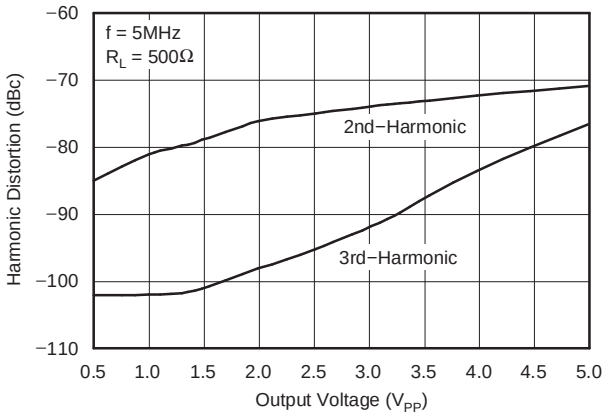


Figure 9.

5MHz HARMONIC DISTORTION vs SUPPLY VOLTAGE

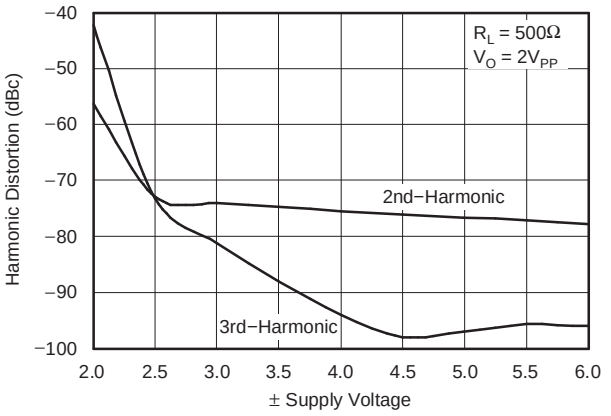


Figure 10.

BUFFER OUTPUT IMPEDANCE

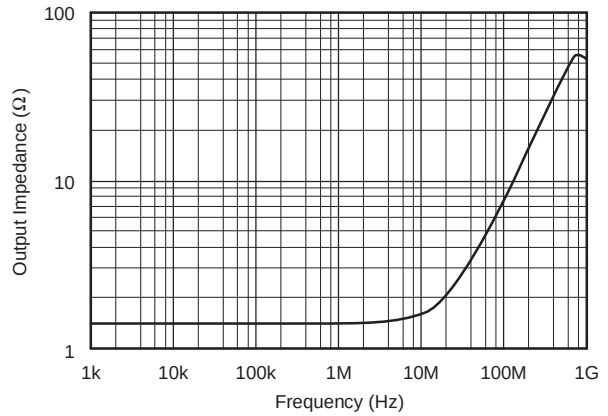


Figure 11.

BUFFER GROUP DELAY TIME vs FREQUENCY

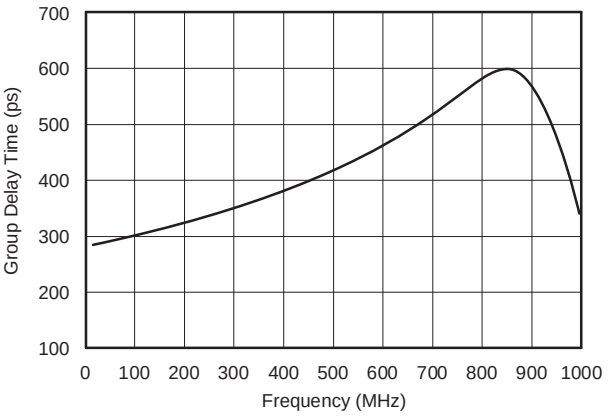


Figure 12.

TYPICAL CHARACTERISTICS: V_S = ±5V (continued)

At T_A = +25°C and R_L = 100Ω, unless otherwise noted.

POWER-SUPPLY REJECTION RATIO vs FREQUENCY

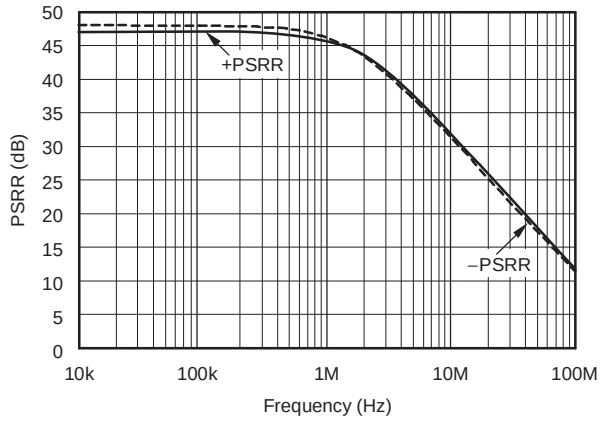


Figure 13.

OUTPUT SWING VOLTAGE vs TEMPERATURE

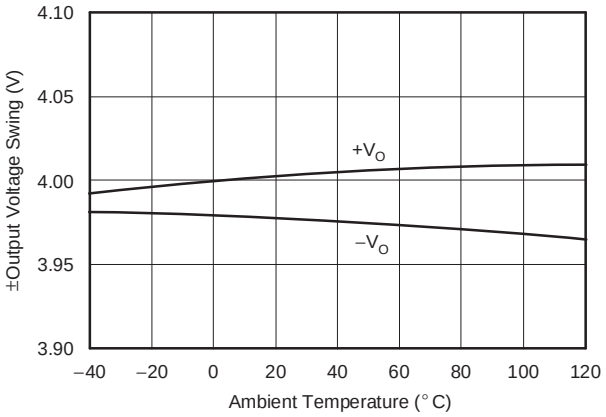


Figure 14.

DC DRIFT vs TEMPERATURE

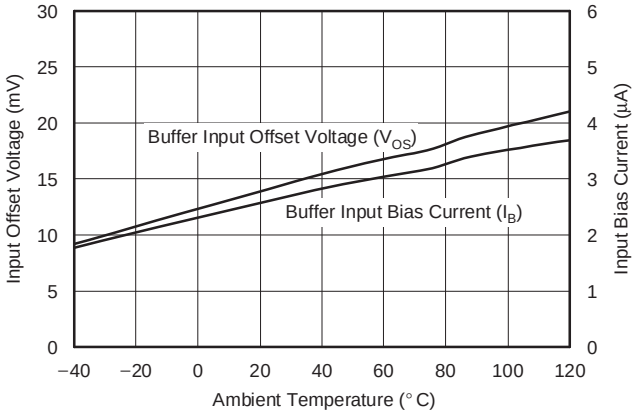


Figure 15.

BUFFER OUTPUT VOLTAGE AND CURRENT LIMITATIONS

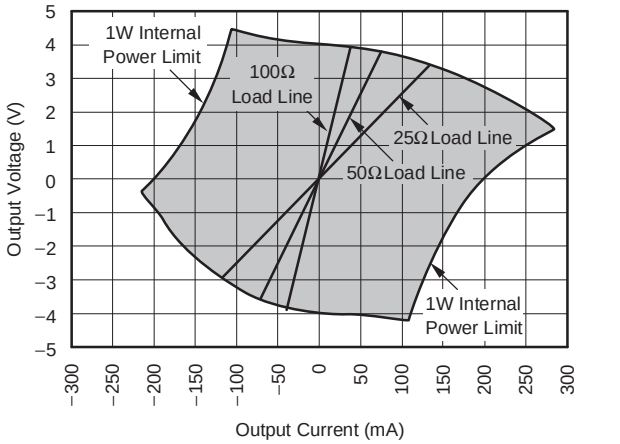


Figure 16.

R_S vs CAPACITIVE LOAD

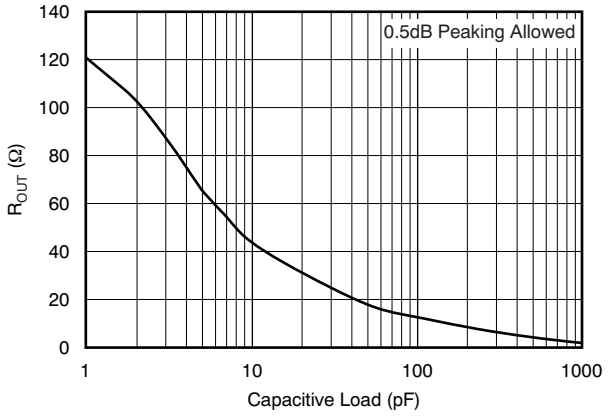


Figure 17.

FREQUENCY RESPONSE vs CAPACITIVE LOAD

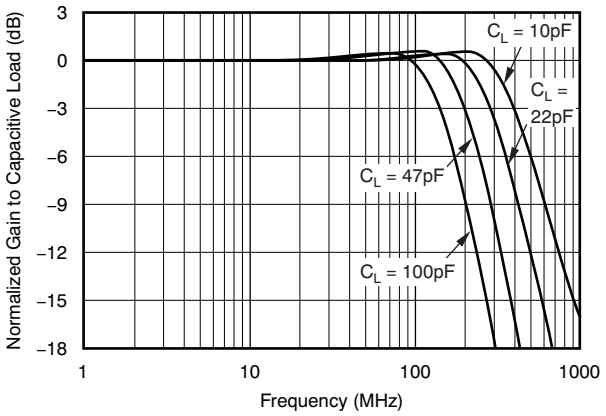


Figure 18.

TYPICAL CHARACTERISTICS: V_S = +5V

At T_A = +25°C and R_L = 100Ω to V_S/2, unless otherwise noted.

BUFFER BANDWIDTH vs OUTPUT VOLTAGE

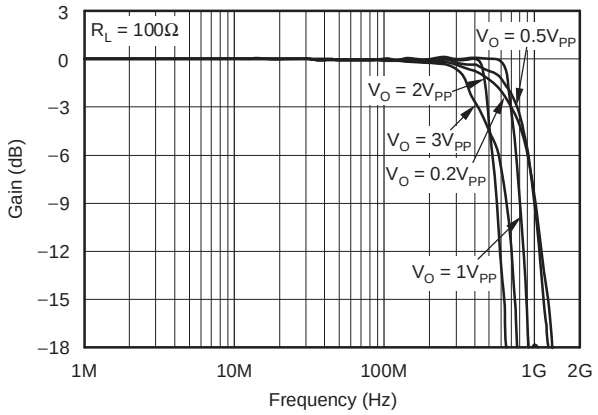


Figure 19.

HARMONIC DISTORTION vs FREQUENCY

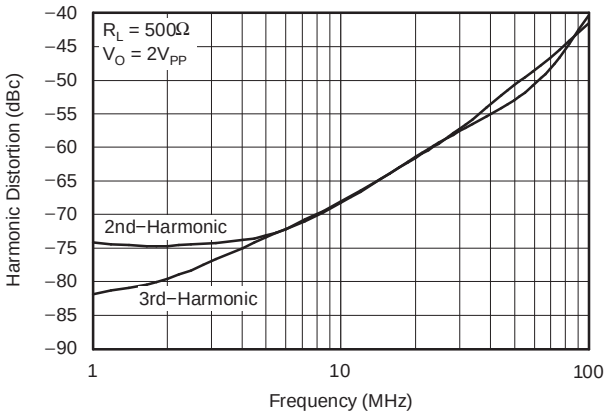


Figure 20.

BUFFER GAIN FLATNESS

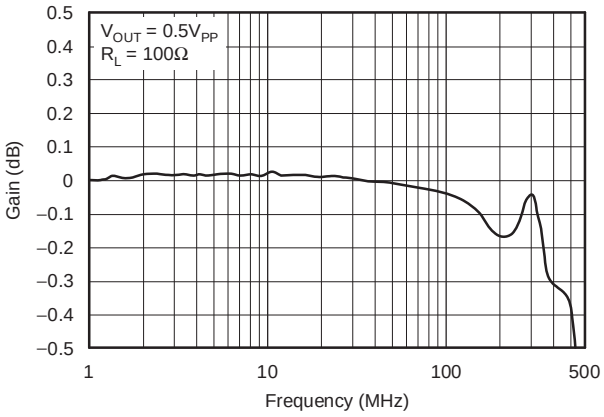


Figure 21.

5MHz HARMONIC DISTORTION vs LOAD RESISTANCE

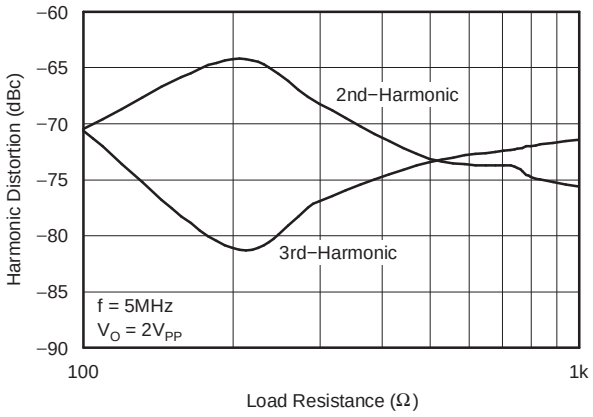


Figure 22.

BUFFER PULSE RESPONSE

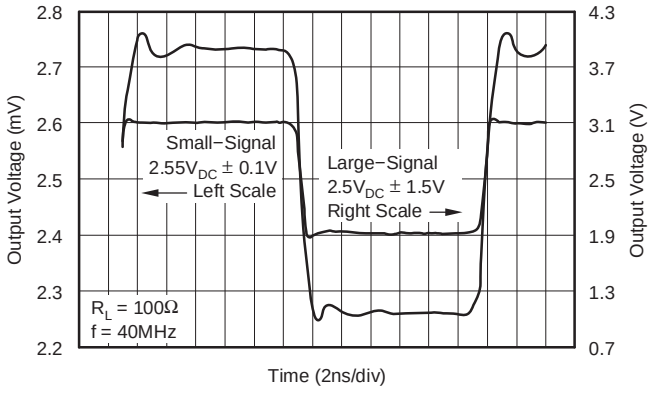


Figure 23.

HARMONIC DISTORTION vs OUTPUT VOLTAGE

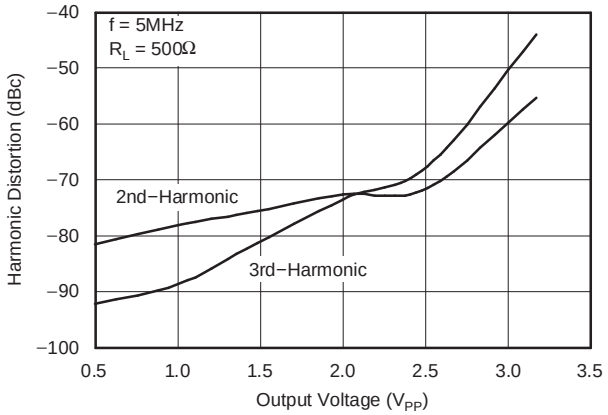


Figure 24.

TYPICAL CHARACTERISTICS: V_S = +3.3V

At T_A = +25°C and R_L = 100Ω to V_S/2, unless otherwise noted.

BUFFER BANDWIDTH vs OUTPUT VOLTAGE

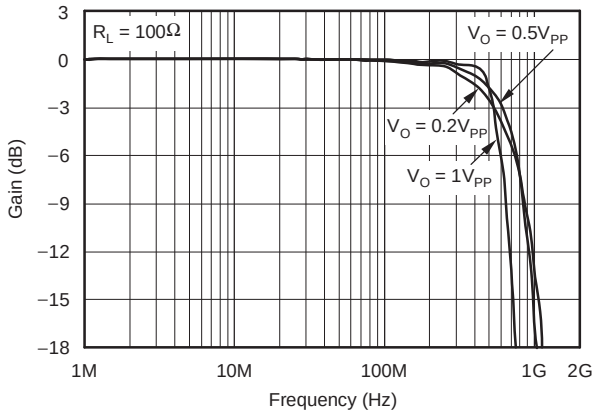


Figure 25.

HARMONIC DISTORTION vs FREQUENCY

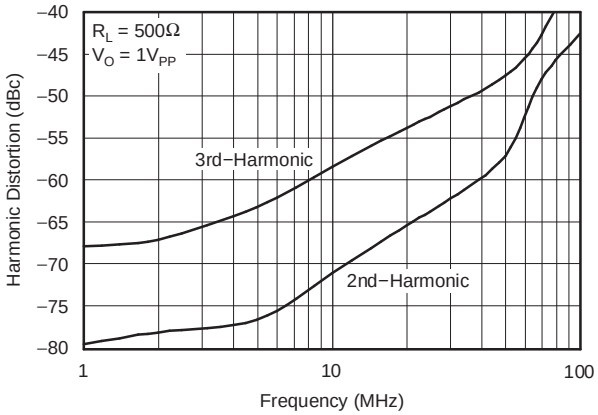


Figure 26.

BUFFER GAIN FLATNESS

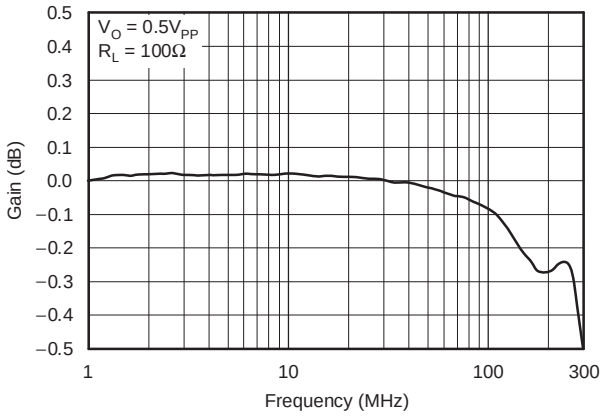


Figure 27.

5MHz HARMONIC DISTORTION vs LOAD RESISTANCE

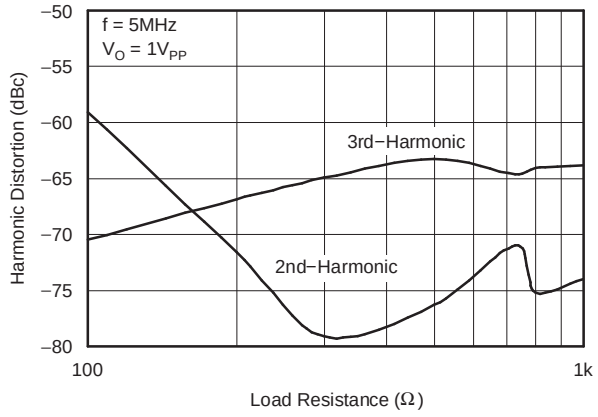


Figure 28.

BUFFER PULSE RESPONSE

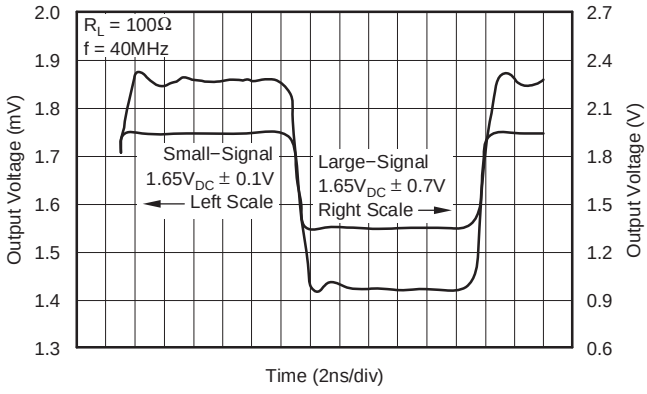


Figure 29.

HARMONIC DISTORTION vs OUTPUT VOLTAGE

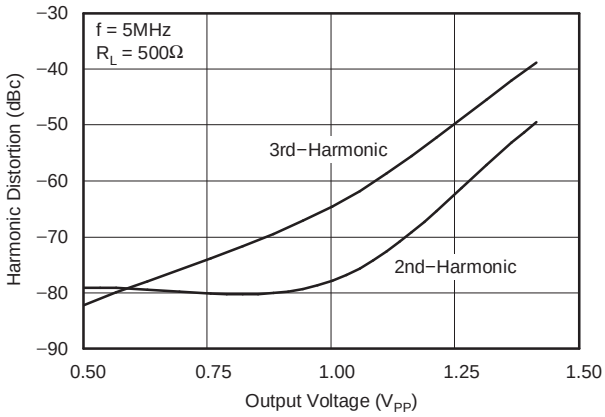


Figure 30.

APPLICATION INFORMATION

WIDEBAND BUFFER OPERATION

The BUF602 gives the exceptional AC performance of a wideband buffer. Requiring only 5.8mA quiescent current, the BUF602 will swing to within 1V of either supply rail and deliver in excess of 60mA at room temperature. This low output headroom requirement, along with supply voltage independent biasing, gives remarkable single (+5V) supply operation. The BUF602 will deliver greater than 500MHz bandwidth driving a $2V_{PP}$ output into 100Ω on a single +5V supply.

Figure 31 shows the DC-coupled, dual power-supply circuit configuration used as the basis of the ±5V Electrical and Typical Characteristics. For test purposes, the input impedance is set to 50Ω with a resistor to ground and the output impedance is set to 50Ω with a series output resistor. Voltage swings reported in the specifications are taken directly at the input and output pins while load powers (dBm) are defined at a matched 50Ω load. In addition to the usual power-supply decoupling capacitors to ground, a 0.01µF capacitor can be included between the two power-supply pins. This optional added capacitor will typically improve the 2nd-harmonic distortion performance by 3dB to 6dB.

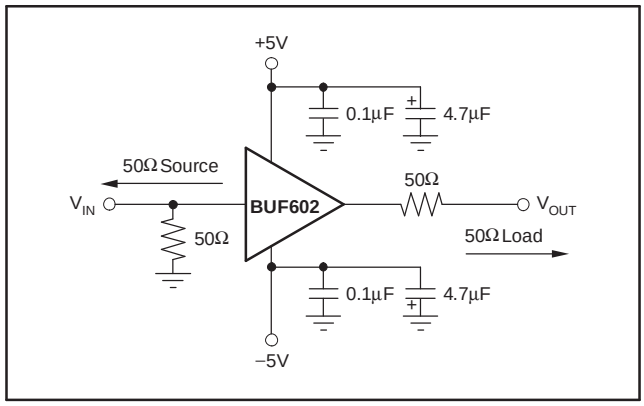


Figure 31. DC-Coupled, Bipolar Supply, Specification and Test Circuit

Figure 32 shows the AC-coupled, single-supply circuit configuration used as the basis of the +5V Electrical and Typical Characteristics. Though not a *rail-to-rail* design, the BUF602 requires minimal input and output voltage headroom compared to other very wideband buffers. It will deliver a $3V_{PP}$ output swing on a single +5V supply with greater than 400MHz bandwidth. The key requirement of broadband single-supply operation of the BUF602 is to maintain output signal swings within the usable voltage ranges. The circuit of Figure 32 establishes an input midpoint bias using the internal midpoint reference. The input signal is then AC-coupled into this midpoint voltage bias. Again, on a single +5V supply, the output voltage can swing to within 1V of either supply pin while delivering more than 60mA output current. A demanding 100Ω load to a midpoint bias is used in this characterization circuit.

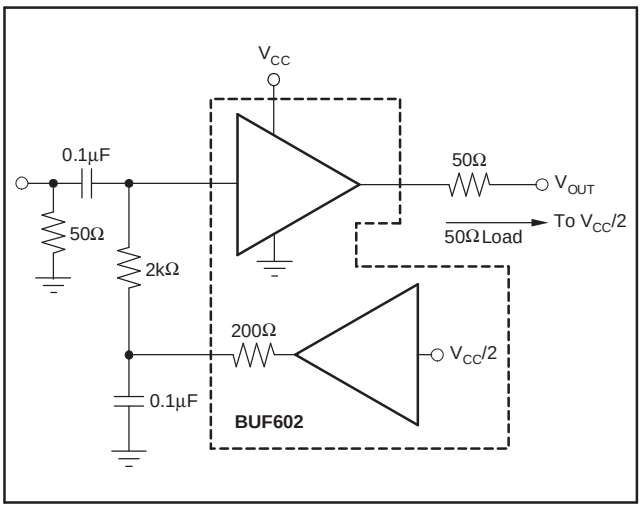


Figure 32. AC-Coupled, Single-Supply, Specification and Test Circuit

LOW-IMPEDANCE TRANSMISSION LINES

The most important equations and technical basics of transmission lines support the results found for the various drive circuits presented here. An ideal transmission medium with zero ohmic impedance would have inductance and capacitance distributed over the transmission cable. Both inductance and capacitance detract from the transmission quality of a line. Each input is connected with high-impedance to the line as in a daisy-chain or loop-through configuration, and each adds capacitance of at least a few picofarads. The typical transmission line impedance (Z_O) defines the line type. In Equation 1, the impedance is calculated by the square root of line inductance (L_T) divided by line capacitance (C_T):

$$Z_O = \sqrt{\frac{L_T}{C_T}} \quad (1)$$

In the same manner, line inductance and capacitance determine the delay time of a transmission line as shown in Equation 2:

$$\tau = \sqrt{L_T \times C_T} \quad (2)$$

Typical values for Z_O are 240Ω for symmetrical traces and 75Ω or 50Ω for coaxial cables. Z_O sometimes decreases to 30Ω to 40Ω in high data rate bus systems for bus lines on printed circuit boards (PCBs). In general, the more complex a bus system is, the lower Z_O will be. Because it increases the capacitance of the transmission medium, a complex system lowers the typical line impedance, resulting in higher drive requirements for the line drivers used here.

Transmission lines are almost always terminated on the transmitter line and always terminated on the receiver side. Unterminated lines generate signal reflections that degrade the pulse fidelity. The driver circuit transmits the output voltage (V_{OUT}) over the line. The signal appears at the end of the line and will be reflected when not properly terminated. The reflected portion of V_{OUT}, called V_{REFL}, returns to the driver. The transmitted signal is the sum of the original signal V_{OUT} and the reflected V_{REFL}.

$$V_T = V_{OUT} + V_{REFL} \quad (3)$$

The magnitude of the reflected signal depends upon the typical line impedance (Z_O) and the value of the termination resistor Z_1.

$$V_{REFL} = V_{OUT} \times \Gamma \quad (4)$$

Γ denotes the reflection factor and is described by Equation 5.

$$\Gamma = \sqrt{\frac{Z_1 - Z_O}{Z_1 + Z_O}} \quad (5)$$

Γ can vary from –1 to +1.

The conditions at the corner points of Equation 5 are as follows:

$Z_O = Z_1$	→	Γ = 0	$V_{REFL} = 0$
$Z_O = \infty$	→	Γ = –1	$V_{REFL} = -V_{OUT}$
$Z_O = 0$	→	Γ = +1	$V_{REFL} = +V_{OUT}$

An unterminated driver circuit complicates the situation even more. V_{REFL} is reflected a second time on the driver side and wanders like a ping-pong ball back and forth over the line. When this happens, it is usually impossible to recover the output signal V_{OUT} on the receiver side.

The figure shown in Figure 33 makes use of the BUF602 as a line driver. The BUF602 exhibits high input impedance and low output impedance, making it ideal whenever a buffer is required.

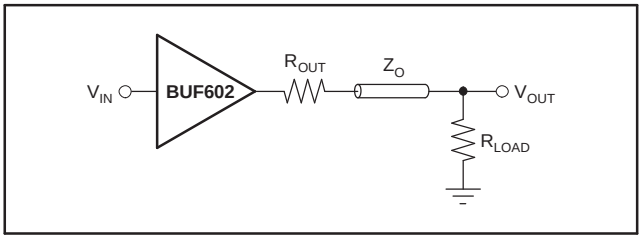


Figure 33. Typical Line Driver Circuit

SELF-BIASED, LOW-IMPEDANCE MID-SUPPLY VOLTAGE REFERENCE

Using the midpoint reference in conjunction with the BUF602 allows the creation of a low-impedance reference from DC to 250MHz.

The 0.1µF external capacitor is used in Figure 34 to filter the noise.

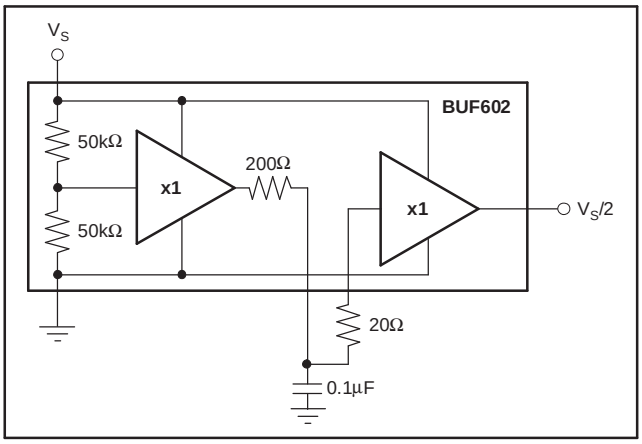


Figure 34. Self-Biased, Low Impedance Mid-Supply Voltage Reference

SELF-REFERENCED, AC-COUPLED WIDEBAND BUFFER

Whenever a high-speed AC-coupled buffer is required, you should consider the BUF602. One feature of the BUF602 is the mid-supply reference voltage, saving external components and power dissipation. A capacitor on the output of the mid-supply reference is recommended to bandlimit the noise contribution of the mid-supply reference voltage generated by the two 50kΩ internal resistors. This circuit is shown on the front page of the datasheet.

DESIGN-IN TOOLS

DEMONSTRATION FIXTURES

Two printed circuit boards (PCBs) are available to assist in the initial evaluation of circuit performance using the BUF602 in its two package options. Both of these are offered free of charge as unpopulated PCBs, delivered with a user's guide. The summary information for these fixtures is shown in Table 1.

Table 1. Demonstration Fixtures by Package

PRODUCT	PACKAGE	BOARD PART NUMBER	LITERATURE REQUEST NUMBER
BUF602ID	SO-8	DEM-BUF-SO-1A	SBAU118
BUF602IDBV	SOT23-5	DEM-BUF-SOT-1A	SBAU117

The demonstration fixtures can be requested at the Texas Instruments web site (www.ti.com) through the BUF602 product folder.

MACROMODELS AND APPLICATIONS SUPPORT

Computer simulation of circuit performance using SPICE is often useful when analyzing the performance of analog circuits and systems. This is particularly true for video and RF amplifier circuits where parasitic capacitance and inductance can have a major effect on circuit performance. A SPICE model for the BUF602 is available through the TI web site (www.ti.com). These models do a good job of predicting small-signal AC and transient performance under a wide variety of operating conditions. They do not do as well in predicting the harmonic distortion or dG/dP characteristics. These models do not attempt to distinguish between package types in their small-signal AC performance.

OUTPUT CURRENT AND VOLTAGE

The BUF602 provides output voltage and current capabilities that are not usually found in wideband buffers. Under no-load conditions at +25°C, the output voltage typically swings closer than 1.2V to either supply rail; the +25°C swing limit is within 1.2V of either rail. Into a 15Ω load (the minimum tested load), it is tested to deliver more than ±60mA.

The specifications described above, though familiar in the industry, consider voltage and current limits separately. In many applications, it is the *voltage* × *current*, or V-I product, which is more relevant to circuit operation. Refer to the *Buffer Output Voltage and Current Limitations* plot (Figure 16) in the Typical Characteristics. The X and Y axes of this graph show the zero-voltage output current limit and the zero-current output voltage limit, respectively. The four quadrants give a more detailed view of the BUF602 output drive capabilities, noting that the graph is bounded by a *Safe Operating Area* of 1W maximum internal power dissipation. Superimposing resistor load lines onto the plot shows that the BUF602 can drive ±3V into 25Ω or ±3.5V into 50Ω without exceeding the output capabilities or the 1W dissipation limit.

The minimum specified output voltage and current over-temperature are set by worst-case simulations at the cold temperature extreme. Only at cold startup will the output current and voltage decrease to the numbers shown in the Electrical Characteristic tables. As the output transistors deliver power, the junction temperatures will increase, decreasing both V_{BE} (increasing the available output voltage swing) and increasing the current gains (increasing the available output current). In steady-state operation, the available output voltage and current will always be greater than that shown in the over-temperature specifications, since the output stage junction temperatures will be higher than the minimum specified operating ambient.

For a buffer, the noise model is shown in Figure 35. Equation 6 shows the general form for the output noise voltage using the terms shown in Figure 35.

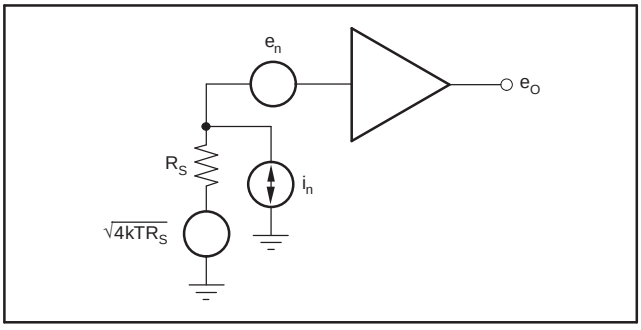


Figure 35. Buffer Noise Analysis Model

$$e_O = \sqrt{e_n^2 + (i_n R_S)^2 + 4kTR_S} \quad \frac{nV}{\sqrt{Hz}} \tag{6}$$

THERMAL ANALYSIS

Due to the high output power capability of the BUF602, heatsinking or forced airflow may be required under extreme operating conditions. Maximum desired junction temperature will set the maximum allowed internal power dissipation as described below. In no case should the maximum junction temperature be allowed to exceed 150°C.

Operating junction temperature (T_J) is given by $T_A + P_D \times \theta_{JA}$. The total internal power dissipation (P_D) is the sum of quiescent power (P_{DQ}) and additional power dissipated in the output stage (P_{DL}) to deliver load power. Quiescent power is simply the specified no-load supply current times the total supply voltage

across the part. P_{DL} will depend on the required output signal and load but would, for a grounded resistive load, be at a maximum when the output is fixed at a voltage equal to 1/2 of either supply voltage (for equal bipolar supplies). Under this condition, $P_{DL} = V_S^2/(4 \times R_L)$.

Note that it is the power in the output stage and not into the load that determines internal power dissipation.

As a worst-case example, compute the maximum T_J using a BUF602IDBV in the circuit on the front page operating at the maximum specified ambient temperature of +85°C and driving a grounded 20Ω load.

$P_D = 10V \times 5.8mA + 5^2/(4 \times 20\Omega) = 370.5mW$

Maximum $T_J = +85°C + (0.37W \times 150°C/W) = 141°C$.

Although this is still below the specified maximum junction temperature, system reliability considerations may require lower tested junction temperatures. The highest possible internal dissipation will occur if the load requires current to be forced into the output for positive output voltages or sourced from the output for negative output voltages. This puts a high current through a large internal voltage drop in the output transistors. The output V-I plot (Figure 16) shown in the Typical Characteristics include a boundary for 1W maximum internal power dissipation under these conditions.

BOARD LAYOUT GUIDELINES

Achieving optimum performance with a high-frequency amplifier like the BUF602 requires careful attention to board layout parasitics and external component types. Recommendations that will optimize performance include:

a) Minimize parasitic capacitance to any AC ground for all of the signal I/O pins. Parasitic capacitance on the output pins can cause instability: on the noninverting input, it can react with the source impedance to cause unintentional bandlimiting. To reduce unwanted capacitance, a window around the signal I/O pins should be opened in all of the ground and power planes around those pins. Otherwise, ground and power planes should be unbroken elsewhere on the board.

b) Minimize the distance (< 0.25") from the power-supply pins to high-frequency 0.1µF decoupling capacitors. At the device pins, the ground and power-plane layout should not be in close proximity to the signal I/O pins. Avoid narrow power and ground traces to minimize inductance between the pins and the decoupling capacitors. The power-supply connections should always be decoupled with these capacitors. An optional supply decoupling capacitor (0.1µF) across the two power supplies (for bipolar operation) will improve 2nd-harmonic distortion performance. Larger (2.2µF to 6.8µF) decoupling capacitors, effective at lower frequency, should also be used on the main supply pins. These may be placed somewhat farther from the device and may be shared among several devices in the same area of the PCB.

c) Careful selection and placement of external components will preserve the high-frequency performance of the BUF602. Resistors should be a very low reactance type. Surface-mount resistors work best and allow a tighter overall layout. Metal film or carbon composition, axially-leaded resistors can also provide good high-frequency performance. Again, keep their leads and PCB traces as short as possible. Never use wirewound type resistors in a high-frequency application.

d) Connections to other wideband devices on the board may be made with short, direct traces or through onboard transmission lines. For short connections, consider the trace and the input to the next device as a lumped capacitive load. Relatively wide traces (50mils to 100mils) should be used, preferably with ground and power planes opened up around them. If a long trace is required, and the 6dB signal loss intrinsic to a doubly-terminated transmission line is acceptable, implement a matched impedance transmission line using microstrip or stripline techniques (consult an ECL design handbook for microstrip and stripline layout techniques). A 50Ω environment is normally not necessary on board, and in fact, a higher impedance environment will improve distortion as shown in the distortion versus load plots.

e) Socketing a high-speed part like the BUF602 is not recommended. The additional lead length and pin-to-pin capacitance introduced by the socket can create an extremely troublesome parasitic network that makes it almost impossible to achieve a smooth, stable frequency response. Best results are obtained by soldering the BUF602 onto the board.

INPUT AND ESD PROTECTION

The BUF602 is built using a very high-speed complementary bipolar process. The internal junction breakdown voltages are relatively low for these very small geometry devices. These breakdowns are reflected in the *Absolute Maximum Ratings* table. All device pins are protected with internal ESD protection diodes to the power supplies as shown in Figure 36.

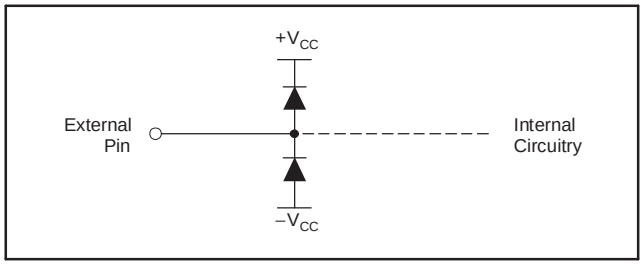


Figure 36. Internal ESD Protection

These diodes provide moderate protection to input overdrive voltages above the supplies as well. The protection diodes can typically support 30mA continuous current. Where higher currents are possible (for example, in systems with ±15V supply parts driving into the BUF602), current-limiting series resistors should be added into the two inputs. Keep these resistor values as low as possible since high values degrade both noise performance and frequency response.

Revision History

Changes from Revision A (August 2006) to Revision B **Page**

- Changed storage temperature range rating in *Absolute Maximum Ratings* table from –40°C to +125°C to –65°C to +125°C 2

Changes from Original (October 2005) to Revision A **Page**

- Added Figure 17. 10
- Added Figure 18. 10
- Changed Demonstration Fixtures title and text. 15

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
BUF602ID	ACTIVE	SOIC	D	8	75	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-45 to 85	BUF 602	Samples
BUF602IDBVR	ACTIVE	SOT-23	DBV	5	3000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-45 to 85	AWO	Samples
BUF602IDBVT	ACTIVE	SOT-23	DBV	5	250	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-45 to 85	AWO	Samples
BUF602IDBVTG4	ACTIVE	SOT-23	DBV	5	250	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-45 to 85	AWO	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals.
TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

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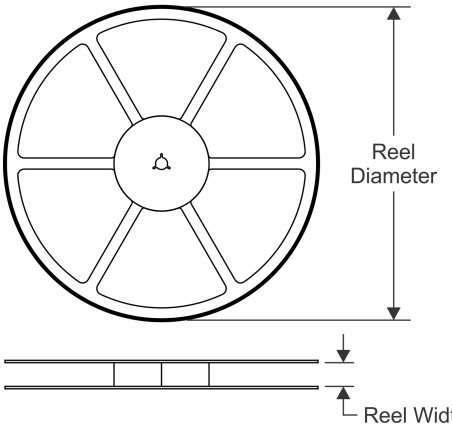
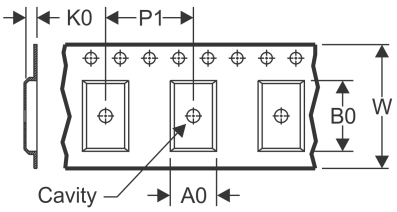
TAPE AND REEL INFORMATION

REEL DIMENSIONS

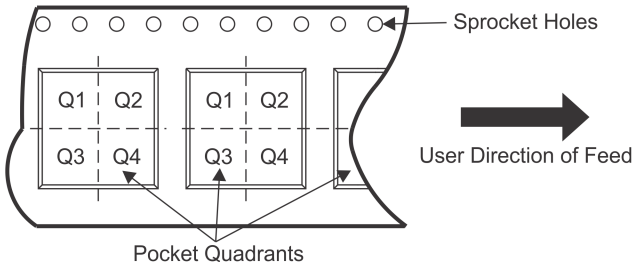


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

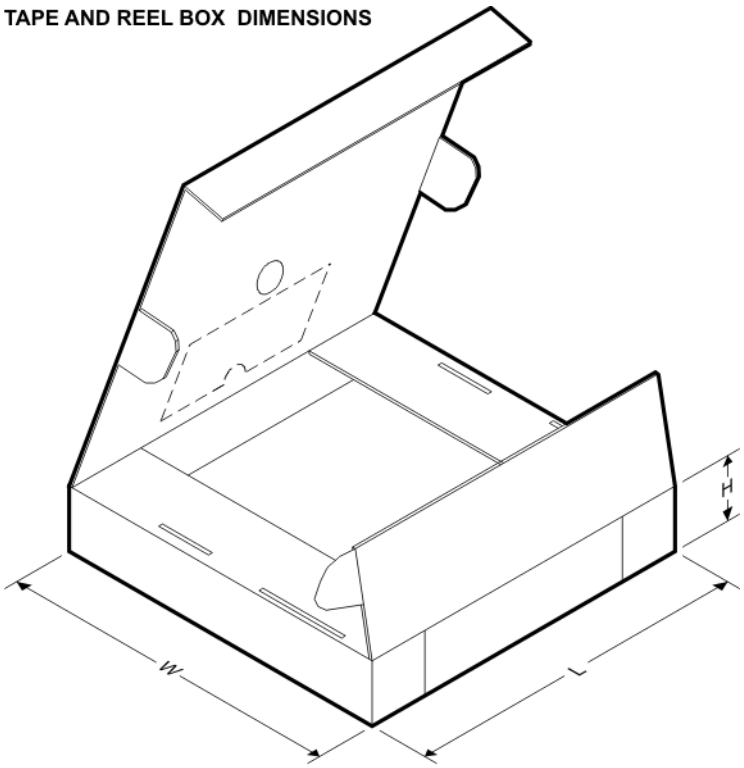
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
BUF602IDBVR	SOT-23	DBV	5	3000	178.0	9.0	3.3	3.2	1.4	4.0	8.0	Q3
BUF602IDBVT	SOT-23	DBV	5	250	178.0	9.0	3.3	3.2	1.4	4.0	8.0	Q3

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

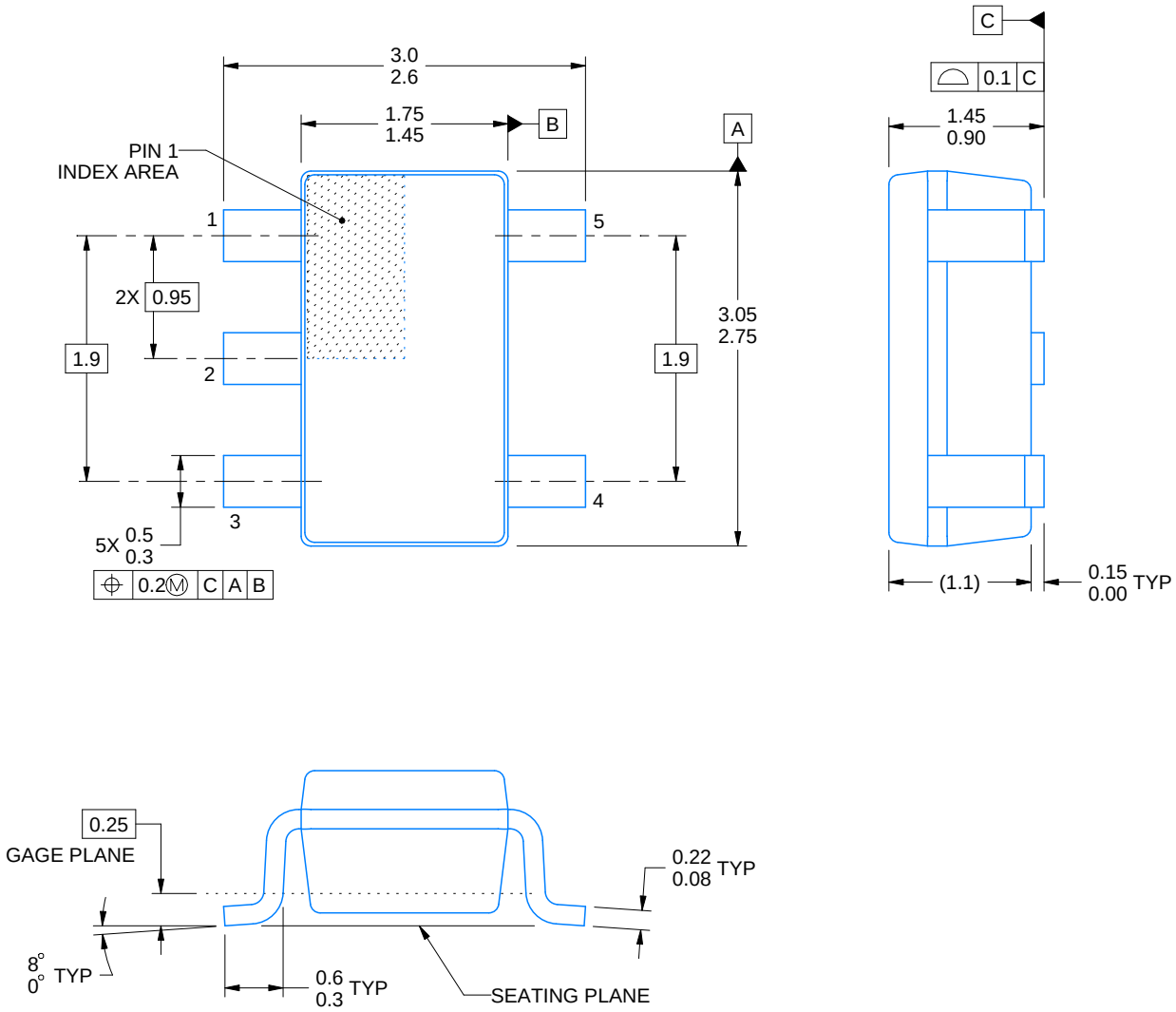
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
BUF602IDBVR	SOT-23	DBV	5	3000	565.0	140.0	75.0
BUF602IDBVT	SOT-23	DBV	5	250	565.0	140.0	75.0

PACKAGE OUTLINE

DBV0005A

SOT-23 - 1.45 mm max height

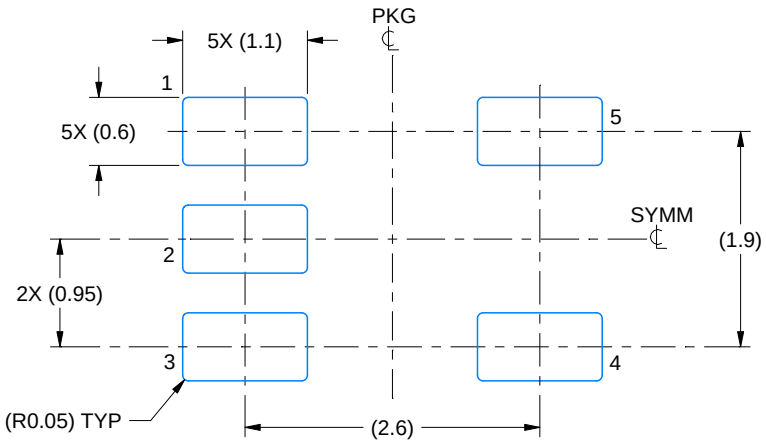
SMALL OUTLINE TRANSISTOR



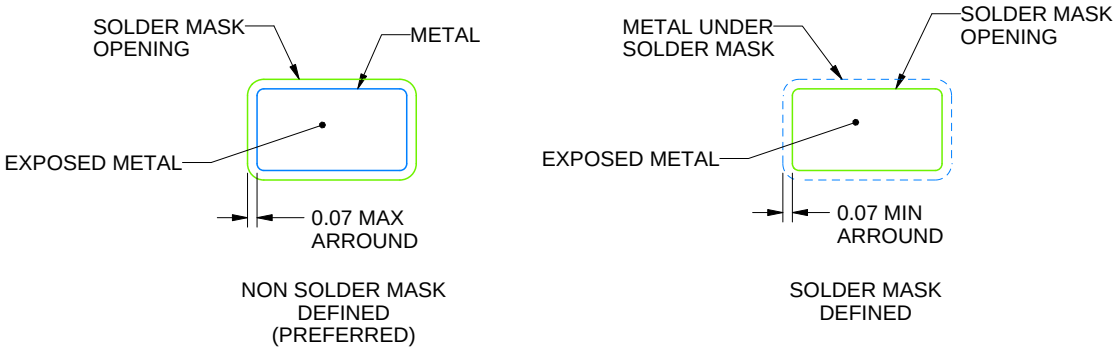
4214839/E 09/2019

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Refernce JEDEC MO-178.
4. Body dimensions do not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:15X

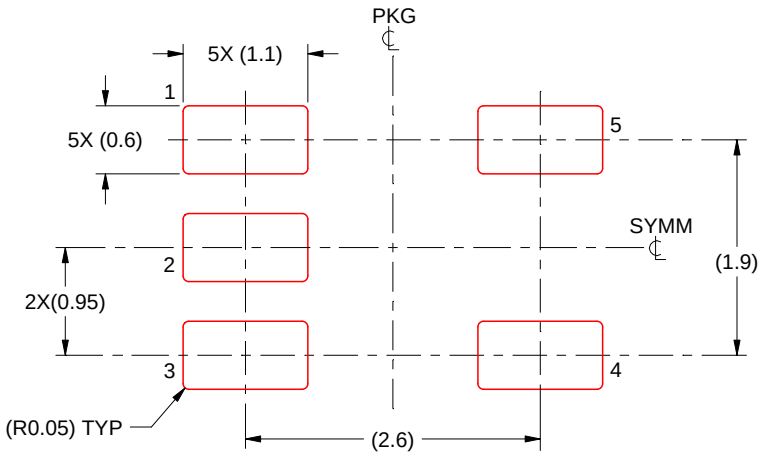


SOLDER MASK DETAILS

4214839/E 09/2019

NOTES: (continued)

5. Publication IPC-7351 may have alternate designs.
6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:15X

4214839/E 09/2019

NOTES: (continued)

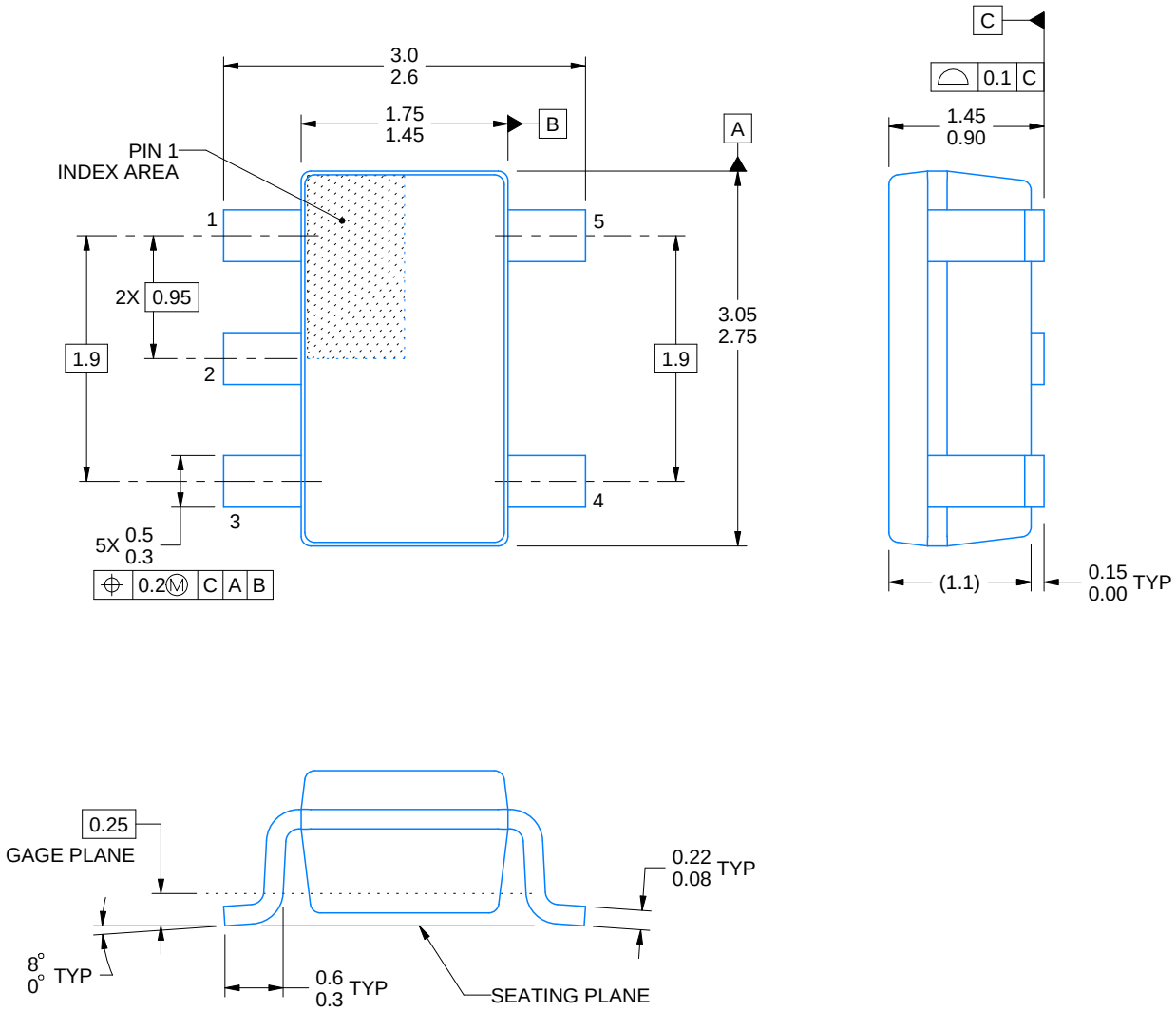
7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
8. Board assembly site may have different recommendations for stencil design.

PACKAGE OUTLINE

DBV0005A

SOT-23 - 1.45 mm max height

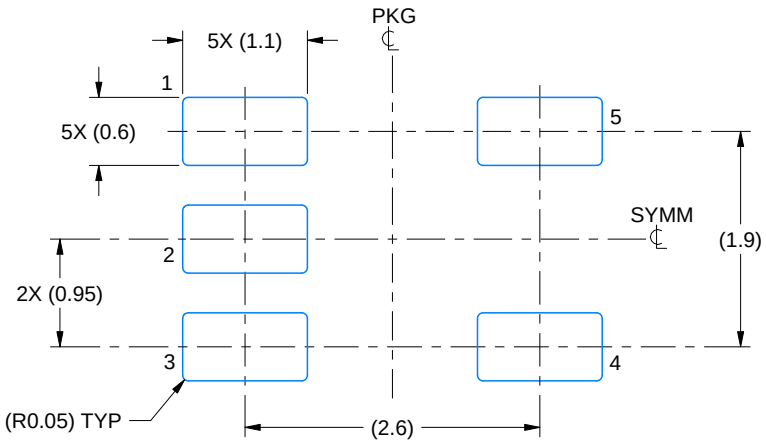
SMALL OUTLINE TRANSISTOR



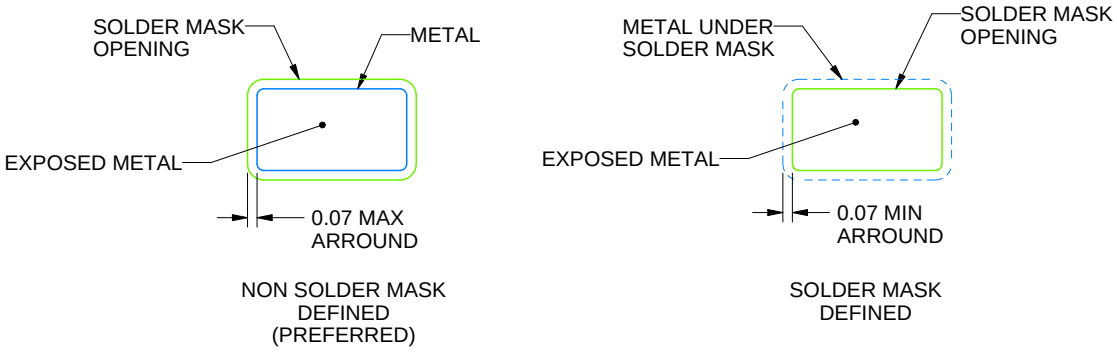
4214839/F 06/2021

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Refernce JEDEC MO-178.
4. Body dimensions do not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.25 mm per side.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:15X

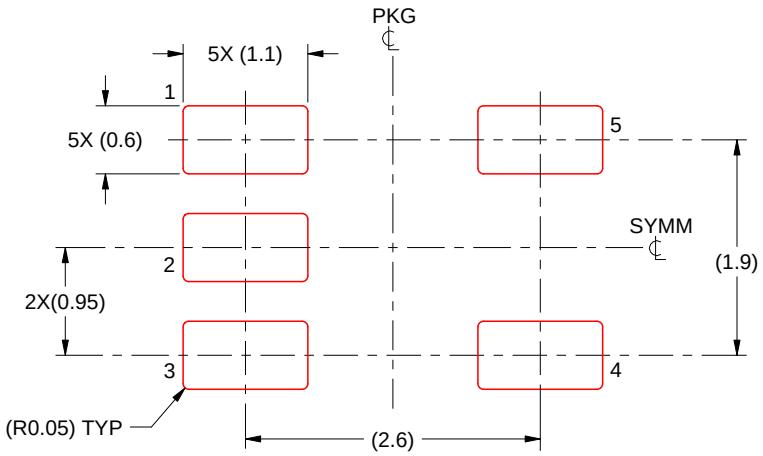


SOLDER MASK DETAILS

4214839/F 06/2021

NOTES: (continued)

5. Publication IPC-7351 may have alternate designs.
6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

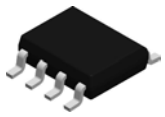


SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:15X

4214839/F 06/2021

NOTES: (continued)

7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
8. Board assembly site may have different recommendations for stencil design.

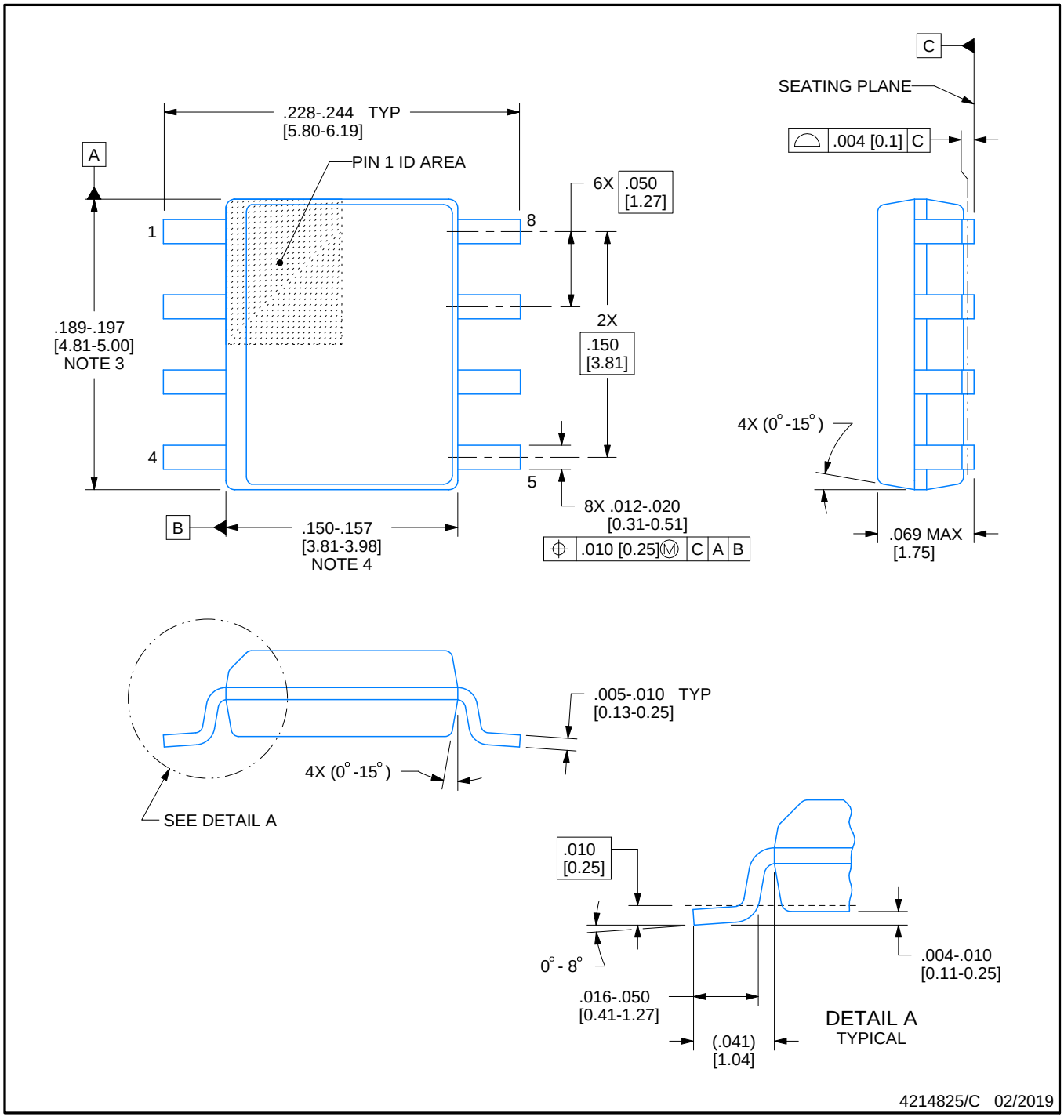


PACKAGE OUTLINE

D0008A

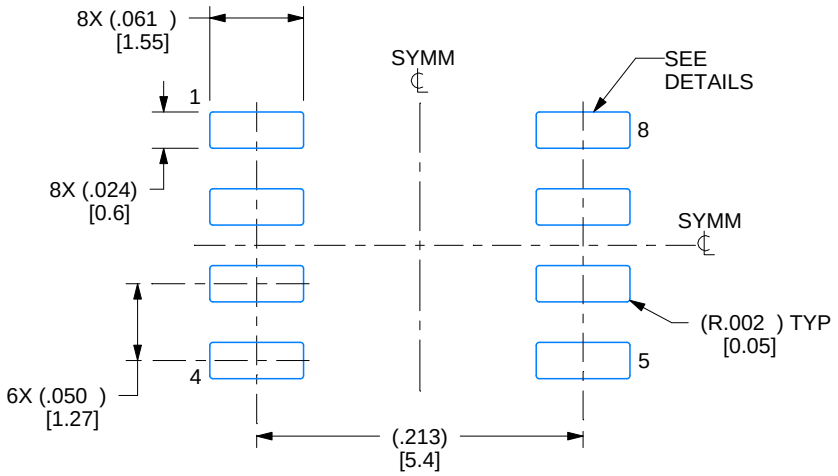
SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT

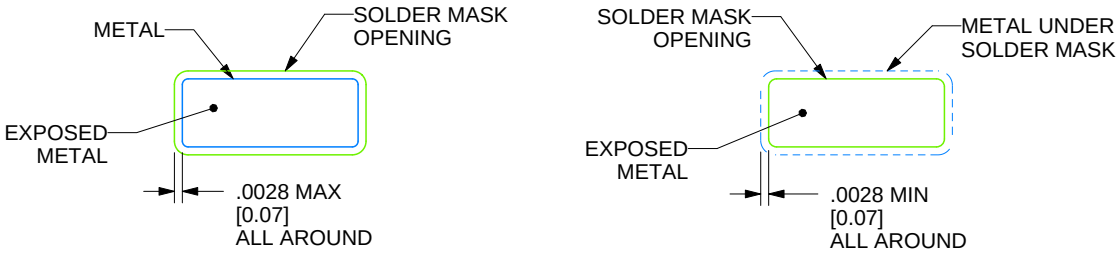


NOTES:

1. Linear dimensions are in inches [millimeters]. Dimensions in parenthesis are for reference only. Controlling dimensions are in inches. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 [0.15] per side.
4. This dimension does not include interlead flash.
5. Reference JEDEC registration MS-012, variation AA.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:8X



SOLDER MASK DETAILS

4214825/C 02/2019

NOTES: (continued)

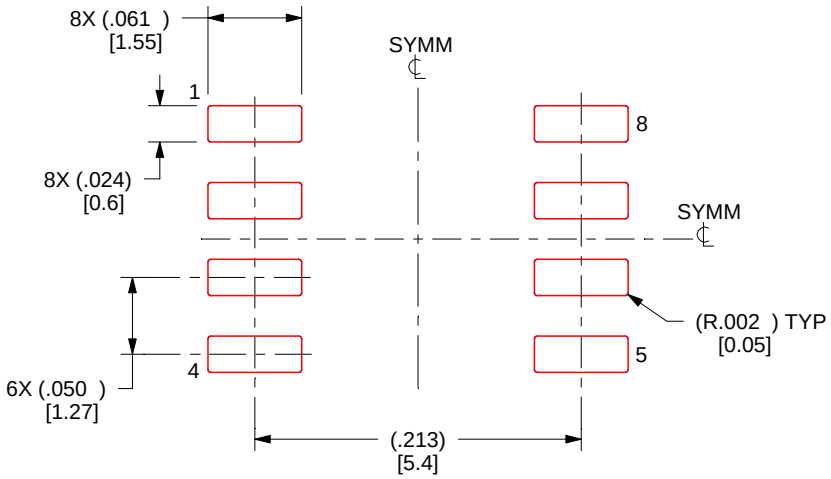
6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

D0008A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



SOLDER PASTE EXAMPLE
BASED ON .005 INCH [0.125 MM] THICK STENCIL
SCALE:8X

4214825/C 02/2019

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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