

## CMOS 14-Stage Ripple-Carry Binary Counter/Divider and Oscillator

### High-Voltage Types (20-Volt Rating)

■ CD4060B consists of an oscillator section and 14 ripple-carry binary counter stages. The oscillator configuration allows design of either RC or crystal oscillator circuits. A RESET input is provided which resets the counter to the all-O's state and disables the oscillator. A high level on the RESET line accomplishes the reset function. All counter stages are master-slave flip-flops. The state of the counter is advanced one step in binary order on the negative transition of  $\phi_1$  (and  $\phi_0$ ). All inputs and outputs are fully buffered. Schmitt trigger action on the input-pulse line permits unlimited input-pulse rise and fall times.

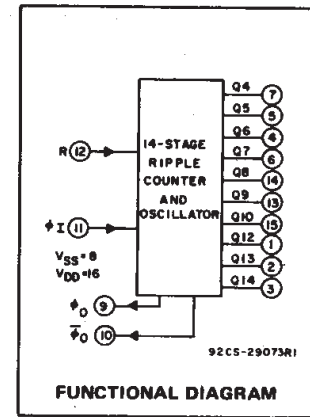
The CD4060B-series types are supplied in 16-lead hermetic dual-in-line ceramic packages (F3A suffix), 16-lead dual-in-line plastic packages (E suffix), 16-lead small-outline packages (M, M96, MT, and NSR suffixes), and 16-lead thin shrink small-outline packages (PW and PWR suffixes).

### Features:

- 12 MHz clock rate at 15 V
- Common reset
- Fully static operation
- Buffered inputs and outputs
- Schmitt trigger input-pulse line
- 100% tested for quiescent current at 20 V
- Standardized, symmetrical output characteristics
- 5-V, 10-V, and 15-V parametric ratings
- Meets all requirements of JEDEC Tentative Standard No. 13B, "Standard Specifications for description of "B" Series CMOS Devices"

### Oscillator Features:

- All active components on chip
- RC or crystal oscillator configuration
- RC oscillator frequency of 690 kHz min. at 15 V



### Applications

- Control counters
- Timers
- Frequency dividers
- Time-delay circuits

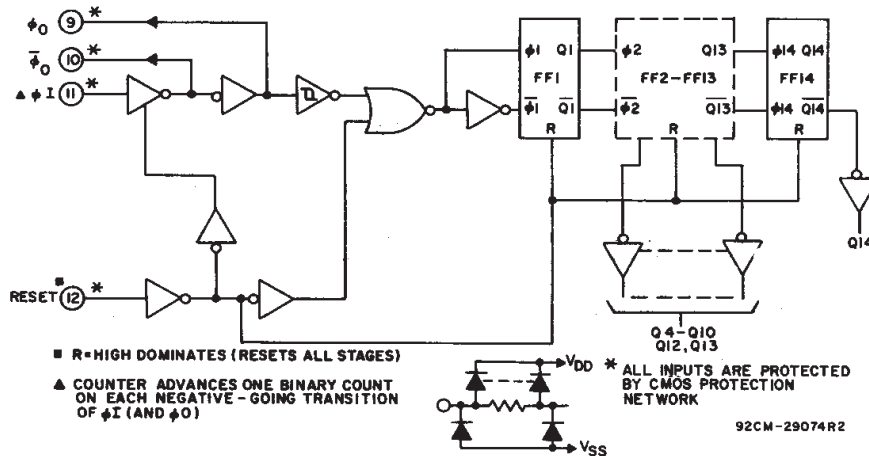


Fig. 1 - Logic diagram.



Fig. 2 - Detail of typical flip-flop stage.

### MAXIMUM RATINGS, Absolute-Maximum Values:

|   |   |
|---|---|
| DC SUPPLY-VOLTAGE RANGE, ( $V_{DD}$ )   | -0.5V to +20V                               |
| Voltages referenced to $V_{SS}$ Terminal  |   |
| INPUT VOLTAGE RANGE, ALL INPUTS   | -0.5V to $V_{DD} + 0.5V$                    |
| DC INPUT CURRENT, ANY ONE INPUT   | $\pm 10\text{mA}$                           |
| POWER DISSIPATION PER PACKAGE ( $P_D$ ):  |   |
| For $T_A = -55^\circ\text{C}$ to $+100^\circ\text{C}$                               | 500mW                                       |
| For $T_A = +100^\circ\text{C}$ to $+125^\circ\text{C}$                              | Derate Linearly at 12mW/°C to 200mW         |
| DEVICE DISSIPATION PER OUTPUT TRANSISTOR  |   |
| FOR $T_A = \text{FULL PACKAGE-TEMPERATURE RANGE}$ (All Package Types)               | 100mW                                       |
| OPERATING-TEMPERATURE RANGE ( $T_A$ )   | $-55^\circ\text{C}$ to $+125^\circ\text{C}$ |
| STORAGE TEMPERATURE RANGE ( $T_{stg}$ )   | $-65^\circ\text{C}$ to $+150^\circ\text{C}$ |
| LEAD TEMPERATURE (DURING SOLDERING):  |   |
| At distance $1/16 \pm 1/32$ inch ( $1.59 \pm 0.79\text{mm}$ ) from case for 10s max | $+265^\circ\text{C}$                        |

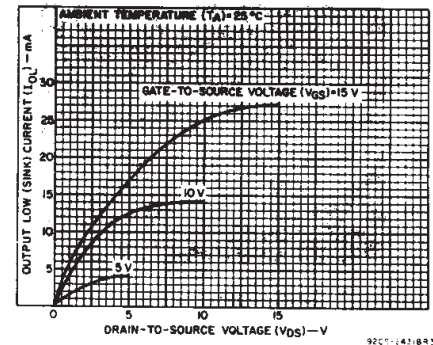


Fig. 3 - Typical n-channel output low (sink) current characteristics.

# CD4060B Types

## STATIC ELECTRICAL CHARACTERISTICS

| CHARACTERISTIC                                      | CONDITIONS         |                     |                     | LIMITS AT INDICATED TEMPERATURES (°C) |       |       |       |       |                   |      | UNITS |
|---|--------------------|---------------------|---------------------|---------------------------------------|-------|-------|-------|-------|-------------------|------|-------|
|   | V <sub>O</sub> (V) | V <sub>IN</sub> (V) | V <sub>DD</sub> (V) | -55                                   | -40   | +85   | +125  | +25   |                   |      |       |
|   |                    |                     |                     |                                       |       |       |       | Min.  | Typ.              | Max. |       |
| Quiescent Device Current, I <sub>DD</sub> Max.      | —                  | 0,5                 | 5                   | 5                                     | 5     | 150   | 150   | —     | 0,04              | 5    | μA    |
|   | —                  | 0,10                | 10                  | 10                                    | 10    | 300   | 300   | —     | 0,04              | 10   |       |
|   | —                  | 0,15                | 15                  | 20                                    | 20    | 600   | 600   | —     | 0,04              | 20   |       |
|   | —                  | 0,20                | 20                  | 100                                   | 100   | 3000  | 3000  | —     | 0,08              | 100  |       |
| Output Low (Sink) Current*, I <sub>OL</sub> Min.    | 0,4                | 0,5                 | 5                   | 0,64                                  | 0,61  | 0,42  | 0,36  | 0,51  | 1                 | —    | mA    |
|   | 0,5                | 0,10                | 10                  | 1,6                                   | 1,5   | 1,1   | 0,9   | 1,3   | 2,6               | —    |       |
|   | 1,5                | 0,15                | 15                  | 4,2                                   | 4     | 2,8   | 2,4   | 3,4   | 6,8               | —    |       |
| Output High (Source) Current*, I <sub>OH</sub> Min. | 4,6                | 0,5                 | 5                   | -0,64                                 | -0,61 | -0,42 | -0,36 | -0,51 | -1                | —    | mA    |
|   | 2,5                | 0,5                 | 5                   | -2                                    | -1,8  | -1,3  | -1,15 | -1,6  | -3,2              | —    |       |
|   | 9,5                | 0,10                | 10                  | -1,6                                  | -1,5  | -1,1  | -0,9  | -1,3  | -2,6              | —    |       |
|   | 13,5               | 0,15                | 15                  | -4,2                                  | -4    | -2,8  | -2,4  | -3,4  | -6,8              | —    |       |
| Output Voltage: Low-Level, V <sub>OL</sub> Max.     | —                  | 0,5                 | 5                   | 0,05                                  |       |       |       | —     | 0                 | 0,05 | V     |
|   | —                  | 0,10                | 10                  | 0,05                                  |       |       |       | —     | 0                 | 0,05 |       |
|   | —                  | 0,15                | 15                  | 0,05                                  |       |       |       | —     | 0                 | 0,05 |       |
| Output Voltage: High-Level, V <sub>OH</sub> Min.    | —                  | 0,5                 | 5                   | 4,95                                  |       |       |       | 4,95  | 5                 | —    | V     |
|   | —                  | 0,10                | 10                  | 9,95                                  |       |       |       | 9,95  | 10                | —    |       |
|   | —                  | 0,15                | 15                  | 14,95                                 |       |       |       | 14,95 | 15                | —    |       |
| Input Low Voltage V <sub>IL</sub> Max.              | 0,5, 4,5           | —                   | 5                   | 1,5                                   |       |       |       | —     | —                 | 1,5  | V     |
|   | 1,9                | —                   | 10                  | 3                                     |       |       |       | —     | —                 | 3    |       |
|   | 1,5, 13,5          | —                   | 15                  | 4                                     |       |       |       | —     | —                 | 4    |       |
| Input High Voltage, V <sub>IH</sub> Min.            | 0,5, 4,5           | —                   | 5                   | 3,5                                   |       |       |       | 3,5   | —                 | —    | V     |
|   | 1,9                | —                   | 10                  | 7                                     |       |       |       | 7     | —                 | —    |       |
|   | 1,5, 13,5          | —                   | 15                  | 11                                    |       |       |       | 11    | —                 | —    |       |
| Input Current I <sub>IN</sub> Max.                  | —                  | 0,18                | 18                  | ±0,1                                  | ±0,1  | ±1    | ±1    | —     | ±10 <sup>-5</sup> | ±0,1 | μA    |

\*Data not applicable to terminal 9 or 10.

## RECOMMENDED OPERATING CONDITIONS

For maximum reliability, nominal operating conditions should be selected so that operation is always within the following ranges

| CHARACTERISTIC   | V <sub>DD</sub> | LIMITS    |      | UNITS |
|--|-----------------|-----------|------|-------|
|  |                 | MIN.      | MAX. |       |
| Supply-Voltage Range (For T <sub>A</sub> = Full Package Temperature Range) | —               | 3         | 18   | V     |
| Input-Pulse Width, t <sub>W</sub> (f = 100 kHz)                            | 5               | 100       | —    | ns    |
|  | 10              | 40        | —    |       |
|  | 15              | 30        | —    |       |
| Input-Pulse Rise Time and Fall Time, t <sub>rφ</sub> , t <sub>fφ</sub>     | 5               | Unlimited |      |       |
|  | 10              | Unlimited |      |       |
|  | 15              | Unlimited |      |       |
| Input-Pulse Frequency, f <sub>φI</sub> (External pulse source)             | 5               | —         | 3,5  | MHz   |
|  | 10              | —         | 8    |       |
|  | 15              | —         | 12   |       |
| Reset Pulse Width, t <sub>W</sub>  | 5               | 120       | —    | ns    |
|  | 10              | 60        | —    |       |
|  | 15              | 40        | —    |       |

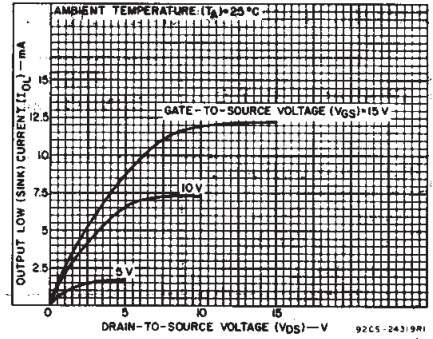


Fig. 4 – Minimum n-channel output low (sink) current characteristics.

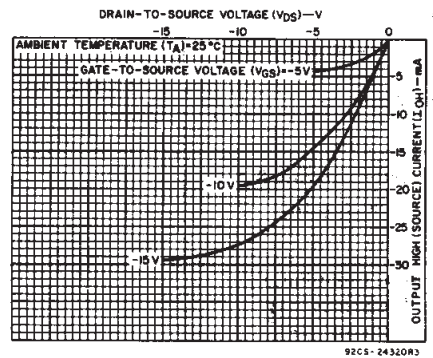


Fig. 5 – Typical p-channel output high (source) current characteristics.

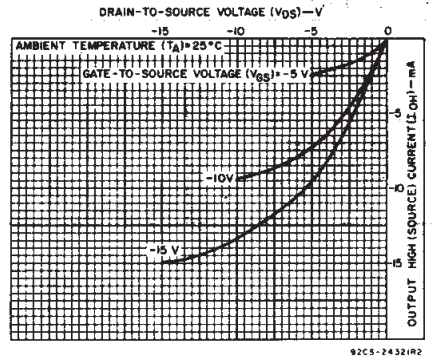


Fig. 6 – Minimum p-channel output high (source) current characteristics.

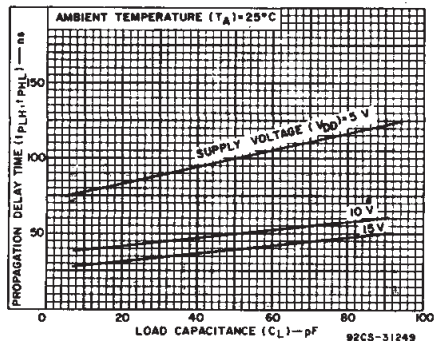


Fig. 7 – Typical propagation delay time (Q<sub>n</sub> to Q<sub>n+1</sub>) as a function of load capacitance.

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# CD4060B Types

DYNAMIC ELECTRICAL CHARACTERISTICS at  $T_A = 25^\circ\text{C}$ , Input  $t_r, t_f = 20\text{ ns}$ ,  
 $C_L = 50\text{ pF}$ ,  $R_L = 200\text{ k}\Omega$

| CHARACTERISTIC   | TEST CONDITIONS      | LIMITS              |           |      | UNITS |      |
|--|----------------------|---------------------|-----------|------|-------|------|
|  |                      | V <sub>DD</sub> (V) | MIN.      | TYP. |       | MAX. |
| <b>Input-Pulse Operation</b>                                     |                      |                     |           |      |       |      |
| Propagation Delay Time, $\phi_I$ to Q4 Out; $t_{PHL}, t_{PLH}$   |                      | 5                   | —         | 370  | 740   | ns   |
|  |                      | 10                  | —         | 150  | 300   |      |
|  |                      | 15                  | —         | 100  | 200   |      |
| Propagation Delay Time, $Q_n$ to $Q_{n+1}$ ; $t_{PHL}, t_{PLH}$  |                      | 5                   | —         | 100  | 200   | ns   |
|  |                      | 10                  | —         | 50   | 100   |      |
|  |                      | 15                  | —         | 40   | 80    |      |
| Transition Time, $t_{THL}, t_{TLH}$                              |                      | 5                   | —         | 100  | 200   | ns   |
|  |                      | 10                  | —         | 50   | 100   |      |
|  |                      | 15                  | —         | 40   | 80    |      |
| Min. Input-Pulse Width, $t_W$                                    | $f = 100\text{ kHz}$ | 5                   | —         | 50   | 100   | ns   |
|  |                      | 10                  | —         | 20   | 40    |      |
|  |                      | 15                  | —         | 15   | 30    |      |
| Input-Pulse Rise & Fall Time, $t_{r\phi}, t_{f\phi}$             |                      | 5                   | Unlimited |      |       |      |
|  |                      | 10                  |           |      |       |      |
|  |                      | 15                  |           |      |       |      |
| Max. Input-Pulse Frequency, $f_{\phi I}$ (External pulse source) |                      | 5                   | 3.5       | 7    | —     | MHz  |
|  |                      | 10                  | 8         | 16   | —     |      |
|  |                      | 15                  | 12        | 24   | —     |      |
| Input Capacitance, $C_I$   | Any Input            |                     | —         | 5    | 7.5   | pF   |
| <b>Reset Operation</b>   |                      |                     |           |      |       |      |
| Propagation Delay Time, $t_{PHL}$                                |                      | 5                   | —         | 180  | 360   | ns   |
|  |                      | 10                  | —         | 80   | 160   |      |
|  |                      | 15                  | —         | 50   | 100   |      |
| Minimum Reset Pulse Width, $t_W$                                 |                      | 5                   | —         | 60   | 120   | ns   |
|  |                      | 10                  | —         | 30   | 60    |      |
|  |                      | 15                  | —         | 20   | 40    |      |



Fig. 8 - Typical propagation delay time ( $\phi_I$  to  $Q_4$  Output) as a function of load capacitance.

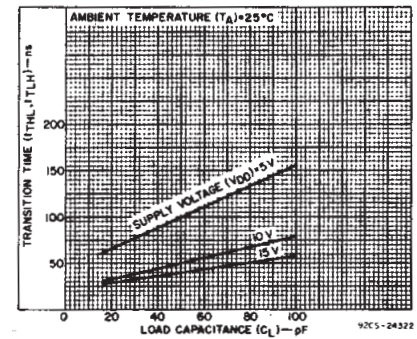


Fig. 9 - Typical transition time as a function of load capacitance.

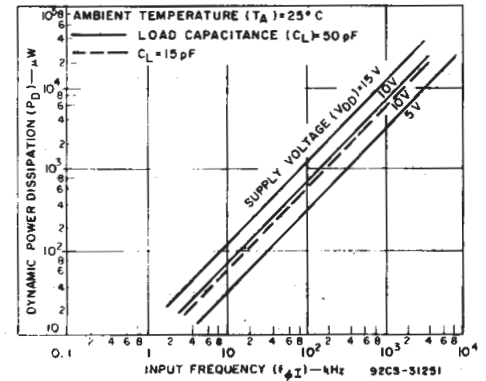


Fig. 10 - Typical dynamic power dissipation as a function of input frequency.



Fig. 11 - Dynamic power dissipation test circuit.



Fig. 12 - Typical RC circuit.

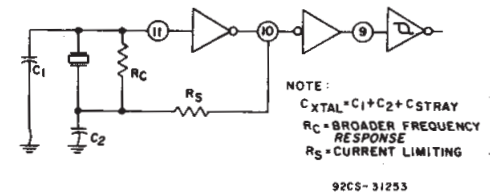


Fig. 13 - Typical crystal circuit.

# CD4060B Types

DYNAMIC ELECTRICAL CHARACTERISTICS at  $T_A = 25^\circ\text{C}$ , Input  $t_r, t_f = 20 \text{ ns}$ ,  $C_L = 50 \text{ pF}$ ,  $R_L = 200 \text{ k}\Omega$  [cont'd]

| CHARACTERISTIC   | TEST CONDITIONS   | VDD (V)                  | LIMITS |               |       | UNITS         |    |
|--|---|--------------------------|--------|---------------|-------|---------------|----|
|  |   |                          | Min.   | Typ.          | Max.  |               |    |
| <b>RC Operation</b>                                    |   |                          |        |               |       |               |    |
| Variation of Frequency (Unit-to-Unit)                  | $C_X = 200 \text{ pF}$ ,<br>$R_S = 560 \text{ k}\Omega$ ,<br>$R_X = 50 \text{ k}\Omega$ | 5                        | —      | $23 \pm 10\%$ | —     | kHz           |    |
|  |   | 10                       | —      | $24 \pm 10\%$ | —     |               |    |
|  |   | 15                       | —      | $25 \pm 10\%$ | —     |               |    |
| Variation of Frequency with voltage change (Same Unit) | $C_X = 200 \text{ pF}$ ,<br>$R_S = 560 \text{ k}\Omega$ ,<br>$R_X = 50 \text{ k}\Omega$ | 5V to 10 V<br>10V to 15V | —      | 1.5<br>0.5    | —     | kHz           |    |
| R <sub>X</sub> max.                                    | $C_X = 10 \mu\text{F}$<br>$= 50 \mu\text{F}$<br>$= 10 \mu\text{F}$                      | 5                        | —      | —             | 20    | M $\Omega$    |    |
|  |   | 10                       | —      | —             | 20    |               |    |
|  |   | 15                       | —      | —             | 10    |               |    |
| C <sub>X</sub> max.                                    | $R_X = 500 \text{ k}\Omega$<br>$= 300 \text{ k}\Omega$<br>$= 300 \text{ k}\Omega$       | 5                        | —      | —             | 1000  | $\mu\text{F}$ |    |
|  |   | 10                       | —      | —             | 50    |               |    |
|  |   | 15                       | —      | —             | 50    |               |    |
| Maximum Oscillator Frequency*                          | $R_X = 5 \text{ k}\Omega$<br>$R_S = 30 \text{ k}\Omega$<br>$C_X = 15 \text{ pF}$        | 10                       | 530    | 650           | 810   | kHz           |    |
|  |   | 15                       | 690    | 800           | 940   |               |    |
| Drive Current at Pin 9 (For Oscillator Design)         | I <sub>OL</sub>   | V <sub>O</sub> = 0.4 V   | 5      | 0.16          | 0.35  | —             | mA |
|  |   | = 0.5 V                  | 10     | 0.42          | 0.8   | —             |    |
|  |   | = 1.5 V                  | 15     | 1             | 2     | —             |    |
|  | I <sub>OH</sub>   | V <sub>O</sub> = 4.6 V   | 5      | -0.16         | -0.35 | —             |    |
|  |   | = 9.5 V                  | 10     | -0.42         | -0.8  | —             |    |
|  |   | = 13.5 V                 | 15     | -1            | -2    | —             |    |

\*RC oscillator applications are not recommended at supply voltages below 7 V for  $R_X < 50 \text{ k}\Omega$ .



Fig. 14 – Quiescent device current.

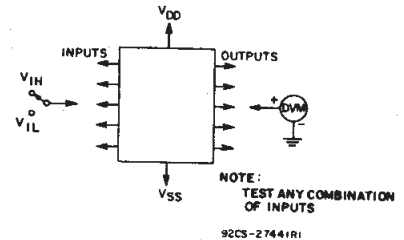


Fig. 15 – Input voltage.

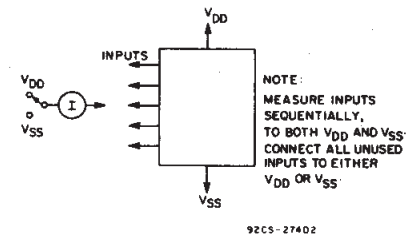
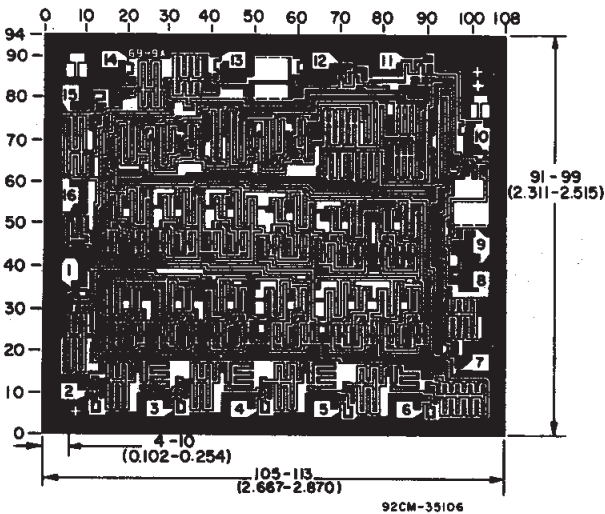


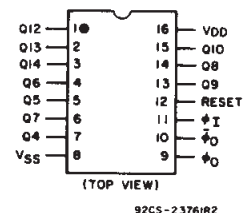
Fig. 16 – Input current.

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Chip dimensions and pad layout for CD4060B

## TERMINAL DIAGRAM



Dimensions in parentheses are in millimeters and are derived from the basic inch dimensions as indicated. Grid graduations are in mils ( $10^{-3}$  inch).

**PACKAGING INFORMATION**

| Orderable Device | Status <sup>(1)</sup> | Package Type | Package Drawing | Pins | Package Qty | Eco Plan <sup>(2)</sup> | Lead/Ball Finish | MSL Peak Temp <sup>(3)</sup> |
|------------------|-----------------------|--------------|-----------------|------|-------------|-------------------------|------------------|------------------------------|
| CD4060BE         | ACTIVE                | PDIP         | N               | 16   | 25          | Pb-Free (RoHS)          | CU NIPDAU        | N / A for Pkg Type           |
| CD4060BEE4       | ACTIVE                | PDIP         | N               | 16   | 25          | Pb-Free (RoHS)          | CU NIPDAU        | N / A for Pkg Type           |
| CD4060BF         | ACTIVE                | CDIP         | J               | 16   | 1           | TBD                     | A42              | N / A for Pkg Type           |
| CD4060BF3A       | ACTIVE                | CDIP         | J               | 16   | 1           | TBD                     | A42              | N / A for Pkg Type           |
| CD4060BF3AS2534  | OBSOLETE              | CDIP         | J               | 16   |             | TBD                     | Call TI          | Call TI                      |
| CD4060BM         | ACTIVE                | SOIC         | D               | 16   | 40          | Green (RoHS & no Sb/Br) | CU NIPDAU        | Level-1-260C-UNLIM           |
| CD4060BM96       | ACTIVE                | SOIC         | D               | 16   | 2500        | Green (RoHS & no Sb/Br) | CU NIPDAU        | Level-1-260C-UNLIM           |
| CD4060BM96E4     | ACTIVE                | SOIC         | D               | 16   | 2500        | Green (RoHS & no Sb/Br) | CU NIPDAU        | Level-1-260C-UNLIM           |
| CD4060BM96G4     | ACTIVE                | SOIC         | D               | 16   | 2500        | Green (RoHS & no Sb/Br) | CU NIPDAU        | Level-1-260C-UNLIM           |
| CD4060BME4       | ACTIVE                | SOIC         | D               | 16   | 40          | Green (RoHS & no Sb/Br) | CU NIPDAU        | Level-1-260C-UNLIM           |
| CD4060BMG4       | ACTIVE                | SOIC         | D               | 16   | 40          | Green (RoHS & no Sb/Br) | CU NIPDAU        | Level-1-260C-UNLIM           |
| CD4060BMT        | ACTIVE                | SOIC         | D               | 16   | 250         | Green (RoHS & no Sb/Br) | CU NIPDAU        | Level-1-260C-UNLIM           |
| CD4060BMTE4      | ACTIVE                | SOIC         | D               | 16   | 250         | Green (RoHS & no Sb/Br) | CU NIPDAU        | Level-1-260C-UNLIM           |
| CD4060BMTG4      | ACTIVE                | SOIC         | D               | 16   | 250         | Green (RoHS & no Sb/Br) | CU NIPDAU        | Level-1-260C-UNLIM           |
| CD4060BNSR       | ACTIVE                | SO           | NS              | 16   | 2000        | Green (RoHS & no Sb/Br) | CU NIPDAU        | Level-1-260C-UNLIM           |
| CD4060BNSRE4     | ACTIVE                | SO           | NS              | 16   | 2000        | Green (RoHS & no Sb/Br) | CU NIPDAU        | Level-1-260C-UNLIM           |
| CD4060BNSRG4     | ACTIVE                | SO           | NS              | 16   | 2000        | Green (RoHS & no Sb/Br) | CU NIPDAU        | Level-1-260C-UNLIM           |
| CD4060BPW        | ACTIVE                | TSSOP        | PW              | 16   | 90          | Green (RoHS & no Sb/Br) | CU NIPDAU        | Level-1-260C-UNLIM           |
| CD4060BPWE4      | ACTIVE                | TSSOP        | PW              | 16   | 90          | Green (RoHS & no Sb/Br) | CU NIPDAU        | Level-1-260C-UNLIM           |
| CD4060BPWG4      | ACTIVE                | TSSOP        | PW              | 16   | 90          | Green (RoHS & no Sb/Br) | CU NIPDAU        | Level-1-260C-UNLIM           |
| CD4060BPWR       | ACTIVE                | TSSOP        | PW              | 16   | 2000        | Green (RoHS & no Sb/Br) | CU NIPDAU        | Level-1-260C-UNLIM           |
| CD4060BPWRE4     | ACTIVE                | TSSOP        | PW              | 16   | 2000        | Green (RoHS & no Sb/Br) | CU NIPDAU        | Level-1-260C-UNLIM           |
| CD4060BPWRG4     | ACTIVE                | TSSOP        | PW              | 16   | 2000        | Green (RoHS & no Sb/Br) | CU NIPDAU        | Level-1-260C-UNLIM           |

<sup>(1)</sup> The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSOLETE:** TI has discontinued the production of the device.

<sup>(2)</sup> Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

**TBD:** The Pb-Free/Green conversion plan has not been defined.

**Pb-Free (RoHS):** TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

**Pb-Free (RoHS Exempt):** This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

**Green (RoHS & no Sb/Br):** TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

<sup>(3)</sup> MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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**TAPE AND REEL INFORMATION**



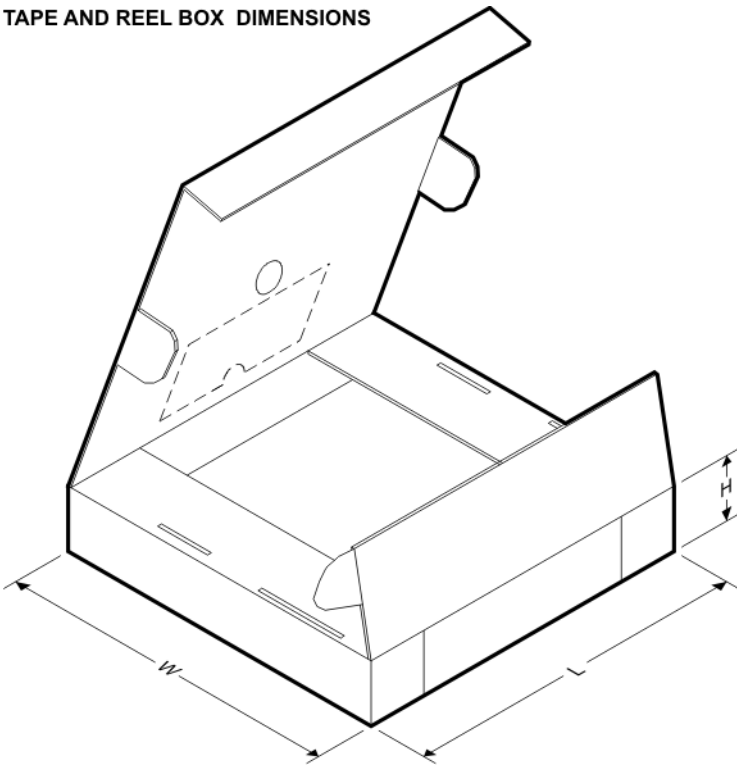
**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**



\*All dimensions are nominal

| Device     | Package Type | Package Drawing | Pins | SPQ  | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|------------|--------------|-----------------|------|------|--------------------|--------------------|---------|---------|---------|---------|--------|---------------|
| CD4060BM96 | SOIC         | D               | 16   | 2500 | 330.0              | 16.4               | 6.5     | 10.3    | 2.1     | 8.0     | 16.0   | Q1            |
| CD4060BNSR | SO           | NS              | 16   | 2000 | 330.0              | 16.4               | 8.2     | 10.5    | 2.5     | 12.0    | 16.0   | Q1            |
| CD4060BPWR | TSSOP        | PW              | 16   | 2000 | 330.0              | 12.4               | 7.0     | 5.6     | 1.6     | 8.0     | 12.0   | Q1            |

**TAPE AND REEL BOX DIMENSIONS**



\*All dimensions are nominal

| Device     | Package Type | Package Drawing | Pins | SPQ  | Length (mm) | Width (mm) | Height (mm) |
|------------|--------------|-----------------|------|------|-------------|------------|-------------|
| CD4060BM96 | SOIC         | D               | 16   | 2500 | 333.2       | 345.9      | 28.6        |
| CD4060BNSR | SO           | NS              | 16   | 2000 | 346.0       | 346.0      | 33.0        |
| CD4060BPWR | TSSOP        | PW              | 16   | 2000 | 346.0       | 346.0      | 29.0        |



PW (R-PDSO-G\*\*)

PLASTIC SMALL-OUTLINE PACKAGE

14 PINS SHOWN



4040064/F 01/97

- NOTES: A. All linear dimensions are in millimeters.  
 B. This drawing is subject to change without notice.  
 C. Body dimensions do not include mold flash or protrusion not to exceed 0,15.  
 D. Falls within JEDEC MO-153

# J (R-GDIP-T\*\*)

14 LEADS SHOWN

# CERAMIC DUAL IN-LINE PACKAGE



| DIM \ PINS ** | 14                     | 16                     | 18                     | 20                     |
|---------------|------------------------|------------------------|------------------------|------------------------|
| A             | 0.300<br>(7,62)<br>BSC | 0.300<br>(7,62)<br>BSC | 0.300<br>(7,62)<br>BSC | 0.300<br>(7,62)<br>BSC |
| B MAX         | 0.785<br>(19,94)       | .840<br>(21,34)        | 0.960<br>(24,38)       | 1.060<br>(26,92)       |
| B MIN         | —                      | —                      | —                      | —                      |
| C MAX         | 0.300<br>(7,62)        | 0.300<br>(7,62)        | 0.310<br>(7,87)        | 0.300<br>(7,62)        |
| C MIN         | 0.245<br>(6,22)        | 0.245<br>(6,22)        | 0.220<br>(5,59)        | 0.245<br>(6,22)        |



4040083/F 03/03

- NOTES:
- All linear dimensions are in inches (millimeters).
  - This drawing is subject to change without notice.
  - This package is hermetically sealed with a ceramic lid using glass frit.
  - Index point is provided on cap for terminal identification only on press ceramic glass frit seal only.
  - Falls within MIL STD 1835 GDIP1-T14, GDIP1-T16, GDIP1-T18 and GDIP1-T20.

# MECHANICAL DATA

NS (R-PDSO-G\*\*)

PLASTIC SMALL-OUTLINE PACKAGE

14-PINS SHOWN



- NOTES:
- A. All linear dimensions are in millimeters.
  - B. This drawing is subject to change without notice.
  - C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15.

D (R-PDSO-G16)

PLASTIC SMALL-OUTLINE PACKAGE



4040047-5/J 09/09

- NOTES:
- A. All linear dimensions are in inches (millimeters).
  - B. This drawing is subject to change without notice.
  - C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 (0,15) per end.
  - D. Body width does not include interlead flash. Interlead flash shall not exceed .017 (0,43) per side.
  - E. Reference JEDEC MS-012 variation AC.

D(R-PDSO-G16)



- NOTES:
- A. All linear dimensions are in millimeters.
  - B. This drawing is subject to change without notice.
  - C. Refer to IPC7351 for alternate board design.
  - D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525
  - E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

N (R-PDIP-T\*\*)

PLASTIC DUAL-IN-LINE PACKAGE

16 PINS SHOWN



- NOTES:
- A. All linear dimensions are in inches (millimeters).
  - B. This drawing is subject to change without notice.
  - Falls within JEDEC MS-001, except 18 and 20 pin minimum body length (Dim A).
  - The 20 pin end lead shoulder width is a vendor option, either half or full width.

**PACKAGING INFORMATION**

| Orderable Device | Status<br>(1) | Package Type | Package Drawing | Pins | Package Qty | Eco Plan<br>(2)  | Lead finish/<br>Ball material<br>(6) | MSL Peak Temp<br>(3) | Op Temp (°C) | Device Marking<br>(4/5) | Samples                 |
|------------------|---------------|--------------|-----------------|------|-------------|------------------|--------------------------------------|----------------------|--------------|-------------------------|-------------------------|
| CD4060BE         | ACTIVE        | PDIP         | N               | 16   | 25          | RoHS & Green     | NIPDAU                               | N / A for Pkg Type   | -55 to 125   | CD4060BE                | <a href="#">Samples</a> |
| CD4060BEE4       | ACTIVE        | PDIP         | N               | 16   | 25          | RoHS & Green     | NIPDAU                               | N / A for Pkg Type   | -55 to 125   | CD4060BE                | <a href="#">Samples</a> |
| CD4060BF         | ACTIVE        | CDIP         | J               | 16   | 1           | Non-RoHS & Green | SNPB                                 | N / A for Pkg Type   | -55 to 125   | CD4060BF                | <a href="#">Samples</a> |
| CD4060BF3A       | ACTIVE        | CDIP         | J               | 16   | 1           | Non-RoHS & Green | SNPB                                 | N / A for Pkg Type   | -55 to 125   | CD4060BF3A              | <a href="#">Samples</a> |
| CD4060BM         | ACTIVE        | SOIC         | D               | 16   | 40          | RoHS & Green     | NIPDAU                               | Level-1-260C-UNLIM   | -55 to 125   | CD4060BM                | <a href="#">Samples</a> |
| CD4060BM96       | ACTIVE        | SOIC         | D               | 16   | 2500        | RoHS & Green     | NIPDAU                               | Level-1-260C-UNLIM   | -55 to 125   | CD4060BM                | <a href="#">Samples</a> |
| CD4060BMG4       | ACTIVE        | SOIC         | D               | 16   | 40          | RoHS & Green     | NIPDAU                               | Level-1-260C-UNLIM   | -55 to 125   | CD4060BM                | <a href="#">Samples</a> |
| CD4060BMT        | ACTIVE        | SOIC         | D               | 16   | 250         | RoHS & Green     | NIPDAU                               | Level-1-260C-UNLIM   | -55 to 125   | CD4060BM                | <a href="#">Samples</a> |
| CD4060BNSR       | ACTIVE        | SO           | NS              | 16   | 2000        | RoHS & Green     | NIPDAU                               | Level-1-260C-UNLIM   | -55 to 125   | CD4060B                 | <a href="#">Samples</a> |
| CD4060BPW        | ACTIVE        | TSSOP        | PW              | 16   | 90          | RoHS & Green     | NIPDAU                               | Level-1-260C-UNLIM   | -55 to 125   | CM060B                  | <a href="#">Samples</a> |
| CD4060BPWR       | ACTIVE        | TSSOP        | PW              | 16   | 2000        | RoHS & Green     | NIPDAU                               | Level-1-260C-UNLIM   | -55 to 125   | CM060B                  | <a href="#">Samples</a> |
| CD4060BPWRE4     | ACTIVE        | TSSOP        | PW              | 16   | 2000        | RoHS & Green     | NIPDAU                               | Level-1-260C-UNLIM   | -55 to 125   | CM060B                  | <a href="#">Samples</a> |
| CD4060BPWRG4     | ACTIVE        | TSSOP        | PW              | 16   | 2000        | RoHS & Green     | NIPDAU                               | Level-1-260C-UNLIM   | -55 to 125   | CM060B                  | <a href="#">Samples</a> |

(1) The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSELETE:** TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

**RoHS Exempt:** TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

**Green:** TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of  $\leq 1000$ ppm threshold. Antimony trioxide based flame retardants must also meet the  $\leq 1000$ ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

**OTHER QUALIFIED VERSIONS OF CD4060B, CD4060B-MIL :**

- Catalog : [CD4060B](#)
- Military : [CD4060B-MIL](#)

NOTE: Qualified Version Definitions:

- Catalog - TI's standard catalog product
- Military - QML certified for Military and Defense Applications



**TAPE AND REEL INFORMATION**

**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**


\*All dimensions are nominal

| Device     | Package Type | Package Drawing | Pins | SPQ  | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|------------|--------------|-----------------|------|------|--------------------|--------------------|---------|---------|---------|---------|--------|---------------|
| CD4060BM96 | SOIC         | D               | 16   | 2500 | 330.0              | 16.4               | 6.5     | 10.3    | 2.1     | 8.0     | 16.0   | Q1            |
| CD4060BNSR | SO           | NS              | 16   | 2000 | 330.0              | 16.4               | 8.2     | 10.5    | 2.5     | 12.0    | 16.0   | Q1            |
| CD4060BPWR | TSSOP        | PW              | 16   | 2000 | 330.0              | 12.4               | 6.9     | 5.6     | 1.6     | 8.0     | 12.0   | Q1            |

**TAPE AND REEL BOX DIMENSIONS**


\*All dimensions are nominal

| Device     | Package Type | Package Drawing | Pins | SPQ  | Length (mm) | Width (mm) | Height (mm) |
|------------|--------------|-----------------|------|------|-------------|------------|-------------|
| CD4060BM96 | SOIC         | D               | 16   | 2500 | 340.5       | 336.1      | 32.0        |
| CD4060BNSR | SO           | NS              | 16   | 2000 | 853.0       | 449.0      | 35.0        |
| CD4060BPWR | TSSOP        | PW              | 16   | 2000 | 853.0       | 449.0      | 35.0        |

D (R-PDSO-G16)

PLASTIC SMALL OUTLINE



- NOTES:
- A. All linear dimensions are in inches (millimeters).
  - B. This drawing is subject to change without notice.
  - C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
  - D. Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
  - E. Reference JEDEC MS-012 variation AC.

D (R-PDSO-G16)

PLASTIC SMALL OUTLINE



4211283-4/E 08/12

- NOTES:
- All linear dimensions are in millimeters.
  - This drawing is subject to change without notice.
  - Publication IPC-7351 is recommended for alternate designs.
  - Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
  - Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.



4220204/A 02/2017

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153.

# EXAMPLE BOARD LAYOUT

PW0016A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



LAND PATTERN EXAMPLE  
EXPOSED METAL SHOWN  
SCALE: 10X



4220204/A 02/2017

NOTES: (continued)

- 6. Publication IPC-7351 may have alternate designs.
- 7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

# EXAMPLE STENCIL DESIGN

PW0016A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



SOLDER PASTE EXAMPLE  
BASED ON 0.125 mm THICK STENCIL  
SCALE: 10X

4220204/A 02/2017

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

# MECHANICAL DATA

NS (R-PDSO-G\*\*)

PLASTIC SMALL-OUTLINE PACKAGE

14-PINS SHOWN



- NOTES:
- A. All linear dimensions are in millimeters.
  - B. This drawing is subject to change without notice.
  - C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15.



# J (R-GDIP-T\*\*)

14 LEADS SHOWN

# CERAMIC DUAL IN-LINE PACKAGE



| DIM \ PINS ** | 14                     | 16                     | 18                     | 20                     |
|---------------|------------------------|------------------------|------------------------|------------------------|
| A             | 0.300<br>(7,62)<br>BSC | 0.300<br>(7,62)<br>BSC | 0.300<br>(7,62)<br>BSC | 0.300<br>(7,62)<br>BSC |
| B MAX         | 0.785<br>(19,94)       | .840<br>(21,34)        | 0.960<br>(24,38)       | 1.060<br>(26,92)       |
| B MIN         | —                      | —                      | —                      | —                      |
| C MAX         | 0.300<br>(7,62)        | 0.300<br>(7,62)        | 0.310<br>(7,87)        | 0.300<br>(7,62)        |
| C MIN         | 0.245<br>(6,22)        | 0.245<br>(6,22)        | 0.220<br>(5,59)        | 0.245<br>(6,22)        |



4040083/F 03/03

- NOTES:
- All linear dimensions are in inches (millimeters).
  - This drawing is subject to change without notice.
  - This package is hermetically sealed with a ceramic lid using glass frit.
  - Index point is provided on cap for terminal identification only on press ceramic glass frit seal only.
  - Falls within MIL STD 1835 GDIP1-T14, GDIP1-T16, GDIP1-T18 and GDIP1-T20.

N (R-PDIP-T\*\*)

PLASTIC DUAL-IN-LINE PACKAGE

16 PINS SHOWN



- NOTES:
- A. All linear dimensions are in inches (millimeters).
  - B. This drawing is subject to change without notice.
  - Falls within JEDEC MS-001, except 18 and 20 pin minimum body length (Dim A).
  - The 20 pin end lead shoulder width is a vendor option, either half or full width.

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