TGA2704SM

9 – 11 GHz 7 W GaAs Power Amplifier

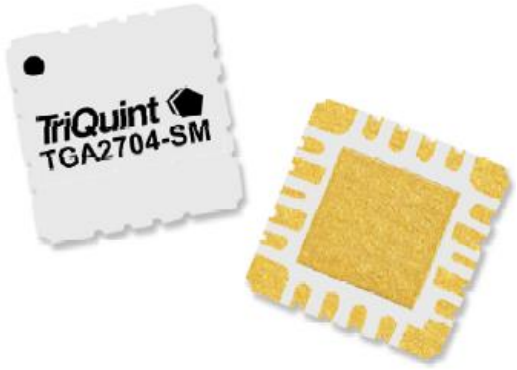
Product Overview

Qorvo's TGA2704-SM is a high power amplifier package fabricated on Qorvo's production 0.25um pHEMT GaAs process. The TGA2704-SM operates from 9 –11 GHz, provides 7 W of saturated output power with 21 dB of small signal gain and 40% power–added efficiency.

The TGA2704-SM features a ceramic QFN de-signed for surface mount to a printed circuit board.

Fully matched to 50 Ohms and with integrated DC blocking capacitors on both I/O ports, the TGA2704-SM is ideally suited to support both commercial and defense related applications.

Lead-free and RoHS compliant.



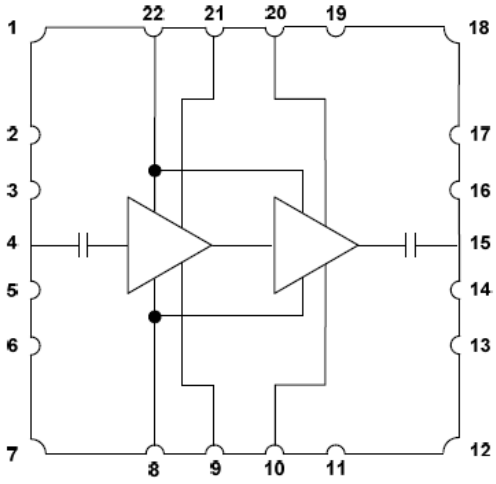
QFN 7 x 7 x 1.27 mm Air Cavity Laminate Package

Key Features

- Frequency Range: 9 – 11 GHz
- P_{SAT} (P_{IN}=22 dBm): 38.5 dBm
- PAE (P_{IN}=22 dBm): 40 %
- Small Signal Gain: 21 dB
- Bias: V_{D1} = 9 V, I_{D1} = 1.05 A, V_G = -0.7V typical
- Package Dimensions: 7.0 x 7.0 x 1.27 mm

Performance is typical across frequency. Please reference electrical specification table and data plots for more details.

Functional Block Diagram



Applications

- Point-to-Point Radio
- Satellite Communications
- Radar, Traffic Control
- Weather Monitoring
- Port Security

Ordering Information

Part No.	Description
TGA2704-SM	9 – 11 GHz 7 W GaAs PA
TGA2704-SMEVB	Evaluation Board

Absolute Maximum Ratings

Parameter	Rating
Drain Voltage (V_D)	10 V
Gate Voltage Range (V_G)	-1.2 to +0.5 V
Drain Current (I_D)	3.85 A
Gate Current (I_G)	-14 to +126 mA
RF Input Power, CW, 50 Ω, T=25 °C	23 dBm
Channel Temperature (T_{CH})	200 °C
Storage Temperature	−55 to +150 °C
Mounting Temperature (30 seconds)	260 °C

Exceeding any one or a combination of the Absolute Maximum Rating conditions may cause permanent damage to the device. Extended application of Absolute Maximum Rating conditions to the device may reduce device reliability.

Recommended Operating Conditions

Parameter	Min	Typ	Max	Units
Drain Voltage (V_D)		9		V
Drain Current, Quiescent (I_{DQ})		1.05		A
Drain Current, RF (I_{D_Drive})	See chart page 4, 6			mA
Gate Voltage Typ. Range (V_G)	−0.3 to −0.9			V
Gate Current, RF (I_{G_Drive})		1.5		mA
Operating Temp. Range	−40	+25	+85	°C

Electrical specifications are measured at specified test conditions. Specifications are not guaranteed over all recommended operating conditions.

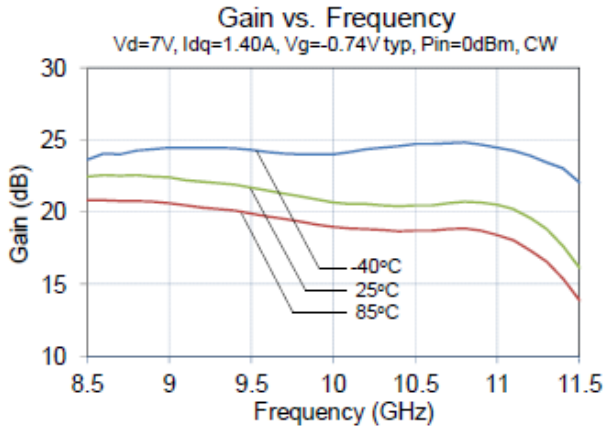
Electrical Specifications

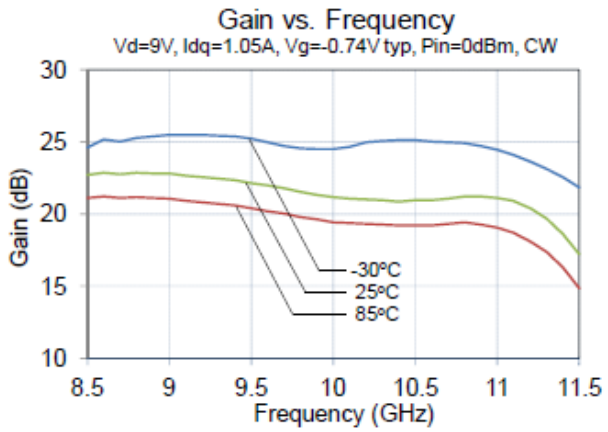
Parameter	Conditions (1) (2)	Min	Typ.	Max	Units
Operational Frequency Range	Unless Otherwise	9		11	GHz
Output Power at Saturation, P_{SAT}	P_{IN} = +22 dBm		38.5		dBm
Output Power at 1dB compression, P_{1dB}	P_{IN} = +16 to +17 dBm range		37.5		dBm
Power Added Efficiency, PAE	P_{IN} = +22 dBm		40		%
Small Signal Gain, S21			21		dB
Input Return Loss, IRL			10		dB
Output Return Loss, ORL			13		dB
P_{SAT} Temperature Coefficient	T_{diff} = (85 – (−40)) °C, P_{in} = +22 dBm		−0.011		dBm/°C

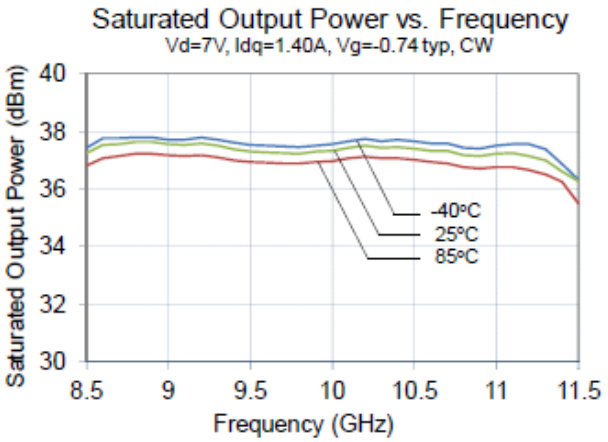
Notes:
1. Test conditions unless otherwise noted: CW, V_D = 9V, I_D = 1.05 A, adjusting V_G (typical -0.7V), T_{BASE} = +25 °C, Z_0 = 50 Ω
2. T_{BASE} is back side of package

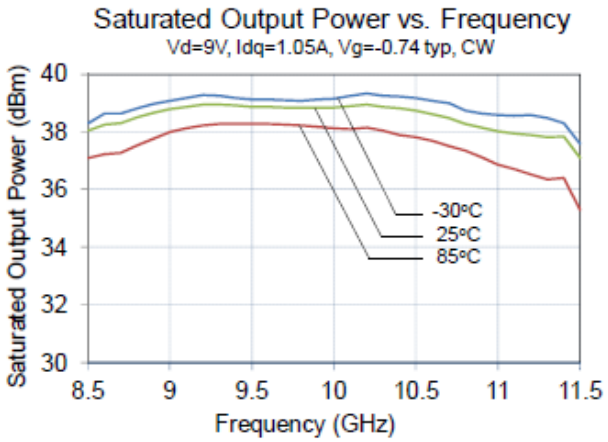
Performance Plots

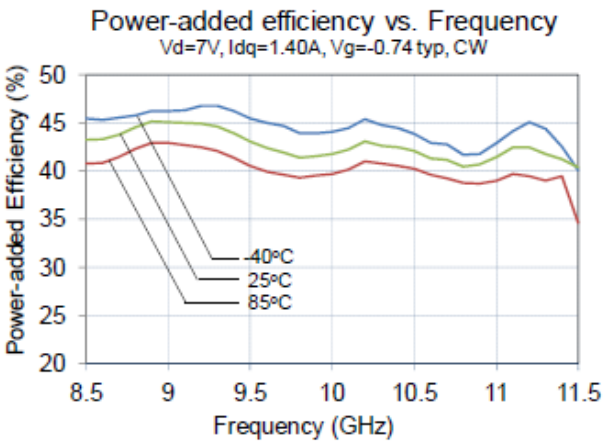
Test conditions unless otherwise noted: CW, V_D/ I_D = 7V/1.4A vs. 9V/1.05A, , adjusting V_G (typical -0.7V), P_{IN} = +22dBm, T_{BASE} = +25 °C, Z_0 = 50 Ω

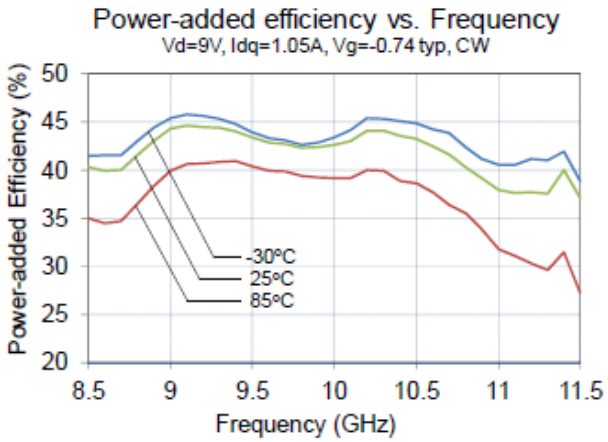






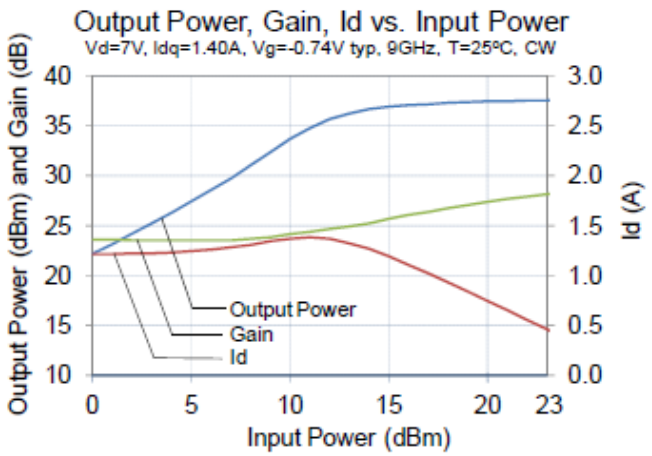


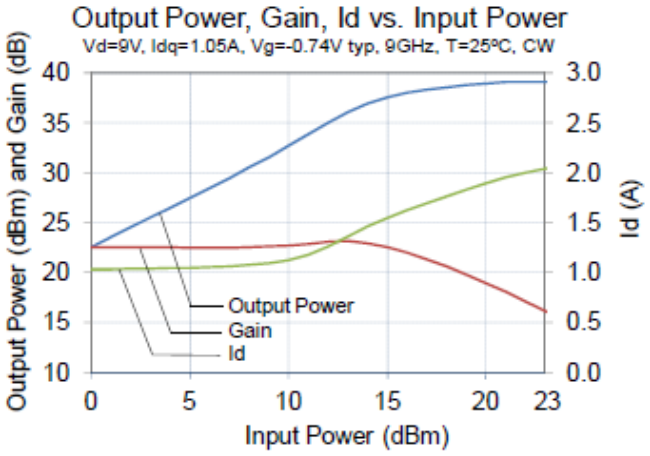


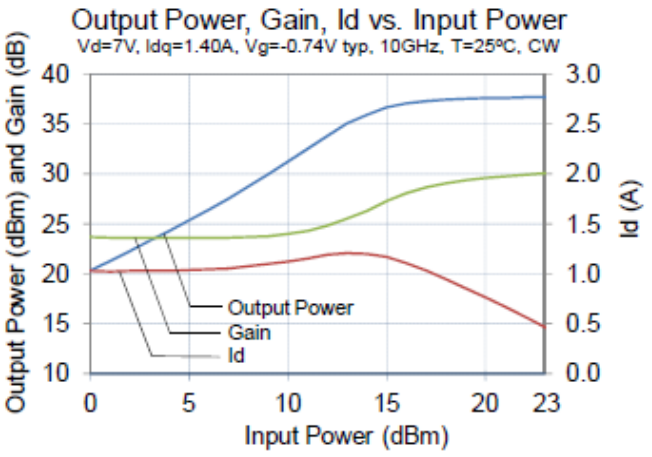


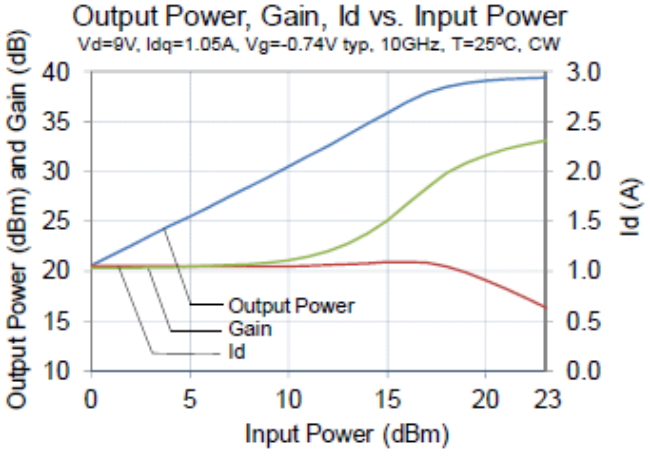
Performance Plots

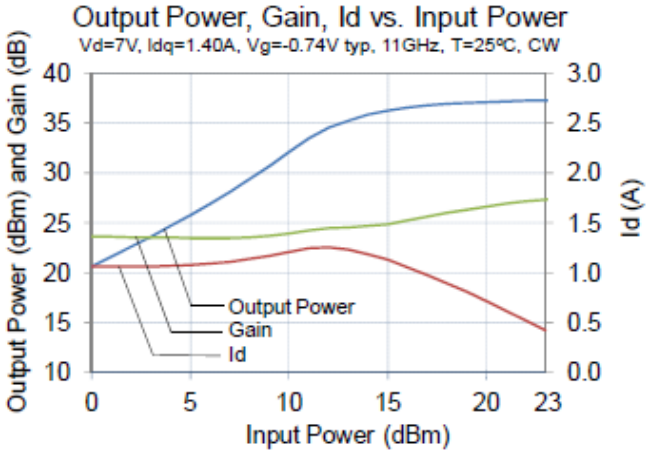
Test conditions unless otherwise noted: CW, V_D/ I_D = 7V/1.4A vs. 9V/1.05A, , adjusting V_G (typical -0.7V), P_{IN} = +22dBm, T_{BASE} = +25 °C, Z_0 = 50 Ω

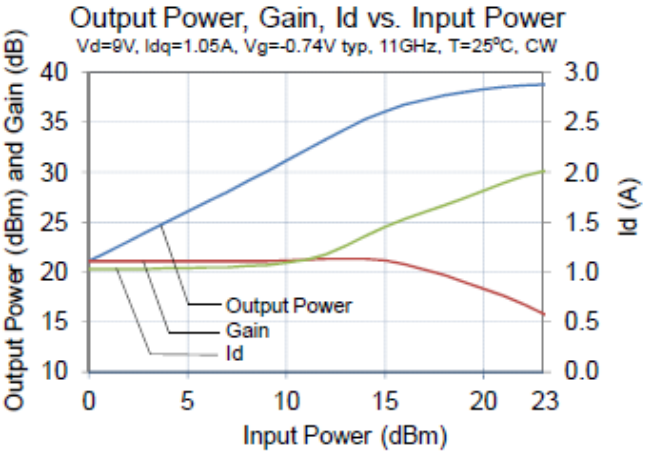






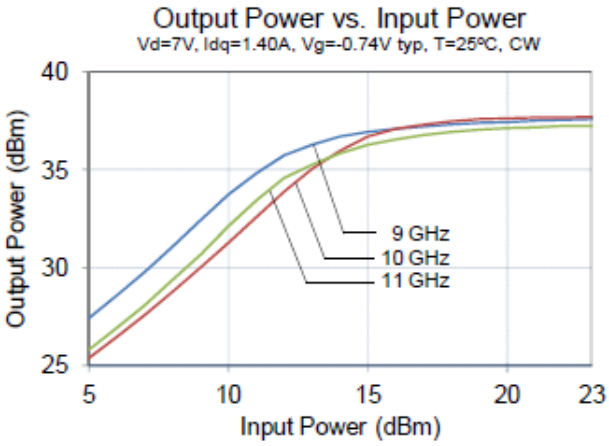


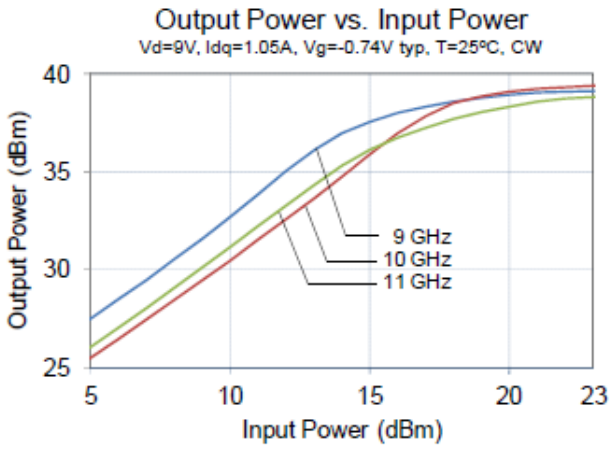


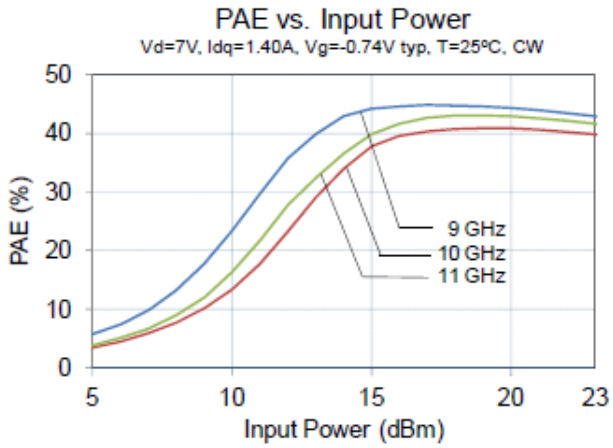


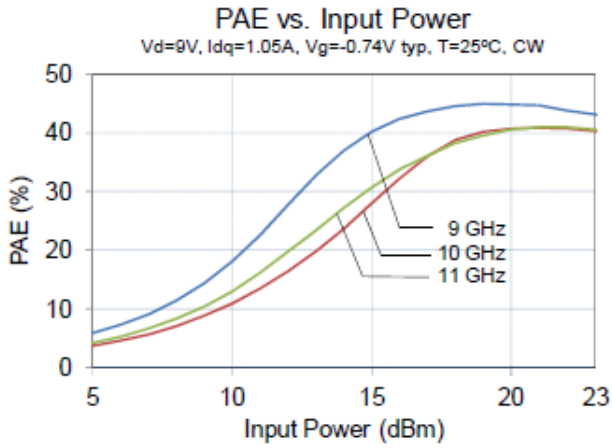
Performance Plots

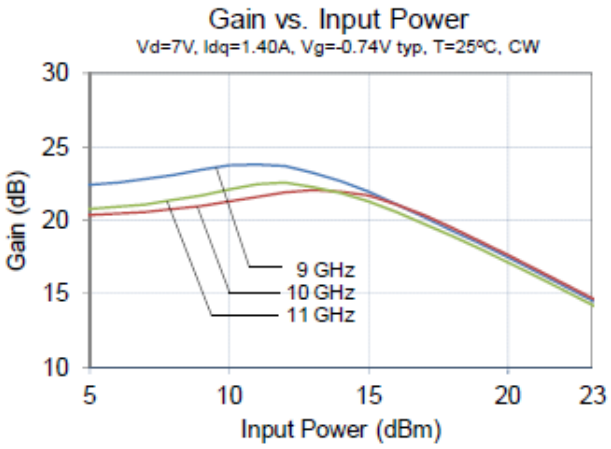
Test conditions unless otherwise noted: CW, V_D/ I_D = 7V/1.4A vs. 9V/1.05A, , adjusting V_G (typical -0.7V), P_{IN} = +22dBm, T_{BASE} = +25 °C, Z_0 = 50 Ω

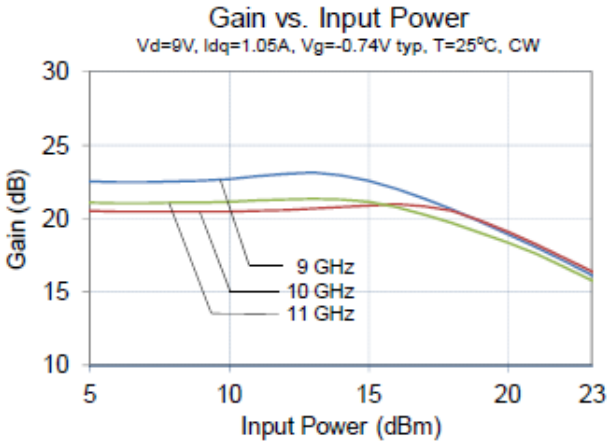






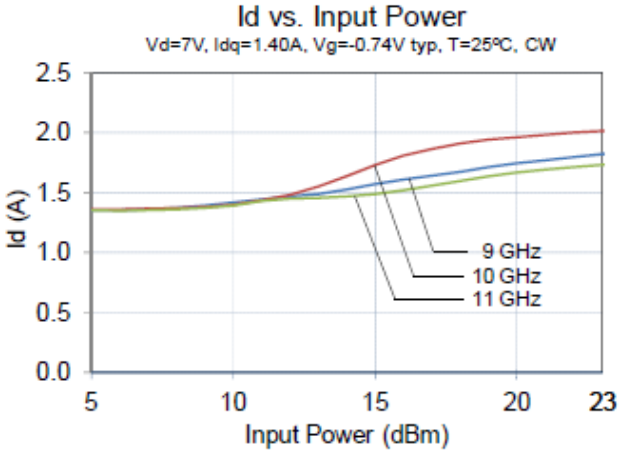


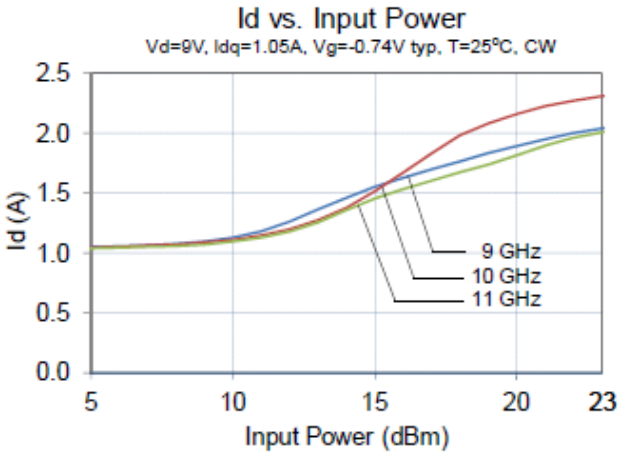


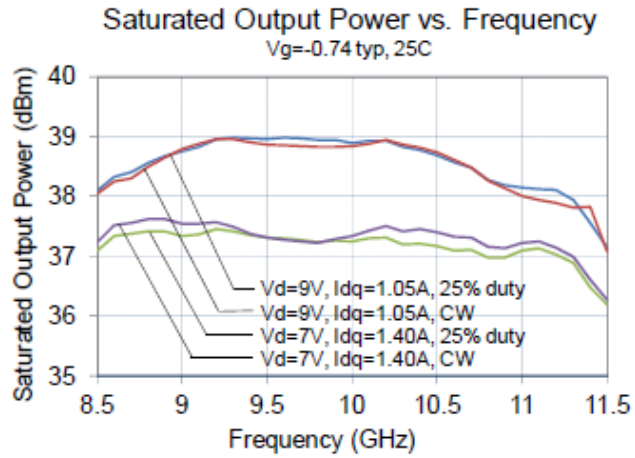


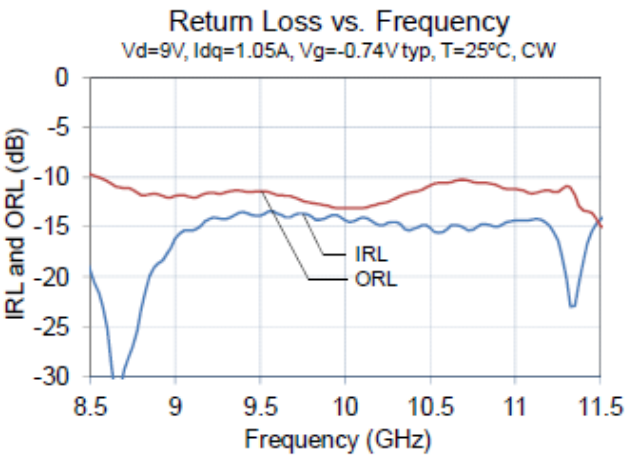
Performance Plots

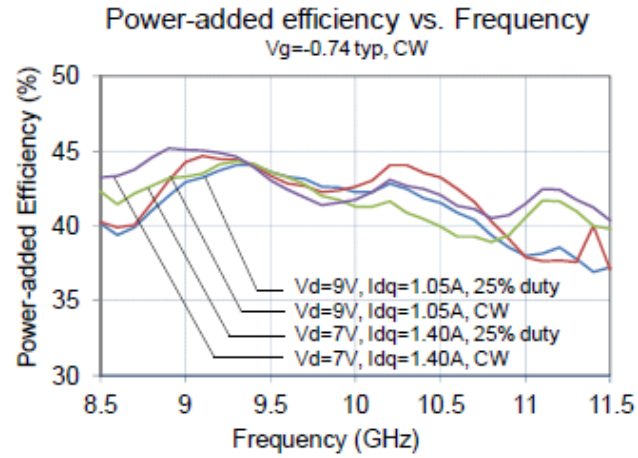
Test conditions unless otherwise noted: CW, V_D/ I_D = 7V/1.4A vs. 9V/1.05A, , adjusting V_G (typical -0.7V), P_{IN} = +22dBm, T_{BASE} = +25 °C, Z_0 = 50 Ω







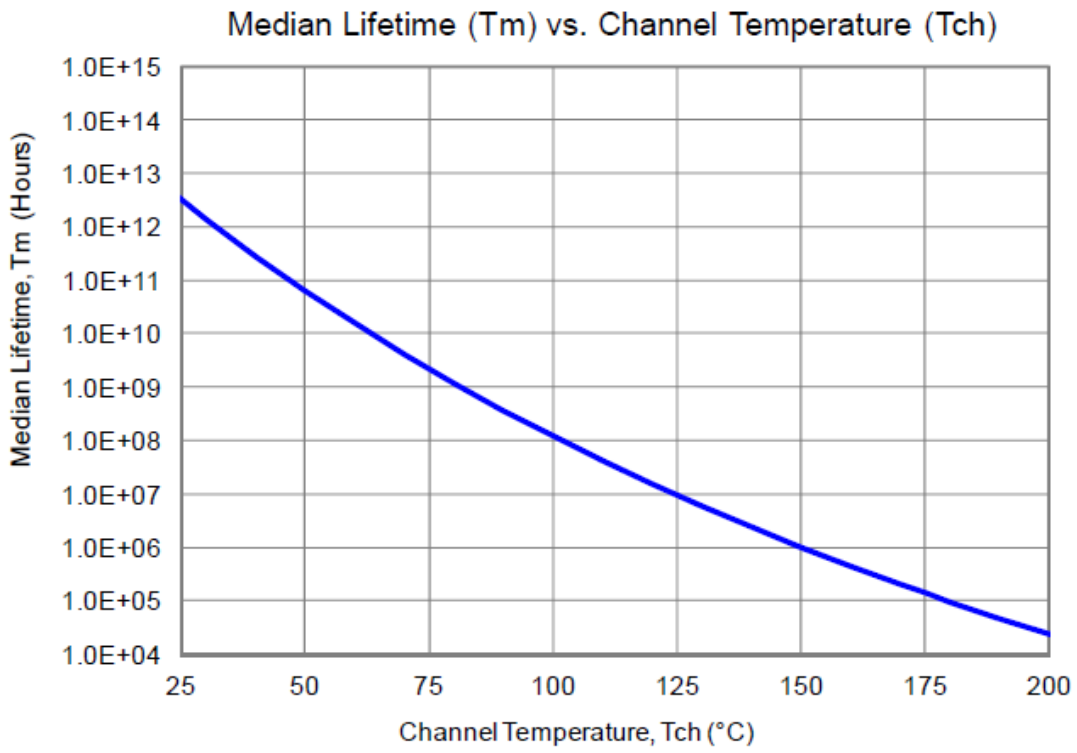




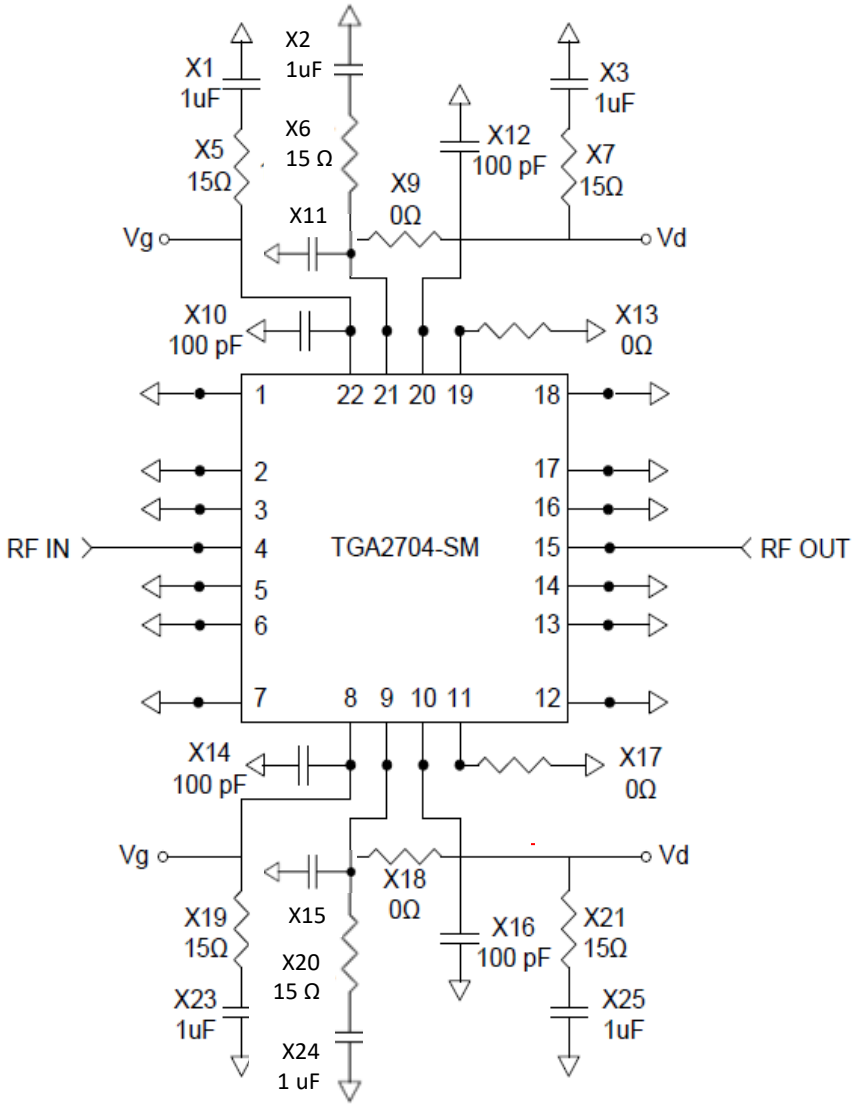
Thermal and Reliability Information

Parameter	Test Conditions [1/]	Value	Units
Thermal Resistance, θ_{JC}	T_{BASE} = 85 °C, CW, V_D = 7 V, I_{DQ} = 1.4 A, no P_{IN}, P_{DISS} = 9.8 W	7.8	ºC/W
Channel Temperature, T_{CH}		161	°C
Median Lifetime, T_M		4.1E+5	Hrs
Thermal Resistance, θ_{JC}	T_{BASE} = 85 °C, CW, V_D = 7 V, I_{DQ} = 1.4 A, I_{D_Drive} = 1.93 A, P_{OUT} = 37.3 dBm, P_{DISS} = 8.1 W	6.4	ºC/W
Channel Temperature, T_{CH}		137	°C
Median Lifetime, T_M		3.1E+6	Hrs
Thermal Resistance, θ_{JC}	T_{BASE} = 85 °C, CW, V_D = 9 V, I_{DQ} = 1.05 A, no P_{IN}, P_{DISS} = 9.5 W	7.5	ºC/W
Channel Temperature, T_{CH}		156	°C
Median Lifetime, T_M		6.1E+5	Hrs
Thermal Resistance, θ_{JC}	T_{BASE} = 85 °C, CW, V_D = 9 V, I_{DQ} = 1.05 A, I_{D_Drive} = 2.11 A, P_{OUT} = 38.9 dBm, P_{DISS} = 11.2 W	6.3	ºC/W
Channel Temperature, T_{CH}		156	°C
Median Lifetime, T_M		6.1E+5	Hrs

Notes:
1. Thermal resistance determined to the back of package T_{BASE}



Recommended Application Circuit



Notes:
1. Tied all V_D's together; tied all V_G's together

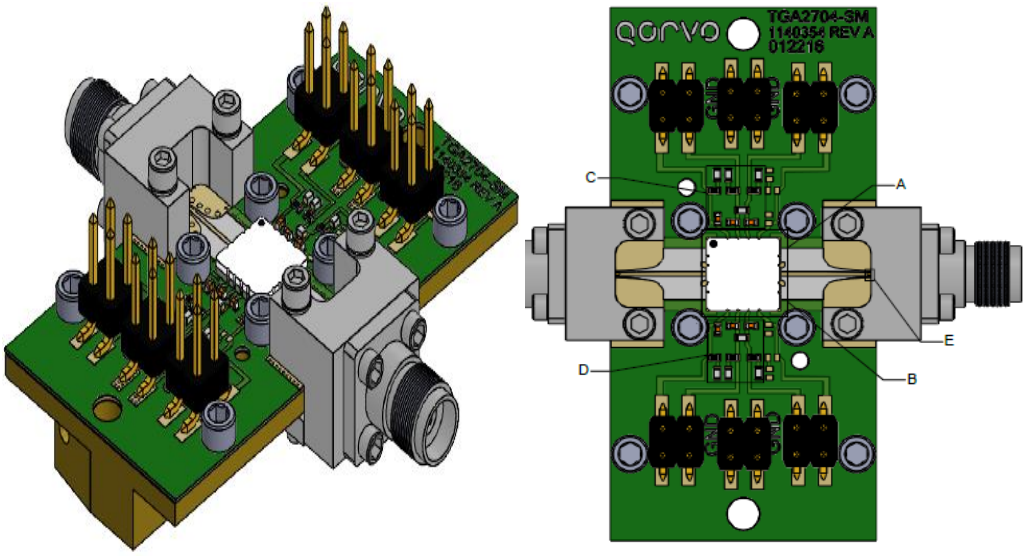
Bias Up Procedure

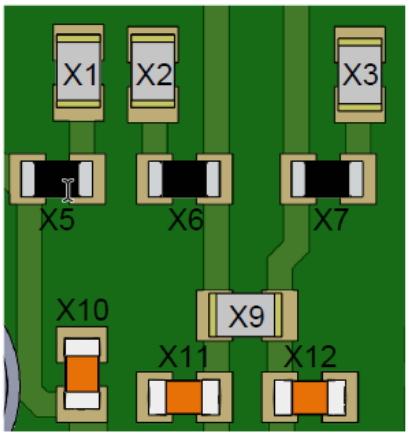
1. Set I_D limit to 3.2 A, I_G limit to 10 mA
2. Apply −1.1 V to V_G
3. Apply +9 V to V_D; ensure I_{DQ} is approx. 0 mA
4. Adjust V_G until I_{DQ} = 1.05 A (V_G ~ −2.7 V +/- Typ.)
5. Turn on RF supply

Bias Down Procedure

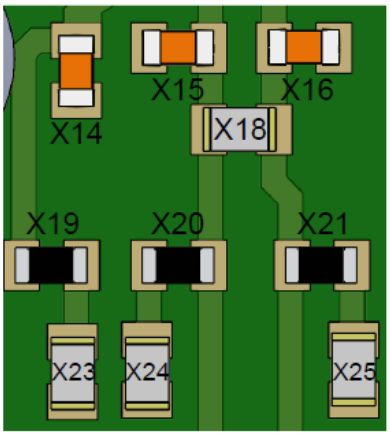
1. Turn off RF supply
2. Reduce V_G to −1.1 V; ensure I_{DQ} is approx. 0 mA
3. Set V_D to 0 V
4. Turn off V_D supply
5. Turn off V_G supply

Application Evaluation Board (EVB)





DETAIL C



DETAIL D

Notes:
1. Board Material is RO4003 0.008” thickness with ½ oz. copper cladding
2. Vias under the ground paddle are copper filled.

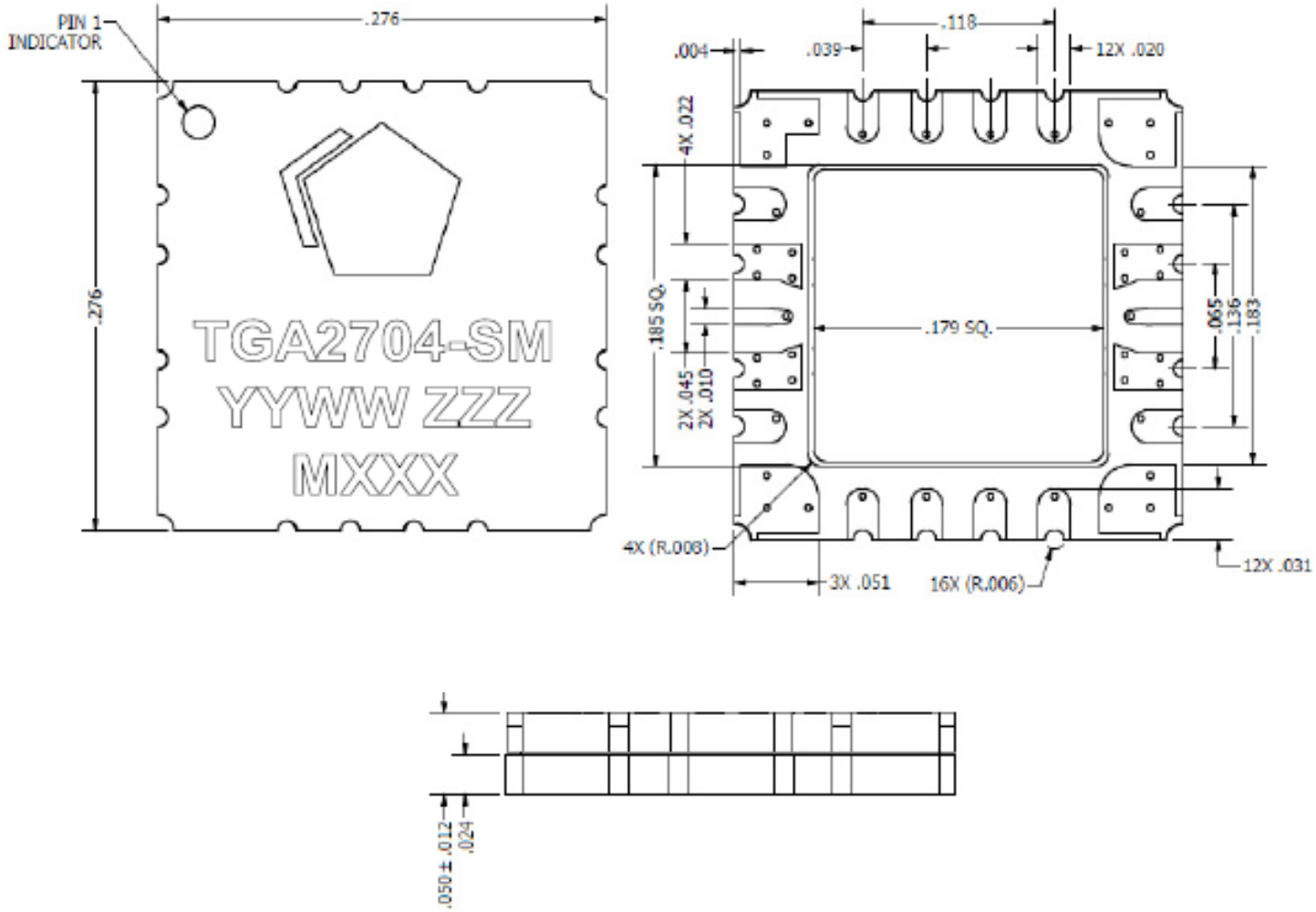
Bill of Materials

Reference Des.	Value	Description	Manuf.	Part Number
X1 – X3, X23 – X25	1 uF	CAP, 1uF, ±20%, 16V, X5R, 0402	Qorvo	
X10 – X12, X14 – X16	100 pF	CAP, 100pF, ±10%, 50V, X7R, 0402	Various	
X5 – X7, X19 – X21	15 Ω	RES, 15 ohm, 1/10W, ±5%, 0402	Various	
X9, X18	0 Ω	RES, 0 ohm, Jumper, 1/10W, ±1%, 0402	Various	

Pin Description

Pad No.	Label	Description
1 – 3, 5 – 7, 12 – 14, 16 – 18	GND	Ground. Must be grounded on PCB
11, 19	GND	Ground. Recommended to ground on PCB
4	RF_{IN}	RF input, matched to 50Ω, DC blocked
8	V_G	Gate voltage. External bypassing required; refer to page 8 for recommendation
9	V_{D1}	Drain 1 voltage. External bypassing required; refer to page 8 for recommendation
10	V_{D2}	Drain 2 voltage. External bypassing required; refer to page 8 for recommendation
15	RF_{OUT}	RF output, matched to 50Ω, DC blocked
20	V_{D2}	Drain 2 voltage. External bypassing required; refer to page 8 for recommendation
21	V_{D1}	Drain 1 voltage. External bypassing required; refer to page 8 for recommendation
22	V_G	Gate voltage. External bypassing required; refer to page 8 for recommendation
	GND	Backside paddle. Multiple conductive filled vias should be employed to minimize inductance and thermal resistance; see Mounting Configuration on page 12 for suggested footprint.

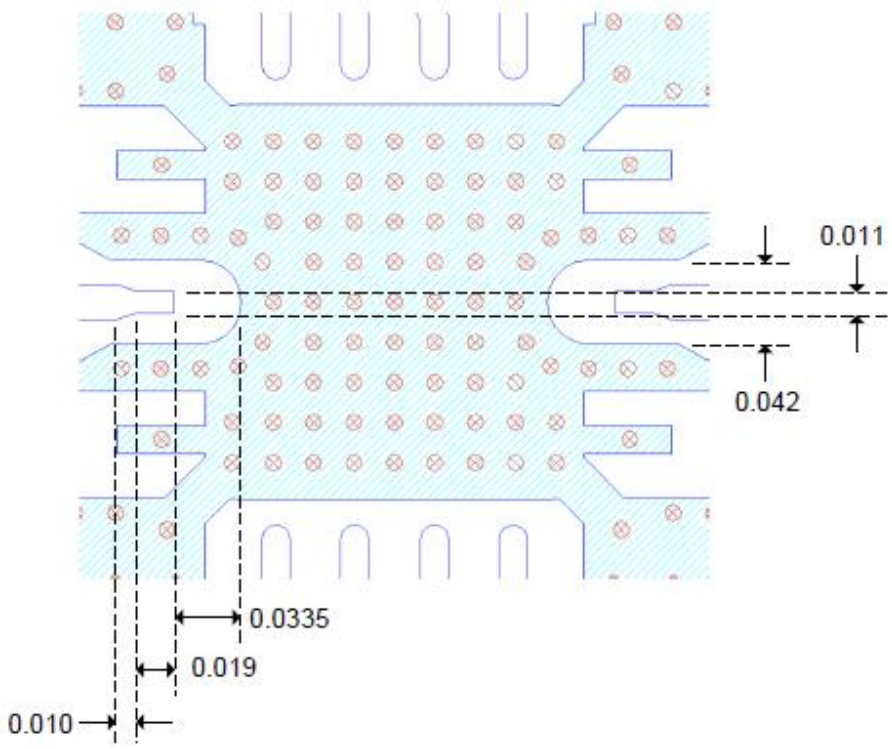
Mechanical Dimensions and Marking



All dimensions in inches and are +/- 0.006 in unless otherwise noted.
Marking:

YYWW	assembly lot start year YY, week WW
ZZZ	part serial number
MXXX	batch ID

PCB Mounting Pattern



Notes:

1. All dimensions are in inches. Angles are in degrees.
2. Ground vias are critical for the proper performance of this device. Vias should use a 0.008 in diameter drill
3. For best thermal performance, vias under the ground paddle should be copper filled.
4. The pad pattern shown has been developed and tested for optimized assembly at Qorvo. The PCB land pattern has been developed to accommodate lead and package tolerances. Since surface mount processes vary from company to company, careful process development is recommended

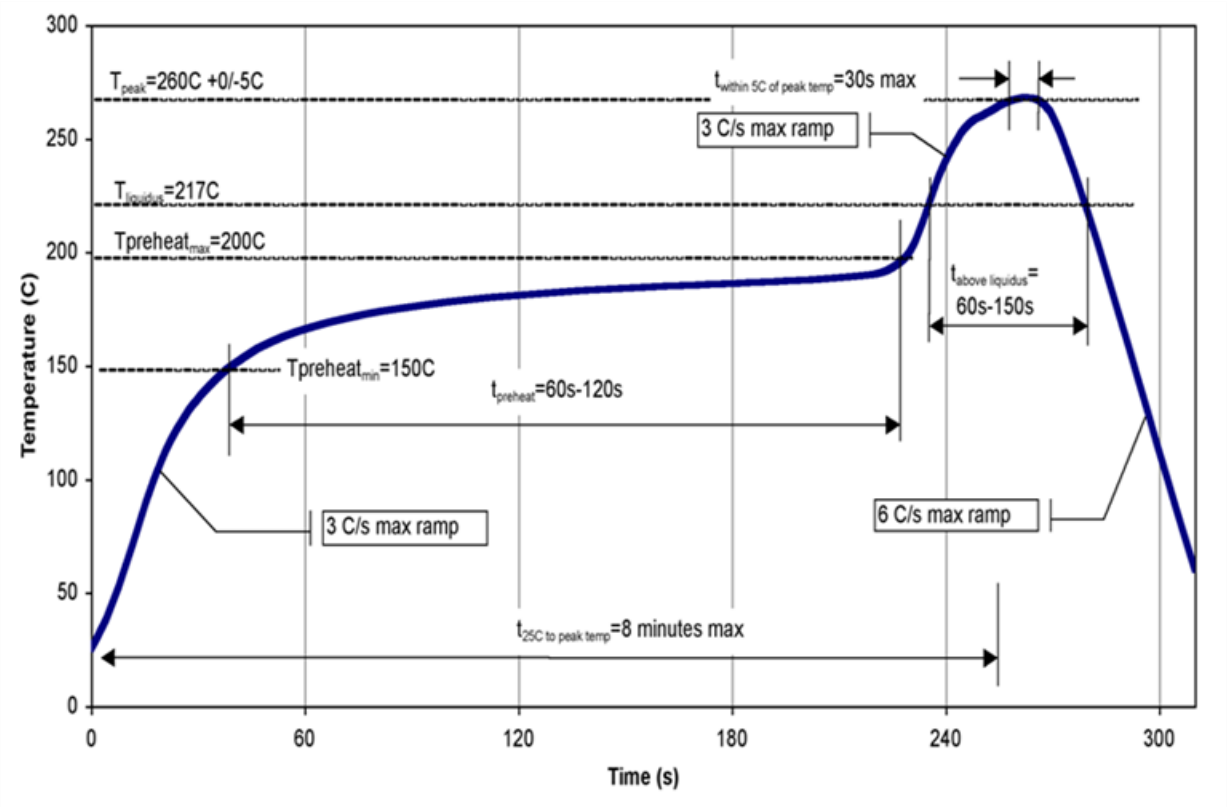
Assembly Notes

Compatible with lead-free soldering processes with 260°C peak reflow temperature.

This package is air-cavity and non-hermetic, and therefore cannot be subjected to aqueous washing. The use of no-clean solder to avoid washing after soldering is highly recommended.

Contact plating: Ni-Au

Solder rework not recommended



Recommended Soldering Temperature Profile

Handling Precautions

Parameter	Rating	Standard
ESD – Human Body Model (HBM)	1A	ANSI/ESD/JEDEC JS-001
ESD – Charged Device Model (CDM)	C3	ANSI/ESD/JEDEC JS-002
MSL – Moisture Sensitivity Level	3	IPC/JEDEC J-STD-020

Caution!
ESD-Sensitive Device

RoHS Compliance

This product is compliant with the 2011/65/EU RoHS directive (Restrictions on the Use of Certain Hazardous Substances in Electrical and Electronic Equipment), as amended by Directive 2015/863/EU.

This product also has the following attributes:

- Lead Free
- Halogen Free (Chlorine, Bromine)
- Antimony Free
- TBBP-A ($C_{15}H_{12}Br_4O_2$) Free
- SVHC Free

Contact Information

For the latest specifications, additional product information, worldwide sales and distribution locations:

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Web: www.qorvo.com

Email: customer.support@qorvo.com

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