Low Dropout Regulator, Wide Input Voltage, Low Iq, 300 mA

NCP718

The NCP718 is 300 mA LDO Linear Voltage Regulator. It is a very stable and accurate device with ultra−low quiescent current consumption (typ. 4 μA over the full temperature range) and a wide input voltage range (up to 24 V). The regulator incorporates several protection features such as Thermal Shutdown and Current Limiting.

Features

- Operating Input Voltage Range: 2.5 V to 24 V
- Fixed Voltage Options Available: 1.2 V to 5 V (upon request)
- Adjustable Voltage Option from 1.2 V to 5 V
- Ultra−Low Quiescent Current: typ. 4 μA over Temperature
- ±2% Accuracy Over Full Load, Line and Temperature Variations
- PSRR: 60 dB at 1 kHz
- Noise: typ. 36 μV_{RMS} from 100 Hz to 100 kHz
- Stable with Small 1 μF Ceramic Capacitor
- Soft−start to Reduce Inrush Current and Overshoots
- Thermal Shutdown and Current Limit Protection
- SOA Limiting for High Vin / High Iout – Static / Dynamic
- Active Discharge Option Available (upon request)
- Available in TSOT−23−5 and WDFN6 2x2 mm Packages
- These Devices are Pb−Free, Halogen Free/BFR Free and are RoHS Compliant

Typical Applications

- Wireless Chargers
- Portable Equipment
- Communication Systems

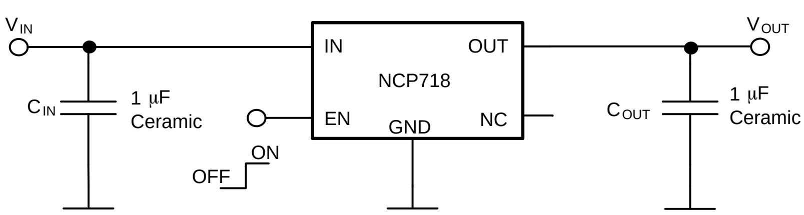

Figure 1. Typical Application Schematic

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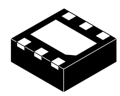
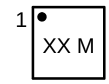
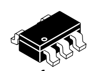
MARKING DIAGRAMS



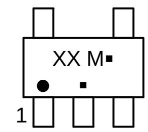
WDFN6
MT SUFFIX
CASE 511BR



XX = Specific Device Code
M = Date Code



TSOT−23−5
SN SUFFIX
CASE 419AE

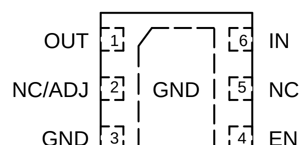


XX = Specific Device Code
M = Date Code*
▪ = Pb−Free Package

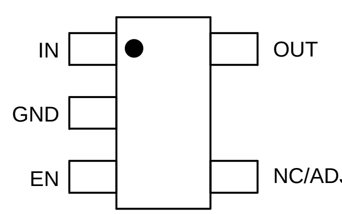
(Note: Microdot may be in either location)

*Date Code orientation and/or position may vary depending upon manufacturing location.

PIN CONNECTIONS



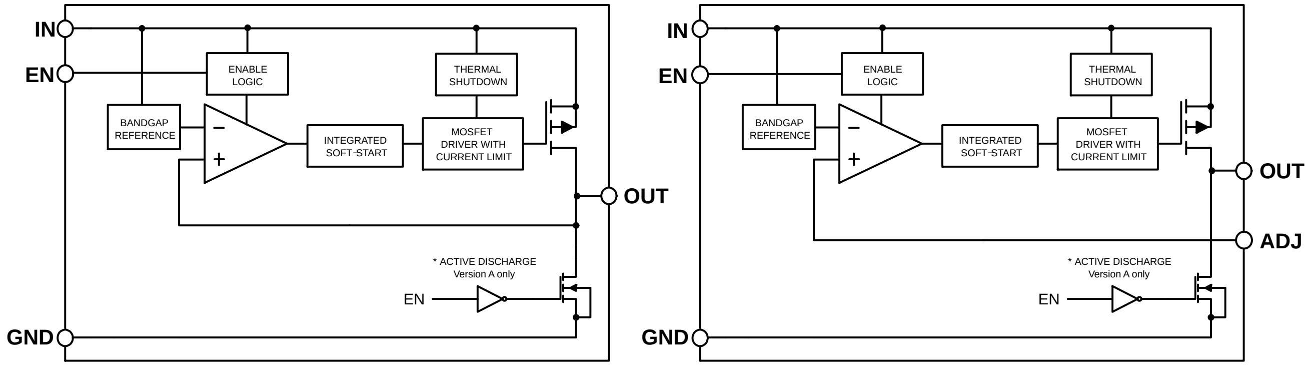
WDFN6 2x2 mm
(Top View)



TSOT−23−5
(Top View)

ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 7 of this data sheet.



Fixed Version　　　　Adjustable Version

Figure 2. Simplified Block Diagram

Table 1. PIN FUNCTION DESCRIPTION

Pin No. (WDFN6)	Pin No. (TSOT−23−5)	Pin Name	Description
6	1	IN	Input pin. A small capacitor is needed from this pin to ground to assure stability.
3, EXP	2	GND	Power supply ground.
4	3	EN	Enable pin. Driving this pin high turns on the regulator. Driving EN pin low puts the regulator into shutdown mode.
2	4	NC / ADJ	Fixed Version: No connection. This pin can be tied to ground to improve thermal dissipation or left disconnected. Adjustable Version: Feedback pin for set−up output voltage. Use resistor divider for voltage selection.
1	5	OUT	Regulated output voltage pin. A small 1 μF ceramic capacitor is needed from this pin to ground to assure stability.
5	−	N/C	No connection. This pin can be tied to ground to improve thermal dissipation or left disconnected.

Table 2. ABSOLUTE MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Input Voltage (Note 1)	V_{IN}	−0.3 to 24	V
Enable Voltage	V_{EN}	−0.3 to $V_{IN+0.3}$	V
Output Voltage	V_{OUT}	−0.3 to $V_{IN+0.3}$ (max. 6)	V
Output Short Circuit Duration	t_{SC}	Indefinite	s
Maximum Junction Temperature	$T_{J(MAX)}$	150	°C
Storage Temperature	T_{STG}	−55 to 150	°C
ESD Capability, Human Body Model (Note 2)	ESD_{HBM}	2000	V
ESD Capability, Charged Device Model (Note 2)	ESD_{CDM}	1000	V

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. Refer to ELECTRICAL CHARACTERISTICS and APPLICATION INFORMATION for Safe Operating Area.
2. This device series incorporates ESD protection and is tested by the following methods:
   ESD Human Body Model tested per AEC−Q100−002 (EIA/JESD22−A114)
   ESD Charged Device Model tested per EIA/JESD22−C101, Field Induced Charge Model.
   Latch up Current Maximum Rating tested per JEDEC standard: JESD78. Latch−up is not guaranteed on ENABLE pin.

Table 3. THERMAL CHARACTERISTICS

Rating	Symbol	Value	Unit
Thermal Characteristics, WDFN6, 2 mm x 2 mm Thermal Resistance, Junction−to−Air	$R_{\theta JA}$	65	°C/W
Thermal Characteristics, TSOT−23−5 Thermal Resistance, Junction−to−Air	$R_{\theta JA}$	235	°C/W

Table 4. ELECTRICAL CHARACTERISTICS -40°C ≤ T_J ≤ 125°C; V_{IN} = 2.5 V or (V_{OUT} + 1.0 V), whatever is greater; I_{OUT} = 1 mA, C_{IN} = C_{OUT} = 1 μF, unless otherwise noted. Typical values are at T_J = +25°C. (Note 3)

Parameter	Test Conditions		Symbol	Min	Typ	Max	Unit
Operating Input Voltage			V_{IN}	2.5		24	V
Output Voltage Accuracy (fixed versions)	−40°C ≤ T_J ≤ 125°C, V_{OUT} + 1 V < V_{IN} < 16 V, 0.1 mA < I_{OUT} < 300 mA (Note 5)	V_{OUT} < 1.8 V	V_{OUT}	−3%		+3%	V
		V_{OUT} ≥ 1.8 V		−2%		+2%	
Reference Voltage	−40°C ≤ T_J ≤ 125°C, V_{OUT} + 1 V < V_{IN} < 16 V		V_{ADJ}		1.2		V
Reference Voltage Accuracy	−40°C ≤ T_J ≤ 125°C, V_{OUT} + 1 V < V_{IN} < 16 V		V_{OUT}	−2%		+2%	V
Line Regulation	V_{OUT} + 1 V ≤ V_{IN} ≤ 16 V, Iout = 1 mA		Reg_{LINE}		10		mV
Load Regulation	I_{OUT} = 0.1 mA to 300 mA		Reg_{LOAD}		10		mV
Dropout Voltage (Package TSOT−23−5)	V_{DO} = V_{IN} – ($V_{OUT(NOM)}$ – 3%), I_{OUT} = 300 mA (Note 4)	2.1 V – 2.4 V	V_{DO}		480		mV
		2.5 V − 2.7 V			320	490	
		2.8 V − 3.2 V			295	465	
		3.3 V – 4.9 V			275	440	
		5 V			250	380	
Dropout Voltage (Package WDFN6)	V_{DO} = V_{IN} – ($V_{OUT(NOM)}$ – 3%), I_{OUT} = 300 mA (Note 4)	2.1 V – 2.4 V	V_{DO}		490		mV
		2.5 V − 2.7 V			335	505	
		2.8 V − 3.2 V			305	475	
		3.3 V – 4.9 V			285	450	
		5 V			260	395	
Maximum Output Current	V_{IN} = V_{OUT} + 1 V (Note 5)		I_{LIM}	300		800	mA
Disable Current	V_{EN} = 0 V, V_{IN} = 5 V		I_{DIS}		0.1	1.0	μA
Quiescent Current	I_{OUT} = 0 mA, −40°C ≤ T_J ≤ 125°C		I_Q		4.0	8.0	μA
Ground current	I_{OUT} = 10 mA		I_{GND}		50		μA
	I_{OUT} = 300 mA				300		
Power Supply Rejection Ratio	V_{IN} = 3.5 V + 100 mVpp, V_{OUT} = 2.5 V, I_{OUT} = 1 mA, Cout = 1 μF	f = 1 kHz	PSRR		60		dB
Output Noise Voltage	V_{OUT} = 1.2 V, I_{OUT} = 10 mA, f = 100 Hz to 100 kHz		V_N		36		μV_{rms}
Enable Input Threshold Voltage	Voltage increasing		V_{EN_HI}	1.2	–	–	V
	Voltage decreasing		V_{EN_LO}	–	–	0.4	
ADJ Pin Current	V_{IN} = V_{OUT} + 1 V		I_{ADJ}		0.1	1.0	μA
EN Pin Current	V_{EN} = 5.5 V		I_{EN}		100		nA
Active Output Discharge Resistance	V_{IN} = 5.5 V, V_{EN} = 0 V		Rdis		100		Ω
Thermal Shutdown Temperature (Note 6)	Temperature increasing from T_J = +25°C		T_{SD}		165		°C
Thermal Shutdown Hysteresis (Note 6)	Temperature falling from T_{SD}		T_{SDH}	–	25	–	°C

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.
3. Performance guaranteed over the indicated operating temperature range by design and/or characterization production tested at T_J = T_A = 25°C. Low duty cycle pulse techniques are used during testing to maintain the junction temperature as close to ambient as possible.
4. Voltage dropout for voltage variants below 2.1 V is given by minimum input voltage 2.5 V.
5. Respect SOA
6. Guaranteed by design and characterization.

TYPICAL CHARACTERISTICS

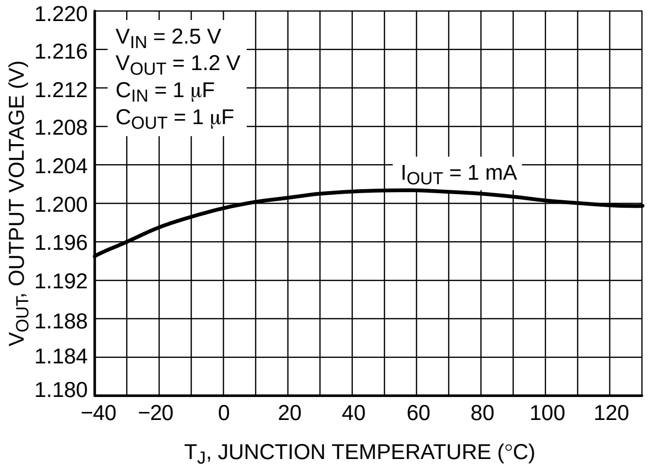


Figure 3. Output Voltage vs. Temperature − V_{OUT} = 1.2 V

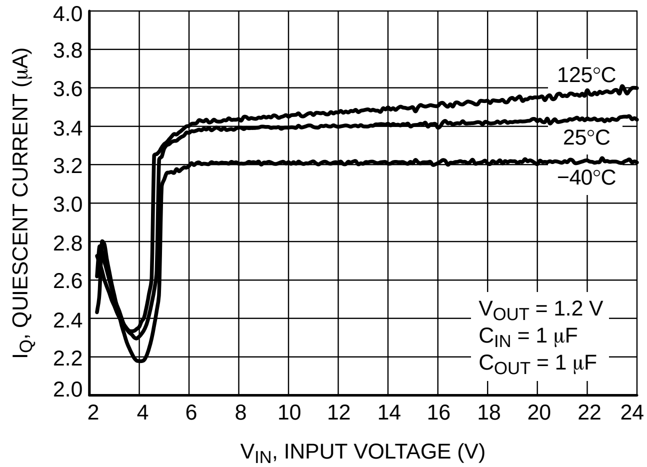


Figure 4. Quiescent Current vs. Input Voltage

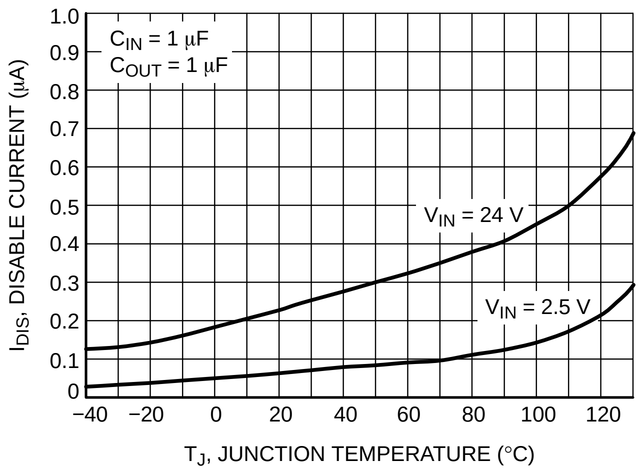


Figure 5. Disable Current vs. Temperature

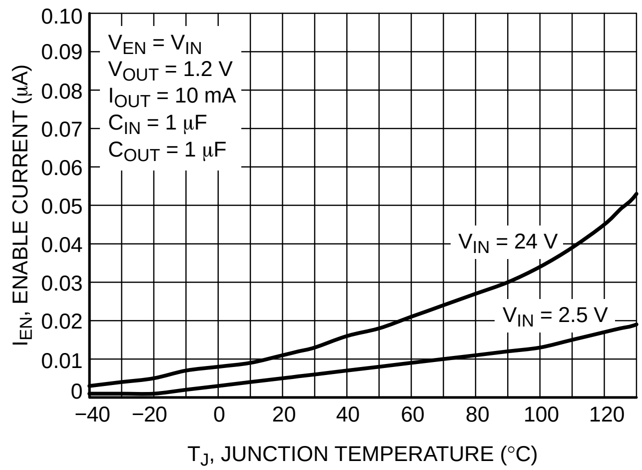


Figure 6. Current to Enable Pin vs. Temperature

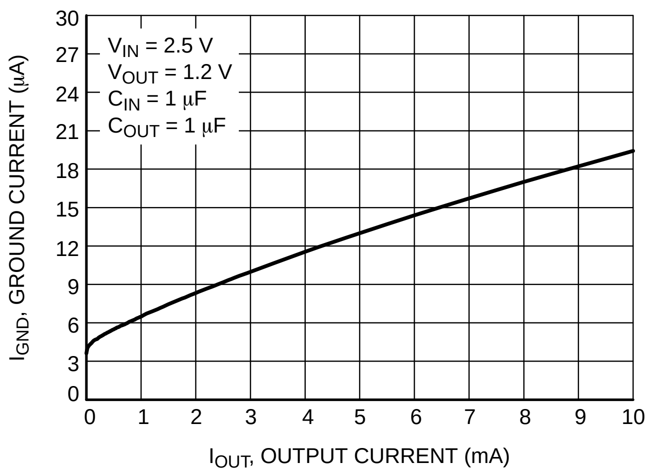


Figure 7. Ground Current vs. Output Current − V_{OUT} = 1.2 V

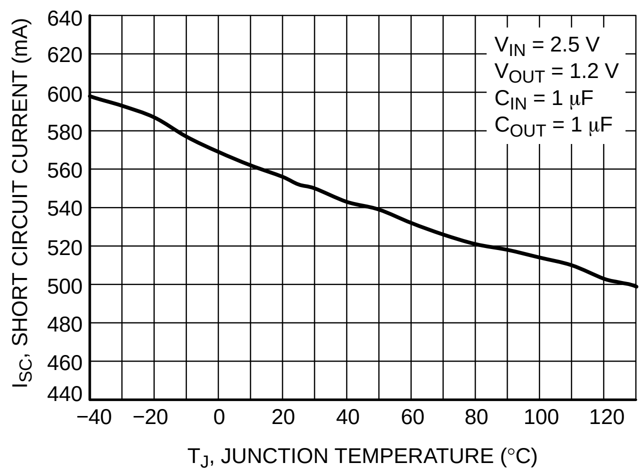


Figure 8. Short Circuit Current vs. Temperature

TYPICAL CHARACTERISTICS

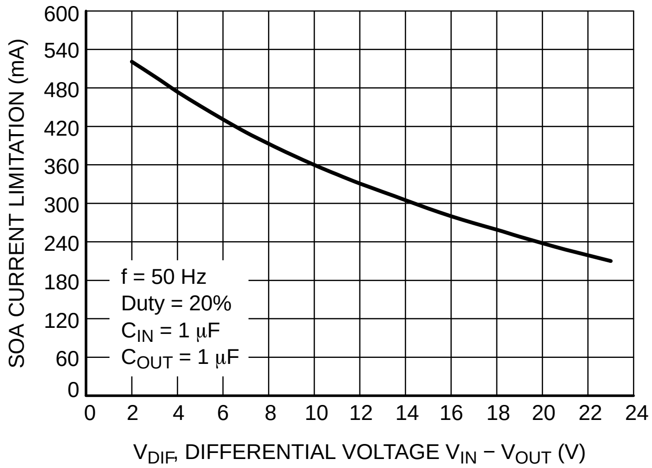


Figure 9. SOA Current Limit vs. Differential Voltage

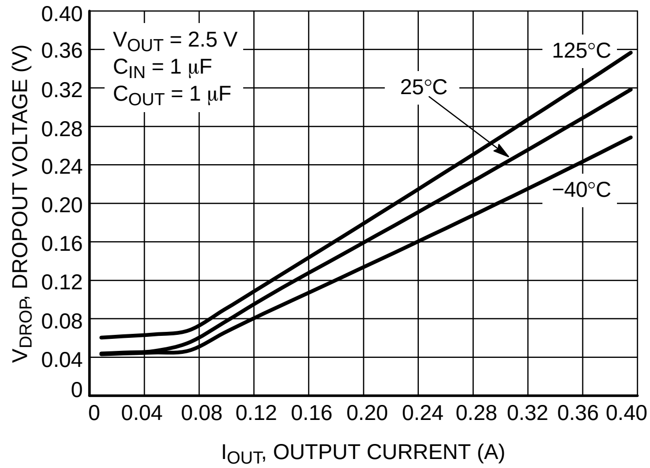


Figure 10. Dropout Voltage vs. Output Current − V_{OUT} = 2.5 V

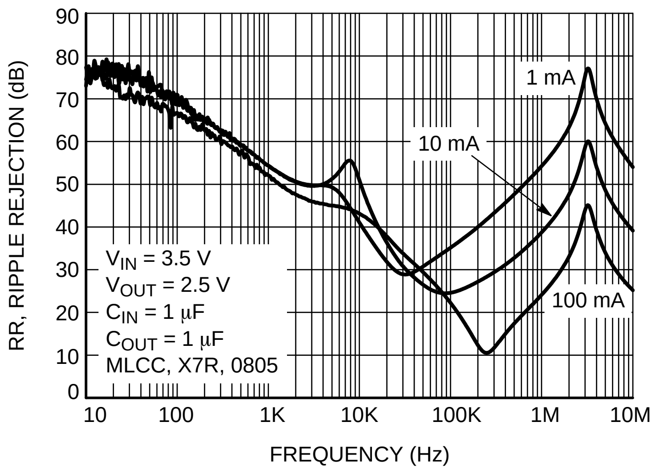


Figure 11. Power Supply Rejection Ratio vs. Current, V_{IN} = 3.5 V, C_{OUT} = 1 µF

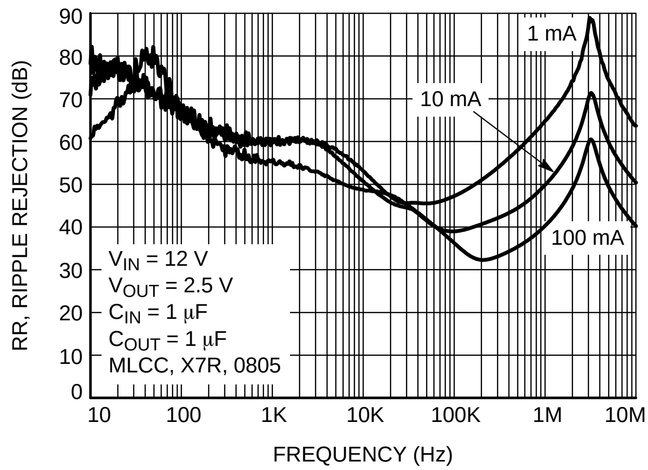


Figure 12. Power Supply Rejection Ratio vs. Current, V_{IN} = 12 V, C_{OUT} = 1 µF

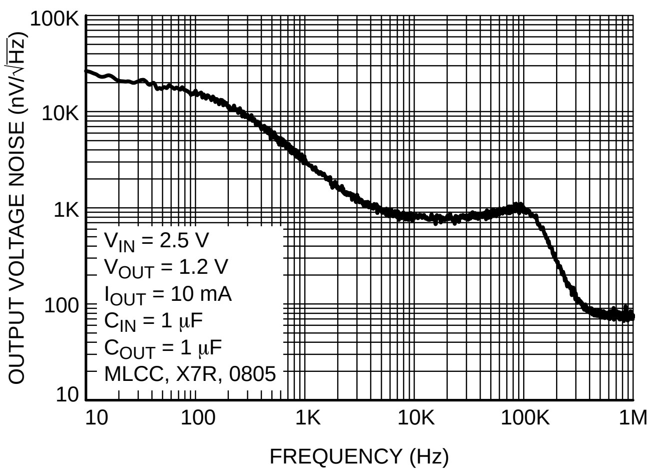


Figure 13. Output Voltage Noise Spectral Density for V_{OUT} = 1.2 V, I_{OUT} = 10 mA, C_{OUT} = 1 µF

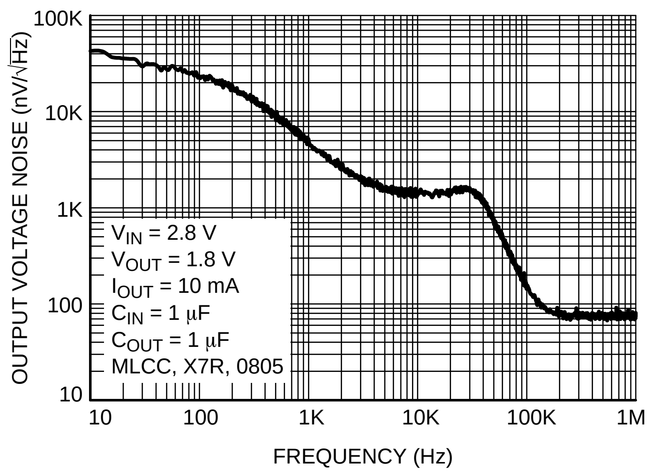


Figure 14. Output Voltage Noise Spectral Density for V_{OUT} = 1.8 V, I_{OUT} = 10 mA, C_{OUT} = 1 µF

APPLICATIONS INFORMATION

The NCP718 is the member of new family of Wide Input Voltage Range Low Dropout Regulators which delivers Ultra Low Ground Current consumption, Good Noise and Power Supply Rejection Ratio Performance. The NCP718 incorporates EN pin and soft−start feature for simple controlling by microprocessor or logic.

Input Decoupling (C_{IN})

It is recommended to connect at least 1 μF ceramic X5R or X7R capacitor between IN and GND pin of the device. This capacitor will provide a low impedance path for any unwanted AC signals or noise superimposed onto constant input voltage. The good input capacitor will limit the influence of input trace inductances and source resistance during sudden load current changes.

Higher capacitance and lower ESR capacitors will improve the overall line transient response.

Output Decoupling (C_{OUT})

The NCP718 does not require a minimum Equivalent Series Resistance (ESR) for the output capacitor. The device is designed to be stable with standard ceramics capacitors with values of 1 μF or greater. The X5R and X7R types have the lowest capacitance variations over temperature thus they are recommended.

Power Dissipation and Heat Sinking

The maximum power dissipation supported by the device is dependent upon board design and layout. Mounting pad configuration on the PCB, the board material, and the ambient temperature affect the rate of junction temperature rise for the part. For reliable operation junction temperature should be limited to +125°C.

The maximum power dissipation the NCP718 can handle is given by:

$$P_{D(MAX)} = \frac{\left[T_{J(MAX)} - T_A\right]}{R_{\theta JA}} \quad \text{(eq. 1)}$$

The power dissipated by the NCP718 for given application conditions can be calculated from the following equations:

$$P_D \approx V_{IN}\left(I_{GND}(I_{OUT})\right) + I_{OUT}\left(V_{IN} - V_{OUT}\right) \quad \text{(eq. 2)}$$

or

$$V_{IN(MAX)} \approx \frac{P_{D(MAX)} + \left(V_{OUT} \times I_{OUT}\right)}{I_{OUT} + I_{GND}} \quad \text{(eq. 3)}$$

Hints

V_{IN} and GND printed circuit board traces should be as wide as possible. When the impedance of these traces is high, there is a chance to pick up noise or cause the regulator to malfunction. Place external components, especially the output capacitor, as close as possible to the NCP718, and make traces as short as possible.

ADJUSTABLE VERSION

The output voltage can be set by using a resistor divider as shown in Figure 15 with a range of 1.2 V to 5 V. The appropriate resistor divider can be found by solving the equation below, while V_{REF} = 1.2 V

$$V_{OUT} = V_{REF} \cdot \frac{(R1 + R2)}{R1} = V_{REF} \cdot \left(1 + \frac{R2}{R1}\right) \quad \text{(eq. 4)}$$

Value of R1 and R2 is recommended to keep below 100 kΩ for R1 and below 1 MΩ for R2 to avoid influence of current I_{ADJ} variation over temperature range.

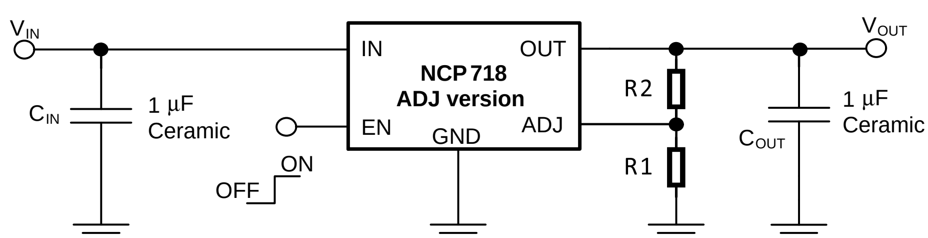


Figure 15. Adjustable Version Connection Schematic

Please note that output noise is amplified by V_{OUT} / V_{ADJ} ratio. For simplified calculation, output noise is equal to 30 μV_{RMS} * V_{OUT}. Do not operate the device at output voltage about 5.2 V, as device can be damaged.

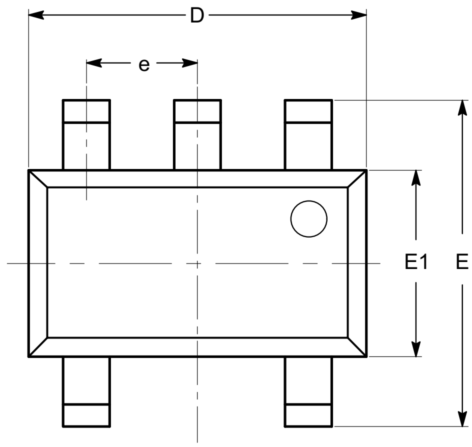
ORDERING INFORMATION

Device Part No.	Voltage Option	Marking	Option	Package	Shipping†
NCP718AMTADJTBG	Adj.	GA	With Active Output Discharge	WDFN6 (Pb−Free)	3000 / Tape & Reel
NCP718AMT120TBG	1.2 V	GN			
NCP718AMT180TBG	1.8 V	GP			
NCP718AMT250TBG	2.5 V	GD			
NCP718AMT300TBG	3.0 V	GQ			
NCP718AMT330TBG	3.3 V	GR			
NCP718AMT500TBG	5.0 V	GM			
NCP718BMTADJTBG	Adj.	GC	Without Active Output Discharge		
NCP718BMT180TBG	1.8 V	GU			
NCP718BMT300TBG	3.0 V	GV			
NCP718BMT330TBG	3.3 V	GW			
NCP718BMT500TBG	5.0 V	GE			
NCP718ASNADJT1G	Adj.	GAA	With Active Output Discharge	TSOT−23−5 (Pb−Free)	3000 / Tape & Reel
NCP718ASN120T1G	1.2 V	GAE			
NCP718ASN150T1G	1.5 V	GAF			
NCP718ASN180T1G	1.8 V	GAD			
NCP718ASN250T1G	2.5 V	GAG			
NCP718ASN300T1G	3.0 V	GAH			
NCP718ASN330T1G	3.3 V	GAJ			
NCP718ASN500T1G	5.0 V	GAK			
NCP718BSNADJT1G	Adj.	GAC	Without Active Output Discharge		
NCP718BSN120T1G	1.2 V	GCA			
NCP718BSN150T1G	1.5 V	GCC			
NCP718BSN180T1G	1.8 V	GCD			
NCP718BSN250T1G	2.5 V	GCF			
NCP718BSN300T1G	3.0 V	GCG			
NCP718BSN330T1G	3.3 V	GCH			
NCP718BSN500T1G	5.0 V	GCE			

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

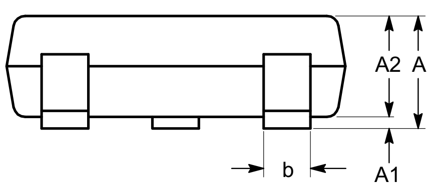
TSOT−23, 5 LEAD
CASE 419AE−01
ISSUE O

DATE 19 DEC 2008

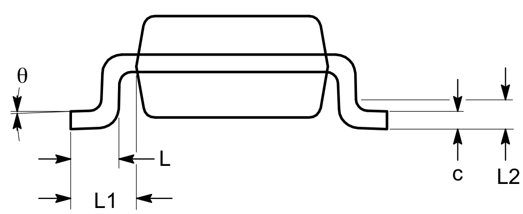


TOP VIEW

SYMBOL	MIN	NOM	MAX
A			1.00
A1	0.01	0.05	0.10
A2	0.80	0.87	0.90
b	0.30		0.45
c	0.12	0.15	0.20
D		2.90 BSC	
E		2.80 BSC	
E1		1.60 BSC	
e		0.95 TYP	
L	0.30	0.40	0.50
L1		0.60 REF	
L2		0.25 BSC	
θ	0º		8º



SIDE VIEW



END VIEW

Notes:

(1) All dimensions are in millimeters. Angles in degrees.
(2) Complies with JEDEC MO-193.

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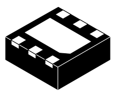
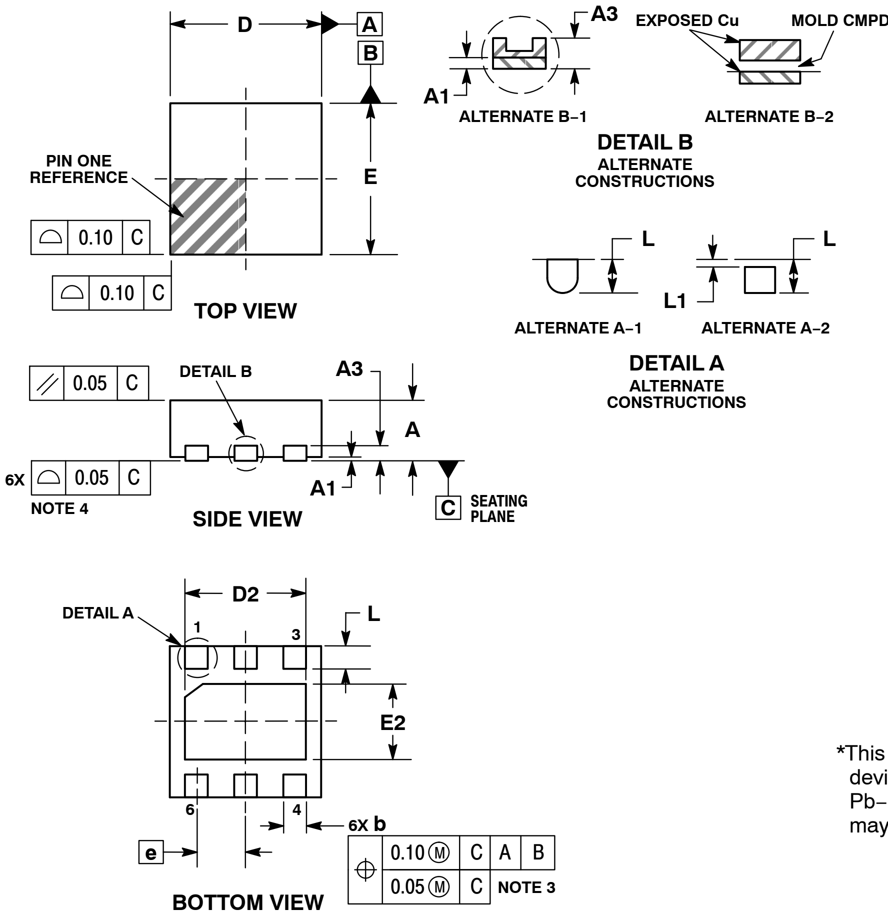
DESCRIPTION:	TSOT−23, 5 LEAD	PAGE 1 OF 1

WDFN6 2x2, 0.65P
CASE 511BR
ISSUE B

DATE 19 JAN 2016



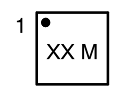
SCALE 4:1



NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. DIMENSION b APPLIES TO PLATED TERMINAL AND IS MEASURED BETWEEN 0.15 AND 0.25 mm FROM THE TERMINAL TIP.
4. COPLANARITY APPLIES TO THE EXPOSED PAD AS WELL AS THE TERMINALS.
5. FOR DEVICES CONTAINING WETTABLE FLANK OPTION, DETAIL A ALTERNATE CONSTRUCTION A−2 AND DETAIL B ALTERNATE CONSTRUCTION B−2 ARE NOT APPLICABLE.

	MILLIMETERS	
DIM	MIN	MAX
A	0.70	0.80
A1	0.00	0.05
A3	0.20 REF	
b	0.25	0.35
D	2.00 BSC	
D2	1.50	1.70
E	2.00 BSC	
E2	0.90	1.10
e	0.65 BSC	
L	0.20	0.40
L1	---	0.15

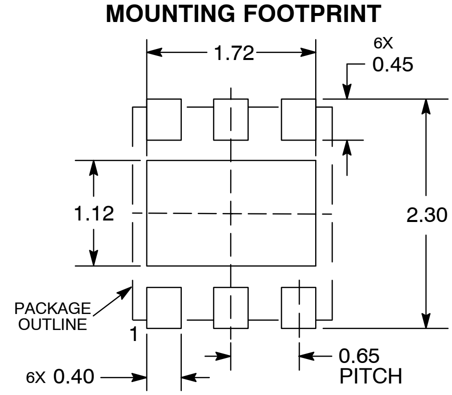
GENERIC MARKING DIAGRAM*



XX = Specific Device Code
M = Date Code

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, “G” or microdot “ ▪”, may or may not be present.

RECOMMENDED MOUNTING FOOTPRINT



DIMENSIONS: MILLIMETERS

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DESCRIPTION:	WDFN6 2X2, 0.65P	PAGE 1 OF 1

PUBLICATION ORDERING INFORMATION

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