

74LVC1G53-Q100

2-channel analog multiplexer/demultiplexer

Rev. 4 — 20 July 2021

Product data sheet

1. General description

The 74LVC1G53-Q100 is a single-pole double-throw analog switch with a digital select input (S), two independent inputs/outputs (Y0 and Y1), a common input/output (Z) and a digital enable input (E). When \bar{E} is HIGH, the switch is turned off. Control inputs can be driven from either 3.3 V or 5 V devices. This feature allows the use of these devices as translators in mixed 3.3 V and 5 V environments.

Schmitt-trigger action at control inputs makes the circuit tolerant of slower input rise and fall times.

This product has been qualified to the Automotive Electronics Council (AEC) standard Q100 (Grade 1) and is suitable for use in automotive applications.

2. Features and benefits

- Automotive product qualification in accordance with AEC-Q100 (Grade 1)
 - Specified from -40 °C to +85 °C and from -40 °C to +125 °C
- Wide supply voltage range from 1.65 V to 5.5 V
- Very low ON resistance:
 - 7.5 Ω (typical) at $V_{CC} = 2.7$ V
 - 6.5 Ω (typical) at $V_{CC} = 3.3$ V
 - 6 Ω (typical) at $V_{CC} = 5$ V
- Switch current capability of 32 mA
- High noise immunity
- CMOS low power consumption
- TTL interface compatibility at 3.3 V
- Latch-up performance meets requirements of JESD 78 Class I
- ESD protection:
 - MIL-STD-883, method 3015 exceeds 2000 V
 - HBM JESD22-A114F exceeds 2000 V
 - MM JESD22-A115-A exceeds 200 V (C = 200 pF, R = 0 Ω)

3. Ordering information

Table 1. Ordering information

Type number	Package			
	Temperature range	Name	Description	Version
74LVC1G53DP-Q100	-40 °C to +125 °C	TSSOP8	plastic thin shrink small outline package; 8 leads; body width 3 mm; lead length 0.5 mm	SOT505-2
74LVC1G53DC-Q100	-40 °C to +125 °C	VSSOP8	plastic very thin shrink small outline package; 8 leads; body width 2.3 mm	SOT765-1

4. Marking

Table 2. Marking codes

Type number	Marking code ^[1]
74LVC1G53DC-Q100	V53
74LVC1G53DP-Q100	V53

[1] The pin 1 indicator is located on the lower left corner of the device, below the marking code.

5. Functional diagram

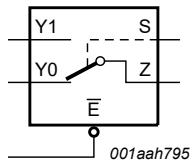


Fig. 1. Logic symbol

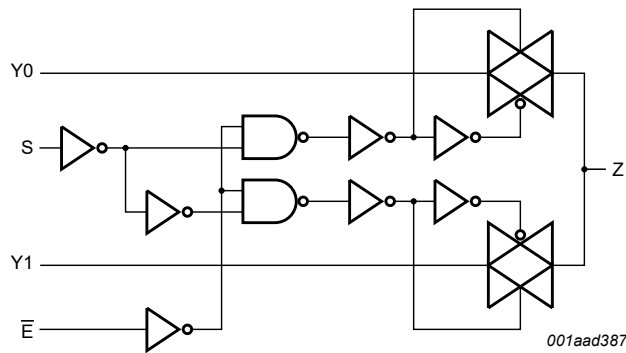


Fig. 2. Logic diagram

6. Pinning information

6.1. Pinning

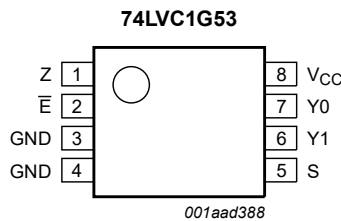


Fig. 3. Pin configuration SOT505-2 (TSSOP8) and SOT765-1 (VSSOP8)

6.2. Pin description

Table 3. Pin description

Symbol	Pin	Description
Z	1	common output or input
\bar{E}	2	enable input (active LOW)
GND	3	ground (0 V)
GND	4	ground (0 V)
S	5	select input
Y1	6	independent input or output
Y0	7	independent input or output
V _{CC}	8	supply voltage

7. Functional description

Table 4. Function table

H = HIGH voltage level; L = LOW voltage level; X = don't care; Z = high-impedance OFF-state.

Input		Channel on
S	\bar{E}	
L	L	Y0 to Z or Z to Y0
H	L	Y1 to Z or Z to Y1
X	H	Z (switch off)

8. Limiting values

Table 5. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134). Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	Min	Max	Unit
V _{CC}	supply voltage		-0.5	+6.5	V
V _I	input voltage	[1]	-0.5	+6.5	V
I _{IK}	input clamping current	V _I < -0.5 V or V _I > V _{CC} + 0.5 V	-50	-	mA
I _{SK}	switch clamping current	V _I < -0.5 V or V _I > V _{CC} + 0.5 V	-	±50	mA
V _{SW}	switch voltage	enable and disable mode [2]	-0.5	V _{CC} + 0.5	V
I _{SW}	switch current	V _{SW} > -0.5 V or V _{SW} < V _{CC} + 0.5 V	-	±50	mA
I _{CC}	supply current		-	100	mA
I _{GND}	ground current		-100	-	mA
T _{stg}	storage temperature		-65	+150	°C
P _{tot}	total power dissipation	T _{amb} = -40 °C to +125 °C [3]	-	250	mW

[1] The minimum input voltage rating may be exceeded if the input current rating is observed.

[2] The minimum and maximum switch voltage ratings may be exceeded if the switch clamping current rating is observed.

[3] For SOT505-2 (TSSOP8) package: P_{tot} derates linearly with 4.6 mW/K above 96 °C.

For SOT765-1 (VSSOP8) package: P_{tot} derates linearly with 4.9 mW/K above 99 °C.

9. Recommended operating conditions

Table 6. Operating conditions

Symbol	Parameter	Conditions	Min	Max	Unit
V_{CC}	supply voltage		1.65	5.5	V
V_I	input voltage		0	5.5	V
V_{SW}	switch voltage	enable and disable mode [1]	0	V_{CC}	V
T_{amb}	ambient temperature		-40	+125	°C
$\Delta t/\Delta V$	input transition rise and fall rate	$V_{CC} = 1.65\text{ V to }2.7\text{ V}$ [2]	-	20	ns/V
		$V_{CC} = 2.7\text{ V to }5.5\text{ V}$ [2]	-	10	ns/V

- [1] To avoid sinking GND current from terminal Z when switch current flows in terminal Yn, the voltage drop across the bidirectional switch must not exceed 0.4 V. If the switch current flows into terminal Z, no GND current will flow from terminal Yn. In this case, there is no limit for the voltage drop across the switch.
- [2] Applies to control signal levels.

10. Static characteristics

Table 7. Static characteristics

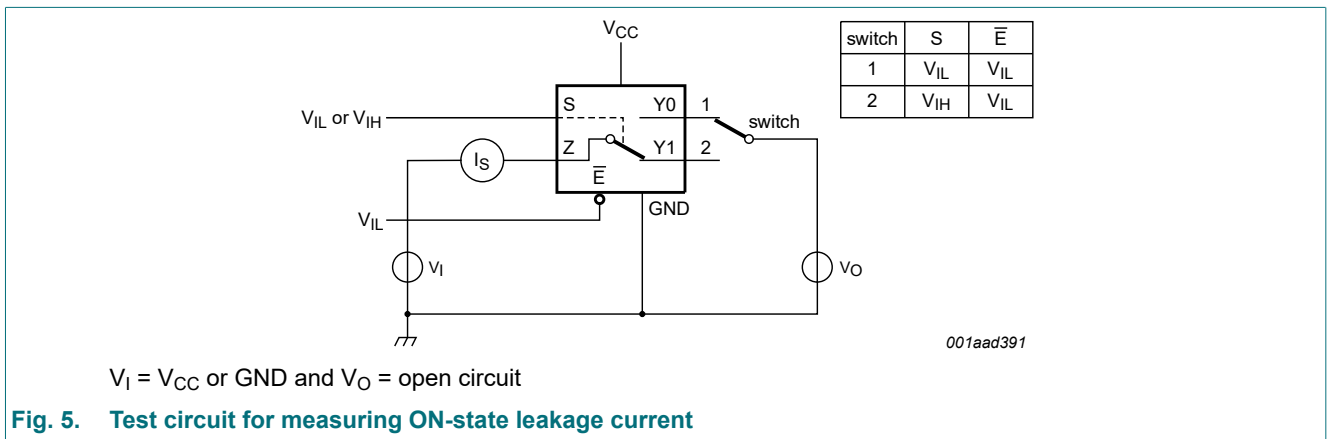
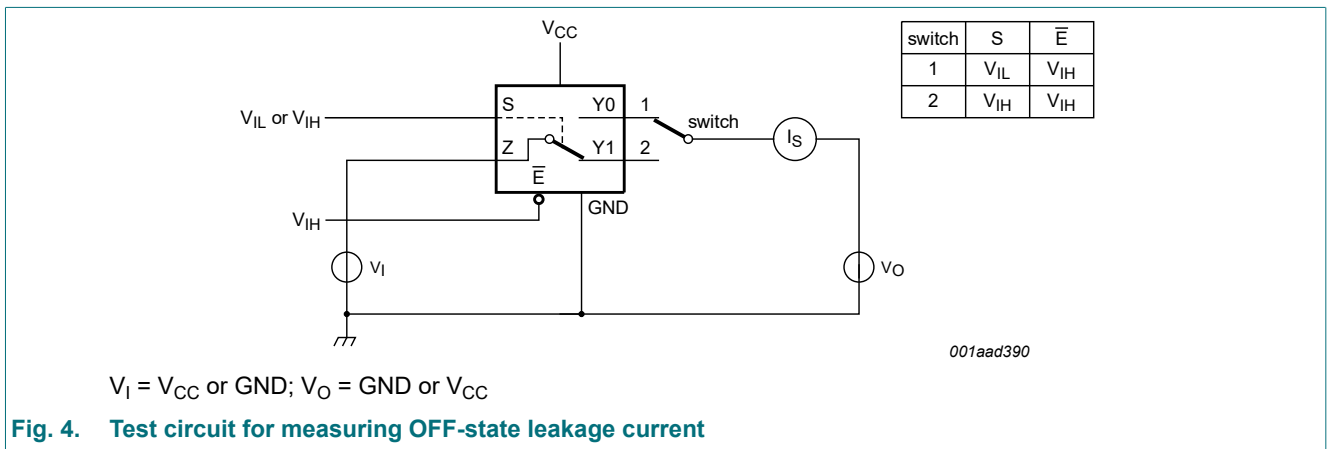
At recommended operating conditions; voltages are referenced to GND (ground 0 V).

Symbol	Parameter	Conditions	-40 °C to +85 °C			-40 °C to +125 °C		Unit
			Min	Typ[1]	Max	Min	Max	
V_{IH}	HIGH-level input voltage	$V_{CC} = 1.65\text{ V to }1.95\text{ V}$	$0.65V_{CC}$	-	-	$0.65V_{CC}$	-	V
		$V_{CC} = 2.3\text{ V to }2.7\text{ V}$	1.7	-	-	1.7	-	V
		$V_{CC} = 3\text{ V to }3.6\text{ V}$	2.0	-	-	2.0	-	V
		$V_{CC} = 4.5\text{ V to }5.5\text{ V}$	$0.7V_{CC}$	-	-	$0.7V_{CC}$	-	V
V_{IL}	LOW-level input voltage	$V_{CC} = 1.65\text{ V to }1.95\text{ V}$	-	-	$0.35V_{CC}$	-	$0.35V_{CC}$	V
		$V_{CC} = 2.3\text{ V to }2.7\text{ V}$	-	-	0.7	-	0.7	V
		$V_{CC} = 3\text{ V to }3.6\text{ V}$	-	-	0.8	-	0.8	V
		$V_{CC} = 4.5\text{ V to }5.5\text{ V}$	-	-	$0.3V_{CC}$	-	$0.3V_{CC}$	V
I_I	input leakage current	pin S and pin \bar{E} ; $V_I = 5.5\text{ V or GND}$; $V_{CC} = 0\text{ V to }5.5\text{ V}$ [2]	-	± 0.1	± 1	-	± 1	μA
$I_{S(OFF)}$	OFF-state leakage current	$V_{CC} = 5.5\text{ V}$; see Fig. 4 [2]	-	± 0.1	± 0.2	-	± 0.5	μA
$I_{S(ON)}$	ON-state leakage current	$V_{CC} = 5.5\text{ V}$; see Fig. 5 [2]	-	± 0.1	± 1	-	± 2	μA
I_{CC}	supply current	$V_I = 5.5\text{ V or GND}$; $V_{SW} = \text{GND or }V_{CC}$; $V_{CC} = 1.65\text{ V to }5.5\text{ V}$ [2]	-	0.1	4	-	4	μA
ΔI_{CC}	additional supply current	pin S and pin \bar{E} ; $V_I = V_{CC} - 0.6\text{ V}$; $V_{SW} = \text{GND or }V_{CC}$; $V_{CC} = 5.5\text{ V}$ [2]	-	5	500	-	500	μA

Symbol	Parameter	Conditions	-40 °C to +85 °C			-40 °C to +125 °C		Unit
			Min	Typ[1]	Max	Min	Max	
C_I	input capacitance		-	2.5	-	-	-	pF
$C_{S(OFF)}$	OFF-state capacitance		-	6.0	-	-	-	pF
$C_{S(ON)}$	ON-state capacitance		-	18	-	-	-	pF

- [1] Typical values are measured at $T_{amb} = 25\text{ °C}$.
- [2] These typical values are measured at $V_{CC} = 3.3\text{ V}$.

10.1. Test circuits



10.2. ON resistance

Table 8. ON resistance

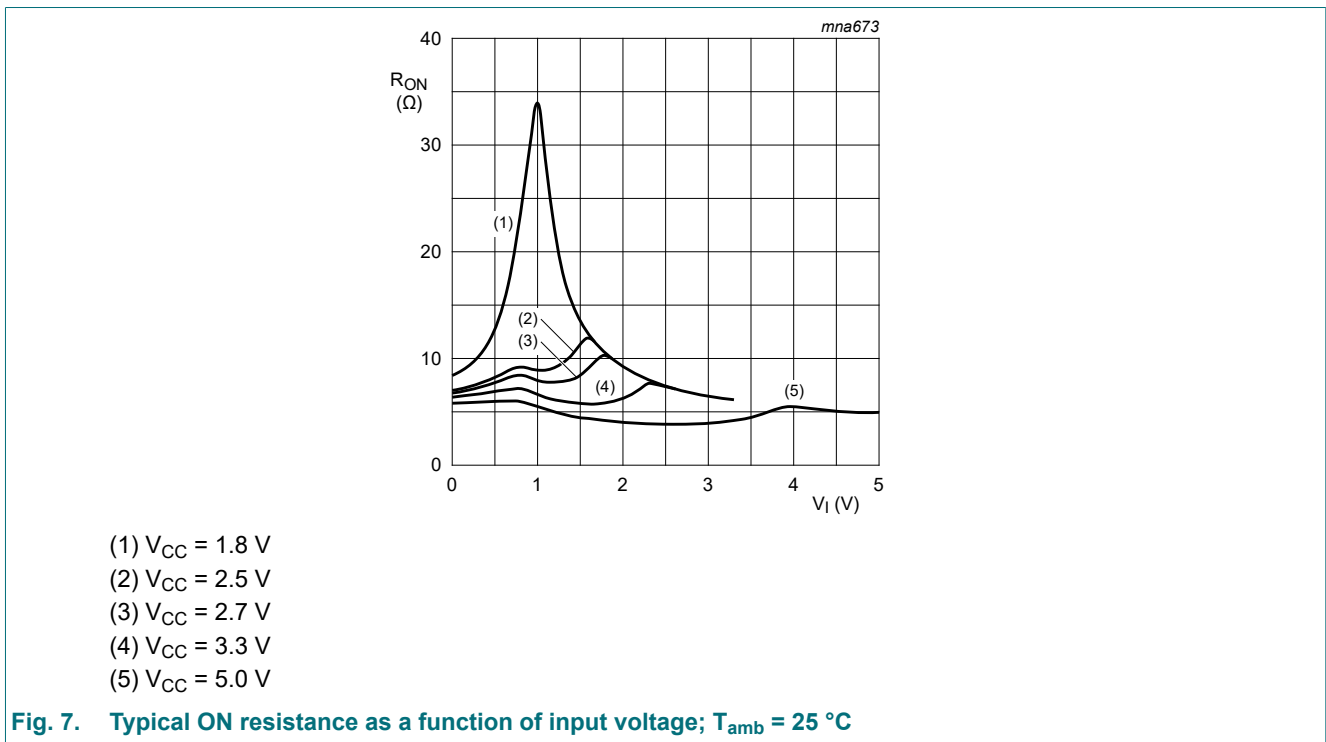
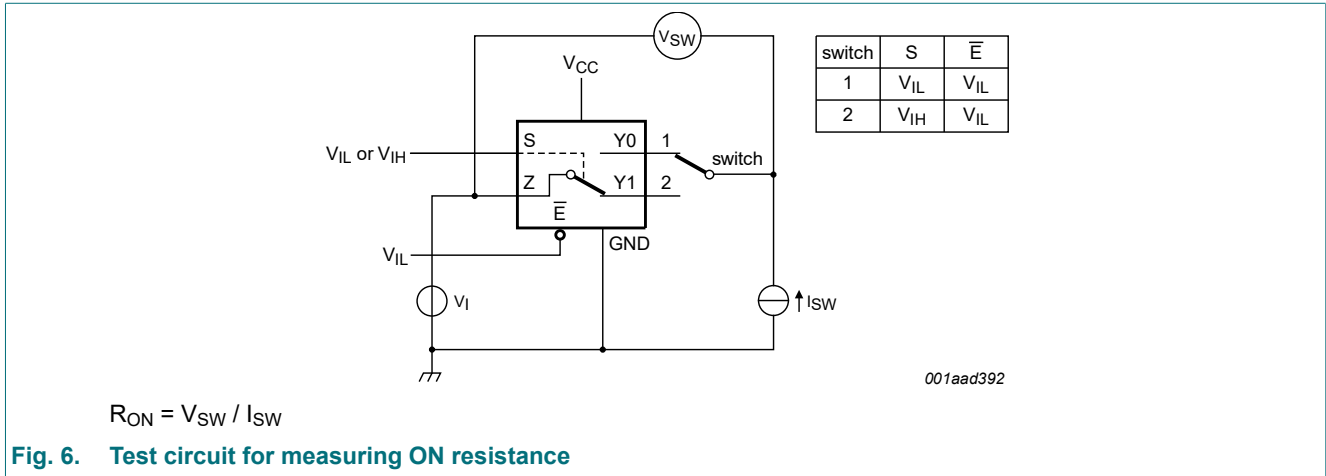
At recommended operating conditions; voltages are referenced to GND (ground 0 V); for graphs see [Fig. 7](#) to [Fig. 12](#).

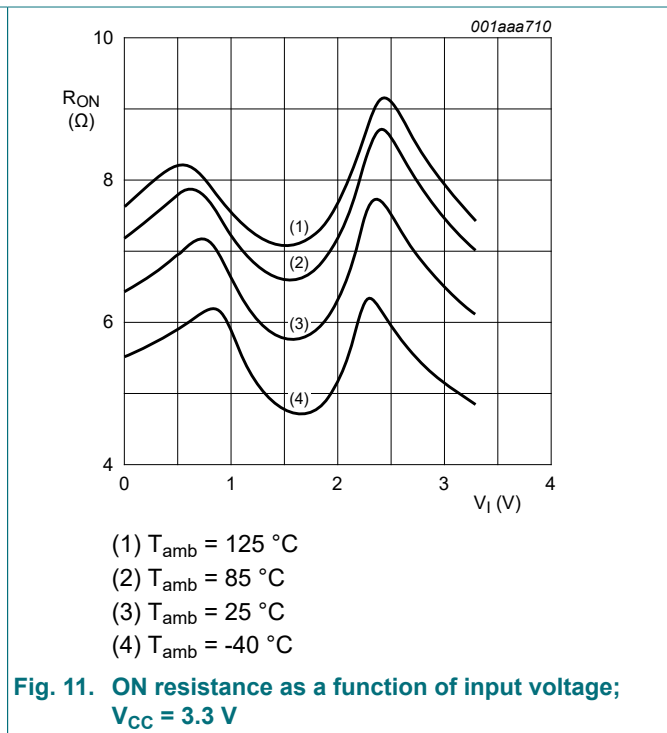
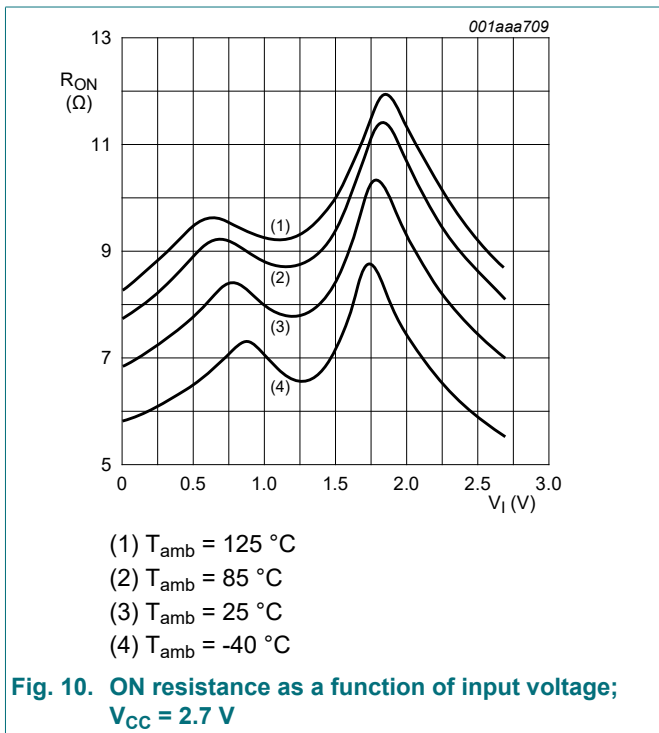
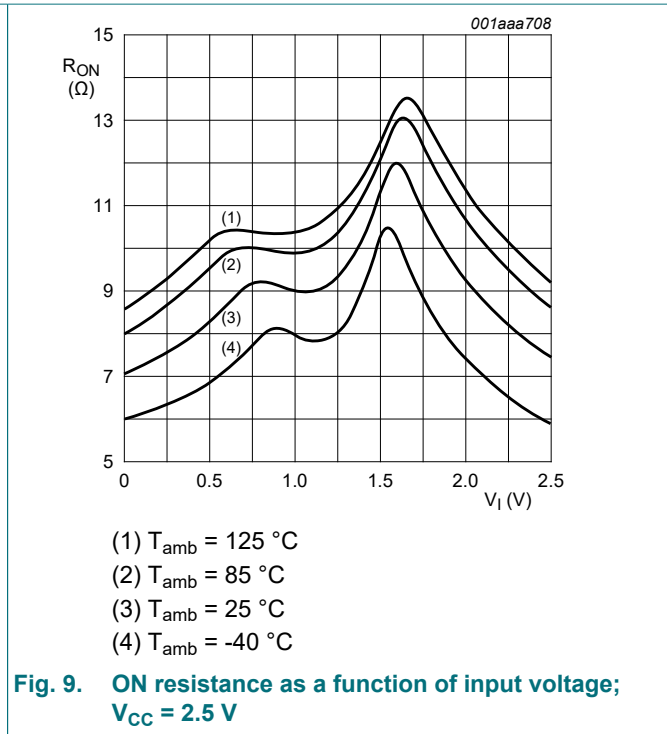
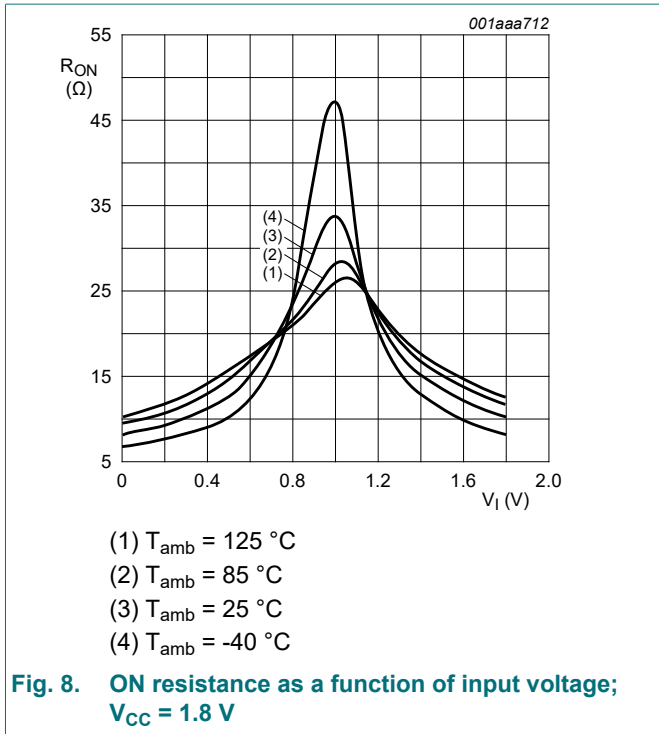
Symbol	Parameter	Conditions	-40 °C to +85 °C			-40 °C to +125 °C		Unit
			Min	Typ[1]	Max	Min	Max	
R _{ON(peak)}	ON resistance (peak)	V _I = GND to V _{CC} ; see Fig. 6						
		I _{SW} = 4 mA; V _{CC} = 1.65 V to 1.95 V	-	34.0	130	-	195	Ω
		I _{SW} = 8 mA; V _{CC} = 2.3 V to 2.7 V	-	12.0	30	-	45	Ω
		I _{SW} = 12 mA; V _{CC} = 2.7 V	-	10.4	25	-	38	Ω
		I _{SW} = 24 mA; V _{CC} = 3 V to 3.6 V	-	7.8	20	-	30	Ω
		I _{SW} = 32 mA; V _{CC} = 4.5 V to 5.5 V	-	6.2	15	-	23	Ω
R _{ON(rail)}	ON resistance (rail)	V _I = GND; see Fig. 6						
		I _{SW} = 4 mA; V _{CC} = 1.65 V to 1.95 V	-	8.2	18	-	27	Ω
		I _{SW} = 8 mA; V _{CC} = 2.3 V to 2.7 V	-	7.1	16	-	24	Ω
		I _{SW} = 12 mA; V _{CC} = 2.7 V	-	6.9	14	-	21	Ω
		I _{SW} = 24 mA; V _{CC} = 3 V to 3.6 V	-	6.5	12	-	18	Ω
		I _{SW} = 32 mA; V _{CC} = 4.5 V to 5.5 V	-	5.8	10	-	15	Ω
		V _I = V _{CC} ; see Fig. 6						
		I _{SW} = 4 mA; V _{CC} = 1.65 V to 1.95 V	-	10.4	30	-	45	Ω
		I _{SW} = 8 mA; V _{CC} = 2.3 V to 2.7 V	-	7.6	20	-	30	Ω
		I _{SW} = 12 mA; V _{CC} = 2.7 V	-	7.0	18	-	27	Ω
		I _{SW} = 24 mA; V _{CC} = 3 V to 3.6 V	-	6.1	15	-	23	Ω
		I _{SW} = 32 mA; V _{CC} = 4.5 V to 5.5 V	-	4.9	10	-	15	Ω
		R _{ON(flat)}	ON resistance (flatness)	V _I = GND to V _{CC} [2]				
I _{SW} = 4 mA; V _{CC} = 1.65 V to 1.95 V	-			26.0	-	-	-	Ω
I _{SW} = 8 mA; V _{CC} = 2.3 V to 2.7 V	-			5.0	-	-	-	Ω
I _{SW} = 12 mA; V _{CC} = 2.7 V	-			3.5	-	-	-	Ω
I _{SW} = 24 mA; V _{CC} = 3 V to 3.6 V	-			2.0	-	-	-	Ω
I _{SW} = 32 mA; V _{CC} = 4.5 V to 5.5 V	-			1.5	-	-	-	Ω

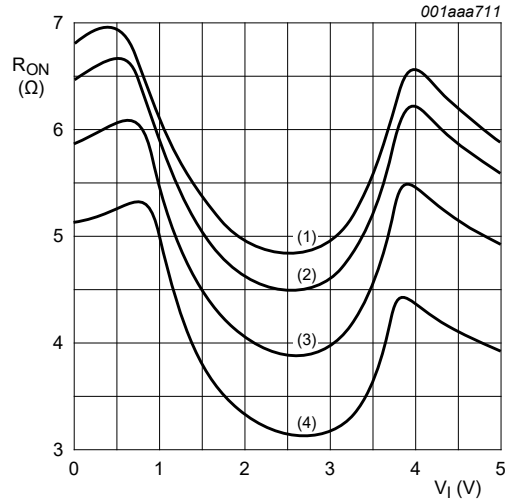
[1] Typical values are measured at T_{amb} = 25 °C and nominal V_{CC}.

[2] Flatness is defined as the difference between the maximum and minimum value of ON resistance measured at identical V_{CC} and temperature.

10.3. ON resistance test circuit and graphs







- (1) $T_{amb} = 125\text{ °C}$
- (2) $T_{amb} = 85\text{ °C}$
- (3) $T_{amb} = 25\text{ °C}$
- (4) $T_{amb} = -40\text{ °C}$

Fig. 12. ON resistance as a function of input voltage; $V_{CC} = 5.0\text{ V}$

11. Dynamic characteristics

Table 9. Dynamic characteristics

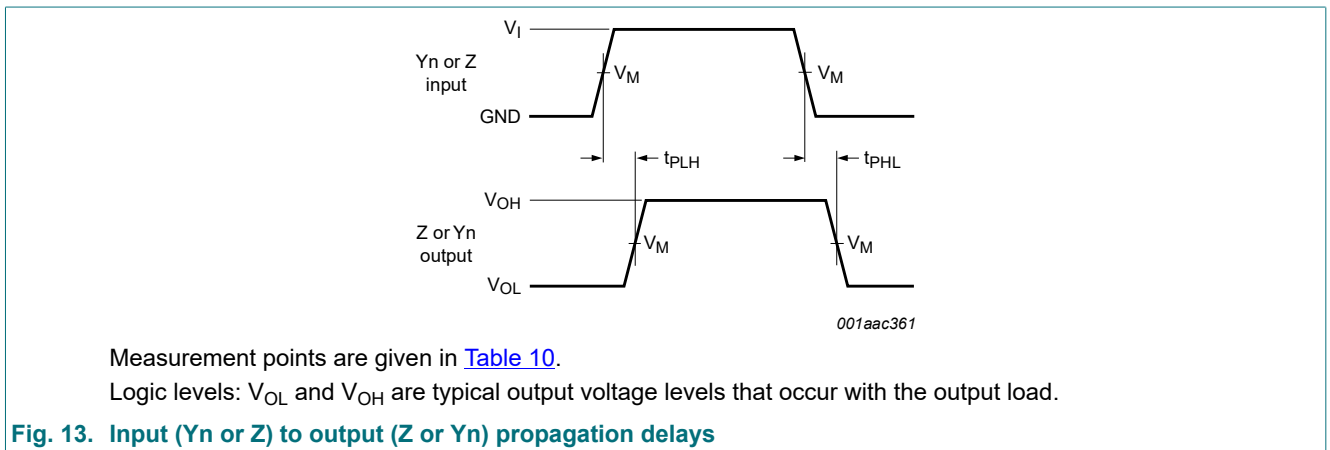
At recommended operating conditions; voltages are referenced to GND (ground = 0 V); for test circuit see Fig. 15.

Symbol	Parameter	Conditions	-40 °C to +85 °C			-40 °C to +125 °C		Unit
			Min	Typ[1]	Max	Min	Max	
t_{pd}	propagation delay	Z to Y_n or Y_n to Z; see Fig. 13 [2] [3]						
		$V_{CC} = 1.65\text{ V to }1.95\text{ V}$	-	-	2	-	2.5	ns
		$V_{CC} = 2.3\text{ V to }2.7\text{ V}$	-	-	1.2	-	1.5	ns
		$V_{CC} = 2.7\text{ V}$	-	-	1.0	-	1.25	ns
		$V_{CC} = 3.0\text{ V to }3.6\text{ V}$	-	-	0.8	-	1.0	ns
		$V_{CC} = 4.5\text{ V to }5.5\text{ V}$	-	-	0.6	-	0.8	ns
t_{en}	enable time	S to Z or Y_n ; see Fig. 14 [2]						
		$V_{CC} = 1.65\text{ V to }1.95\text{ V}$	2.6	6.7	10.3	2.6	12.9	ns
		$V_{CC} = 2.3\text{ V to }2.7\text{ V}$	1.9	4.1	6.4	1.9	8.0	ns
		$V_{CC} = 2.7\text{ V}$	1.9	4.0	5.5	1.8	7.0	ns
		$V_{CC} = 3.0\text{ V to }3.6\text{ V}$	1.8	3.4	5.0	1.8	6.3	ns
		$V_{CC} = 4.5\text{ V to }5.5\text{ V}$	1.3	2.6	3.8	1.3	4.8	ns
		\bar{E} to Z or Y_n ; see Fig. 14 [2]						
		$V_{CC} = 1.65\text{ V to }1.95\text{ V}$	1.9	4.0	7.3	1.9	9.2	ns
		$V_{CC} = 2.3\text{ V to }2.7\text{ V}$	1.4	2.5	4.4	1.4	5.5	ns
		$V_{CC} = 2.7\text{ V}$	1.1	2.6	3.9	1.1	4.9	ns
		$V_{CC} = 3.0\text{ V to }3.6\text{ V}$	1.2	2.2	3.8	1.2	4.8	ns
		$V_{CC} = 4.5\text{ V to }5.5\text{ V}$	1.0	1.7	2.6	1.0	3.3	ns

Symbol	Parameter	Conditions	-40 °C to +85 °C			-40 °C to +125 °C		Unit
			Min	Typ[1]	Max	Min	Max	
t _{dis}	disable time	S to Z or Yn; see Fig. 14 [2]						
		V _{CC} = 1.65 V to 1.95 V	2.1	6.8	10.0	2.1	12.5	ns
		V _{CC} = 2.3 V to 2.7 V	1.4	3.7	6.1	1.4	7.7	ns
		V _{CC} = 2.7 V	1.4	4.9	6.2	1.4	7.8	ns
		V _{CC} = 3.0 V to 3.6 V	1.1	4.0	5.4	1.1	6.8	ns
		V _{CC} = 4.5 V to 5.5 V	1.0	2.9	3.8	1.0	4.8	ns
		E to Z or Yn; see Fig. 14 [2]						
		V _{CC} = 1.65 V to 1.95 V	2.3	5.6	8.6	2.3	11.0	ns
		V _{CC} = 2.3 V to 2.7 V	1.2	3.2	4.8	1.2	6.0	ns
		V _{CC} = 2.7 V	1.4	4.0	5.2	1.4	6.5	ns
		V _{CC} = 3.0 V to 3.6 V	2.0	3.7	5.0	2.0	6.3	ns
		V _{CC} = 4.5 V to 5.5 V	1.3	2.9	3.8	1.3	4.8	ns

- [1] Typical values are measured at T_{amb} = 25 °C and nominal V_{CC}.
- [2] t_{pd} is the same as t_{PLH} and t_{PHL}; t_{en} is the same as t_{PZH} and t_{PZL}; t_{dis} is the same as t_{PLZ} and t_{PHZ}
- [3] Propagation delay is the calculated RC time constant of the typical ON resistance of the switch and the specified capacitance when driven by an ideal voltage source (zero output impedance).

11.1. Waveforms and test circuits



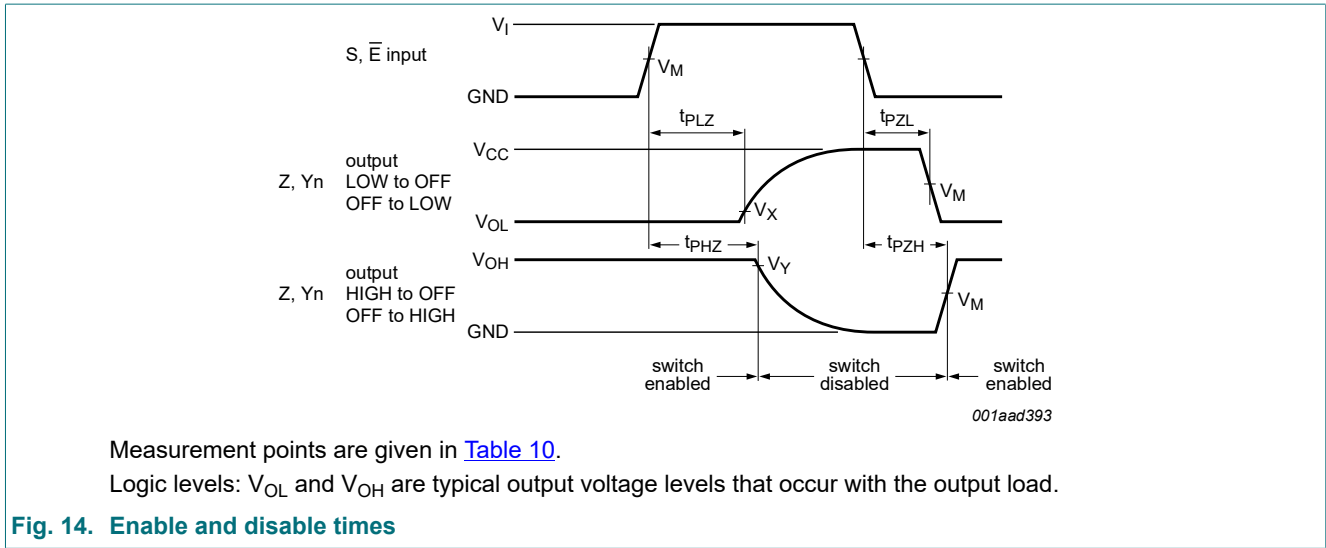


Table 10. Measurement points

Supply voltage	Input	Output		
V_{CC}	V_M	V_M	V_X	V_Y
1.65 V to 2.7 V	$0.5 \times V_{CC}$	$0.5 \times V_{CC}$	$V_{OL} + 0.15 \text{ V}$	$V_{OH} - 0.15 \text{ V}$
2.7 V to 5.5 V	$0.5 \times V_{CC}$	$0.5 \times V_{CC}$	$V_{OL} + 0.3 \text{ V}$	$V_{OH} - 0.3 \text{ V}$

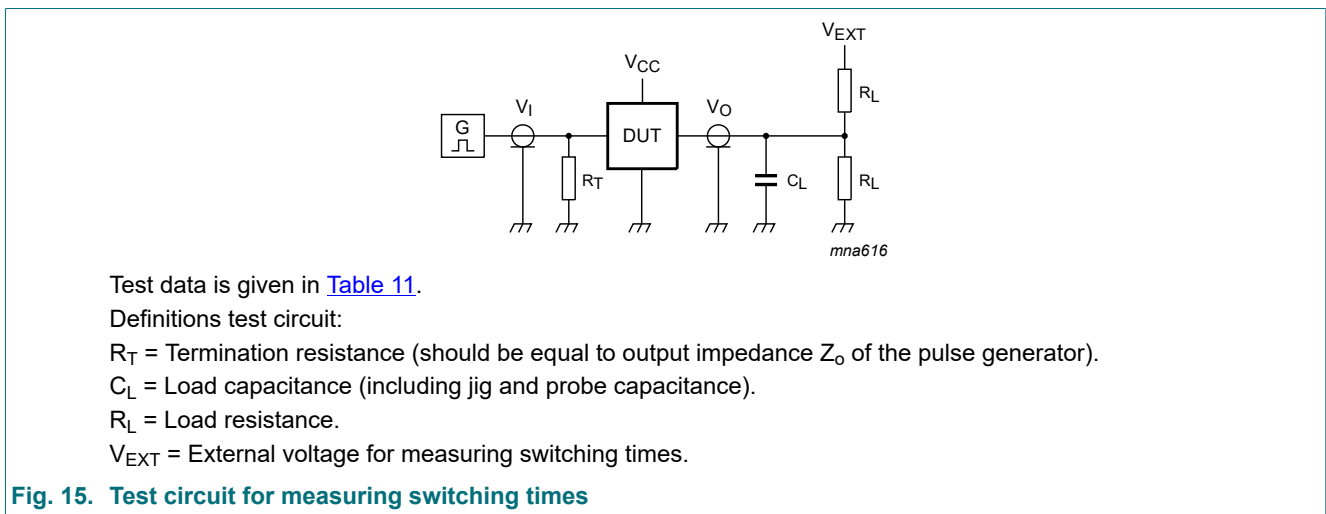


Table 11. Test data

Supply voltage	Input		Load		V_{EXT}		
V_{CC}	V_I	t_r, t_f	C_L	R_L	t_{PLH}, t_{PHL}	t_{PZH}, t_{PHZ}	t_{PZL}, t_{PLZ}
1.65 V to 1.95 V	V_{CC}	$\leq 2.0 \text{ ns}$	30 pF	1 k Ω	open	GND	$2 \times V_{CC}$
2.3 V to 2.7 V	V_{CC}	$\leq 2.0 \text{ ns}$	30 pF	500 Ω	open	GND	$2 \times V_{CC}$
2.7 V	V_{CC}	$\leq 2.5 \text{ ns}$	50 pF	500 Ω	open	GND	$2 \times V_{CC}$
3 V to 3.6 V	V_{CC}	$\leq 2.5 \text{ ns}$	50 pF	500 Ω	open	GND	$2 \times V_{CC}$
4.5 V to 5.5 V	V_{CC}	$\leq 2.5 \text{ ns}$	50 pF	500 Ω	open	GND	$2 \times V_{CC}$

11.2. Additional dynamic characteristics

Table 12. Additional dynamic characteristics

At recommended operating conditions; voltages are referenced to GND (ground = 0 V); $T_{amb} = 25\text{ }^{\circ}\text{C}$.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
THD	total harmonic distortion	$f_i = 600\text{ Hz to }20\text{ kHz}; R_L = 600\text{ }\Omega; C_L = 50\text{ pF}; V_I = 0.5\text{ V (p-p)}$; see Fig. 16				
		$V_{CC} = 1.65\text{ V}$	-	0.260	-	%
		$V_{CC} = 2.3\text{ V}$	-	0.078	-	%
		$V_{CC} = 3.0\text{ V}$	-	0.078	-	%
$f_{(-3dB)}$	-3 dB frequency response	$R_L = 50\text{ }\Omega; C_L = 5\text{ pF}$; see Fig. 17				
		$V_{CC} = 1.65\text{ V}$	-	200	-	MHz
		$V_{CC} = 2.3\text{ V}$	-	300	-	MHz
		$V_{CC} = 3.0\text{ V}$	-	300	-	MHz
α_{iso}	isolation (OFF-state)	$R_L = 50\text{ }\Omega; C_L = 5\text{ pF}; f_i = 10\text{ MHz}$; see Fig. 18				
		$V_{CC} = 1.65\text{ V}$	-	-42	-	dB
		$V_{CC} = 2.3\text{ V}$	-	-42	-	dB
		$V_{CC} = 3.0\text{ V}$	-	-40	-	dB
Q_{inj}	charge injection	$C_L = 0.1\text{ nF}; V_{gen} = 0\text{ V}; R_{gen} = 0\text{ }\Omega; f_i = 1\text{ MHz}; R_L = 1\text{ M}\Omega$; see Fig. 19				
		$V_{CC} = 1.8\text{ V}$	-	3.3	-	pC
		$V_{CC} = 2.5\text{ V}$	-	4.1	-	pC
		$V_{CC} = 3.3\text{ V}$	-	5.0	-	pC
		$V_{CC} = 4.5\text{ V}$	-	6.4	-	pC
		$V_{CC} = 5.5\text{ V}$	-	7.5	-	pC

11.3. Test circuits

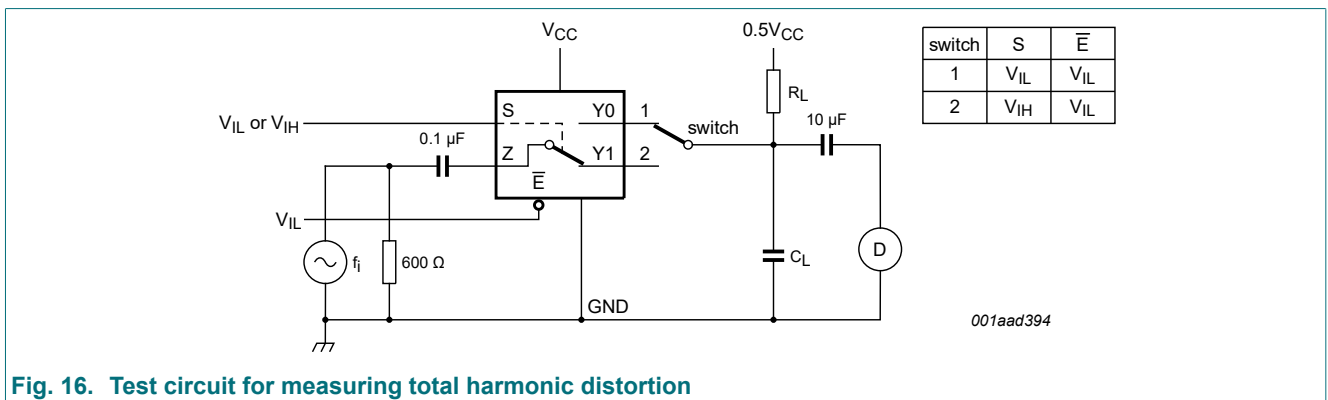
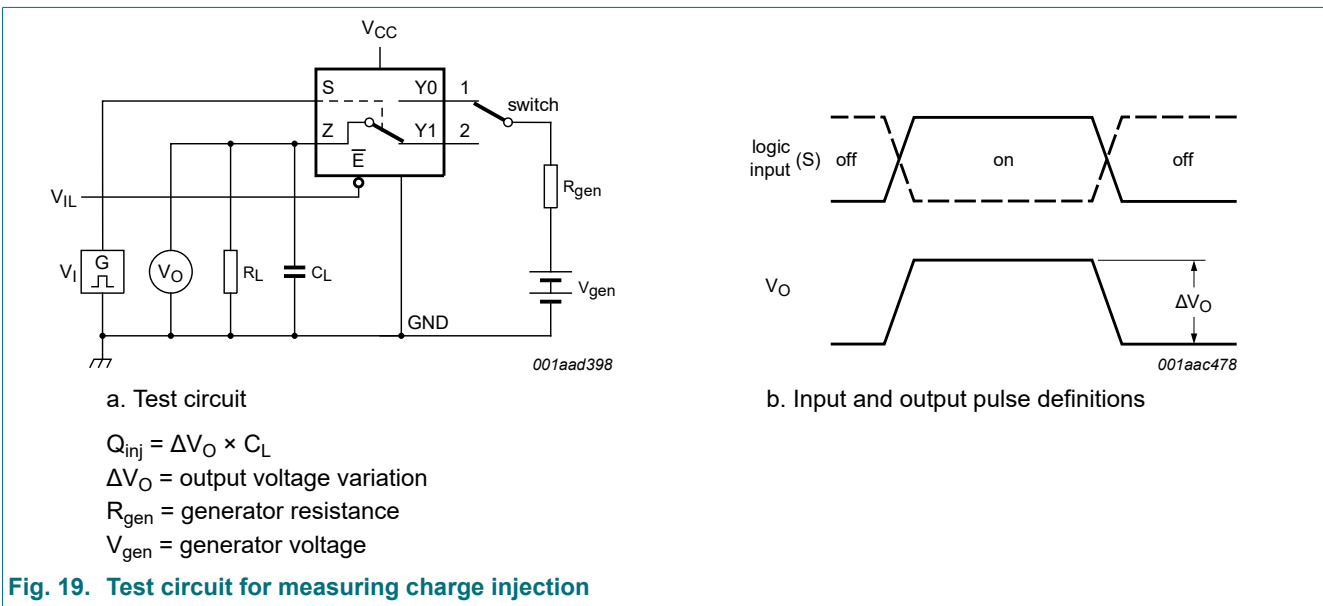
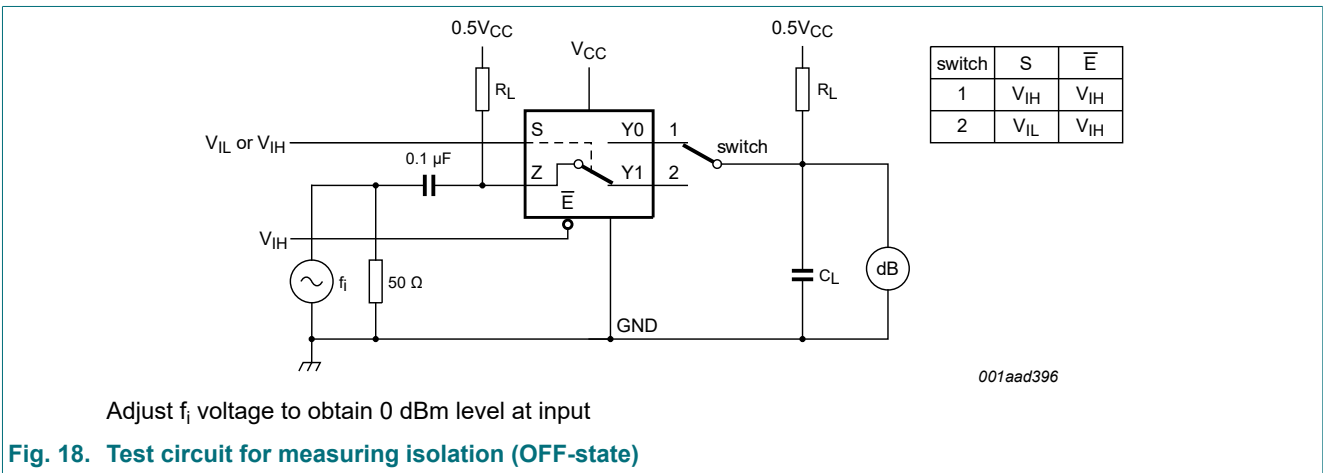
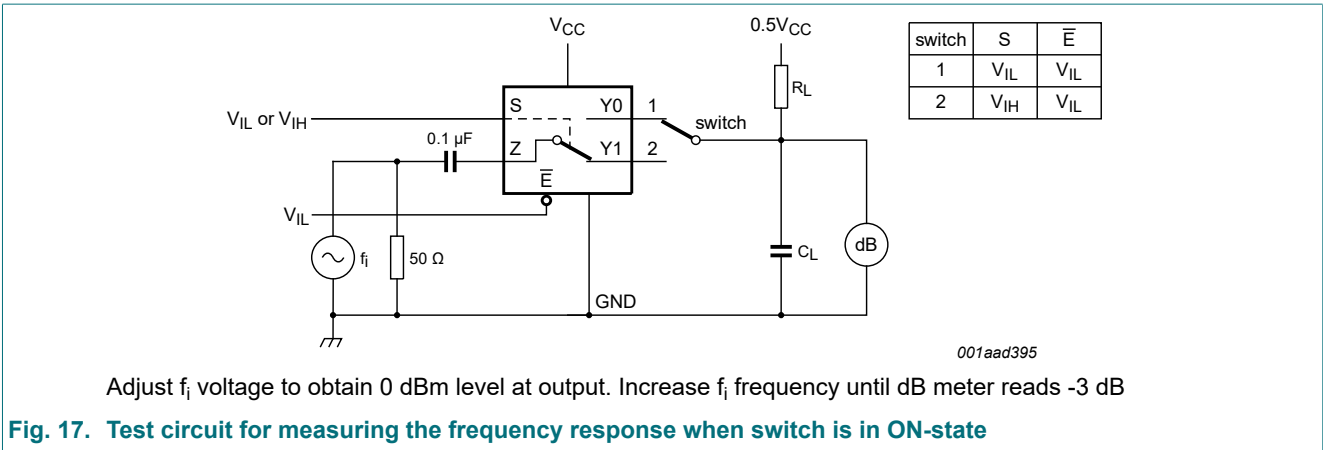


Fig. 16. Test circuit for measuring total harmonic distortion



12. Package outline

TSSOP8: plastic thin shrink small outline package; 8 leads; body width 3 mm; lead length 0.5 mm SOT505-2

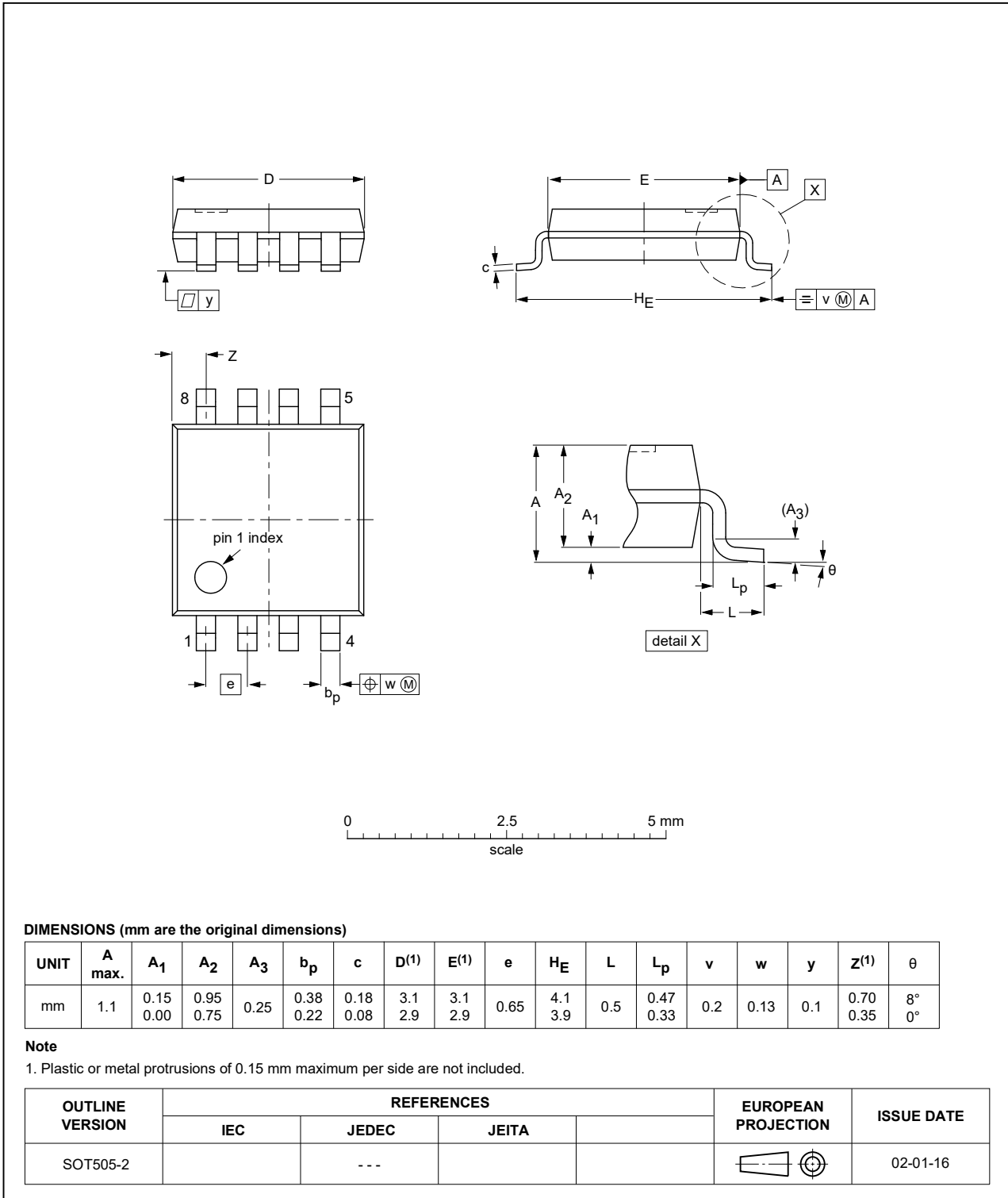


Fig. 20. Package outline SOT505-2 (TSSOP8)

VSSOP8: plastic very thin shrink small outline package; 8 leads; body width 2.3 mm

SOT765-1

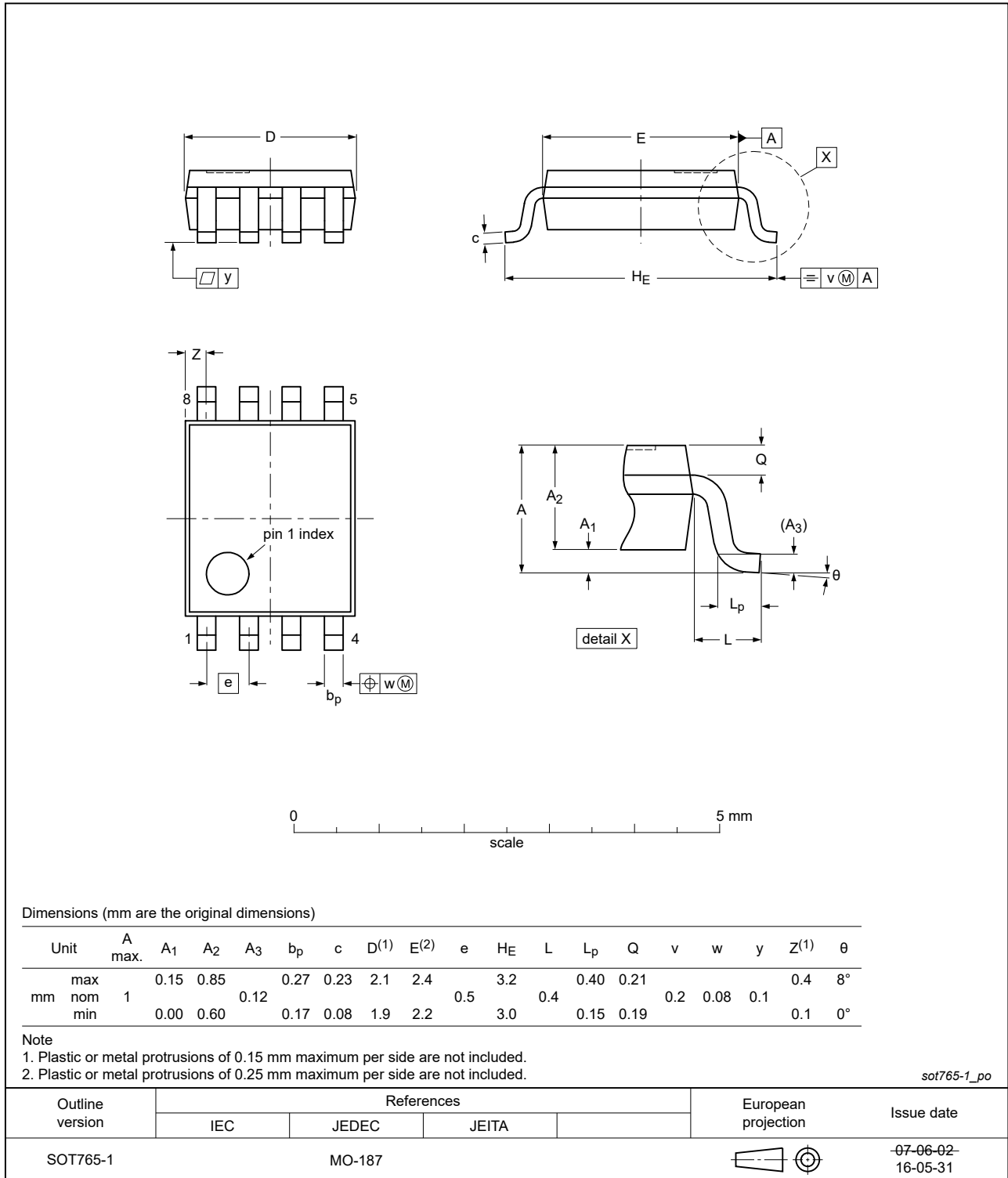


Fig. 21. Package outline SOT765-1 (VSSOP8)

13. Abbreviations

Table 13. Abbreviations

Acronym	Description
CMOS	Complementary Metal-Oxide Semiconductor
DUT	Device Under Test
ESD	ElectroStatic Discharge
HBM	Human Body Model
MIL	Military
MM	Machine Model
TTL	Transistor-Transistor Logic

14. Revision history

Table 14. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
74LVC1G53_Q100 v.4	20210720	Product data sheet	-	74LVC1G53_Q100 v.3
Modifications:	<ul style="list-style-type: none"> Section 1 updated. Section 8: Derating values for P_{tot} total power dissipation updated. 			
74LVC1G53_Q100 v.3	20180817	Product data sheet	-	74LVC1G53_Q100 v.2
Modifications:	<ul style="list-style-type: none"> The format of this data sheet has been redesigned to comply with the identity guidelines of Nexperia. Legal texts have been adapted to the new company name where appropriate. 			
74LVC1G53_Q100 v.2	20161209	Product data sheet	-	74LVC1G53_Q100 v.1
Modifications:	<ul style="list-style-type: none"> Table 7: The maximum limits for leakage current and supply current have changed. 			
74LVC1G53_Q100 v.1	20130129	Product data sheet	-	-

15. Legal information

Data sheet status

Document status [1][2]	Product status [3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

- [1] Please consult the most recently issued document before initiating or completing a design.
- [2] The term 'short data sheet' is explained in section "Definitions".
- [3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the internet at <https://www.nexperia.com>.

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