NEWHAVEN DISPLAY INTERNATIONAL

Product Specification

NHD-0420CW-AB3

Character OLED Display Module

NHD-	Newhaven Display
0420-	4 Lines x 20 Characters
CW-	Character OLED Module
A-	Model
B-	Blue
3-	2.7V~5.5V Supply Voltage

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REACH Compliant

RoHS Compliant

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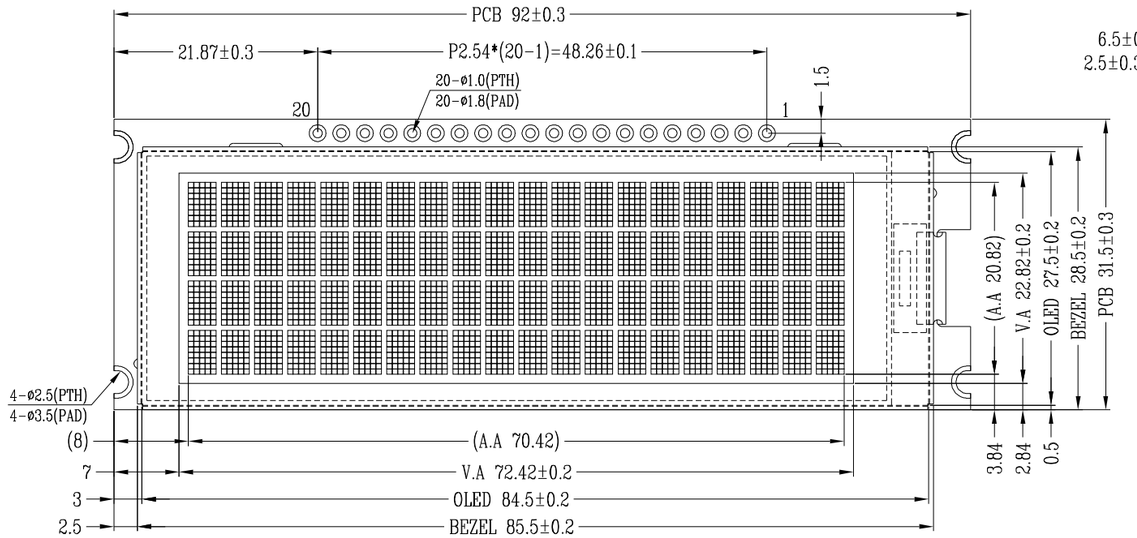
Additional Resources

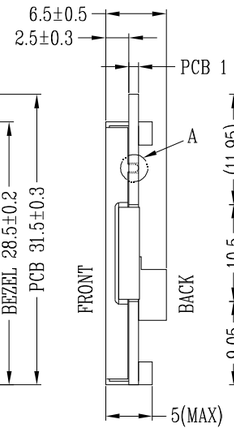
- **Support Forum:** https://support.newhavendisplay.com/hc/en-us/community/topics
- **GitHub:** https://github.com/newhavendisplay
- **Example Code:** https://support.newhavendisplay.com/hc/en-us/categories/4409527834135-Example-Code/
- **Knowledge Center:** https://www.newhavendisplay.com/knowledge_center.html
- **Quality Center:** https://www.newhavendisplay.com/quality_center.html
- **Precautions for using LCDs/LCMs:** https://www.newhavendisplay.com/specs/precautions.pdf
- **Warranty / Terms & Conditions:** https://www.newhavendisplay.com/terms.html

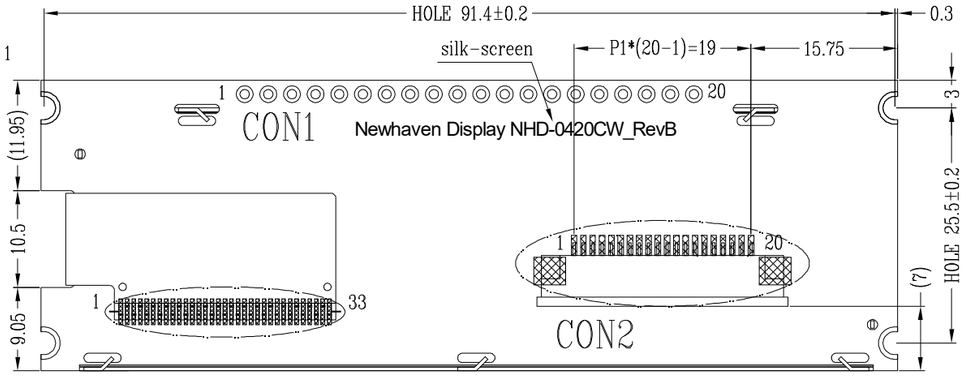
Document Revision History

Revision	Date	Description	Changed By
0	12/15/2014	Initial Release	AK
1	04/06/2015	Pin Description, Electrical Characteristics Updated	PB
2	02/01/2016	Recommended Connector P/Ns Added	SB
3	02/02/2017	Thru-Hole Diameter Increased, Quality Table Updated, I2C Interface Updated	SB
4	10/25/2022	Minimum Supply Voltage Value Updated	KL
5	11/16/2022	Logic Voltage Range Updated	KL

Mechanical Drawing







DETAIL A
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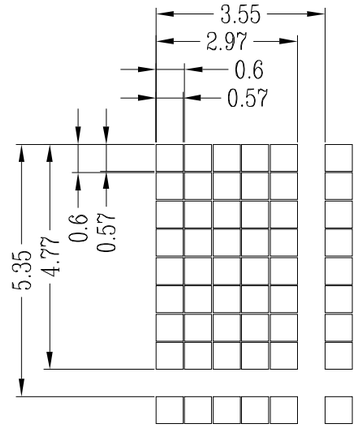


Pin Assignment:

NO.	1	2	3	4	5	6	7	8	9	10
Symbol	VSS	VDD	REGVDD	D/C	R/W	E	D0	D1	D2	D3
NO.	11	12	13	14	15	16	17	18	19	20
Symbol	D4	D5	D6	D7	CS	RES	BS0	BS1	BS2	VSS(FrameGround)

Product Description: 4 x 20 Character Blue Slim OLED

1. OLED Driver IC: US2066
2. OLED Interface: 4/8-bit Parallel, SPI, I²C
3. OLED Power Requirement:
   - 3.3V Operation: VDD=3.3V, REGVDD=0V
   - 5.0V Operation: VDD=5.0V, REGVDD=5.0V
4. Mating Connector: 20pin, 2.54mm pitch; Ex. Molex 52271-2079

Standard Tolerance:
(Unless otherwise specified)
Linear: ±0.3mm

NEWHAVEN DISPLAY INTERNATIONAL

Drawing/Part Number: NHD-0420CW-AB3		Revision: -
Unless otherwise specified: • Dimensions are in Millimeters • Third Angle Projection	Drawn By: K. Lewis	Approved By: K. Lewis
	Drawn Date: 11/16/2022	Approved Date: 11/16/2022

Pin Description

Parallel Interface:

Pin No.	Symbol	External Connection	Function Description
1	V_{SS}	Power Supply	Ground
2	V_{DD}	Power Supply	Supply Voltage for OLED and Logic V_{DD}=3.3V for 3.3V operation, V_{DD}=5.0V for 5.0V operation
3	$REGV_{DD}$	Power Supply	Internal 5V I/O Regulator select signal $REGV_{DD}$=0V for 3.3V operation, $REGV_{DD}$=5.0V for 5.0V operation
4	D/C	MPU	Data/Command select signal. D/C=0: Command, D/C=1: Data
5	R/W	MPU	Read/Write select signal, R/W=1: Read R/W=0: Write
6	E	MPU	Operation Enable signal. Falling edge triggered.
7-10	DB0 – DB3	MPU	Four low order bi-directional three-state data bus lines. These four are not used during 4-bit operation.
11-14	DB4 – DB7	MPU	Four high order bi-directional three-state data bus lines.
15	/CS	MPU	Active LOW Chip Select signal
16	/RES	MPU	Active LOW Reset signal
17-19	BS0 – BS2	MPU	MPU interface select signal
20	V_{SS}	Power Supply	Ground

Serial Interface:

Pin No.	Symbol	External Connection	Function Description
1	V_{SS}	Power Supply	Ground
2	V_{DD}	Power Supply	Supply Voltage for OLED and Logic V_{DD}=3.3V for 3.3V operation, V_{DD}=5.0V for 5.0V operation
3	$REGV_{DD}$	Power Supply	Internal 5V I/O Regulator select signal $REGV_{DD}$=0V for 3.3V operation, $REGV_{DD}$=5.0V for 5.0V operation
4-6	NC	-	No Connect. Tie to Ground
7	SCLK	MPU	Serial Clock signal
8	SDI	MPU	Serial Data Input signal
9	SDO	MPU	Serial Data Output signal
10-14	NC	-	No Connect. Tie to Ground
15	/CS	MPU	Active LOW Chip Select signal
16	/RES	MPU	Active LOW Reset signal
17-19	BS0 – BS2	MPU	MPU interface select signal
20	V_{SS}	Power Supply	Ground

I^2C Interface:

Pin No.	Symbol	External Connection	Function Description
1	V_{SS}	Power Supply	Ground
2	V_{DD}	Power Supply	Supply Voltage for OLED and Logic V_{DD} = 3.3V for 3.3V operation ONLY, **5.0V mode not supported**
3	$REGV_{DD}$	Power Supply	Internal 5V I/O Regulator select signal $REGV_{DD}$=0V for 3.3V operation ONLY, **5.0V mode not supported**
4	SA0	MPU	Slave Address select signal
5-6	NC	-	No Connect. Tie to Ground
7	SCL	MPU	Serial Clock signal
8	SDA_{IN}	MPU	Serial Data Input.
9	SDA_{OUT}	MPU	Serial Data Output. Tie together with SDA_{IN} (pin 8)
10-15	NC	-	No Connect. Tie to Ground
16	/RES	MPU	Active LOW Reset signal
17-19	BS0 – BS2	MPU	MPU interface select signal
20	V_{SS}	Power Supply	Ground

MPU Interface Pin Selections

Pin Name	4-bit Parallel 6800 interface	4-bit Parallel 8080 interface	8-bit Parallel 6800 interface	8-bit Parallel 8080 interface	Serial Interface	I²C Interface
BS0	1	1	0	0	0	0
BS1	0	1	0	1	0	1
BS2	1	1	1	1	0	0

MPU Interface Pin Assignment Summary

Bus Interface	Data/Command Interface								Control Signals				
	D7	D6	D5	D4	D3	D2	D1	D0	E	R/W	/CS	D/C	/RES
4-bit 6800	D[7:4]				Tie LOW				E	R/W	/CS	D/C	/RES
4-bit 8080	D[7:4]				Tie LOW				/RD	/WR	/CS	D/C	/RES
8-bit 6800	D[7:0]								E	R/W	/CS	D/C	/RES
8-bit 8080	D[7:0]								/RD	/WR	/CS	D/C	/RES
SPI	Tie LOW					SDO	SDI	SCLK	Tie LOW		/CS	Tie LOW	/RES
I²C	Tie LOW					SDA_{OUT}	SDA_{IN}	SCL	Tie LOW			SA0	/RES

Electrical Characteristics

Item	Symbol	Condition	Min.	Typ.	Max.	Unit
Operating Temperature Range	T_{OP}	Absolute Max	-40	-	+85	°C
Storage Temperature Range	T_{ST}	Absolute Max	-40	-	+90	°C
Supply Voltage for logic	V_{DD}	3.3V operation	2.7	3.3	3.6	V
		5.0V operation	4.4	5.0	5.5	V
Supply Voltage for I/O Regulator	$REGV_{DD}$	V_{DD} = 5V	4.4	5.0	5.5	V
Supply Current	I_{DD}	-	-	70	135	mA
Sleep Mode Current	$(I_{DD})_{SLEEP}$	-	-	2	5	mA
"H" Level input	V_{IH}	-	0.8 * V_{DD}	-	V_{DD}	V
"L" Level input	V_{IL}	-	V_{SS}	-	0.2 * V_{DD}	V
"H" Level output	V_{OH}	-	0.9 * V_{DD}	-	V_{DD}	V
"L" Level output	V_{OL}	-	V_{SS}	-	0.1 * V_{DD}	V

Optical Characteristics

Item		Symbol	Condition	Min.	Typ.	Max.	Unit
Optimal Viewing Angles	Top	φY+	Cr ≥ 10,000:1	80	-	-	°
	Bottom	φY-		80	-	-	°
	Left	θX-		80	-	-	°
	Right	θX+		80	-	-	°
Contrast Ratio		Cr	-	10,000:1	-	-	-
Response Time	Rise	Tr	-	-	10	-	µs
	Fall	Tf	-	-	10	-	µs
Brightness			50% Checkerboard	60	80	-	cd/m^2
Lifetime			Ta=25°C 50% Checkerboard	40,000	-	-	Hrs.

Note: Lifetime at typical temperature is based on accelerated high-temperature operation. Lifetime is tested at average 50% pixels on and is rated as Hours until **Half-Brightness**. The Display OFF command can be used to extend the lifetime of the display.
Luminance of active pixels will degrade faster than inactive pixels. Residual (burn-in) images may occur. To avoid this, every pixel should be illuminated uniformly.

Controller Information

Built-in US2066 controller: https://support.newhavendisplay.com/hc/en-us/articles/4414485495703--US2066

DDRAM Address

1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20
00	01	02	03	04	05	06	07	08	09	0A	0B	0C	0D	0E	0F	10	11	12	13
20	21	22	23	24	25	26	27	28	29	2A	2B	2C	2D	2E	2F	30	31	32	33
40	41	42	43	44	45	46	47	48	49	4A	4B	4C	4D	4E	4F	50	51	52	53
60	61	62	63	64	65	66	67	68	69	6A	6B	6C	6D	6E	6F	70	71	72	73

Table of Commands

1. Fundamental Command List														
Command	**IS**	**RE**	**SD**	**Instruction Code**										**Description**
				D/C#	**R/W# (WR#)**	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**	
Clear Display	**X**	**X**	**0**	0	0	0	0	0	0	0	0	0	1	Write "20H" to DDRAM and set DDRAM address to "00H" from AC.
Return Home	**X**	**0**	**0**	0	0	0	0	0	0	0	0	1	*	Set DDRAM address to "00H" from AC and return cursor to its original position if shifted. The contents of DDRAM are not changed.
Entry Mode Set	**X**	**0**	**0**	0	0	0	0	0	0	0	1	I/D	S	Assign cursor / blink moving direction with DDRAM address. I/D = "1": cursor/ blink moves to right and DDRAM address is increased by 1 (POR) I/D = "0": cursor/ blink moves to left and DDRAM address is decreased by 1 Assign display shift with DDRAM address. S = "1": make display shift of the enabled lines by the DS4 to DS1 bits in the shift enable instruction. Left/ right direction depends on I/D bit selection. S = "0": display shift disable (POR)
	X	**1**	**0**	0	0	0	0	0	0	0	1	BDC	BDS	Common bi-direction function. BDC = "0": COM31 -> COM0 BDC = "1": COM0 -> COM31 Segment bi-direction function. BDS = "0": SEG99 -> SEG0, BDS = "1": SEG0 -> SEG99
Display ON/ OFF Control	**X**	**0**	**0**	0	0	0	0	0	0	1	D	C	B	Set display/cursor/blink ON/OFF D = "1": display ON, D = "0": display OFF (POR), C = "1": cursor ON, C = "0": cursor OFF (POR), B = "1": blink ON, B = "0": blink OFF (POR).
Extended Function Set	**X**	**1**	**0**	0	0	0	0	0	0	1	FW	BW	NW	Assign font width, black/white inverting of cursor, and 4line display mode control bit. FW = "1": 6-dot font width, FW = "0": 5-dot font width (POR), B/W = "1": black/white inverting of cursor enable, B/W = "0": black/white inverting of cursor disable (POR) NW = "1": 3-line or 4-line display mode NW = "0": 1-line or 2-line display mode

1. Fundamental Command Set														
Command	**IS**	**RE**	**SD**	**Instruction Code**										**Description**
				D/C#	**R/W# (WR#)**	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**	
Cursor or Display Shift	**0**	**0**	**0**	0	0	0	0	0	1	S/C	R/L	*	*	Set cursor moving and display shift control bit, and the direction, without changing DDRAM data. S/C = "1": display shift, S/C = "0": cursor shift, R/L = "1": shift to right, R/L = "0": shift to left
Double Height (4-Line)/ Display-dot Shift	**0**	**1**	**0**	0	0	0	0	0	1	UD2	UD1	*	DH'	UD2~1: Assign different doubt height format (POR=11b) Refer to Table 7-2 for details DH' = "1": display shift enable DH' = "0": dot scroll enable (POR)
Shift Enable	**1**	**1**	**0**	0	0	0	0	0	1	DS4	DS3	DS2	DS1	DS[4:1]=1111b (POR) when DH' = 1b Determine the line for display shift. DS1 = "1/0": 1st line display shift enable/disable DS2 = "1/0": 2nd line display shift enable/disable DS3 = "1/0": 3rd line display shift enable/disable DS4 = "1/0": 4th line display shift enable/disable.
Scroll Enable	**1**	**1**	**0**	0	0	0	0	0	1	HS4	HS3	HS2	HS1	HS[4:1]=1111b (POR) when DH' = 0b Determine the line for horizontal smooth scroll. HS1 = "1/0": 1st line dot scroll enable/disable HS2 = "1/0": 2nd line dot scroll enable/disable HS3 = "1/0": 3rd line dot scroll enable/disable HS4 = "1/0": 4th line dot scroll enable/disable.
Function Set	**X**	**0**	**0**	0	0	0	0	1	*	N	DH	**RE (0)**	**IS**	Numbers of display line, N when N = "1": 2-line (NW=0b) / 4-line (NW=1b), when N = "0": 1-line (NW=0b) / 3-line (NW=1b) DH = " 1/0": Double height font control for 2-line mode enable/ disable (POR=0) Extension register, RE ("0") Extension register, IS
	X	**1**	**0**	0	0	0	0	1	*	N	BE	**RE (1)**	**REV**	CGRAM blink enable BE = 1b: CGRAM blink enable BE = 0b: CGRAM blink disable (POR) Extension register, RE ("1") Reverse bit REV = "1": reverse display, REV = "0": normal display (POR)

1. Fundamental Command Set

Command	IS	RE	SD	Instruction Code										Description
				D/C#	R/W# (WR#)	D7	D6	D5	D4	D3	D2	D1	D0	
Set CGRAM Address	0	0	0	0	0	0	1	AC5	AC4	AC3	AC2	AC1	AC0	Set CGRAM address in address counter. (POR=00 0000)
Set DDRAM Address	0	0	0	0	0	1	AC6	AC5	AC4	AC3	AC2	AC1	AC0	Set DDRAM address in address counter. (POR=000 0000)
Set Scroll Quantity	X	1	0	0	0	1	*	SQ5	SQ4	SQ3	SQ2	SQ1	SQ0	Set the quantity of horizontal dot scroll. (POR=00 0000) Valid up to SQ[5:0] = 110000b
Read Busy Flag and Address/ Part ID	X	X	0	0	1	BF	AC6 / ID6	AC5 / ID5	AC4 / ID4	AC3 / ID3	AC2 / ID2	AC1 / ID1	AC0 / ID0	Can be known whether during internal operation or not by reading BF. The contents of address counter or the part ID can also be read. When it is read the first time, the address counter can be read. When it is read the second time, the part ID can be read. BF = "1": busy state BF = "0": ready state
Write Data	X	X	0	1	0	D7	D6	D5	D4	D3	D2	D1	D0	Write data into internal RAM (DDRAM / CGRAM).
Read Data	X	X	0	1	1	D7	D6	D5	D4	D3	D2	D1	D0	Read data from internal RAM (DDRAM / CGRAM).

2. Extended Command Set

Command	IS	RE	SD	Instruction Code											Description
				D/C#	R/W# (WR#)	Hex	D7	D6	D5	D4	D3	D2	D1	D0	
Function Selection A	X X	1 1	0 0	0 1	0 0	71 A[7:0]	0 A_7	1 A_6	1 A_5	1 A_4	0 A_3	0 A_2	0 A_1	1 A_0	A[7:0] = 00h, Disable internal V_{DD} regulator at 5V I/O application mode A[7:0] = 5Ch, Enable internal V_{DD} regulator at 5V I/O application mode (POR)
Function Selection B	X X	1 1	0 0	0 1	0 0	72	0 *	1 *	1 *	1 *	0 ROM 1	0 ROM 0	1 OPR 1	0 OPR 0	OPR[1:0]: Select the character no. of character generator ROM[1:0]: Select character ROM

OPR[1:0]	CGROM	CGRAM
00b	240	8
01b	248	8
10b	250	6
11b	256	0

RO[1:0]	ROM
00b	A
01b	B
01b	C
11b	Invalid

OLED Characterization	X	1	X	0	0	78/79	0	1	1	1	1	0	0	SD	Extension Register, SD SD=0b: OLED Command set is disabled (POR) SD=1b: OLED Command set is enabled.

3. OLED Command Set

Command	IS	RE	SD	Instruction Code										Description
				D/C #	R/W# (WR#)	Hex	D7	D6	D5	D4	D3	D2	D1	D0	
Set Contrast Control	**X** **X**	**1** **1**	**1** **1**	0 0	0 0	81 A[7:0]	1 A_7	0 A_6	0 A_5	0 A_4	0 A_3	0 A_2	0 A_1	1 A_0	Double byte command to select 1 out of 256 contrast steps. Contrast increases as the value increases. (POR = 7Fh)
Set Display Clock Divide Ratio / Oscillator Frequency	**X** **X**	**1** **1**	**1** **1**	0 0	0 0	D5 A[7:0]	1 A_7	1 A_6	0 A_5	1 A_4	0 A_3	1 A_2	0 A_1	1 A_0	A[3:0]: Define the divide ratio {D) of the display clocks (DCLK) divide ratio = A[3:0] + 1 (POR=0000b) A[7:4]: Set the Oscillator Frequency, FOSC. Oscillator Frequency increases with the value of A[7:4] and vice versa. (POR=0111b) Range:0000b~1111b Frequency increases as setting value increases.
Set Phase Length	**X** **X**	**1** **1**	**1** **1**	0 0	0 0	D9 A[7:0]	1 A_7	1 A_6	0 A_5	1 A_4	1 A_3	0 A_2	0 A_1	1 A_0	A[3:0]: Phase 1 period of up to 32 DCLK; clock 0 is an valid entry with 2 DCLK (POR=1000b) A[7:4]: Phase 2 period of up to 15 DCLK; clock 0 is invalid entry (POR=0111b)
Set SEG Pins Hardware Configuration	**X** **X**	**1** **1**	**1** **1**	0 0	0 0	DB A[6:4]	1 0	1 A_6	0 A_5	1 A_4	1 0	0 0	1 0	1 0	A[6:4] / Hex Code / V_{COMH} Deselect level 000b / 00h / ~0.65 x V_{CC} 001b / 10h / ~0.71 x V_{CC} 010B / 20h / ~0.77 x V_{CC} (POR) 011 / 30h / ~0.83 x V_{CC} 100b / 40h / 1 x V_{CC}

1. OLED Command Set

Command	IS	RE	SD	Instruction Code										Description
				D/C #	R/W# (WR#)	Hex	D7	D6	D5	D4	D3	D2	D1	D0	
Function Selection C	X X	1 1	1 1	0 0	0 0	DC A[7:0]	1 A_7	1 A_6	0 A_5	1 A_4	1 A_3	1 A_2	0 A_1	0 A_0	Set VSL & GPIO Set VSL: A[7] = 0b: Internal VSL (POR) A[7] = 1b: Enable external VSL Set GPIO: A[1:0]= 00b represents GPIO pin HiZ, input disabled (always read as low) A[1:0]= 01b represents GPIO pin HiZ, input enabled A[1:0]= 10b represents GPIO pin output Low (RESET) A[1:0]= 11b represents GPIO pin output High
Set Fade Out and Blinking	X X	1 1	1 1	0 0	0 0	23 A[5:0]	0 *	0 *	1 A_5	0 A_4	0 A_3	0 A_2	1 A_1	1 A_0	A[5:4] = 00b Disable Fade Out / Blinking Mode[RESET] A[5:4] = 10b Enable Fade Out mode. Once Fade Mode is enabled, contrast decrease gradually to all pixels OFF. Output follows RAM content when Fade mode is disabled. A[5:4] = 11b Enable Blinking mode. Once Blinking Mode is enabled, contrast decrease gradually to all pixels OFF and then contrast increases gradually to normal display. This process loops continuously until the Blinking mode is disabled. A[3:0] : Set time interval for each fade step

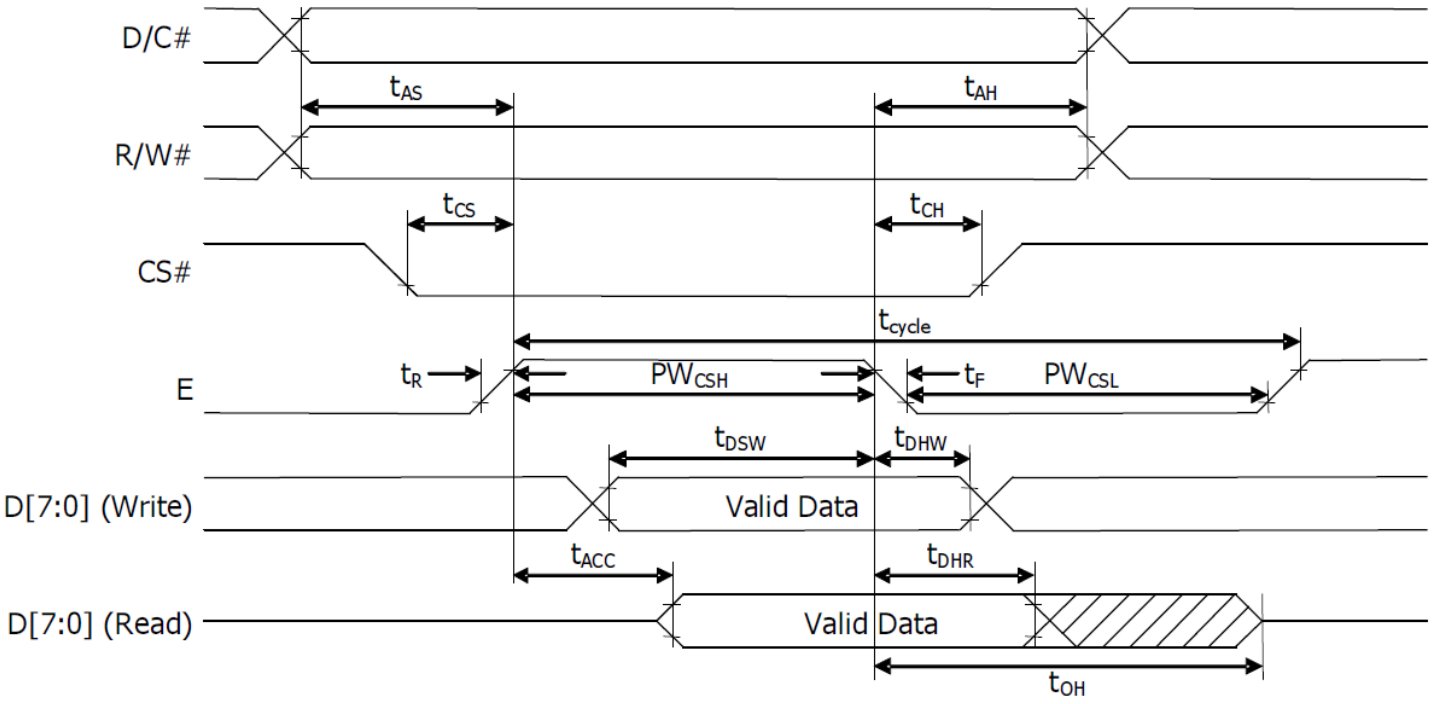
A[3:0]	Time interval of for each fade step
0000b	8 Frames
0001b	16 Frames
0010b	24 Frames
:	:
1110b	120 Frames
1111b	128 Frames

Timing Characteristics

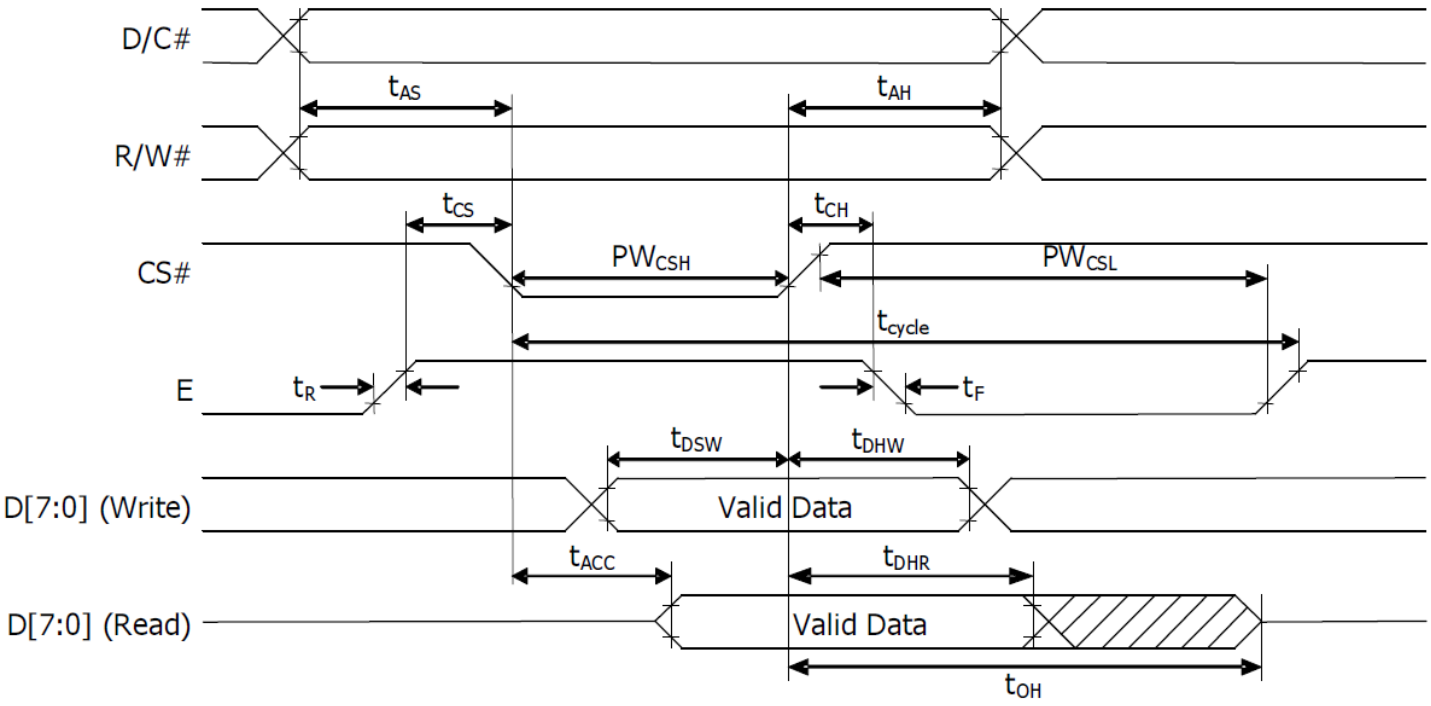
6800-Series Parallel Interface:

Symbol	Parameter	Min	Typ	Max	Unit
t_{cycle}	Clock Cycle Time (write cycle)	400	-	-	ns
t_{AS}	Address Setup Time	13	-	-	ns
t_{AH}	Address Hold Time	17	-	-	ns
t_{CS}	Chip Select Time	0	-	-	ns
t_{CH}	Chip Select Hold Time	0	-	-	ns
t_{DSW}	Write Data Setup Time	35	-	-	ns
t_{DHW}	Write Data Hold Time	18	-	-	ns
t_{DHR}	Read Data Hold Time	13	-	-	ns
t_{OH}	Output Disable Time	10	-	90	ns
t_{ACC}	Access Time (RAM) Access Time (command)	-	-	125	ns
PW_{CSL}	Chip Select Low Pulse Width (read RAM) Chip Select Low Pulse Width (read Command) Chip Select Low Pulse Width (write)	250 250 50	- - -	- - -	ns ns ns
PW_{CSH}	Chip Select High Pulse Width (read) Chip Select High Pulse Width (write)	155 55	- -	- -	ns ns
t_R	Rise Time	-	-	15	ns
t_F	Fall Time	-	-	15	ns

Condition 1: /CS low pulse width > E high pulse width



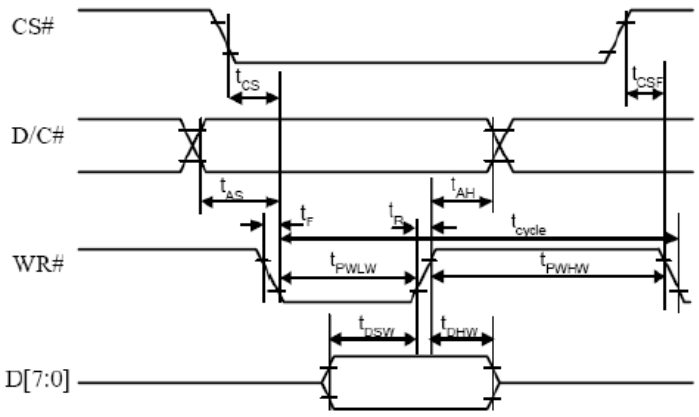
Condition 2: /CS low pulse width < E high pulse width



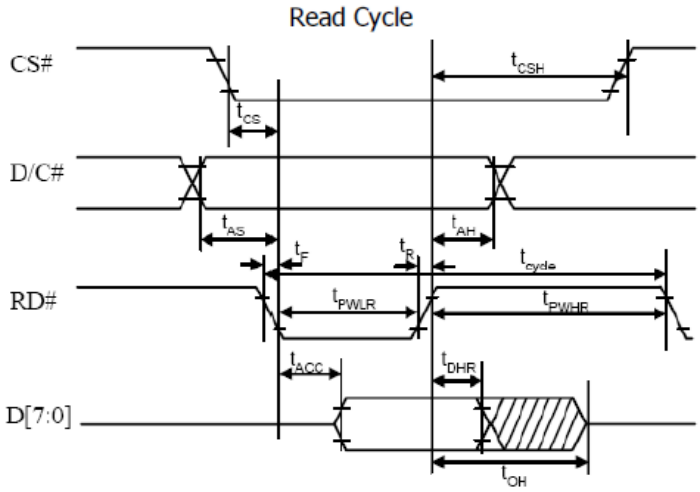
8080-Series Parallel Interface:

Symbol	Parameter	Min	Typ	Max	Unit
t_{cycle}	Clock Cycle Time (write cycle)	400	-	-	ns
t_{AS}	Address Setup Time	13	-	-	ns
t_{AH}	Address Hold Time	17	-	-	ns
t_{CS}	Chip Select Time	0	-	-	ns
t_{CSH}	Chip Select hold time to read signal	0	-	-	ns
t_{DSW}	Write Data Setup Time	35	-	-	ns
t_{DHW}	Write Data Hold Time	18	-	-	ns
t_{DHR}	Read Data Hold Time	13	-	-	ns
t_{OH}	Output Disable Time	10	-	70	ns
t_{ACC}	Access Time (RAM) Access Time (command)	-	-	125	ns
PW_{CSL}	Chip Select Low Pulse Width (read RAM) - t_{PWLR} Chip Select Low Pulse Width (read Command) - t_{PWLR} Chip Select Low Pulse Width (write) - t_{PWLW}	250 250 50	- - -	- - -	ns ns ns
PW_{CSH}	Chip Select High Pulse Width (read) - t_{PWHR} Chip Select High Pulse Width (write) - t_{PWHW}	155 55	- -	- -	ns ns
t_R	Rise Time	-	-	15	ns
t_F	Fall Time	-	-	15	ns

Write cycle

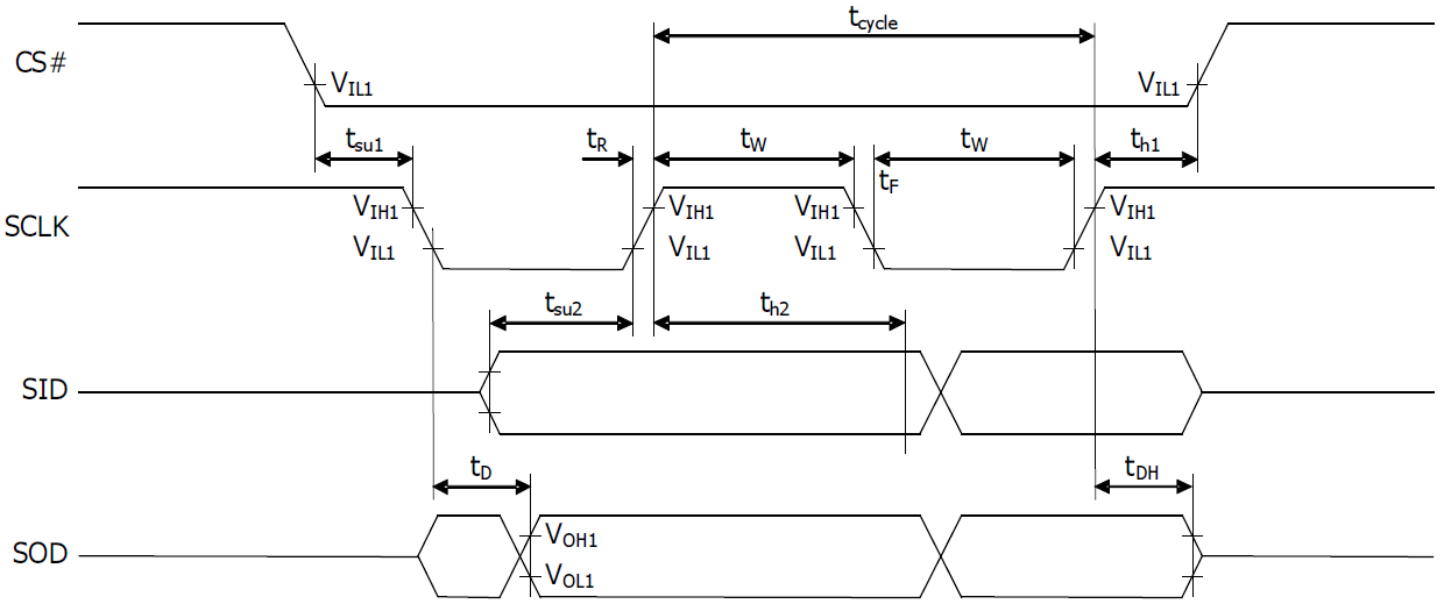


Read Cycle



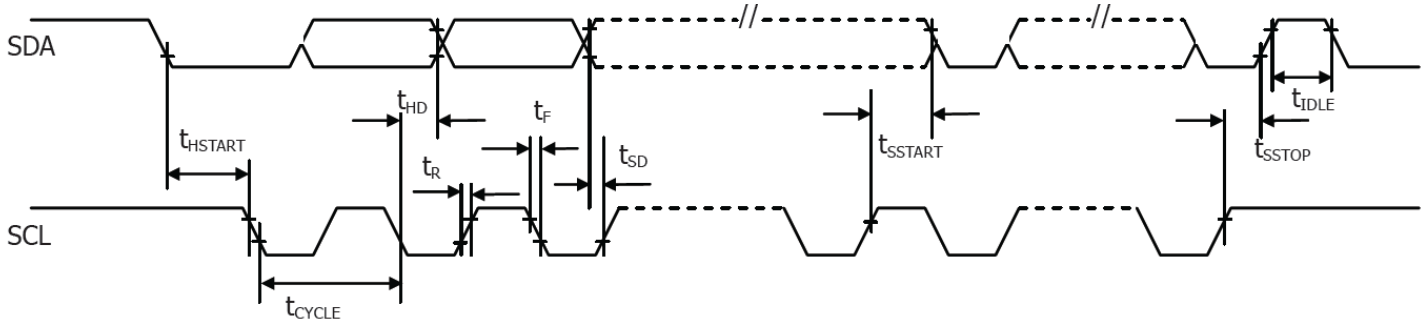
Serial Interface:

Symbol	Parameter	Min	Typ	Max	Unit
t_C	Serial Clock Cycle Time	1	-	20	µs
t_R, t_F	Serial clock rise/fall time	-	-	15	ns
t_W	Serial clock width (high, low)	400	-	-	ns
t_{su1}	Chip select setup time	60	-	-	ns
t_{h1}	Chip select hold time	20	-	-	ns
t_{su2}	Serial input data setup time	200	-	-	ns
t_{h2}	Serial input data hold time	TBD	-	-	ns
t_D	Serial output data delay time	-	-	TBD	ns
t_{DH}	Serial output data hold time	10	-	70	ns



I²C Interface:

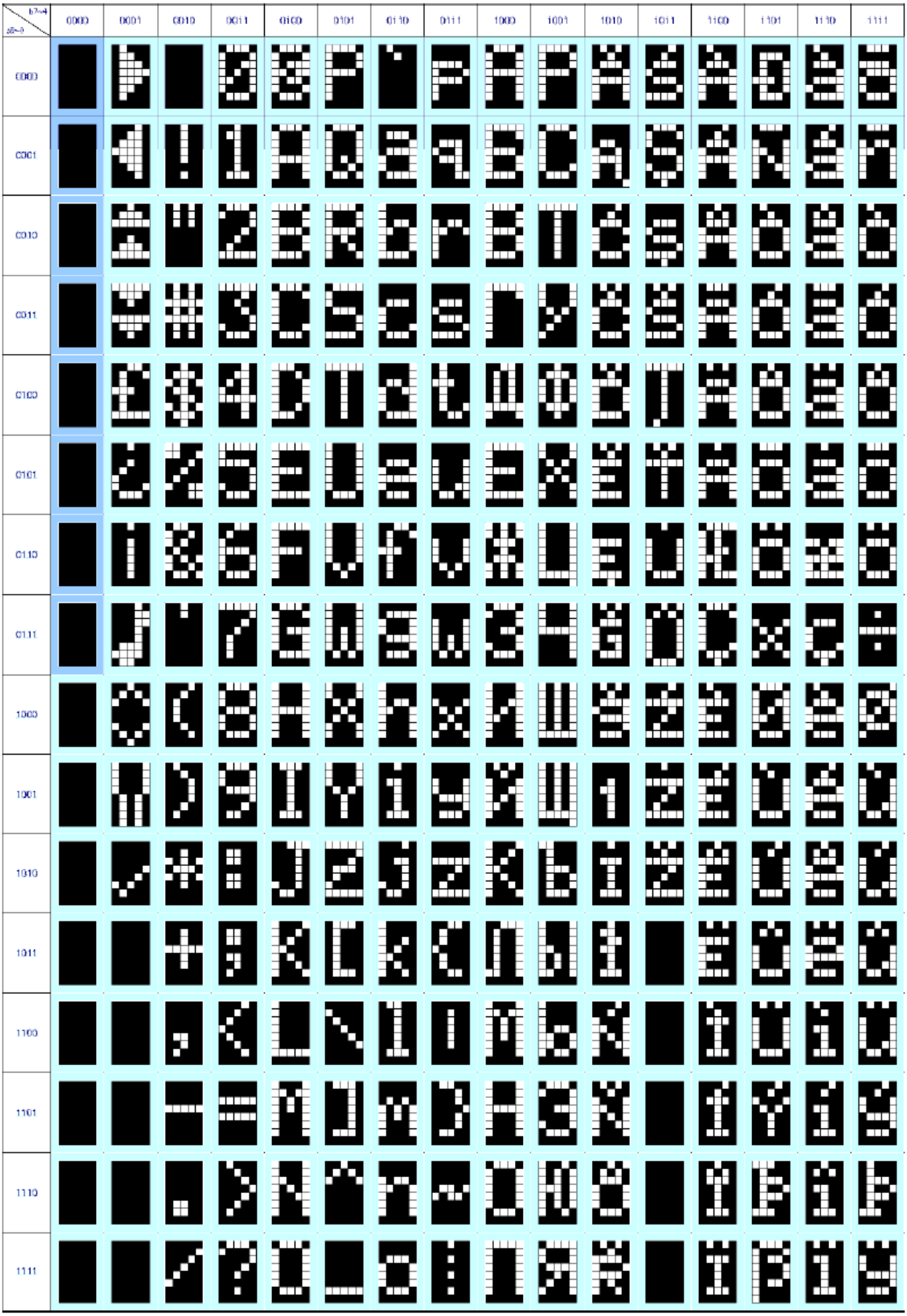
Symbol	Parameter	Min	Typ	Max	Unit
t_{cycle}	Clock Cycle Time	2.5	-	-	µs
t_{HSTART}	Start Condition Hold Time	0.6	-	-	µs
t_{HD}	Data Hold Time (for "SDA_{OUT}" pin)	5	-	-	ns
	Data Hold Time (for "SDA_{IN}" pin)	300	-	-	ns
t_{SD}	Data Setup Time	100	-	-	ns
t_{SSTART}	Start condition setup time (Only for a repeated Start Condition)	0.6	-	-	µs
t_{SSTOP}	Stop condition Setup Time	0.6	-	-	µs
t_R	Rise Time for data and clock pin	-	-	300	ns
t_F	Fall Time for data and clock pin	-	-	300	ns
t_{IDLE}	Idle Time before a new transmission can start	1.3	-	-	µS



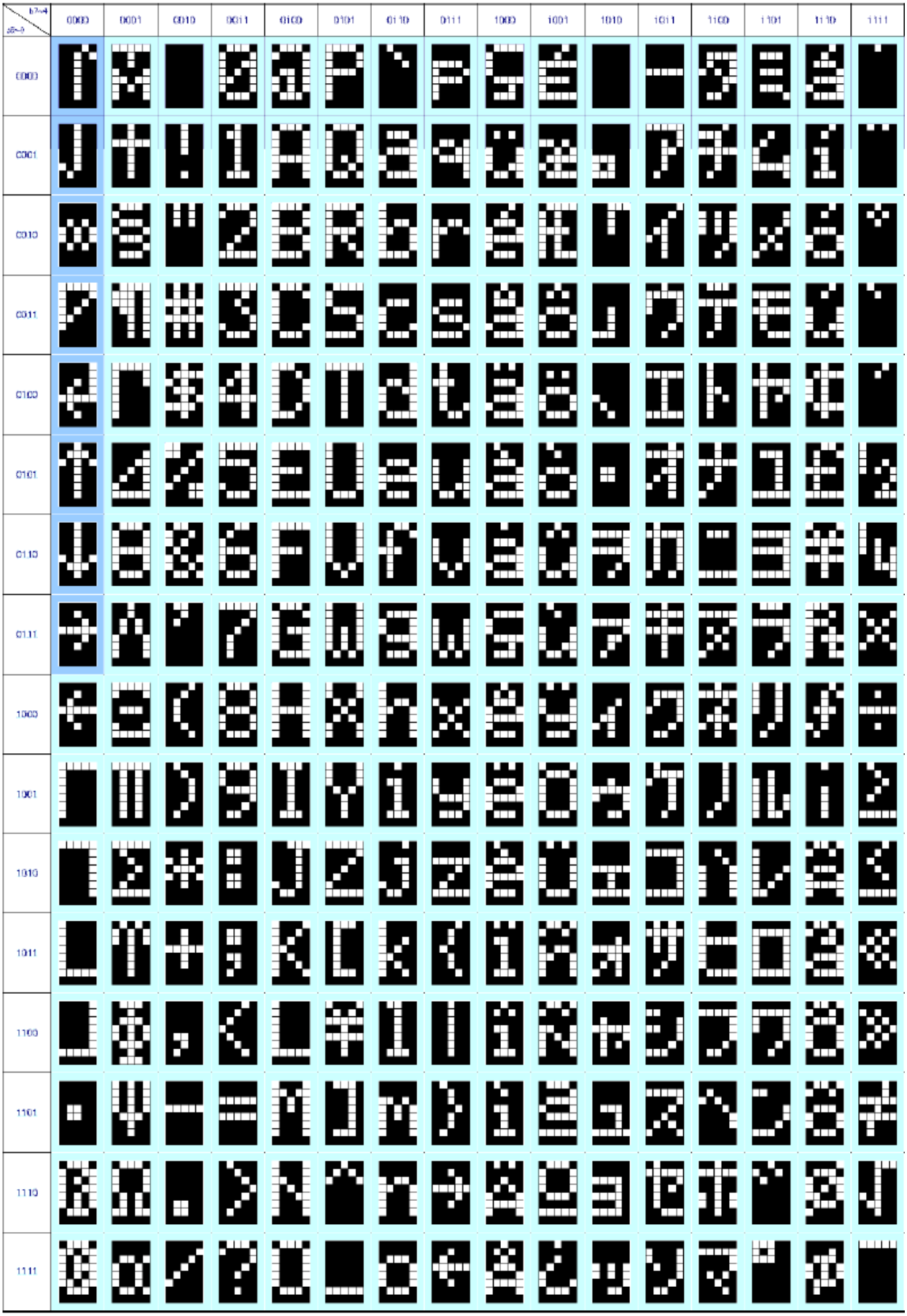
Built-in Font Tables

ROM A (ROM[1:0] = [0:0])

ROM B (ROM[1:0] = [0:1])



ROM C (ROM[1:0] = [1:0])



Example Program Code

```
void command(char i)
{
        C_S = 0;        //chip select LOW – active
        P1 = i;         //data on port
        D_C = 0;        //data/command select LOW – command
        R_W = 0;        //read/write select LOW – write
        E  = 1;         //enable HIGH
        delayms(1);     //delay
        E  = 0;         //enable LOW – data latched
}
```

```
void data(char i)
{
        C_S = 0;        //chip select LOW – active
        P1 = i;         //data on port
        D_C = 1;        //data/command select HIGH – data
        R_W = 0;        //read/write select LOW – write
        E  = 1;         //enable HIGH
        delayms(1);     //delay
        E  = 0;         //enable LOW – data latched
}
```

```
void output()
{
        int i;
        command(0x01);          //clear display
        command(0x02);          //return home
        for(i=0;i<20;i++)
        {
                data(0x1F);     //write solid blocks
        }
        command(0xA0);          //line 2
        for(i=0;i<20;i++)
        {
                data(0x1F);     //write solid blocks
        }
        command(0xC0);          //line 3
        for(i=0;i<20;i++)
        {
                data(0x1F);     //write solid blocks
        }
        command(0xE0);          //line 4
        for(i=0;i<20;i++)
        {
                data(0x1F);     //write solid blocks
        }
}
```

```
void init()
```

```
{
        RES = 1;                //reset HIGH – inactive
        delayms(1);             //delay
        command(0x2A);          //function set (extended command set)
        command(0x71);          //function selection A
        data(0x00);             // disable internal VDD regulator (2.8V I/O). data(0x5C) = enable regulator (5V I/O)
        command(0x28);          //function set (fundamental command set)
        command(0x08);          //display off, cursor off, blink off
        command(0x2A);          //function set (extended command set)
        command(0x79);          //OLED command set enabled
        command(0xD5);          //set display clock divide ratio/oscillator frequency
        command(0x70);          //set display clock divide ratio/oscillator frequency
        command(0x78);          //OLED command set disabled
        command(0x09);          //extended function set (4-lines)
        command(0x06);          //COM SEG direction
        command(0x72);          //function selection B
        data(0x00);             //ROM CGRAM selection
        command(0x2A);          //function set (extended command set)
        command(0x79);          //OLED command set enabled
        command(0xDA);          //set SEG pins hardware configuration
        command(0x10);          //set SEG pins hardware configuration
        command(0xDC);          //function selection C
        command(0x00);          //function selection C
        command(0x81);          //set contrast control
        command(0x7F);          //set contrast control
        command(0xD9);          //set phase length
        command(0xF1);          //set phase length
        command(0xDB);          //set VCOMH deselect level
        command(0x40);          //set VCOMH deselect level
        command(0x78);          //OLED command set disabled
        command(0x28);          //function set (fundamental command set)
        command(0x01);          //clear display
        command(0x80);          //set DDRAM address to 0x00
        command(0x0C);          //display ON
        delayms(100);           //delay
}
```

```
void main(void)
{
        init();
        while(1)
        {
                output();
                delayms(2000);
        }
}
```

Quality Information

Test Item	Content of Test	Test Condition	Note
High Temperature storage	Test the endurance of the display at high storage temperature.	+90°C , 240hrs	2
Low Temperature storage	Test the endurance of the display at low storage temperature.	-40°C , 240hrs	1,2
High Temperature Operation	Test the endurance of the display by applying electric stress (voltage & current) at high temperature.	+85°C 240hrs	2
Low Temperature Operation	Test the endurance of the display by applying electric stress (voltage & current) at low temperature.	-40°C , 240hrs	1,2
High Temperature / Humidity Operation	Test the endurance of the display by applying electric stress (voltage & current) at high temperature with high humidity.	+60°C , 90% RH , 240hrs	1,2
Thermal Shock resistance	Test the endurance of the display by applying electric stress (voltage & current) during a cycle of low and high temperatures.	-40°C,30min -> 25°C,5min -> 85°C,30min = 1 cycle 100 cycles	
Vibration test	Test the endurance of the display by applying vibration to simulate transportation and use.	10-22Hz , 1.5mm amplitude. 22-500Hz, 1.5G 30min in each of 3 directions X,Y,Z	3
Static electricity test	Test the endurance of the display by applying electric static discharge.	V_S=800V, R_S=1.5kΩ, C_S=100pF One time	

Note 1: No condensation to be observed.
Note 2: Conducted after 2 hours of storage at 25°C, 0%RH.
Note 3: Test performed on product itself, not inside a container.
Evaluation Criteria:
1: Display is fully functional during operational tests and after all tests, at room temperature.
2: No observable defects.
3: Luminance >50% of initial value.
4: Current consumption within 50% of initial value