

Preliminary Specifications Subject to Change without Notice

DESCRIPTION

The JW[®]5393 and JW[®]5393F are monolithic buck switching regulators based on I2 architecture for fast transient response. Operating with an input range of 4.5V~18V, JW5393 and JW5393F deliver 3A of continuous output current with two integrated N-Channel MOSFETs. The internal synchronous power switches provide high efficiency without the use of an external Schottky diode. At light loads, JW5393 operates in low frequency to maintain high efficiency.

JW5393 and JW5393F guarantee robustness with output short protection, thermal protection, current run-away protection and input under voltage lockout.

JW5393 and JW5393F are available in SOT563 package, which provide a compact solution with minimal external components.

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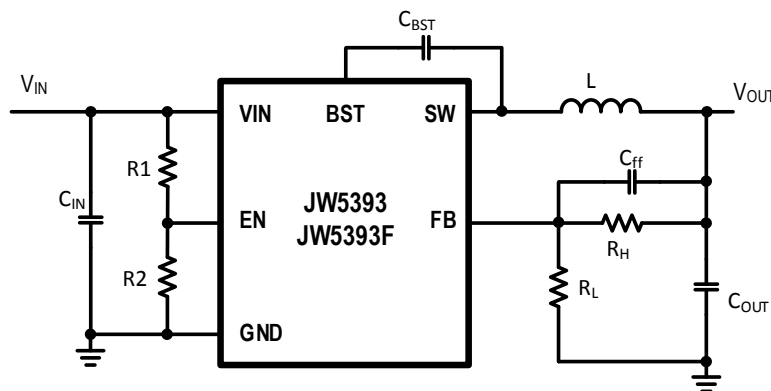
FEATURES

- 4.5V to 18V operating input range
- 3A output current
- Up to 95% efficiency
- PFM mode (JW5393) at light load
- FCC mode (JW5393F) at light load
- 600kHz switching frequency
- Internal soft-start
- Input under voltage lockout
- Current run-away protection
- Output short protection
- Thermal protection
- Available in SOT563 package

APPLICATIONS

- Distributed Power Systems
- Networking Systems
- FPGA, DSP, ASIC Power Supplies
- Green Electronics/ Appliances
- Notebook Computers

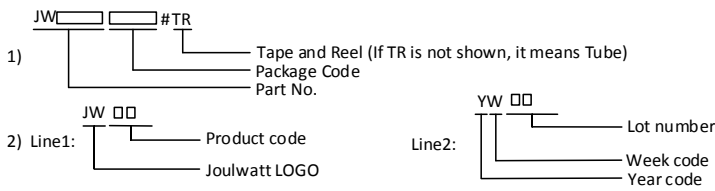
TYPICAL APPLICATION



ORDER INFORMATION

DEVICE ¹⁾	PACKAGE	TOP MARKING ²⁾	ENVIRONMENTAL ³⁾
JW5393SOTI#TR	SOT563	JW7□ YW□□	Green
JW5393FSOTI#TR	SOT563	JW8□ YW□□	Green

Notes:

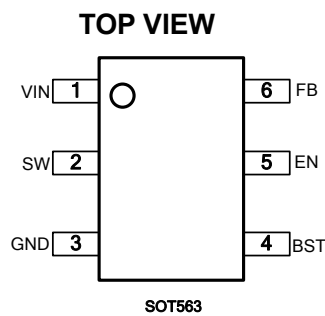


3) All Joulwatt products are packaged with Pb-free and Halogen-free materials and compliant to RoHS standards.

DEVICE INFORMATION

DEVICE	Operation Mode at light load	Function	Package
JW5393SOTI#TR	PFM	-	SOT563
JW5393FSOTI#TR	FCCM	-	SOT563

PIN CONFIGURATION



ABSOLUTE MAXIMUM RATING¹⁾

VIN, EN Pin.....	-0.3V to 20V
SW Pin.....	-0.3V(-5V for 10ns) to 20V(22V for 10ns)
BST Pin.....	SW-0.3V to SW+4V
All other Pins	-0.3V to 4V
Junction Temperature ²⁾	150°C
Lead Temperature	260°C
Storage Temperature	-65°C to +150°C

RECOMMENDED OPERATING CONDITIONS³⁾

Input Voltage VIN	4.5V to 18V
Output Voltage VOUT	0.8V to VIN*Dmax
Operating Junction Temperature.....	-40°C to +125°C

THERMAL PERFORMANCE⁴⁾

	θ_{JA}	θ_{JC}
SOT563.....	145.....	45°C/W

Note:

- 1) Exceeding these ratings may damage the device. These stress ratings do not imply function operation of the device at any other conditions beyond those indicated under RECOMMENDED OPERATING CONDITIONS.
- 2) The JW5393 and JW5393F include thermal protection that is intended to protect the device in overload conditions. Continuous operation over the specified absolute maximum operating junction temperature may damage the device.
- 3) The device is not guaranteed to function outside of its operating conditions.
- 4) Measured on JESD51-7, 4-layer PCB.

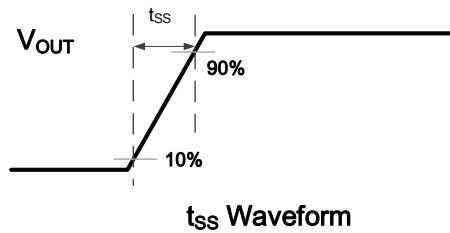
ELECTRICAL CHARACTERISTICS

V_{IN}=12V, T_J=25°C, unless otherwise stated.

Item	Symbol	Conditions	Min.	Typ.	Max.	Unit
V _{IN} Under Voltage Lock-out Threshold	V _{IN_MIN}	V _{IN} rising	4.0	4.2	4.5	V
V _{IN} Under Voltage Lock-out Hysteresis	V _{IN_MIN_HYST}			350		mV
Shutdown Supply Current	I _{SD}	V _{EN} =0V			1	μA
Supply Current	I _Q	V _{EN} =5V, V _{FB} =1.2V		150	220	μA
Feedback Voltage	V _{FB}	4.5≤V _{IN} ≤18V	792	800	808	mV
		T _J =-40 °C~125 °C	784	800	816	mV
FB Leakage Current	I _{FB}	V _{FB} =0.85V			100	nA
Top Switch Resistance	R _{DS(ON)T}			65		mΩ
Bottom Switch Resistance	R _{DS(ON)B}			38		mΩ
Top Switch Leakage Current	I _{LEAK_TOP}	V _{IN} =18V, V _{EN} =0V, V _{SW} =0V			1	μA
Bottom Switch Leakage Current	I _{LEAK_BOT}	V _{IN} =18, V _{EN} =0V, V _{SW} =18V			4	μA
Bottom Switch Current Limit	I _{LIM_BOT}		3	3.5	4	A
Negative Current Limit	I _{LIM_NEG}	JW5393F	-1.27	-1.5	-1.72	A
Minimum On Time ⁵⁾	T _{ON_MIN}			100		ns
Minimum Off Time	T _{OFF_MIN}	V _{FB} =0.4V		120		ns
Maximum On Time	T _{ON_Max}			4		us
EN Rising Threshold	V _{EN_H}	V _{EN} rising	1.1	1.2	1.3	V
EN Falling Threshold	V _{EN_L}	V _{EN} falling	0.98	1.05	1.12	V
Switching Frequency	F _{SW}		480	600	720	kHz
Soft-Start Period ⁵⁾⁶⁾	t _{SS}		1	1.4	2	ms
Thermal Shutdown ⁵⁾	T _{TSD}			160		°C
Thermal Shutdown Hysteresis ⁵⁾	T _{TSD_HYST}			20		°C

Note:

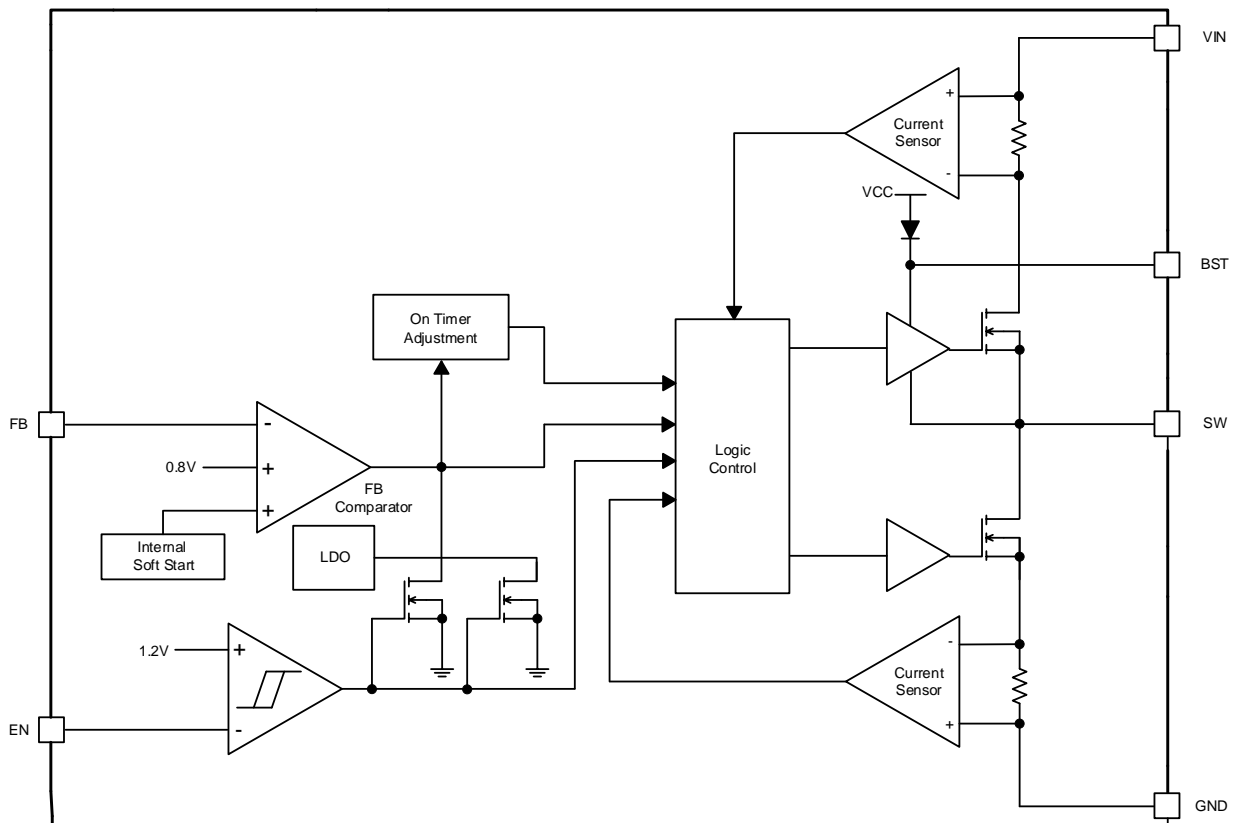
- 5) Guaranteed by design.
- 6) Soft-Start Period is tested from 10% to 90% of the steady state output voltage.



PIN DESCRIPTION

SOT563	Name	Description
1	VIN	Input voltage pin. VIN supplies power to the IC. Connect a 4.5V to 18V supply to VIN and bypass VIN to GND with a suitably large capacitor to eliminate noise on the input to the IC.
2	SW	SW is the switching node that supplies power to the output. Connect the output LC filter from SW to the output load.
3	GND	Ground pin.
4	BST	Connect a 0.1µF capacitor between BST and SW pin to supply current for the top switch driver.
5	EN	Drive EN pin high to turn on the regulator and low to turn off the regulator.
6	FB	Output feedback pin. FB senses the output voltage and is regulated by the control loop to 0.8 V. Connect a resistive divider at FB.

BLOCK DIAGRAM



FUNCTIONAL DESCRIPTION

JW5393 and JW5393F are synchronous step-down regulators based on I2 control architecture. It regulates input voltages from 4.5V to 18V down to an output voltage as low as 0.8V, and is capable of supplying up to 3A of load current.

Shut-Down Mode

The regulator shuts down when voltage at EN pin is driven below 0.4V. The entire regulator is off and the supply current consumed by the regulator drops below 1 μ A.

Power Switch

N-Channel MOSFET switches are integrated on the JW5393 and JW5393F to down convert the input voltage to the regulated output voltage. Since the top MOSFET needs a gate voltage great than the input voltage, a boost capacitor connected between BST and SW pins is required to drive the gate of the top switch. The boost capacitor is charged by the internal 3.3V rail when SW is low.

V_{IN} Under-Voltage Protection

A resistive divider can be connected between V_{IN} and ground, with the central tap connected to EN, so that when V_{IN} drops to the pre-set value, EN drops below 1.05V to trigger input under voltage lockout protection.

Output Current Run-Away Protection

At start-up, due to the high voltage at input and low voltage at output, current inertia of the output inductor can be easily built up, resulting in a large start-up output current. A valley current limit is designed in JW5393 and JW5393F so that only when output current drops below the valley current limit can the top power switch be turned on. By such control mechanism, the output current at start-up is well controlled.

Output Short Protection

When the output is shorted to ground, the regulator is allowed to switch for 2048 cycles. If the short condition is cleared within this period, then the regulator resumes normal operation. If the short condition is still present after 2048 switching cycles, then no switching is allowed and the regulator enters hiccup mode for 6144 cycles. After the 6144 hiccup cycles, the regulator will try to start-up again. If the short condition still exists after 2048 cycles of switching, the regulator enters hiccup mode. This process of start-up and hiccup iterate itself until the short condition is removed.

Thermal Protection

When the temperature of the regulator rises above 160°C, it is forced into thermal shut-down. Only when core temperature drops below 140°C can the regulator become active again.

APPLICATION INFORMATION

Output Voltage Set

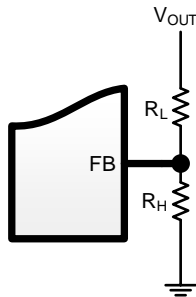
The output voltage is determined by the resistor divider connected at the FB pin, and the voltage ratio is:

$$V_{FB} = V_{OUT} * \frac{R_L}{R_H + R_L}$$

where V_{FB} is the feedback voltage and V_{OUT} is the output voltage.

If R_L is determined, and then R_H can be calculated by:

$$R_H = R_L * \left(\frac{V_{OUT}}{0.8} - 1 \right)$$



Input Capacitor

The input capacitor is used to supply the AC input current to the step-down converter and maintaining the DC input voltage. The ripple current through the input capacitor can be calculated by:

$$I_{CIN} = I_{OUT} * \sqrt{\frac{V_{OUT}}{V_{IN}} * \left(1 - \frac{V_{OUT}}{V_{IN}} \right)}$$

where I_{OUT} is the load current, V_{OUT} is the output voltage, V_{IN} is the input voltage.

Thus the input capacitor can be calculated by the following equation when the input ripple voltage is determined.

$$C_{IN} = \frac{I_{OUT}}{f_s * \Delta V_{IN}} * \frac{V_{OUT}}{V_{IN}} * \left(1 - \frac{V_{OUT}}{V_{IN}} \right)$$

where C_{IN} is the input capacitance value, f_s is

the switching frequency, ΔV_{IN} is the input ripple voltage.

The input capacitor can be electrolytic, tantalum or ceramic. To minimizing the potential noise, a small X5R or X7R ceramic capacitor, i.e. 0.1 μ F, should be placed as close to the IC as possible when using electrolytic capacitors.

A 22 μ F/25V ceramic capacitor is recommended in typical application.

Output Capacitor

The output capacitor is required to maintain the DC output voltage, and the capacitance value determines the output ripple voltage. The output voltage ripple can be calculated by:

$$\Delta V_{OUT} = \frac{V_{OUT}}{f_s * L} * \left(1 - \frac{V_{OUT}}{V_{IN}} \right) * \left(R_{ESR} + \frac{1}{8 * f_s * C_{OUT}} \right)$$

where C_{OUT} is the output capacitance value and R_{ESR} is the equivalent series resistance value of the output capacitor.

The output capacitor can be low ESR electrolytic, tantalum or ceramic, which lower ESR capacitors get lower output ripple voltage. The output capacitors also affect the system stability and transient response, and a 22 μ F~44 μ F ceramic capacitor is recommended in typical application.

Inductor

The inductor is used to supply constant current to the output load, and the value determines the ripple current which affect the efficiency and the output voltage ripple. The ripple current is typically allowed to be 40% of the maximum switch current limit, thus the inductance value can be calculated by:

$$L = \frac{V_{OUT}}{f_s * \Delta I_L} * \left(1 - \frac{V_{OUT}}{V_{IN}}\right)$$

where V_{IN} is the input voltage, V_{OUT} is the output voltage, f_s is the switching frequency, and ΔI_L is the peak-to-peak inductor ripple current.

External Bootstrap Capacitor

The bootstrap capacitor is required to supply voltage to the top switch driver. A 0.1µF low ESR ceramic capacitor is recommended to be connected to the BST pin and SW pin.

PCB Layout Note

For minimum noise problem and best operating performance, the PCB is preferred to following the guidelines as reference.

1. Place the input decoupling capacitor as close to JW5393/JW5393F (VIN pin and GND pin) as possible to eliminate noise at the input pin. The loop area formed by input capacitor and GND must be minimized.
2. Put the feedback trace as short as possible, and far away from the inductor and noisy power traces like SW node.

3. The ground plane on the PCB should be as large as possible for better heat dissipation.
4. Keep the switching node SW short to prevent excessive capacitive coupling
5. Make V_{IN} , V_{OUT} and ground bus connections as wide as possible. This reduces any voltage drops on the input or output paths of the converter and maximizes efficiency.

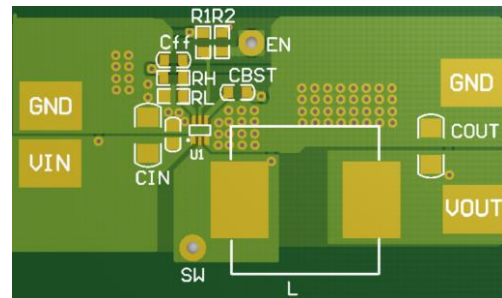


Figure 1. PCB Layout Recommendation

PACKAGE OUTLINE

SOT563	UNIT: mm
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SYMBOL	MILLIMETER		
	MIN	NOM	MAX
A	0.525	—	0.60
A1	0.00	—	0.05
b	0.17	0.22	0.27
c	0.09	—	0.18
D	1.50	1.60	1.70
E	1.50	1.60	1.70
E1	1.10	1.20	1.30
e	0.45	0.50	0.55
L	0.10	0.20	0.30
L1	0.20	0.30	0.4
θ	9° REF		

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE

Package Type	Pin1 Quadrant
SOT563	3

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