Cyclone III LS FPGA Development Board

Reference Manual

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Contents

Additional Information

1. Overview

Introduction

This document describes the hardware features of the Cyclone® III LS FPGA development board, including the detailed pin-out and component reference information required to create custom FPGA designs that interface with all components of the board.

General Description

The Cyclone III LS FPGA development board provides a hardware platform for developing and prototyping low-power, secure, high-volume, feature-rich designs as well as to demonstrate the Cyclone III LS device's on-chip memory, embedded multipliers, and the Nios® II embedded soft processor. The board provides a wide range of peripherals and memory interfaces to facilitate the development of the Cyclone III LS FPGA designs.

Two high-speed mezzanine card (HSMC) connectors are available to add additional functionality via a variety of HSMCs available from Altera® and various partners.

To see a list of the latest HSMCs available or to download a copy of the HSMC specification, refer to the Development Board Daughtercards page of the Altera website (www.altera.com).

The Cyclone III LS FPGAs are the first to offer a suite of security features at the silicon, software, and intellectual property (IP) level on a low-power, high-functionality FPGA. This suite of security features protects your IP from tampering, reverse engineering, and cloning. Additionally, these devices enable you to introduce redundancy in a single chip using design separation, which in turn reduces the size, weight, and power of your applications.

The Cyclone III LS FPGA development board is especially suitable for low-power, secure, logic-rich applications that require stringent signal and power integrity solutions.

For more information on the following topics, refer to the respective documents:

- Cyclone III device family, refer to the *Cyclone III Device Handbook*.
- Cyclone III LS security features, refer to the Partitioning FPGA Designs for Redundancy and Information Security Webcast page of the Altera website.
- HSMC Specification, refer to the *High Speed Mezzanine Card (HSMC) Specification*.

Board Component Blocks

The board features the following major component blocks:

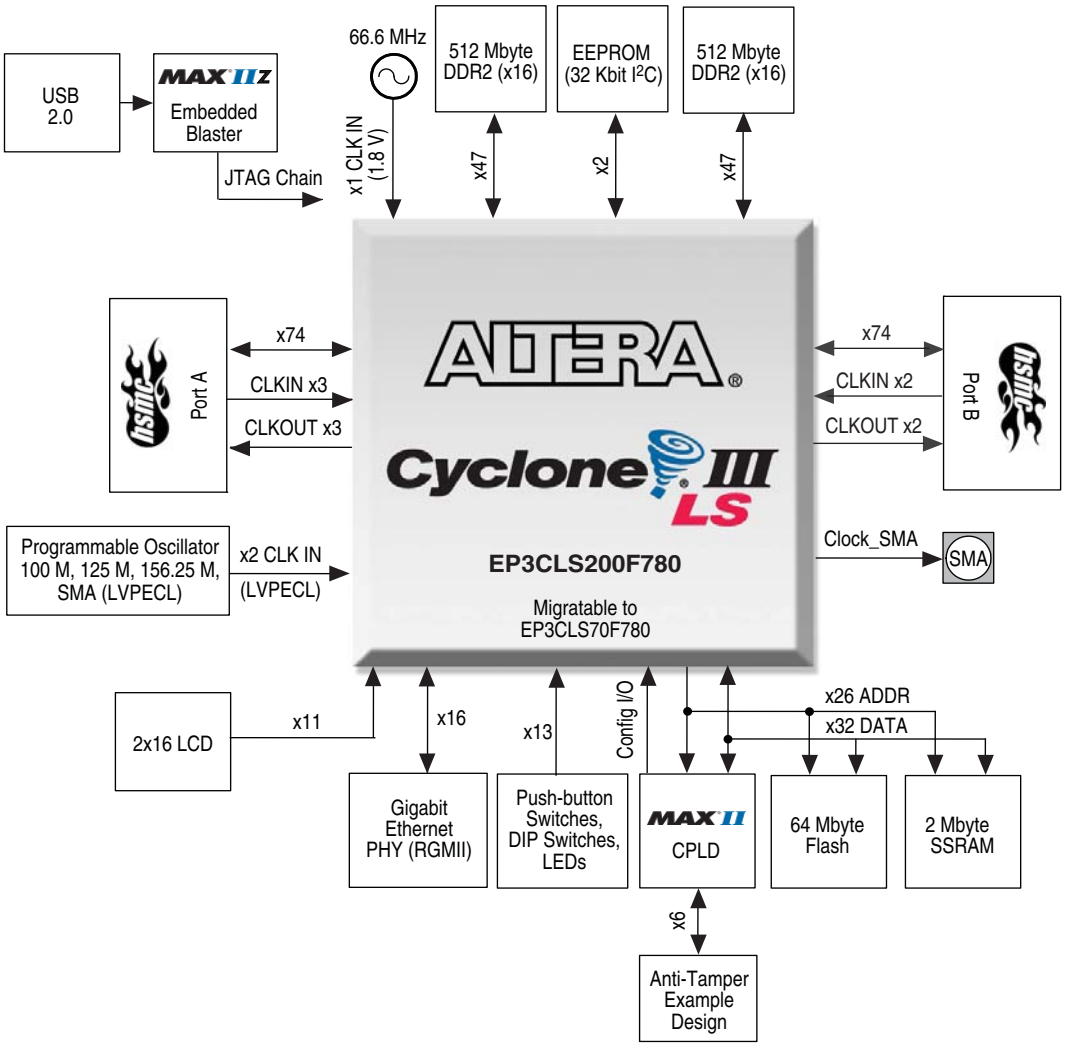
- Cyclone III LS EP3CLS200F780 FPGA in the 780-pin FineLine BGA (FBGA) package
  - 198,464 LEs
  - 8,211 Kbit on-die memory
  - 20 global clocks
  - 413 user I/O
  - 4 phase locked loops (PLLs)
  - 396 18x18 multipliers
  - 1.2-V core power
- MAX® II EPM2210F256 CPLD in the 256-pin FBGA package
  - 2.5-V core power
- FPGA configuration circuitry
  - MAX II CPLD EPM2210 System Controller and flash passive serial (PS) configuration
  - On-board USB-Blaster™ for use with the Quartus® II Programmer
- On-Board ports
  - Two HSMC expansion ports
  - One gigabit Ethernet port
- On-Board memory
  - Two 512-Mbit 64-bit DDR2
  - 2-Mbyte Synchronous Static Random Access Memory (SSRAM)
  - 64-Mbyte flash
  - I²C EEPROM
- On-Board clocking circuitry
  - Four on-board oscillators
    - 50-MHz oscillator
    - 66.6-MHz oscillator
    - 100-MHz oscillator
    - Programmable oscillator with a default frequency of 125-MHz
  - LVPECL SMA connectors for external clock input
  - LVDS SMA connectors for external clock output
  - SMA connector for FPGA clock output

- General user I/O
  - LEDs and display
    - Four user LEDs
    - Two-line character LCD display
    - One configuration done LED
    - Three anti-tamper example design status LEDs
    - Five Ethernet LEDs
  - Push-Button switches
    - One CPU reset push-button switch
    - One MAX II configuration reset push-button switch
    - One PGM configure push-button switch (configure the FPGA from flash memory)
    - One PGM select push-button switch (select image to load from flash memory)
    - One VCCA shutdown push-button switch
    - One CRC error insert push-button switch
    - Four general user push-button switches
  - DIP switches
    - Four user DIP switches
    - Eight MAX II CPLD EPM2210 System Controller DIP switches
- Power supply
  - 14-V – 20-V DC input
  - On-board power measurement circuitry

Development Board Block Diagram

Figure 1–1 shows the block diagram of the Cyclone III LS FPGA development board.

Figure 1–1. Cyclone III LS FPGA Development Board Block Diagram



Handling the Board

When handling the board, it is important to observe the following static discharge precaution:

CAUTION

Without proper anti-static handling, the board can be damaged. Therefore, use anti-static handling precautions when touching the board.

2. Board Components

Introduction

This chapter introduces the major components on the Cyclone III LS FPGA development board. Figure 2–1 illustrates major component locations and Table 2–1 provides a brief description of all component features of the board.

A complete set of schematics, a physical layout database, and GERBER files for the development board reside in the Cyclone III LS FPGA development kit documents directory.

For information about powering up the board and installing the demonstration software, refer to the *Cyclone III LS FPGA Development Kit User Guide*.

This chapter consists of the following sections:

Board Overview

This section provides an overview of the Cyclone III LS FPGA development board, including an annotated board image and component descriptions. Figure 2–1 provides an overview of the development board features.

Figure 2–1. Overview of the Cyclone III LS FPGA Development Board Features

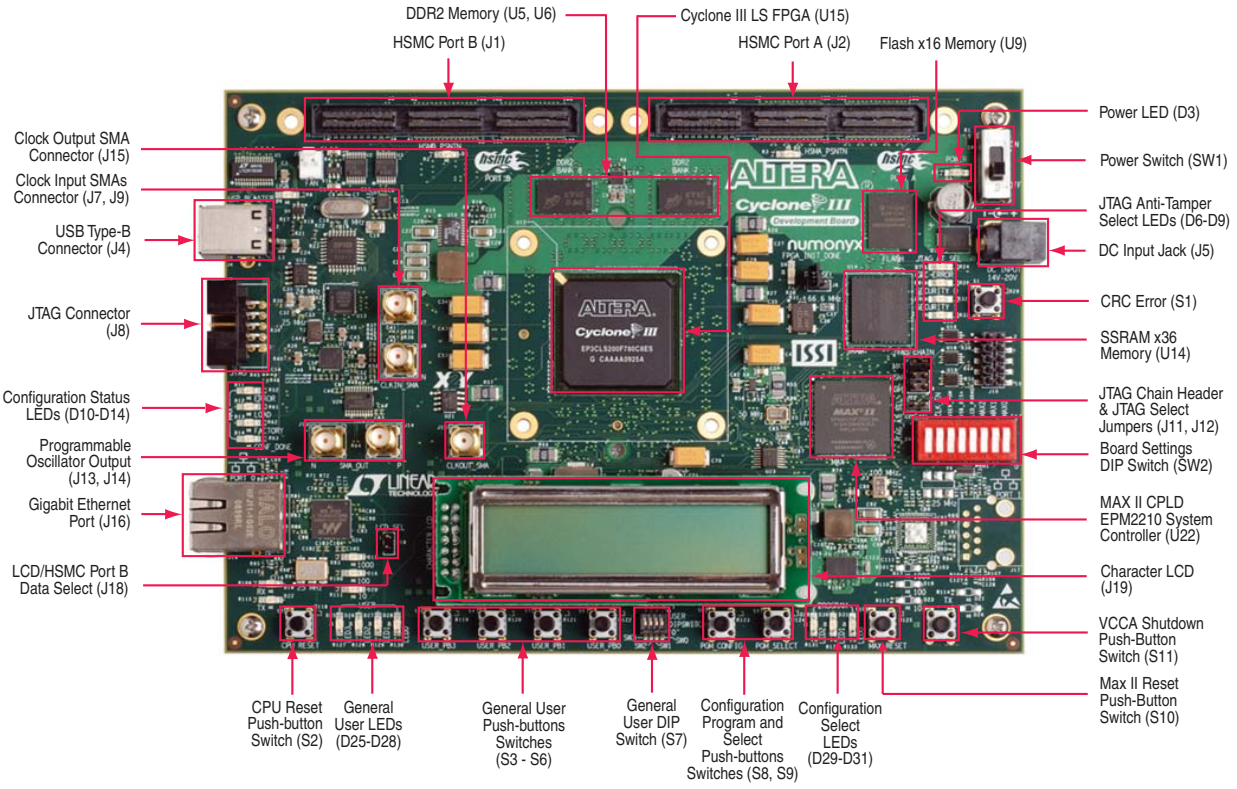


Table 2–1 describes the components and lists their corresponding board references.

Table 2–1. Cyclone III LS FPGA Development Board Components (Part 1 of 3)

Board Reference	Type	Description
Featured Devices		
U15	FPGA	EP3CLS200F780, 780-pin FBGA.
U22	CPLD	EPM2210F256, 256-pin FBGA.
Configuration, Status, and Setup Elements		
J4	USB type-B connector	Connects to the computer to enable embedded USB-Blaster JTAG.
J11	JTAG chain header	Enables and disables devices in the JTAG chain.
J12	Anti-Tamper JTAG select header	Placing a shunt on this jumper breaks the default JTAG chain, giving FPGA JTAG signals control to the MAX II EPM2210 System Controller.
D6	Anti-Tamper JTAG select LED	Illuminated when the default JTAG chain is broken and the MAX II EPM2210 System Controller has control of the FPGA JTAG signals.
SW2	Board settings DIP switch	Controls the MAX II CPLD EPM2210 System Controller functions such as clock enable, SMA clock input control, and which image to load from flash memory at power-up.
J8	JTAG connector	Disables embedded blaster (for use with external USB-Blasters).
D13	Configuration done LED	Illuminates when the FPGA is configured.

Table 2–1. Cyclone III LS FPGA Development Board Components (Part 2 of 3)

Board Reference	Type	Description
D11	Load LED	Illuminates when the MAX II CPLD EPM2210 System Controller is actively configuring the FPGA.
D10	Error LED	Illuminates when the FPGA configuration from flash memory fails.
D12	Factory LED	Illuminates when the factory image is loaded to the FPGA.
D29, D30, D31	Configuration select LEDs	Illuminates to show the LED sequence that determines which flash memory image loads to the FPGA when PGM SEL is pressed.
D15, D16, D18, D20, D22	Ethernet LEDs	Shows the connection speed as well as transmit or receive activity.
D2	HSMC port A present LED	Illuminates when a daughtercard is plugged into the HSMC port A.
D1	HSMC port B present LED	Illuminates when a daughtercard is plugged into the HSMC port B.
D3	Power LED	Illuminates when 12-V power is present.
J18	LCD/HSMC Port B data select	Controls data multiplexing to the FPGA from the LCD or HSMB_D[65:75]. Placing a shunt on the jumper allows the FPGA to control the LCD signals.
J6	PS standard/fast select	Placing a shunt sets the MSEL pins for passive serial standard configuration. Otherwise, the MSEL pins is set for passive serial fast configuration.
S2	CPU reset push-button switch	Press to reset the FPGA logic.
S11	VCCA shutdown push-button switch	Turns VCCA power to the FPGA on and off. This switch initiates a power-on reset.
S10	MAX II reset push-button switch	Press to reset the MAX II CPLD EPM2210 System Controller.
S9	PGM select push-button switch	Toggles the PGM LEDs which selects the program image that loads from flash memory to the FPGA.
S8	PGM configure push-button switch	Configure the FGPA from flash memory based on the PGM LEDs setting.
Clock Circuitry		
U17	Programmable oscillator (125 MHz default)	Programmable oscillator with a default frequency of 125.00 MHz. The frequency is programmable using the MAX II CPLD EPM2210 System Controller. For general use such as HSMC logic or gigabit Ethernet (125 M/156.25 M)
X3	66.6 MHz oscillator	66.6 MHz crystal oscillator for general purpose logic and DDR2 memory.
X5	50 MHz oscillator	50 MHz crystal oscillator for general purpose logic.
Y3	100 MHz oscillator	100 MHz crystal oscillator for configuration purpose.
J7, J9	Clock FPGA input SMAs	Drive LVPECL-compatible clock inputs into the clock multiplexer buffer (U20).
J15	Clock FPGA output SMA	Drive out 2.5-V CMOS clock output from the FPGA.
J13, J14	Clock output SMAs	LVDS output clock from the clock multiplexer buffer (U20).
General User Input/Output		
D25, D26, D27, D28	User LEDs	Four user LEDs. Illuminates when driven low.
S7	User DIP switch	Quad user DIP switches. When the switch is ON, a logic 0 is selected.

Table 2–1. Cyclone III LS FPGA Development Board Components (Part 3 of 3)

Board Reference	Type	Description
S3, S4, S5, S6	User push-button switches	Four user push-button switches. Driven low when pressed.
J19	Character LCD	Connector which interfaces to the provided 16 character × 2 line LCD module.
Memory Devices		
U5, U6	DDR2 x16 memory	Two independent 16-bit, 64-Mbyte DDR2 devices.
U14	SSRAM x36 memory	Standard synchronous RAM which makes a 36-bit 2-Mbyte SSRAM port.
U9	Flash x16 memory	Synchronous burst mode flash device which provides a 16-bit 64-Mbyte non-volatile memory port.
U21	EEPROM	I^2C EEPROM
Components and Interfaces		
J2	HSMC port A	Provides 80 CMOS or 17 LVDS channels per the HSMC specification.
J1	HSMC port B	Provides 76 CMOS channels per the HSMC specification.
J16	Gigabit Ethernet	RJ-45 connector which provides a 10/100/1000 Ethernet connection via a Marvell 88E1111 PHY and the FPGA-based Altera Triple Speed Ethernet MegaCore function in RGMII mode.
Anti-Tamper Interface		
J10	JTAG header to MAX II general I/O	JTAG header connected to general purpose I/O (GPIO) on the MAX II EPM2210 System Controller.
D8, D9, D10	Anti-Tamper status LEDs	Three anti-tamper status indicator LEDs.
S1	CRC error push-button	Insert a CRC error when running the anti-tamper example design.
Power Supply		
J5	DC input jack	Accepts a 14-V – 20-V DC power supply.
SW1	Power switch	Switch to power on or off the board when power is supplied from the DC input jack.

Featured Device: Cyclone III LS Device

The Cyclone III LS FPGA development board features the Cyclone III LS EP3CLS200F780 device (U15) in a 780-pin FBGA package.

For more information about Cyclone III device family, refer to the *Cyclone III Device Handbook*.

Table 2–2 describes the features of the Cyclone III LS EP3CLS200F780 device.

Table 2–2. Cyclone III LS Device EP3CLS200F780 Features

Equivalent LEs	M9K RAM Blocks	Total RAM Kbits	18-bit × 18-bit Multipliers	PLLs	Package Type
198,464	891	8,211	396	4	780-pin FBGA

Table 2–3 lists the Cyclone III LS device component reference and manufacturing information.

Table 2–3. Cyclone III LS Device Component Reference and Manufacturing Information

Board Reference	Description	Manufacturer	Manufacturing Part Number	Manufacturer Website
U15	FPGA, Cyclone III LS F780, 198K LEs, lead-free	Altera Corporation	EP3CLS200F780C7N	www.altera.com

I/O Resources

Figure 2–2 illustrates the bank organization and I/O count for the EP3CLS200 device in the 780-pin FBGA package.

Figure 2–2. EP3CLS200 Device I/O Bank Diagram

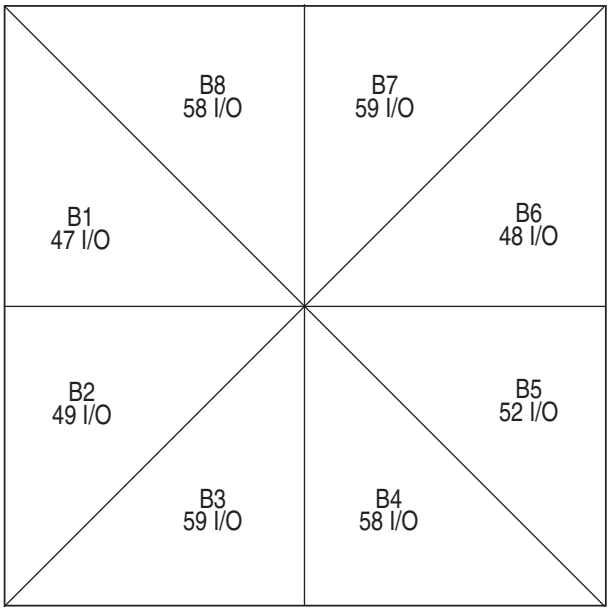


Table 2–4 lists the Cyclone III LS device pin count and usage by function on the development board.

Table 2–4. Cyclone III LS Device Pin Count and Usage (Part 1 of 2)

Function	I/O Standard	I/O Count	Special Pins
DDR2	1.8-V SSTL	94	2 differential clocks, 4 DQS
MAX Bus	2.5-V CMOS	8	—
Flash, SSRAM, FSM Bus	2.5-V CMOS	82	—
HSMC Port A	2.5-V CMOS + LVDS	84	34 LVDS, 2 differential clock inputs, 1 clock input
HSMC Port B	2.5-V CMOS	84	1 differential clock input, 1 clock input
Gigabit Ethernet	2.5-V CMOS	16	1 clock input
Buttons	1.8-V / 2.5-V CMOS	5	1 DEV_CLRn
Switches	1.8-V CMOS	5	—
LCD *(1)*	2.5-V CMOS	11	—

Table 2–4. Cyclone III LS Device Pin Count and Usage (Part 2 of 2)

Function	I/O Standard	I/O Count	Special Pins
LEDs	1.8-V CMOS	5	1 INIT_DONE
Clocks or Oscillators	1.8-V / 2.5-V CMOS + LVDS	5	2 differential clock input, 1 clock input
EEPROM	2.5-V CMOS	2	—
Device I/O Total:		**390**	

Note to Table 2–4:

(1) The LCD signals are multiplexed with HSMB_D[65:75] and therefore not included in the total pin count.

MAX II CPLD EPM2210 System Controller

The board utilizes the EPM2210 System Controller, an Altera MAX II CPLD, for the following purposes:

- FPGA configuration from flash memory
- Power consumption monitoring
- Virtual JTAG interface for PC-based GUI
- Control registers for clocks
- Control registers for remote system update
- Anti-Tamper example design

The development kit includes the anti-tamper example design in the *<install_dir>***kits\cycloneIIILS_3cls200_fpga\examples\max2\at_example\readme_at_example.txt** directory.

Figure 2–3 illustrates the MAX II CPLD EPM2210 System Controller's functionality and external circuit connections as a block diagram.

Figure 2–3. MAX II CPLD EPM2210 System Controller Block Diagram

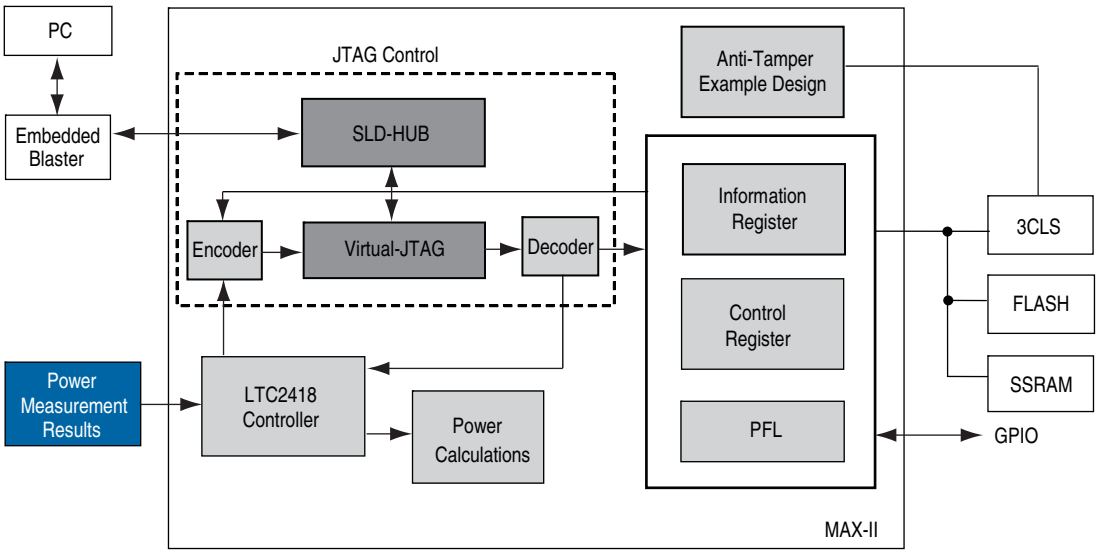


Table 2–5 lists the I/O signals present on the MAX II CPLD EPM2210 System Controller. The signal names and functions are relative to the MAX II device (U22).

Table 2–5. MAX II CPLD EPM2210 System Controller Device Pin-Out (Part 1 of 4)

Schematic Signal Name	I/O Standard	EPM2210 Pin Number	EP3CLS200 Pin Number	Description
CLK50_EN	2.5-V	H16	—	50 MHz oscillator enable
CLK66_EN		H13	—	66.6 MHz oscillator enable
CLK_CONFIG		J12	—	100 MHz configuration clock input
CLK_ENABLE		N7	—	DIP - clock oscillator enable
CLK_SEL		T5	—	DIP - clock select SMA or oscillator
CLKIN_50		J5	—	50 MHz clock input
CPU_RESETn		R8	W27	FPGA reset push-button switch
CRC_ERROR		K5	P26	FPGA CRC error
CRC_ERROR_MAX		K12	—	CRC error LED
CRC_ERROR_PB		R16	—	CRC error insert push-button switch
CRC_LATCH_SIG		K4	AF5	Anti-Tamper FPGA general I/O
FLASH_ADVn		B3	AF18	FSM bus flash memory address valid
FLASH_CEn		E6	AH22	FSM bus flash memory chip enable
FLASH_CLK		C6	AH6	FSM bus flash memory clock
FLASH_OEn		B4	AD7	FSM bus flash memory output enable
FLASH_RDYBSYn		D6	V4	FSM bus flash memory ready
FLASH_RESETn		C4	AH5	FSM bus flash memory reset
FLASH_WEn		A4	AH17	FSM bus flash memory write enable
FPGA_CONF_DONE		J1	P22	FPGA configuration done
FPGA_CONFIG_D0		D3	K1	FPGA configuration data
FPGA_DCLK		H4	L6	FPGA configuration clock
FPGA_EPM2210_TCK		C15	—	FPGA JTAG TCK
FPGA_EPM2210_TDI		E13	—	FPGA JTAG TDI
FPGA_EPM2210_TDO		E14	—	FPGA JTAG TDO
FPGA_EPM2210_TMS		C14	—	FPGA JTAG TMS
FPGA_INIT_DONE		N5	P27	FPGA INIT_DONE signal
FPGA_nCONFIG		T2	M3	FPGA configuration active
FPGA_nSTATUS		H3	M1	FPGA configuration ready
FPGA_TCK		P14	—	Anti-Tamper example design JTAG connector TCK
FPGA_TDI		P15	—	Anti-Tamper example design JTAG connector TDI
FPGA_TDO		M14	—	Anti-Tamper example design JTAG connector TDO
FPGA_TMS		N13	—	Anti-Tamper example design JTAG connector TMS
FSM_A0		C13	AG6	FSM bus address
FSM_A1		B16	AD14	FSM bus address
FSM_A2		C12	AA17	FSM bus address

Table 2–5. MAX II CPLD EPM2210 System Controller Device Pin-Out (Part 2 of 4)

Schematic Signal Name	I/O Standard	EPM2210 Pin Number	EP3CLS200 Pin Number	Description
FSM_A3	2.5-V	A15	AE12	FSM bus address
FSM_A4		D12	AF21	FSM bus address
FSM_A5		B14	AH2	FSM bus address
FSM_A6		C11	AB12	FSM bus address
FSM_A7		B13	AG24	FSM bus address
FSM_A8		D11	AE25	FSM bus address
FSM_A9		A13	AH21	FSM bus address
FSM_A10		E11	AD25	FSM bus address
FSM_A11		B12	AC9	FSM bus address
FSM_A12		C10	AF4	FSM bus address
FSM_A13		A12	AE10	FSM bus address
FSM_A14		D10	AH26	FSM bus address
FSM_A15		B11	AG22	FSM bus address
FSM_A16		E10	AF12	FSM bus address
FSM_A17		A11	AE19	FSM bus address
FSM_A18		B10	AA9	FSM bus address
FSM_A19		C9	AE6	FSM bus address
FSM_A20		A10	AG18	FSM bus address
FSM_A21		D9	AE11	FSM bus address
FSM_A22		B9	AB16	FSM bus address
FSM_A23		D4	AE13	FSM bus address
FSM_A24		B1	AG11	FSM bus address
FSM_A25		D5	AE9	FSM bus address
FSM_D0		E9	AH9	FSM bus data
FSM_D1		A9	AH24	FSM bus data
FSM_D2		A8	AF25	FSM bus data
FSM_D3		B8	AE5	FSM bus data
FSM_D4		E8	AB11	FSM bus data
FSM_D5		A7	AD24	FSM bus data
FSM_D6		D8	AF9	FSM bus data
FSM_D7		B7	AE7	FSM bus data
FSM_D8		C8	AE23	FSM bus data
FSM_D9		A6	AF15	FSM bus data
FSM_D10		B6	AD17	FSM bus data
FSM_D11		E7	AF20	FSM bus data
FSM_D12		A5	AH25	FSM bus data
FSM_D13		D7	AE18	FSM bus data
FSM_D14		B5	AD6	FSM bus data
FSM_D15		C7	AG20	FSM bus data

Table 2–5. MAX II CPLD EPM2210 System Controller Device Pin-Out (Part 3 of 4)

Schematic Signal Name	I/O Standard	EPM2210 Pin Number	EP3CLS200 Pin Number	Description
FSM_D16		N9	AH20	FSM bus data
FSM_D17		T8	AH18	FSM bus data
FSM_D18		T9	AF8	FSM bus data
FSM_D19		R9	AE20	FSM bus data
FSM_D20		P9	AB19	FSM bus data
FSM_D21		T10	AB10	FSM bus data
FSM_D22		M10	AC17	FSM bus data
FSM_D23		T11	AD10	FSM bus data
FSM_D24		N10	AG9	FSM bus data
FSM_D25		R11	AE21	FSM bus data
FSM_D26		P10	AD22	FSM bus data
FSM_D27		T12	AH23	FSM bus data
FSM_D28		M11	AG5	FSM bus data
FSM_D29		R12	AB9	FSM bus data
FSM_D30		N11	AD9	FSM bus data
FSM_D31		T13	AD16	FSM bus data
HEARTBEAT		M1	AH7	Anti-Tamper FPGA general I/O
HSMA_PRSNTn		J16	—	HSMC port A present
HSMB_PRSNTn		J13	—	HSMC port B present
JTAG_AT_SEL	2.5-V	K16	—	Jumper OFF (default): Select JTAG chain Jumper ON: MAX II controls FPGA JTAG
JTAG_SECURE		R5	—	DIP - JTAG security mode ON/OFF
M2Z_CONF_DONE		R13	—	On-board USB-Blaster FPGA configuration done
M2Z_D0		T15	—	On-board USB-Blaster FPGA configuration data
M2Z_DCLK		N12	—	On-board USB-Blaster FPGA configuration clock
M2Z_nCONFIG		R14	—	On-board USB-Blaster FPGA configuration active
M2Z_nSTATUS		M12	—	On-board USB-Blaster FPGA configuration ready
MAX2_BEn0		F5	AG21	FSM bus MAX II byte enable 0
MAX2_BEn1		F2	AF11	FSM bus MAX II byte enable 1
MAX2_BEn2		F6	AG2	FSM bus MAX II byte enable 2
MAX2_BEn3		F1	AC16	FSM bus MAX II byte enable 3
MAX2_CLK		E1	AE24	FSM bus MAX II clock
MAX2_CSn		E2	AG4	FSM bus MAX II chip select
MAX2_OEn		F3	AC10	FSM bus MAX II output enable
MAX2_WEn		F4	AA8	FSM bus MAX II write enable
MAX_CONF_DONE		E15	—	FPGA configuration done LED
MAX_DIP0		F16	—	DIP - Anti-Tamper example design
MAX_DIP1		G13	—	DIP - Anti-Tamper example design
AT_ACTIVE		F15	—	DIP - Anti-Tamper example design ON/OFF

Table 2–5. MAX II CPLD EPM2210 System Controller Device Pin-Out (Part 4 of 4)

Schematic Signal Name	I/O Standard	EPM2210 Pin Number	EP3CLS200 Pin Number	Description
MAX_ERROR	2.5-V	G3	—	FPGA configuration error LED
MAX_FACTORY		G4	—	FPGA factory configuration LED
MAX_LOAD		G2	—	FPGA configuration active LED
MAX_RESETn		M9	—	MAX II reset push-button switch
PGM_CONFIG		K2	—	Load the flash memory image identified by the PGM LEDs
PGM_LED0		J2	—	Flash memory PGM select indicator 0
PGM_LED1		J4	—	Flash memory PGM select indicator 1
PGM_LED2		K1	—	Flash memory PGM select indicator 2
PGM_SEL		J3	—	Toggles the PGM_LED[0:2] sequence
PLL_CE		L13	—	Programmable oscillator chip select
PLL_OD0		M15	—	Programmable oscillator output divider 0
PLL_OD1		L12	—	Programmable oscillator output divider 1
PLL_OD2		M16	—	Programmable oscillator output divider 2
PLL_PR0		L11	—	Programmable oscillator prescaler 0
PLL_PR1		L15	—	Programmable oscillator prescaler 1
PLL_RSTn		N16	—	Programmable oscillator reset
SECURITY		K3	AG12	Anti-Tamper FPGA general I/O
SECURITY_LED0		L1	—	Anti-Tamper example design security LED0
SECURITY_LED1		L2	—	Anti-Tamper example design security LED1
SENSE_ADC_F0		L3	—	Power monitor frequency
SENSE_CS0n		N1	—	Power monitor chip select
SENSE_SCK		L5	—	Power monitor serial peripheral interface (SPI) clock
SENSE_SDI		M3	—	Power monitor SPI data in
SENSE_SDO		L4	—	Power monitor SPI data out
SRAM_MODE		P4	—	FSM bus SSRAM burst sequence selection
SRAM_ZZ		L14	AH14	FSM bus SSRAM power sleep mode
USB_DISABLEn		G14	—	DIP - embedded USB-Blaster disable
USB_LED		F12	—	Embedded USB-Blaster active LED
USER_PGM		M6	—	DIP - factory or user load on power-up

Table 2–6 lists the MAX II CPLD EPM2210 System Controller component reference and manufacturing information.

Table 2–6. MAX II CPLD EPM2210 System Controller Component Reference and Manufacturing Information

Board Reference	Description	Manufacturer	Manufacturing Part Number	Manufacturer Website
U22	IC - MAX II CPLD EPM2210 256FBGA -3 LF 2.5 V VCCINT	Altera Corporation	EPM2210F256C3N	www.altera.com

Configuration, Status, and Setup Elements

This section describes the board's configuration, status, and setup elements.

Configuration

This section describes the FPGA, flash memory, and MAX II CPLD EPM2210 System Controller device programming methods supported by the Cyclone III LS FPGA development board. The Cyclone III LS FPGA development board supports the following three configuration methods:

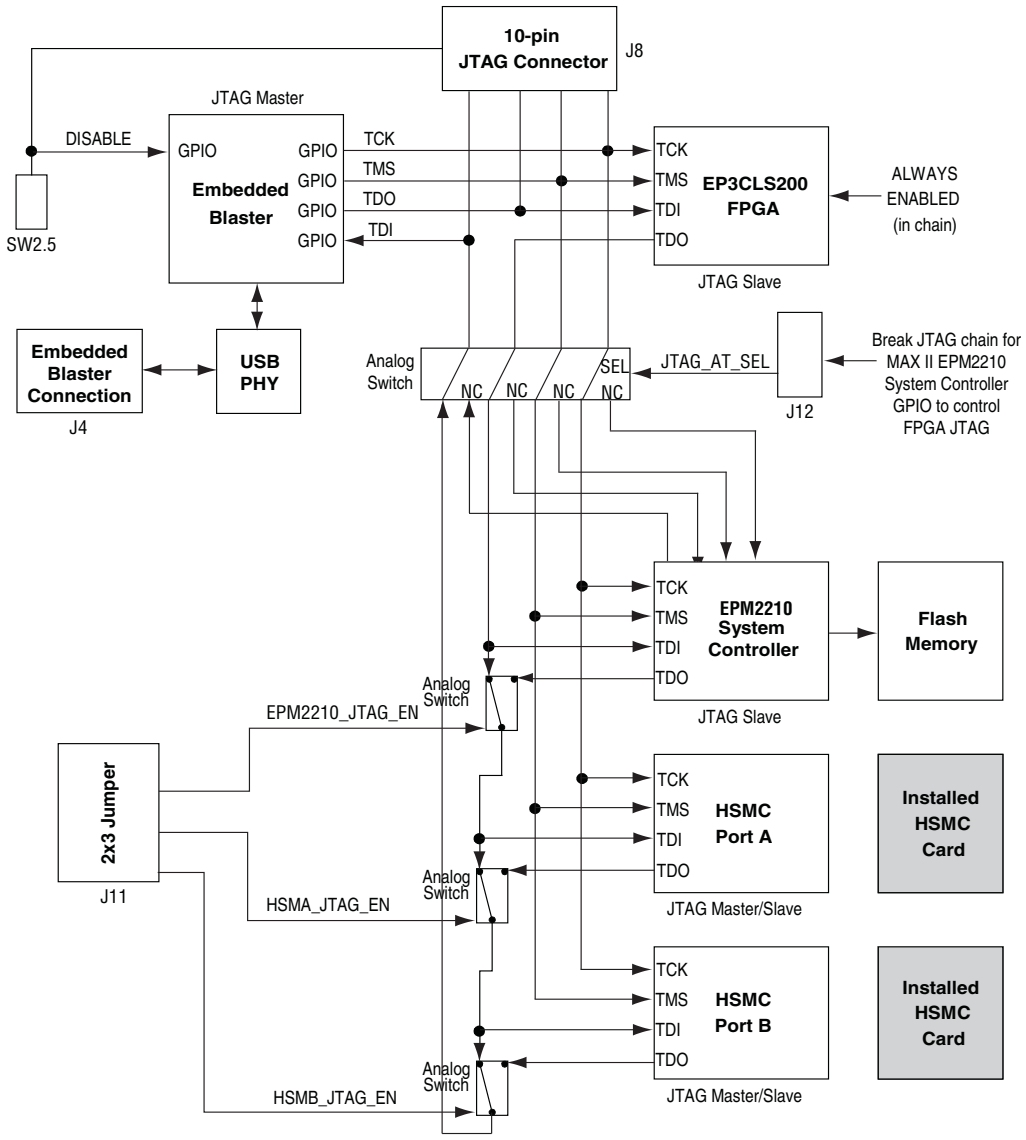
- Embedded USB-Blaster is the default method for configuring the FPGA at any time using the Quartus II Programmer in JTAG mode with the supplied USB cable.
- Flash memory download is used for storing FPGA images which the MAX II CPLD EPM2210 System Controller uses to configure the Cyclone III LS device either on board power up or after the the PGM configure push-button switch (S8) is pressed.
- External USB-Blaster for configuring the FPGA using an external USB-Blaster.

FPGA Programming over Embedded USB-Blaster

The USB-Blaster is implemented using a USB Type-B connector (J4), a FTDI USB 2.0 PHY device (U11), and an Altera MAX IIZ CPLD (U13). This allows the configuration of the FPGA using a USB cable directly connected between the USB port on the board (J4) and a USB port of a PC running the Quartus II software. The JTAG chain is normally mastered by the embedded USB-Blaster found in the MAX IIZ CPLD EPM240Z.

The embedded USB-Blaster is automatically disabled when an external USB-Blaster is connected to the JTAG chain. Figure 2–4 illustrates the JTAG chain.

Figure 2–4. JTAG Chain



For normal JTAG operation, the shunt jumper must be removed from the JTAG_AT_SEL jumper (J12). To connect a device or interface to the chain, the corresponding shunt must be installed onto the JTAG chain header (J11). Remove all of the shunt jumpers to only have the FPGA in the chain.

The MAX II CPLD EPM2210 System Controller must be in the chain to use the power monitor or the Board Test System. For this setting, install the upper-most jumper shunt onto the JTAG chain header (J11).

When a shunt is installed on the JTAG_AT_SEL jumper (J12), the default JTAG chain breaks and the MAX II EPM2210 System Controller gains control of the FPGA JTAG. For more information on the anti-tamper example design, refer to *<install_dir>***\kits\cycloneIIILS_3cls200_fpga\examples\max2\at_example\readme_at_example.txt**.

Flash Memory Programming

Flash memory programming is possible through a variety of methods using the Cyclone III LS device.

The default method is to use the factory design called the Board Update Portal. This design is an embedded webserver, which serves the Board Update Portal web page. The web page allows you to select new FPGA designs including hardware, software, or both in an industry-standard S-Record File (**.flash**) and write the design to the user hardware page (page 1) of the flash memory over the network.

The secondary method is to use the pre-built parallel flash loader (PFL) design included in the development kit. The development board implements the Altera PFL megafunction for flash memory programming. The PFL megafunction is a block of logic that is programmed into an Altera programmable logic device (FPGA or CPLD). The PFL functions as a utility for writing to a compatible flash memory device. This pre-built design contains the PFL megafunction that allows you to write either page 0, page 1, or other areas of flash memory over the USB interface using the Quartus II software. This method is used to restore the development board to its factory default settings.

Other methods to program the flash memory can be used as well, including the Nios® II processor.

For more information on the Nios II processor, refer to the Nios II Processor page of the Altera website (www.altera.com).

FPGA Programming from Flash Memory

On either power-up or by pressing the PGM configure push-button switch (S8), the MAX II CPLD EPM2210 System Controller's PFL configures the FPGA from the flash memory hardware page 0 or 1 based on whether `PGM_LED0` or `PGM_LED1` is illuminated. Table 2–8 defines the hardware page that loads when the PGM configure push-button switch (S8) is pressed. The PFL megafunction reads 16-bit data from the flash memory and converts it to passive serial (PS) format. This 1-bit data is then written to the FPGA's dedicated configuration pins during configuration.

Figure 2–5 shows the PFL configuration.

Figure 2–5. PFL Configuration

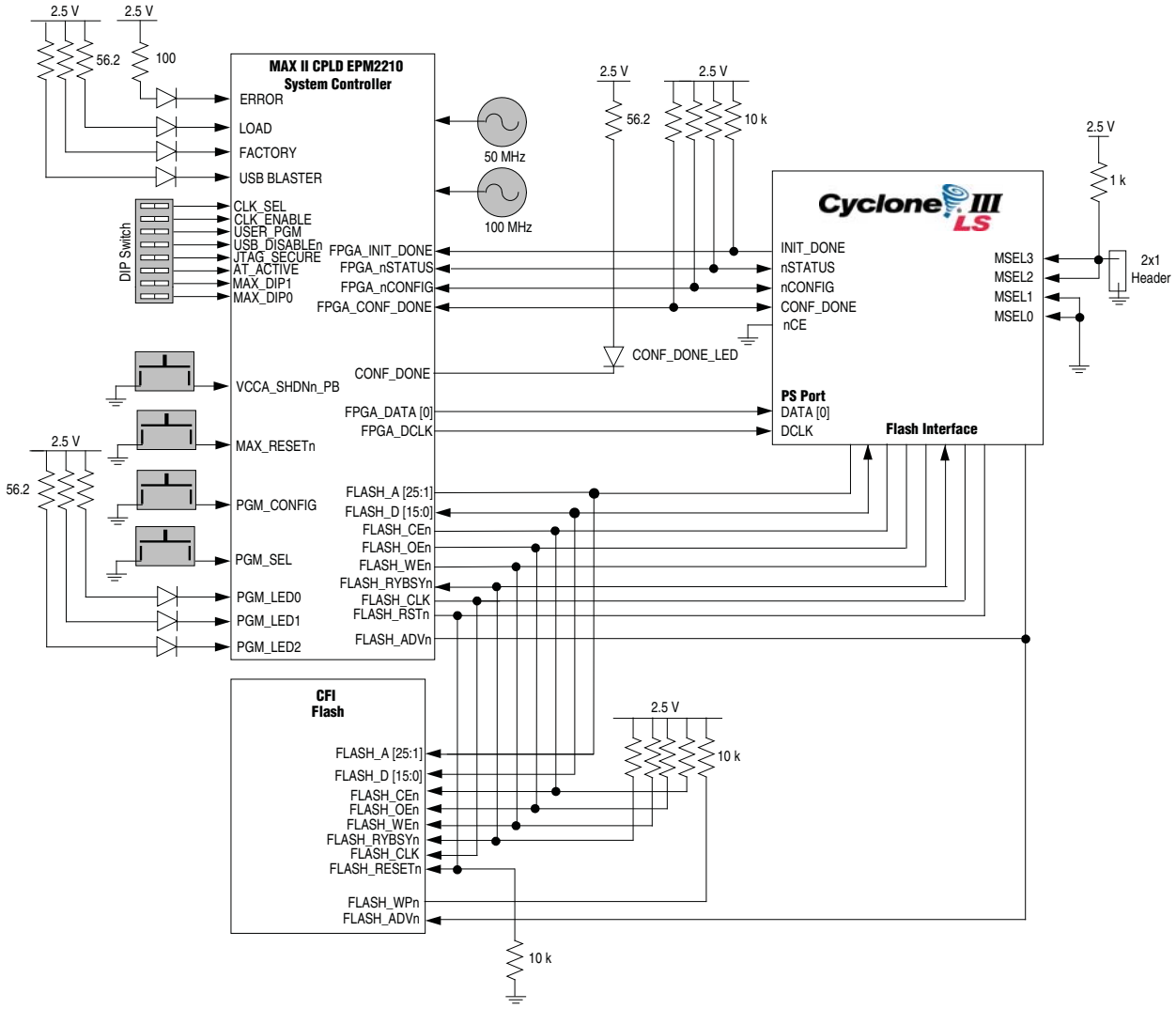


Table 2–7 shows the flash memory map storage.

Table 2–7. Flash Memory Map

Name	Size	Address
Unused	32 KB	0x03FF-FFFF 0x03FF-8000
	32 KB	0x03FF-7FFF 0x03FF-0000
	32 KB	0x03FE-FFFF 0x03FE-8000
	32 KB	0x03FE-7FFF 0x03FE-0000
User software	24,320 KB	0x03FD-FFFF 0x0282-0000
Factory software	8,192 KB	0x0281-FFFF 0x0202-0000
zipfs — HTML, web content	8,192 KB	0x0201-FFFF 0x0182-0000
Unused	6,095 KB	0x0181-FFFF 0x0128-0000
User hardware 2	6,357 KB	0x0127-FFFF 0x00C6-0000
User hardware 1	6,357 KB	0x00C5-FFFF 0x0064-0000
Factory hardware	6,357 KB	0x0063-FFFF 0x0002-0000
PFL option bits	32 KB	0x0001-FFFF 0x0001-8000
Reserved	32 KB	0x0001-7FFF 0x0001-0000
Ethernet option bits (MAC address)	32 KB	0x0000-FFFF 0x0000-8000
User design reset vector	32 KB	0x0000-7FFF 0x0000-0000

There are two pages reserved for the FPGA configuration data. The factory hardware page is considered page 0 and is loaded upon power-up if the USER_PGM DIP switch (SW2.6) is set to '0'. Otherwise, the user hardware page 1 is loaded. Pressing the PGM configure push-button switch (S8) loads the FPGA with a hardware page based on which PGM_LED[2:0] (D29, D30, D31) LED is illuminated. Table 2–8 defines the hardware page that loads when the PGM configure push-button switch (S8) is pressed.

Table 2–8. PGM Configure Push-Button Switch (S8) LED Settings *(1)*

PGM_LED0	PGM_LED1	PGM_LED2	Design
ON	OFF	OFF	Factory hardware
OFF	ON	OFF	User hardware 1
OFF	OFF	ON	User hardware 2

Note to Table 2–8:

(1) ON indicates a setting of '0' while OFF indicates a setting of '1'.

FPGA Programming over External USB-Blaster

The JTAG programming header provides another method for configuring the FPGA (U15) using an external USB-Blaster device with the Quartus II Programmer running on a PC. The external USB-Blaster is connected to the board through the JTAG connector (J8). Removing all shunt jumpers from the JTAG chain header (J11) removes all devices from the JTAG chain so that the FPGA is the only device on the chain. To add the MAX II CPLD EPM2210 System Controller to the JTAG chain, place a shunt on the JTAG chain header (J11) pin 1 and 2.

For more information on the following topics, refer to the respective documents:

- Board Update Portal, refer to the *Cyclone III LS FPGA Development Kit User Guide*.
- PFL design, refer to the *Cyclone III LS FPGA Development Kit User Guide*.
- PFL megafunction, refer to *AN 386: Using the Parallel Flash Loader with the Quartus II Software.*

Status Elements

The development board includes status LEDs. This section describes the status elements.

Table 2–9 lists the LED board references, names, and functional descriptions.

Table 2–9. Board-Specific LEDs (Part 1 of 2)

Board Reference	LED Name	Description
D3	Power	Blue LED. Illuminates when 12-V power is active.
D7	JTAG_AT_SEL	Green LED. Illuminated when the default JTAG chain is broken and the MAX II EPM2210 System Controller has control of the FPGA JTAG pins.
D13	CONF DONE	Green LED. Illuminates when the FPGA is successfully configured. Driven by the MAX II CPLD EPM2210 System Controller.
D14	INIT DONE	Green LED. Illuminates when the FPGA is successfully configured and is in user mode. This setting must be selected in the Quartus II programmer.
D11	LOAD	Green LED. Illuminates when the MAX II CPLD EPM2210 System Controller is actively configuring the FPGA. Driven by the MAX II CPLD EPM2210 System Controller.
D10	Error	Red LED. Illuminates when the MAX II CPLD EPM2210 System Controller fails to configure the FPGA. Driven by the MAX II CPLD EPM2210 System Controller.
D12	FACTORY	Green LED. Illuminates when the factory image is loaded to the FPGA. Driven by the MAX II CPLD EPM2210 System Controller.

Table 2–9. Board-Specific LEDs (Part 2 of 2)

Board Reference	LED Name	Description
D29, D30, D31	PROGRAM (PGM_LED[2:0])	Green LEDs. Illuminates to show the LED sequence that determines which flash memory image loads to the FPGA when PGM select push-button switch is pressed. Driven by the MAX II CPLD EPM2210 System Controller.
D22	ENET TX	Green LED. Illuminates to indicate Ethernet PHY transmit activity. Driven by the Marvell 88E1111 PHY.
D18	ENET RX	Green LED. Illuminates to indicate Ethernet PHY receive activity. Driven by the Marvell 88E1111 PHY.
D20	10	Green LED. Illuminates to indicate Ethernet linked at 10 Mbps connection speed. Driven by the Marvell 88E1111 PHY.
D16	100	Green LED. Illuminates to indicate Ethernet linked at 100 Mbps connection speed. Driven by the Marvell 88E1111 PHY.
D15	1000	Green LED. Illuminates to indicate Ethernet linked at 1000 Mbps connection speed. Driven by the Marvell 88E1111 PHY.
D2	HSMA PRSNTn	Green LED. Illuminates when HSMC port A has a board or cable plugged-in such that pin 160 becomes grounded. Driven by the add-in card.
D1	HSMB PRSNTn	Green LED. Illuminates when HSMC port B has a board or cable plugged-in such that pin 160 becomes grounded. Driven by the add-in card.
D4	USB	Green LED. Illuminates when the embedded USB-Blaster is in use to program the FPGA. Driven by the MAX II CPLD EPM2210 System Controller and MAX IIZ.

Table 2–10 lists the board-specific LEDs component references and manufacturing information.

Table 2–10. Board-Specific LEDs Component References and Manufacturing Information

Board Reference	Description	Manufacturer	Manufacturer Part Number	Manufacturer Website
D1, D2, D4, D7, D11-D16, D18, D20, D22, D29-D31	Green LEDs	Lumex, Inc.	SML-LX1206GC-TR	www.lumex.com
D10	Red LED	Lumex, Inc.	SML-LX1206IC-TR	www.lumex.com
D3	Blue LED	Lumex, Inc.	SML-LX1206USBC-TR	www.lumex.com

Setup Elements

The development board includes several different kinds of setup elements. This section describes the following setup elements:

- Board settings DIP switch
- JTAG chain header switch
- Configuration push-button switches

Board Settings DIP Switch

The board settings DIP switch (SW2) controls various features specific to the board and the MAX II CPLD EPM2210 System Controller logic design. Table 2–11 shows the switch controls and descriptions.

Table 2–11. Board Settings DIP Switch Controls

Switch	Schematic Signal Name	Description	Default *(1)*
1	MAX_DIP0	Reserved	ON
2	MAX_DIP1	Reserved	ON
3	AT_ACTIVE	ON: Anti-Tamper example design disable OFF: Anti-Tamper example design enable	ON
4	JTAG_SECURE	ON: Cyclone III LS JTAG lock feature inactive OFF: Cyclone III LS JTAG lock feature active	ON
5	USB_DISABLEn	ON : Embedded USB-Blaster disable OFF : Embedded USB-Blaster enable	OFF
6	USER_PGM	ON: Load factory design from flash memory upon power-up OFF: Load user hardware page 1 from flash memory upon power-up	ON
7	CLK_ENABLE	ON : On-board oscillators enable OFF : On-board oscillators disable	OFF
8	CLK_SEL	ON : Programmable oscillator clock select OFF : SMA input clock select	OFF

Note to Table 2–11:

(1) ON indicates a setting of '0' while OFF indicates a setting of '1'.

Table 2–12 lists the board settings DIP switch component reference and manufacturing information.

Table 2–12. Board Settings DIP Switch Component Reference and Manufacturing Information

Board Reference	Description	Manufacturer	Manufacturer Part Number	Manufacturer Website
SW2	Eight-position rocker DIP switch	Grayhill	76SB08ST	www.grayhill.com

JTAG Chain Header Switch

The JTAG chain header switch (J11) is provided to either remove or include devices in the active JTAG chain. However, the Cyclone III LS FPGA device is always in the JTAG chain. Refer to Figure 2–4 on page 2–12 for the JTAG chain functionality.

Table 2–13 shows the switch controls and its descriptions.

Table 2–13. JTAG Chain Header (J11) Switch Controls

Switch	Schematic Signal Name	Description	Default
1	EPM2210_JTAG_EN	ON : MAX II CPLD EPM2210 System Controller in-chain OFF : Bypass MAX II CPLD EPM2210 System Controller	ON
2	HSMA_JTAG_EN	ON : HSMA in-chain OFF : Bypass HSMA	OFF
3	HSMB_JTAG_EN	ON : HSMB in-chain OFF : Bypass HSMB	OFF

Table 2–14 lists the JTAG chain header switch component reference and manufacturing information.

Table 2–14. JTAG Chain Header Switch Component Reference and Manufacturing Information

Board Reference	Device Description	Manufacturer	Manufacturer Part Number	Manufacturer Website
J11	2x3 100 mil jumper	Samtec	TSW-103-07-L-D	www.samtec.com

Anti-Tamper JTAG Select Header Switch

The anti-tamper JTAG select header switch (J12) is provided to disable the normal JTAG chain, giving control of the FPGA JTAG signals to the MAX II CPLD EMP2210 System Controller GPIO signals. Note that when a shunt jumper is placed onto the anti-tamper JTAG select header switch (J12), none of the devices in the JTAG chain can be detected by the USB embedded blaster or the JTAG header. Refer to Figure 2–4 on page 2–12 for the JTAG chain functionality.

Table 2–15 shows the anti-tamper JTAG select header switch controls and descriptions.

Table 2–15. Anti-Tamper JTAG Select Header Switch Controls

Switch	Schematic Signal Name	Description	Default
1	JTAG_AT_SEL	ON: MAX II CPLD EPM2210 System Controller GPIO controls the FPGA JTAG signals. OFF: Normal JTAG chain functionality	OFF

Table 2–16 lists the anti-tamper JTAG select header switch component reference and manufacturing information.

Table 2–16. Anti-Tamper JTAG Select Header Switch Component Reference and Manufacturing Information

Board Reference	Description	Manufacturer	Manufacturer Part Number	Manufacturer Website
J12	2x1 100 mil jumper	3M/ESD	929665-09-36-I	www.3m.com

LCD/HSMC Port B Data Select Header Switch

The LCD/HSMC port B data select header switch (J18) is provided to control data multiplexing of the LCD and HSMB_D[65:75] signals to the Cyclone III LS device. If the shunt is not placed on the jumper, the FPGA can control the LCD_HSMB_SEL signal. The default value of this switch is a logic '1'.

Table 2–17 shows the LCD/HSMC port B data select header switch controls and descriptions.

Table 2–17. LCD/HSMC Port B Data Select Header Switch Controls

Switch	Schematic Signal Name	Description	Default
1	LCD_HSMB_SEL	ON: FPGA control of the LCD signals. OFF: FPGA control of the HSMB_D[65:75] signals.	OFF

Table 2–18 lists the LCD/HSMC port B data select header switch component reference and manufacturing information.

Table 2–18. LCD/HSMB Data Select Header Switch Component Reference and Manufacturing Information

Board Reference	Description	Manufacturer	Manufacturer Part Number	Manufacturer Website
J18	2x1 100 mil jumper	3M/ESD	929665-09-36-I	www.3m.com

Configuration Push-button Switches

The PGM configure push-button switch, PGM_CONFIG (S8), is an input to the MAX II CPLD EPM2210 System Controller. The push-button switch forces a reconfiguration of the FPGA from flash memory. The location in the flash memory is based on the PGM_LED[2:0] setting when the button is released. Valid settings include PGM_LED0, PGM_LED1, or PGM_LED2 illuminated. There are three pages in flash memory reserved for FPGA designs.

The PGM select push-button switch, PGM_SEL (S9), toggles the program LEDs (D29, D30, D31) sequence. Refer to Table 2–8 on page 2–16 for the PGM_LED[2:0] sequence definitions.

The CPU reset push-button switch, CPU_RESETn (S2) is a dedicated reset switch for the embedded processors which is wired to the FPGA DEV_CLRn pin, while the MAX II reset push-button switch, MAX_RESETn (S10), resets the MAX II CPLD EPM2210 System Controller.

Table 2–19 lists the configuration push-button switches component reference and manufacturing information.

Table 2–19. Configuration Push-button Switches Component Reference and Manufacturing Information

Board Reference	Description	Manufacturer	Manufacturer Part Number	Manufacturer Website
S2, S8, S9, S10	Push-button switch	Panasonic	EVQPAC07K	www.panasonic.com/industrial/

Clock Circuitry

This section describes the board's clock inputs and outputs.

Cyclone III LS FPGA Clock Inputs

Figure 2–6 shows the Cyclone III LS FPGA development board clock inputs.

Figure 2–6. Cyclone III LS FPGA Development Board Clock Inputs

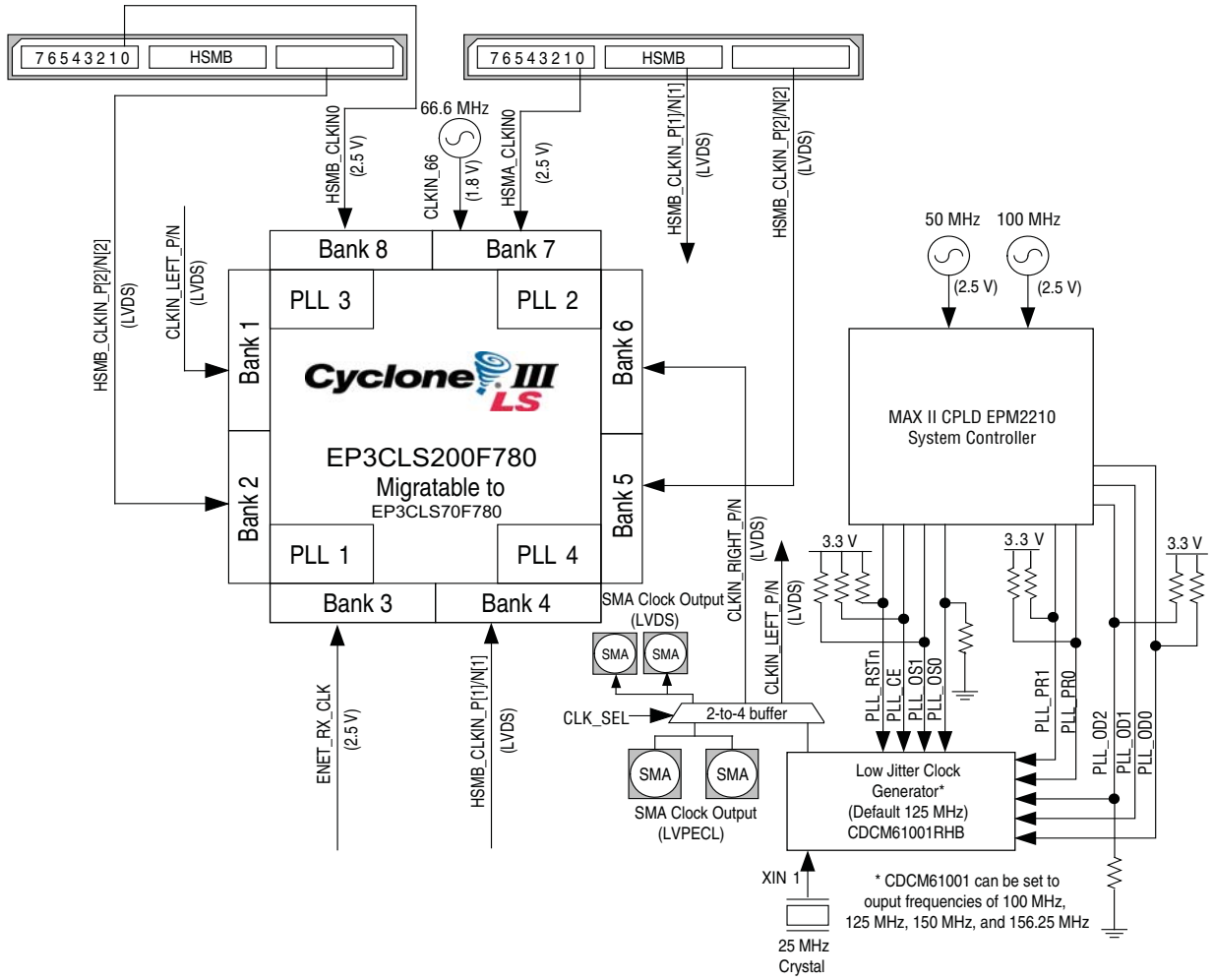


Table 2–20 shows the external clock inputs for the Cyclone III LS FPGA development board.

Table 2–20. Cyclone III LS FPGA Development Board Clock Inputs (Part 1 of 2)

Source	Schematic Signal Name	Cyclone III LS Device Pin Number	I/O Standard	Description
X3	CLKIN_66	B16	1.8-V	66.6 MHz oscillator used for the memories or general purpose clock input.
SMA or 125.000 MHz (Default Frequency) *(1)*	CLKIN_LEFT_P	N2	LVDS	Input to the fan-out buffer (U20) which drives LVDS input to the left edge of PLL input.
	CLKIN_LEFT_N	N1		
	CLKIN_RIGHT_P	N27		Input to the fan-out buffer (U20) which drives LVDS input to the right edge of PLL input.
	CLKIN_RIGHT_N	N28		
Samtec HSMC	HSMA_CLKIN0	A16	LVTTL	Single-ended input from the installed HSMC port A cable or board.

Table 2–20. Cyclone III LS FPGA Development Board Clock Inputs (Part 2 of 2)

Source	Schematic Signal Name	Cyclone III LS Device Pin Number	I/O Standard	Description
Samtec HSMC	HSMA_CLKIN_P1	AG16	LVTTL	LVTTL inputs from the installed HSMC port A cable or board. Can also support LVDS inputs when the termination resistor is installed.
	HSMA_CLKIN_N1	AH16		
Samtec HSMC	HSMA_CLKIN_P2	T27	LVTTL	LVTTL input from the installed HSMC port A cable or board. Can also support LVDS inputs. when the termination resistor is installed
	HSMA_CLKIN_N2	T28		
Samtec HSMC	HSMB_CLKIN0	B13	LVTTL	Single-ended input from the installed HSMC port B cable or board.
Samtec HSMC	HSMB_CLKIN_P2	T2	LVTTL	LVTTL input from the installed HSMC port B cable or board. Can also support LVDS inputs when the termination resistor is installed.
	HSMB_CLKIN_N2	T1		

Note to Table 2–20:

(1) CDCM61001 has a default frequency of 125 MHz, but can also be set to frequencies of 100 MHz, 150 MHz, and 156.25 MHz by the MAX II CPLD EPM2210 System Controller..

Cyclone III LS FPGA Clock Outputs

Figure 2–7 shows the Cyclone III LS FPGA development board clock outputs.

Figure 2–7. Cyclone III LS FPGA Development Board Clock Outputs

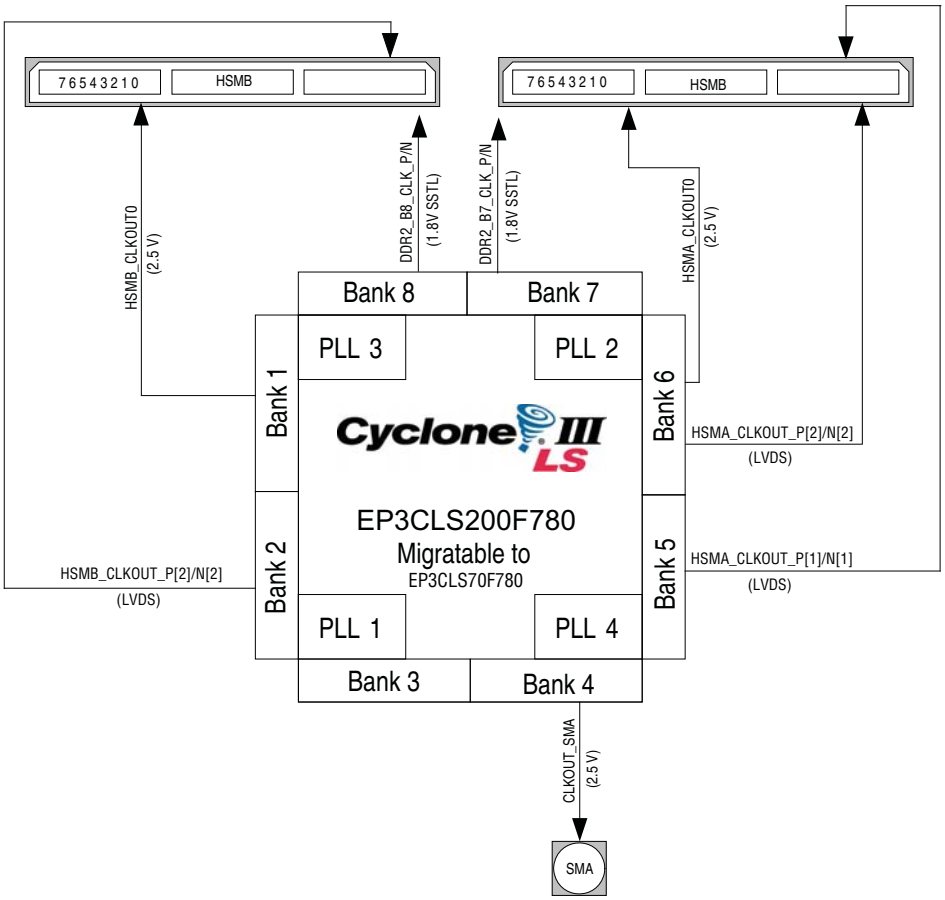


Table 2–21 lists the clock outputs for the Cyclone III LS FPGA development board.

Table 2–21. Cyclone III LS FPGA Development Board Clock Outputs

Connector	Schematic Signal Name	Cyclone III LS Device Pin Number	I/O Standard	Description
SMA (J15)	CLKOUT_SMA	AC15	2.5-V	FPGA CMOS output or GPIO
Samtec HSMC	HSMA_CLKOUT0	P28	2.5-V	FPGA CMOS output or GPIO
Samtec HSMC	HSMA_CLKOUT_P1	V28	LVDS or 2.5-V	LVDS output or two 2.5-V CMOS outputs.
	HSMA_CLKOUT_N1	U28		
Samtec HSMC	HSMA_CLKOUT_P2	M25	LVDS or 2.5-V	LVDS output or two 2.5-V CMOS outputs.
	HSMA_CLKOUT_N2	N26		
Samtec HSMC	HSMB_CLKOUT0	D2	2.5-V	FPGA CMOS output or GPIO
Samtec HSMC	HSMB_CLKOUT_P2	T6	LVDS or 2.5-V	LVDS output or two 2.5-V CMOS outputs.
	HSMB_CLKOUT_N2	T5		

Table 2–22 lists the crystal oscillators component references and manufacturing information.

Table 2–22. Crystal Oscillator Component References and Manufacturing Information

Board Reference	Description	Manufacturer	Manufacturer Part Number	Manufacturer Website
X3	66.6 MHz Crystal Oscillator	ECS Inc.	ECS-3953C-666-X	www.ecsxtal.com
U17	Single Output Programmable Clock Generator	Texas Instruments	CDCM61001RHB	www.ti.com
X5	50.00 MHz Crystal Oscillator	ECS Inc.	ECS-3525-500-B-xx	www.ecsxtal.com
Y3	100.00 MHz Crystal Oscillator	Pletronics	SM5545TEX-100.00M	www.pletronics.com

General User Input/Output

This section describes the user I/O interface to the FPGA, including the push-buttons, DIP switches, status LEDs, and character LCD.

User-Defined Push-Button Switches

The development board includes five user-defined push-button switches: four general user push-button switches and one CPU reset. For information on the system and safe reset push-button switches, refer to "Configuration Push-button Switches" on page 2–20.

Board references S3 through S6 are push-button switches that allow you to interact with the Cyclone III LS device. When the switch is pressed and held down, the device pin is set to logic 0; when the switch is released, the device pin is set to logic 1. There is no board-specific function for these general user push-button switches.

The board reference S2 is the CPU reset push-button switch, CPU_RESETn, which is an input to the Cyclone III LS device and the MAX II CPLD EPM2210 System Controller. CPU_RESETn is intended to be the master reset signal for the FPGA design loaded into the Cyclone III LS device. This switch also acts as a regular I/O pin.

Table 2–23 lists the user-defined push-button switch schematic signal names and their corresponding Cyclone III LS device pin numbers.

Table 2–23. User-Defined Push-Button Switch Schematic Signal Names and Functions

Board Reference	Description	Schematic Signal Name	I/O Standard	Cyclone III LS Device Pin Number
S6	User-defined push-button switch. When the switch is pressed, a logic 0 is selected. When the switch is released, a logic 1 is selected.	USER_PB0	1.8-V	F24
S5		USER_PB1		G17
S4		USER_PB2		E25
S3		USER_PB3		D21
S2		CPU_RESETn	2.5-V	W27

Table 2–24 lists the user-defined push-button switch component reference and the manufacturing information.

Table 2–24. User-Defined Push-Button Switch Component Reference and Manufacturing Information

Board Reference	Description	Manufacturer	Manufacturer Part Number	Manufacturer Website
S2 to S6	Push-button switch	Panasonic	EVQPAC07K	www.panasonic.com/industrial/

User-Defined DIP Switches

Board reference S7 is a 4-pin DIP switch. The switches are user-defined and provided for additional FPGA input control. There is no board-specific function for these switches.

Table 2–25 lists the user-defined DIP switch schematic signal names and their corresponding Cyclone III LS pin numbers.

Table 2–25. User-Defined DIP Switch Schematic Signal Names and Functions

Board Reference	Description	Schematic Signal Name	I/O Standard	Cyclone III LS Device Pin Number
S7.1	User-defined DIP switch connected to the FPGA device. When the switch is in the OFF position, a logic 1 is selected. When the switch is in the ON position, a logic 0 is selected.	USER_DIP0	1.8-V	B2
S7.2		USER_DIP1		B7
S7.3		USER_DIP2		D7
S7.4		USER_DIP3		A13

Table 2–26 lists the user-defined DIP switch component reference and the manufacturing information.

Table 2–26. User-Defined DIP Switch Component Reference and Manufacturing Information

Board Reference	Description	Manufacturer	Manufacturer Part Number	Manufacturer Website
S7	Four-position DIP switch	C & K Components	TDA04H0SB1	www.ck-components.com

User-Defined LEDs

The development board includes four general purpose LEDs. This section describes all user-defined LEDs. For information on board-specific or status LEDs, refer to "Status Elements" on page 2–16.

Board references D25 through D28 are four user-defined LEDs which allow status and debugging signals to be driven to the LEDs from the FPGA designs loaded into the Cyclone III LS device. The LEDs illuminate when a logic 0 is driven, and turns off when a logic 1 is driven. There is no board-specific function for these LEDs.

Table 2–27 lists the user-defined LED schematic signal names and their corresponding Cyclone III LS pin numbers.

Table 2–27. User-Defined LED Schematic Signal Names and Functions

Board Reference	Description	Schematic Signal Name	I/O Standard	Cyclone III LS Device Pin Number
D28	User-defined LEDs. Driving a logic 0 on the I/O port turns the LED ON. Driving a logic 1 on the I/O port turns the LED OFF.	USR_LED0	1.8-V	E24
D27		USR_LED1		G18
D26		USR_LED2		C21
D25		USR_LED3		C7

Table 2–28 lists the user-defined LED component reference and the manufacturing information.

Table 2–28. User-Defined LED Component Reference and Manufacturing Information

Board Reference	Device Description	Manufacturer	Manufacturer Part Number	Manufacturer Website
D25 to D28	Green LEDs	Lumex, Inc.	SML-LX1206GC-TR	www.lumex.com

LCD

The development board contains a single 14-pin 0.1" pitch dual-row header that interfaces to a 16 character × 2 line Lumex LCD display. The LCD has a 14-pin receptacle that mounts directly to the board's 14-pin header, so it can be easily removed for access to components under the display. You can also use the header for debugging or other purposes.

The LCD signals are multiplexed with HSMC port B data signals HSMB_D65 through HSMB_D75. The LCD/HSMC port B data select header switch (J18) is used to control data multiplexing on the LCD signals and the HSMB_D[65:75] signals to the Cyclone III LS device. If the shunt is not placed on the jumper, the FPGA can control the LCD_HSMB_SEL signal. When the LCD_HSMB_SEL signal is set to '1' (shunt removed), the FPGA controls the HSMB_D[65:75] signals. When the LCD_HSMB_SEL is set to '0' (shunt installed), the FPGA controls the LCD signals. The default value is set to '1'.

Table 2–29 summarizes the LCD pin assignments. The signal names and directions are relative to the Cyclone III LS FPGA.

Table 2–29. LCD Pin Assignments, Schematic Signal Names, and Functions

Board Reference	Description	Schematic Signal Name	I/O Standard	Cyclone III LS Device Pin Number
J19.4	LCD chip select (LCD_CSn) when LCD_HSMB_SEL is set to a logic 0.	LCD_HSMB_D[65]	2.5-V	P1
J19.11	LCD data bus bit 4 (LCD_DATA4) when LCD_HSMB_SEL is set to a logic 0.	LCD_HSMB_D[66]		AE4
J19.5	LCD write enable (LCD_WEn) when LCD_HSMB_SEL is set to a logic 0.	LCD_HSMB_D[67]		J4
J19.14	LCD data bus bit 7 (LCD_DATA7) when LCD_HSMB_SEL is set to a logic 0.	LCD_HSMB_D[68]		AE1
J19.12	LCD data bus bit 5 (LCD_DATA5) when LCD_HSMB_SEL is set to a logic 0.	LCD_HSMB_D[69]		AF1
J19.13	LCD data bus bit 6 (LCD_DATA6) when LCD_HSMB_SEL is set to a logic 0.	LCD_HSMB_D[70]		AD2
J19.4	LCD data or command select (LCD_D_Cn) when LCD_HSMB_SEL is set to a logic 0.	LCD_HSMB_D[71]		L1
J19.7	LCD data bus bit 0 (LCD_DATA0) when LCD_HSMB_SEL is set to a logic 0.	LCD_HSMB_D[72]		V5
J19.8	LCD data bus bit 1 (LCD_DATA1) when LCD_HSMB_SEL is set to a logic 0.	LCD_HSMB_D[73]		W4
J19.10	LCD data bus bit 3 (LCD_DATA3) when LCD_HSMB_SEL is set to a logic 0.	LCD_HSMB_D[74]		W6
J19.9	LCD data bus bit 2 (LCD_DATA2) when LCD_HSMB_SEL is set to a logic 0.	LCD_HSMB_D[75]		W7
J18	To control the LCD via the FPGA, a shunt should be placed on this jumper, or the FPGA must drive a logic 0.	LCD_HSMB_SEL	1.8-V	D20

Table 2–30 shows the LCD pin definitions, and is an excerpt from the Lumex data sheet.

For more information such as timing, character maps, interface guidelines, and other related documentation, visit www.lumex.com.

Table 2–30. LCD Pin Definitions and Functions (Part 1 of 2)

Pin Number	Symbol	Level	Function	
1	V_{DD}	—	Power supply	5 V
2	V_{SS}	—		GND (0 V)
3	V_0	—		For LCD drive
4	RS	H/L	Register select signal H: Data input L: Instruction input	

Table 2–30. LCD Pin Definitions and Functions (Part 2 of 2)

Pin Number	Symbol	Level	Function
5	R/W	H/L	H: Data read (module to MPU) L: Data write (MPU to module)
6	E	H, H to L	Enable
7–14	DB0–DB7	H/L	Data bus, software selectable 4-bit or 8-bit mode

The particular model used does not have a backlight and the LCD drive pin is not connected.

Table 2–31 lists the LCD component references and the manufacturing information.

Table 2–31. LCD Component References and Manufacturing Information

Board Reference	Description	Manufacturer	Manufacturer Part Number	Manufacturer Website
J19	2×7 pin, 100 mil, vertical header	Samtec	TSM-107-07-G-D	www.samtec.com
	2×16 character display, 5×8 dot matrix	Lumex Inc.	LCM-S01602DSR/C	www.lumex.com

Components and Interfaces

This section describes the development board's communication ports and interface cards relative to the Cyclone III LS device. The development board supports the following communication ports:

- 10/100/1000 Ethernet
- HSMC

10/100/1000 Ethernet

A Marvell 88E1111 PHY device is used for 10/100/1000 BASE-T Ethernet connection. The device is an auto-negotiating Ethernet PHY with an RGMII interface to the FPGA. The MAC function must be provided in the FPGA for typical networking applications. The Marvell 88E1111 PHY uses 2.5-V and 1.2-V power rails and requires a 25-MHz reference clock driven from a dedicated oscillator. It interfaces to a Halo Electronics HFJ11-1G02E model RJ45 with internal magnetics that can be used for driving copper lines with Ethernet traffic.

Figure 2–8 shows the RGMII interface between the FPGA (MAC) and Marvell 88E1111 PHY.

Figure 2–8. RGMII Interface between FPGA (MAC) and Marvell 88E1111 PHY

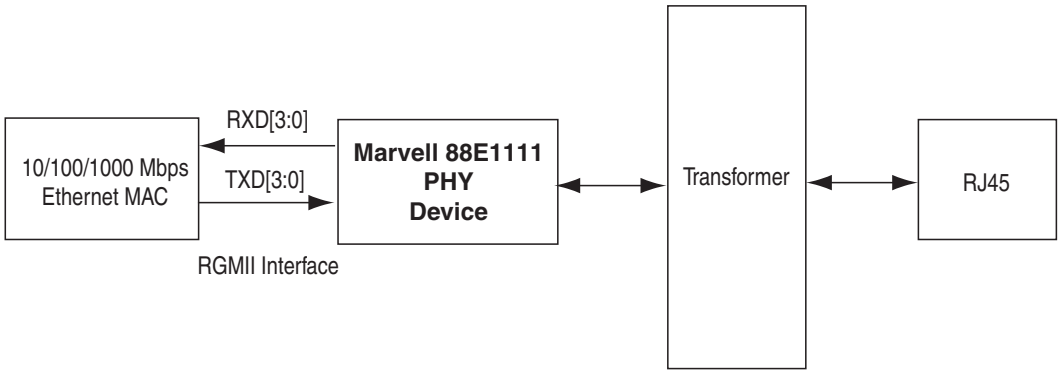


Table 2–32 lists the Ethernet PHY interface pin assignments.

Table 2–32. Ethernet PHY Pin Assignments, Signal Names and Functions

Board Reference	Description	Schematic Signal Name	I/O Standard	Cyclone III LS Device Pin Number
U24.8	RGMII transmit clock	ENET_GTX_CLK	2.5-V	AC14
U24.23	Management bus interrupt	ENET_INTn		N23
U24.25	Management bus control	ENET_MDC		AH12
U24.24	Management bus data	ENET_MDIO		AH27
U24.28	Device reset	ENET_RESETn		AF24
U24.2	RGMII receive clock	ENET_RX_CLK		AG13
U24.94	RGMII receive control	ENET_RX_DV		AH15
U24.95	RGMII receive data	ENET_RXD0		AF13
U24.92	RGMII receive data	ENET_RXD1		AB14
U24.93	RGMII receive data	ENET_RXD2		AH13
U24.91	RGMII receive data	ENET_RXD3		AG8
U24.9	RGMII transmit control	ENET_TX_EN		AF6
U24.11	RGMII transmit data	ENET_TXD0		AE14
U24.12	RGMII transmit data	ENET_TXD1		AD12
U24.14	RGMII transmit data	ENET_TXD2		AB17
U24.16	RGMII transmit data	ENET_TXD3		AC6

Table 2–33 lists the Ethernet PHY interface component reference and manufacturing information.

Table 2–33. Ethernet PHY Component Reference and Manufacturing Information

Board Reference	Description	Manufacturer	Manufacturing Part Number	Manufacturer Website
U24	Ethernet PHY BASE-T device	Marvell Semiconductor	88E1111-B2-CAAIC000	www.marvell.com

High-Speed Mezzanine Cards

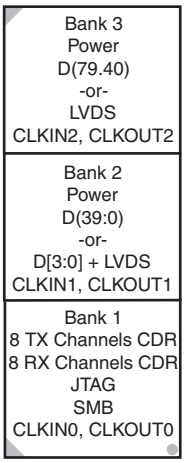
The development board contains two HSMC interfaces called port A and port B. HSMC port A interface supports both single-ended and differential signaling while HSMC port B interface only supports single-ended signaling. The HSMC interface also allows JTAG, SMB, clock outputs and inputs, as well as power for compatible HSMC cards. The HSMC is an Altera-developed open specification, which allows you to expand the functionality of the development board through the addition of daughtercards (HSMCs).

For more information about the HSMC specification such as signaling standards, signal integrity, compatible connectors, and mechanical information, refer to the *High Speed Mezzanine Card (HSMC) Specification* manual.

The HSMC connector has a total of 172 pins, including 120 signal pins, 39 power pins, and 13 ground pins. The ground pins are located between the two rows of signal and power pins, acting both as a shield and a reference. The HSMC host connector is based on the 0.5 mm-pitch QSH/QTH family of high-speed, board-to-board connectors from Samtec. There are three banks in this connector. Bank 1 has every third pin removed as done in the QSH-DP/QTH-DP series. Bank 2 and bank 3 have all the pins populated as done in the QSH/QTH series.

Figure 2–9 shows the bank arrangement of signals with respect to the Samtec connector's three banks.

Figure 2–9. HSMC Signal and Bank Diagram



The HSMC interface has programmable bi-directional I/O pins that can be used as 2.5-V LVCMOS, which is 3.3-V LVTTL-compatible. These pins can also be used as various differential I/O standards including, but not limited to, LVDS, mini-LVDS, and RSDS with up to 17 full-duplex channels.

As noted in the *High Speed Mezzanine Card (HSMC) Specification* manual, LVDS and single-ended I/O standards are only guaranteed to function when mixed according to either the generic single-ended pin-out or generic differential pin-out.

Table 2–34 lists the HSMC port A interface pin assignments, signal names, and functions.

Table 2–34. HSMC Port A Pin Assignments, Schematic Signal Names, and Functions (Part 1 of 3) *(1)*

Board Reference	Description	Schematic Signal Name	I/O Standard	Cyclone III LS Device Pin Number
J2.33	Management serial data	HSMA_SDA	2.5-V	T26
J2.34	Management serial clock	HSMA_SCL		R26
J2.35	JTAG clock signal	JTAG_TCK		—
J2.36	JTAG mode select signal	JTAG_TMS		—
J2.37	JTAG data output	HSMA_JTAG_TDO		—
J2.38	JTAG data input	HSMA_JTAG_TDI		—
J2.39	Dedicated CMOS clock out	HSMA_CLKOUT0		P28
J2.40	Dedicated CMOS clock in	HSMA_CLKIN0		A16
J2.41	Dedicated CMOS I/O bit 0	HSMA_D0		AC22
J2.42	Dedicated CMOS I/O bit 1	HSMA_D1		AC21
J2.43	Dedicated CMOS I/O bit 2	HSMA_D2		AD21
J2.44	Dedicated CMOS I/O bit 3	HSMA_D3		W28
J2.47	LVDS TX bit 0 or CMOS bit 4	HSMA_TX_P0	LVDS or 2.5-V	AA23
J2.48	LVDS RX bit 0 or CMOS bit 5	HSMA_RX_P0		K24
J2.49	LVDS TX bit 0n or CMOS bit 6	HSMA_TX_N0		AA24
J2.50	LVDS RX bit 0n or CMOS bit 7	HSMA_RX_N0		J24
J2.53	LVDS TX bit 1 or CMOS bit 8	HSMA_TX_P1		Y23
J2.54	LVDS RX bit 1 or CMOS bit 9	HSMA_RX_P1		G23
J2.55	LVDS TX bit 1n or CMOS bit 10	HSMA_TX_N1		W23
J2.56	LVDS RX bit 1n or CMOS bit 11	HSMA_RX_N1		G24
J2.59	LVDS TX bit 2 or CMOS bit 12	HSMA_TX_P2		R23
J2.60	LVDS RX bit 2 or CMOS bit 13	HSMA_RX_P2		D26
J2.61	LVDS TX bit 2n or CMOS bit 14	HSMA_TX_N2		R24
J2.62	LVDS RX bit 2n or CMOS bit 15	HSMA_RX_N2		D27
J2.65	LVDS TX bit 3 or CMOS bit 16	HSMA_TX_P3		R27
J2.66	LVDS RX bit 3 or CMOS bit 17	HSMA_RX_P3		D28
J2.67	LVDS TX bit 3n or CMOS bit 18	HSMA_TX_N3		R28
J2.68	LVDS RX bit 3n or CMOS bit 19	HSMA_RX_N3		C28
J2.71	LVDS TX bit 4 or CMOS bit 20	HSMA_TX_P4		U23
J2.72	LVDS RX bit 4 or CMOS bit 21	HSMA_RX_P4		E27
J2.73	LVDS TX bit 4n or CMOS bit 22	HSMA_TX_N4		U24
J2.74	LVDS RX bit 4n or CMOS bit 23	HSMA_RX_N4		E26
J2.77	LVDS TX bit 5 or CMOS bit 24	HSMA_TX_P5		U25
J2.78	LVDS RX bit 5 or CMOS bit 25	HSMA_RX_P5		F28
J2.79	LVDS TX bit 5n or CMOS bit 26	HSMA_TX_N5		U26
J2.80	LVDS RX bit 5n or CMOS bit 27	HSMA_RX_N5		E28

Table 2–34. HSMC Port A Pin Assignments, Schematic Signal Names, and Functions (Part 2 of 3) *(1)*

Board Reference	Description	Schematic Signal Name	I/O Standard	Cyclone III LS Device Pin Number
J2.83	LVDS TX bit 6 or CMOS bit 28	HSMA_TX_P6	LVDS or 2.5-V	V23
J2.84	LVDS RX bit 6 or CMOS bit 29	HSMA_RX_P6		G25
J2.85	LVDS TX bit 6n or CMOS bit 30	HSMA_TX_N6		V24
J2.86	LVDS RX bit 6n or CMOS bit 31	HSMA_RX_N6		F25
J2.89	LVDS TX bit 7 or CMOS bit 32	HSMA_TX_P7		V25
J2.90	LVDS RX bit 7 or CMOS bit 33	HSMA_RX_P7		G27
J2.91	LVDS TX bit 7n or CMOS bit 34	HSMA_TX_N7		W26
J2.92	LVDS RX bit 7n or CMOS bit 35	HSMA_RX_N7		G28
J2.95	LVDS or CMOS clock out 1 or CMOS bit 36	HSMA_CLKOUT_P1		V28
J2.96	LVDS or CMOS clock in 1 or CMOS bit 37	HSMA_CLKIN_P1		AG16
J2.97	LVDS or CMOS clock out 1 or CMOS bit 38	HSMA_CLKOUT_N1		U28
J2.98	LVDS or CMOS clock in 1 or CMOS bit 39	HSMA_CLKIN_N1		AH16
J2.101	LVDS TX bit 8 or CMOS bit 40	HSMA_TX_P8		W24
J2.102	LVDS RX bit 8 or CMOS bit 41	HSMA_RX_P8		H26
J2.103	LVDS TX bit 8n or CMOS bit 42	HSMA_TX_N8		W25
J2.104	LVDS RX bit 8n or CMOS bit 43	HSMA_RX_N8		G26
J2.107	LVDS TX bit 9 or CMOS bit 44	HSMA_TX_P9		AA26
J2.108	LVDS RX bit 9 or CMOS bit 45	HSMA_RX_P9		J27
J2.109	LVDS TX bit 9n or CMOS bit 46	HSMA_TX_N9		Y26
J2.110	LVDS RX bit 9n or CMOS bit 47	HSMA_RX_N9		J28
J2.113	LVDS TX bit 10 or CMOS bit 48	HSMA_TX_P10		AA27
J2.114	LVDS RX bit 10 or CMOS bit 49	HSMA_RX_P10		K27
J2.115	LVDS TX bit 10n or CMOS bit 50	HSMA_TX_N10		AA28
J2.116	LVDS RX bit 10n or CMOS bit 51	HSMA_RX_N10		K28
J2.119	LVDS TX bit 11 or CMOS bit 52	HSMA_TX_P11		AB27
J2.120	LVDS RX bit 11 or CMOS bit 53	HSMA_RX_P11		J25
J2.121	LVDS TX bit 11n or CMOS bit 54	HSMA_TX_N11		AB28
J2.122	LVDS RX bit 11n or CMOS bit 55	HSMA_RX_N11		J26
J2.125	LVDS TX bit 12 or CMOS bit 56	HSMA_TX_P12		AD28
J2.126	LVDS RX bit 12 or CMOS bit 57	HSMA_RX_P12		M26
J2.127	LVDS TX bit 12n or CMOS bit 58	HSMA_TX_N12		AC28
J2.128	LVDS RX bit 12n or CMOS bit 59	HSMA_RX_N12		M27
J2.131	LVDS TX bit 13 or CMOS bit 60	HSMA_TX_P13		AA25
J2.132	LVDS RX bit 13 or CMOS bit 61	HSMA_RX_P13		K25
J2.133	LVDS TX bit 13n or CMOS bit 62	HSMA_TX_N13		AB26
J2.134	LVDS RX bit 13n or CMOS bit 63	HSMA_RX_N13		K26
J2.137	LVDS TX bit 14 or CMOS bit 64	HSMA_TX_P14		AF28
J2.138	LVDS RX bit 14 or CMOS bit 65	HSMA_RX_P14		L24

Table 2–34. HSMC Port A Pin Assignments, Schematic Signal Names, and Functions (Part 3 of 3) *(1)*

Board Reference	Description	Schematic Signal Name	I/O Standard	Cyclone III LS Device Pin Number
J2.139	LVDS TX bit 14n or CMOS bit 66	HSMA_TX_N14	LVDS or 2.5-V	AE28
J2.140	LVDS RX bit 14n or CMOS bit 67	HSMA_RX_N14		L25
J2.143	LVDS TX bit 15 or CMOS bit 68	HSMA_TX_P15		AF27
J2.144	LVDS RX bit 15 or CMOS bit 69	HSMA_RX_P15		M23
J2.145	LVDS TX bit 15n or CMOS bit 70	HSMA_TX_N15		AE26
J2.146	LVDS RX bit 15n or CMOS bit 71	HSMA_RX_N15		L23
J2.149	LVDS TX bit 16 or CMOS bit 72	HSMA_TX_P16		AD26
J2.150	LVDS RX bit 16 or CMOS bit 73	HSMA_RX_P16		K22
J2.151	LVDS TX bit 16n or CMOS bit 74	HSMA_TX_N16		AD27
J2.152	LVDS RX bit 16n or CMOS bit 75	HSMA_RX_N16		K23
J2.155	LVDS or CMOS clock out 2 or CMOS bit 76	HSMA_CLKOUT_P2		M25
J2.156	LVDS or CMOS clock in 2 or CMOS bit 77	HSMA_CLKIN_P2		T27
J2.157	LVDS or CMOS clock out 2n or CMOS bit 78	HSMA_CLKOUT_N2		N26
J2.158	LVDS or CMOS clock in 2n or CMOS bit 79	HSMA_CLKIN_N2		T28
J2.160	HSMC port A presence detect	HSMA_PRSNTn	2.5-V	—

Note to Table 2–34:

(1) Board references J2.1 to J2.32 are not connected.

The HSMB data signals 65 through 75, HSMB_D[65:75], are multiplexed with the LCD data and control signals. The LCD/HSMC port B data select header switch (J18) controls data multiplexing to the FPGA from the LCD or HSMB_D[65:75]. To control the HSMB_D[65:75] signals via the FPGA, set LCD_HSMB_SEL to logic 1 by removing the shunt from the LCD/HSMC port B data select header switch (J18).

Table 2–35 lists the HSMC port B interface pin assignments, signal names, and functions.

Table 2–35. HSMC Port B Pin Assignments, Schematic Signal Names, and Functions (Part 1 of 4) *(1)*

Board Reference	Description	Schematic Signal Name	I/O Standard	Cyclone III LS Device Pin Number
J1.33	Management serial data	HSMB_SDA	2.5-V	G5
J1.34	Management serial clock	HSMB_SCL		J5
J1.35	JTAG clock signal	JTAG_TCK		–
J1.36	JTAG mode select signal	JTAG_TMS		–
J1.37	JTAG data output	HSMB_JTAG_TDO		–
J1.38	JTAG data input	HSMB_JTAG_TDI		–
J1.39	Dedicated CMOS clock out	HSMB_CLKOUT0		D2
J1.40	Dedicated CMOS clock in	HSMB_CLKIN0		B13
J1.41	Dedicated CMOS I/O bit 0	HSMB_D0		M5
J1.42	Dedicated CMOS I/O bit 1	HSMB_D1		W5
J1.43	Dedicated CMOS I/O bit 2	HSMB_D2		M4

Table 2–35. HSMC Port B Pin Assignments, Schematic Signal Names, and Functions (Part 2 of 4) *(1)*

Board Reference	Description	Schematic Signal Name	I/O Standard	Cyclone III LS Device Pin Number
J1.44	Dedicated CMOS I/O bit 3	HSMB_D3	2.5-V	V6
J1.47	Dedicated CMOS I/O bit 4	HSMB_D4		L5
J1.48	Dedicated CMOS I/O bit 5	HSMB_D5		U2
J1.49	Dedicated CMOS I/O bit 6	HSMB_D6		L4
J1.50	Dedicated CMOS I/O bit 7	HSMB_D7		U3
J1.53	Dedicated CMOS I/O bit 8	HSMB_D8		K5
J1.54	Dedicated CMOS I/O bit 9	HSMB_D9		U5
J1.55	Dedicated CMOS I/O bit 10	HSMB_D10		K4
J1.56	Dedicated CMOS I/O bit 11	HSMB_D11		P4
J1.59	Dedicated CMOS I/O bit 12	HSMB_D12		J7
J1.60	Dedicated CMOS I/O bit 13	HSMB_D13		P3
J1.61	Dedicated CMOS I/O bit 14	HSMB_D14		J6
J1.62	Dedicated CMOS I/O bit 15	HSMB_D15		N6
J1.65	Dedicated CMOS I/O bit 16	HSMB_D16		H6
J1.66	Dedicated CMOS I/O bit 17	HSMB_D17		M6
J1.67	Dedicated CMOS I/O bit 18	HSMB_D18		H2
J1.68	Dedicated CMOS I/O bit 19	HSMB_D19		K3
J1.71	Dedicated CMOS I/O bit 20	HSMB_D20		H1
J1.72	Dedicated CMOS I/O bit 21	HSMB_D21		K2
J1.73	Dedicated CMOS I/O bit 22	HSMB_D22		G6
J1.74	Dedicated CMOS I/O bit 23	HSMB_D23		J3
J1.77	Dedicated CMOS I/O bit 24	HSMB_D24		G3
J1.78	Dedicated CMOS I/O bit 25	HSMB_D25		J1
J1.79	Dedicated CMOS I/O bit 26	HSMB_D26		G1
J1.80	Dedicated CMOS I/O bit 27	HSMB_D27		J2
J1.83	Dedicated CMOS I/O bit 28	HSMB_D28		G2
J1.84	Dedicated CMOS I/O bit 29	HSMB_D29		H3
J1.85	Dedicated CMOS I/O bit 30	HSMB_D30		F4
J1.86	Dedicated CMOS I/O bit 31	HSMB_D31		E3
J1.89	Dedicated CMOS I/O bit 32	HSMB_D32		F1
J1.90	Dedicated CMOS I/O bit 33	HSMB_D33		E4
J1.91	Dedicated CMOS I/O bit 34	HSMB_D34		F5
J1.92	Dedicated CMOS I/O bit 35	HSMB_D35		D1
J1.95	Dedicated CMOS I/O bit 36	HSMB_D36		E1
J1.96	Dedicated CMOS I/O bit 37	HSMB_D37		D3
J1.97	Dedicated CMOS I/O bit 38	HSMB_D38		E2
J1.98	Dedicated CMOS I/O bit 39	HSMB_D39		C1
J1.101	Dedicated CMOS I/O bit 40	HSMB_D40		AE3

Table 2–35. HSMC Port B Pin Assignments, Schematic Signal Names, and Functions (Part 3 of 4) *(1)*

Board Reference	Description	Schematic Signal Name	I/O Standard	Cyclone III LS Device Pin Number
J1.102	Dedicated CMOS I/O bit 41	HSMB_D41	2.5-V	AE2
J1.103	Dedicated CMOS I/O bit 42	HSMB_D42		AC4
J1.104	Dedicated CMOS I/O bit 43	HSMB_D43		AD3
J1.107	Dedicated CMOS I/O bit 44	HSMB_D44		AB2
J1.108	Dedicated CMOS I/O bit 45	HSMB_D45		AD1
J1.109	Dedicated CMOS I/O bit 46	HSMB_D46		AB4
J1.110	Dedicated CMOS I/O bit 47	HSMB_D47		AD4
J1.113	Dedicated CMOS I/O bit 48	HSMB_D48		AA2
J1.114	Dedicated CMOS I/O bit 49	HSMB_D49		AC1
J1.115	Dedicated CMOS I/O bit 50	HSMB_D50		AA1
J1.116	Dedicated CMOS I/O bit 51	HSMB_D51		AB1
J1.119	Dedicated CMOS I/O bit 52	HSMB_D52		AA6
J1.120	Dedicated CMOS I/O bit 53	HSMB_D53		AB5
J1.121	Dedicated CMOS I/O bit 54	HSMB_D54		Y2
J1.122	Dedicated CMOS I/O bit 55	HSMB_D55		AB3
J1.125	Dedicated CMOS I/O bit 56	HSMB_D56		Y1
J1.126	Dedicated CMOS I/O bit 57	HSMB_D57		AB6
J1.127	Dedicated CMOS I/O bit 58	HSMB_D58		Y6
J1.128	Dedicated CMOS I/O bit 59	HSMB_D59		AA5
J1.131	Dedicated CMOS I/O bit 60	HSMB_D60		W1
J1.132	Dedicated CMOS I/O bit 61	HSMB_D61		Y3
J1.133	Dedicated CMOS I/O bit 62	HSMB_D62		W2
J1.134	Dedicated CMOS I/O bit 63	HSMB_D63		AA4
J1.137	Dedicated CMOS I/O bit 64	HSMB_D64		W3
U29.7	Dedicated CMOS I/O bit 65 when LCD_HSMB_SEL is set to a logic 1.	LCD_HSMB_D65		P1
U28.4	Dedicated CMOS I/O bit 66 when LCD_HSMB_SEL is set to a logic 1.	LCD_HSMB_D66		AE4
U29.9	Dedicated CMOS I/O bit 67 when LCD_HSMB_SEL is set to a logic 1.	LCD_HSMB_D67		J4
U28.12	Dedicated CMOS I/O bit 68 when LCD_HSMB_SEL is set to a logic 1.	LCD_HSMB_D68		AE1
	Dedicated CMOS I/O bit 69 when LCD_HSMB_SEL is set to a logic 1.	LCD_HSMB_D69		AF1
U28.9	Dedicated CMOS I/O bit 70 when LCD_HSMB_SEL is set to a logic 1.	LCD_HSMB_D70		AD2
U29.4	Dedicated CMOS I/O bit 71 when LCD_HSMB_SEL is set to a logic 1.	LCD_HSMB_D71		L1
U27.4	Dedicated CMOS I/O bit 72 when LCD_HSMB_SEL is set to a logic 1.	LCD_HSMB_D72		V5

Table 2–35. HSMC Port B Pin Assignments, Schematic Signal Names, and Functions (Part 4 of 4) *(1)*

Board Reference	Description	Schematic Signal Name	I/O Standard	Cyclone III LS Device Pin Number
U27.7	Dedicated CMOS I/O bit 73 when LCD_HSMB_SEL is set to a logic 1.	LCD_HSMB_D73	2.5-V	W4
U27.12	Dedicated CMOS I/O bit 74 when LCD_HSMB_SEL is set to a logic 1.	LCD_HSMB_D74		W6
U27.9	Dedicated CMOS I/O bit 75 when LCD_HSMB_SEL is set to a logic 1.	LCD_HSMB_D75		W7
J1.155	LVDS or CMOS clock out 2 or CMOS bit 76	HSMB_CLKOUT_P2		T6
J1.156	LVDS or CMOS clock in 2 or CMOS bit 77	HSMB_CLKIN_P2		T2
J1.157	LVDS or CMOS clock out 2 or CMOS bit 77	HSMB_CLKOUT_N2		T5
J1.158	LVDS or CMOS clock in 2n or CMOS bit 79	HSMB_CLKIN_N2		T1
J1.160	HSMC port B presence detect LED	HSMB_PRSNTn		—
J18	To control the HSMB_D[65:75] via the FPGA, the shunt should be removed from this jumper, or the FPGA must drive a logic 1.	LCD_HSMB_SEL	1.8-V	D20

Note to Table 2–35:

(1) Board references J1.1 to J1.32 are not connected.

Table 2–36 lists the HSMC connector component reference and manufacturing information.

Table 2–36. HSMC Connector Component Reference and Manufacturing Information

Board Reference	Description	Manufacturer	Manufacturing Part Number	Manufacturer Website
J1 and J2	HSMC, custom version of QSH-DP family high-speed socket.	Samtec	ASP-122953-01	www.samtec.com

Memory

This section describes the board's memory interface support and also their signal names, types, and connectivity relative to the Cyclone III LS device. The board has the following memory interfaces:

- DDR2
- SSRAM
- Flash
- EEPROM

For more information about the memory interfaces, refer to the following documents:

- *AN 438: Constraining and Analyzing Timing for External Memory Interfaces in Stratix IV, Stratix III, and Cyclone III Devices.*
- *AN 445: Design Guidelines for Implementing DDR and DDR2 SDRAM Interfaces in Cyclone III Devices.*

DDR2

There are two DDR2 devices, providing 512 Mbit of memory each for a total of 1024 Mbit of on-board DDR2 SDRAM. Each device interface has a 16-bit data bus, which can be configured to run individually or together as a 32-bit data bus. One of the device is pinned out to FPGA bank 7 and a second device is pinned out to FPGA bank 8. These memory interfaces are designed to run at a maximum fequency of 167 MHz for a maximum theoretical bandwidth of over 10.6 Gbps. The internal bus in the FPGA is typically 2 or 4 times the width at full rate or half rate respectively. For example, a 167 MHz 16-bit interface will become a 83.5 MHz 64-bit bus.

Table 2–37 lists the DDR2 bank 7 pin assignments, signal names, and its functions. The signal names and types are relative to the Cyclone III LS device in terms of I/O setting and direction.

Table 2–37. DDR2 Bank 7 Pin Assignments, Signal Names and Functions (Part 1 of 2)

Board Reference	Description	Schematic Signal Name	I/O Standard	Cyclone III LS Device Pin Number
U6.M8	Address bus	DDR2_B7_A0	1.8-V SSTL Class I	E19
U6.M3	Address bus	DDR2_B7_A1		C24
U6.M7	Address bus	DDR2_B7_A2		A23
U6.N2	Address bus	DDR2_B7_A3		C15
U6.N8	Address bus	DDR2_B7_A4		D19
U6.N3	Address bus	DDR2_B7_A5		D16
U6.N7	Address bus	DDR2_B7_A6		A22
U6.P2	Address bus	DDR2_B7_A7		A15
U6.P8	Address bus	DDR2_B7_A8		A20
U6.P3	Address bus	DDR2_B7_A9		A17
U6.M2	Address bus	DDR2_B7_A10		C16
U6.P7	Address bus	DDR2_B7_A11		D18
U6.R2	Address bus	DDR2_B7_A12		D15
U6.R8	Address bus	DDR2_B7_A13		D17
U6.R3	Address bus	DDR2_B7_A14		E16
U6.R7	Address bus	DDR2_B7_A15		E17
U6.L2	Bank address bus	DDR2_B7_BA0		F22
U6.L3	Bank address bus	DDR2_B7_BA1		F19
U6.L1	Bank address bus	DDR2_B7_BA2		F16
U6.L7	Column address select	DDR2_B7_CASn		F17
U6.K2	Clock enable	DDR2_B7_CKE		B15
U6.L8	Chip select rank 0	DDR2_B7_CSn		A19
U6.K9	Termination enable rank 0	DDR2_B7_ODT		A18
U6.K7	Row address select	DDR2_B7_RASn		G16
U6.K3	Write enable	DDR2_B7_WEn		B24
U6.J8	Clock P	DDR2_B7_CLK_P	Differential 1.8-V SSTL Class I	D25
U6.K8	Clock N	DDR2_B7_CLK_N		C25

Table 2–37. DDR2 Bank 7 Pin Assignments, Signal Names and Functions (Part 2 of 2)

Board Reference	Description	Schematic Signal Name	I/O Standard	Cyclone III LS Device Pin Number
U6.F3	Write mask byte lane 0	DDR2_DM0	1.8-V SSTL Class I	C22
U6.B3	Write mask byte lane 1	DDR2_DM1		B25
U6.G8	Data bus byte lane 0	DDR2_DQ0		G20
U6.G2	Data bus byte lane 0	DDR2_DQ1		B19
U6.H7	Data bus byte lane 0	DDR2_DQ2		B21
U6.H3	Data bus byte lane 0	DDR2_DQ3		G19
U6.H1	Data bus byte lane 0	DDR2_DQ4		C19
U6.H9	Data bus byte lane 0	DDR2_DQ5		A21
U6.F1	Data bus byte lane 0	DDR2_DQ6		B18
U6.F9	Data bus byte lane 0	DDR2_DQ7		B22
U6.C8	Data bus byte lane 1	DDR2_DQ8		A26
U6.C2	Data bus byte lane 1	DDR2_DQ9		B27
U6.D7	Data bus byte lane 1	DDR2_DQ10		D23
U6.D3	Data bus byte lane 1	DDR2_DQ11		D22
U6.D1	Data bus byte lane 1	DDR2_DQ12		F21
U6.D9	Data bus byte lane 1	DDR2_DQ13		A25
U6.B1	Data bus byte lane 1	DDR2_DQ14		E21
U6.B9	Data bus byte lane 1	DDR2_DQ15		A27
U6.F7	Data strobe P byte lane 0	DDR2_DQS0		C18
U6.B7	Data strobe P byte lane 1	DDR2_DQS1		E22

Table 2–38 lists the DDR2 bank 8 pin assignments, signal names, and its functions. The signal names and types are relative to the Cyclone III LS device in terms of I/O setting and direction.

Table 2–38. DDR2 Bank 8 Pin Assignments, Signal Names and Functions (Part 1 of 2)

Board Reference	Description	Schematic Signal Name	I/O Standard	Cyclone III LS Device Pin Number
U5.M8	Address bus	DDR2_B8_A0	1.8-V SSTL Class I	C5
U5.M3	Address bus	DDR2_B8_A1		F7
U5.M7	Address bus	DDR2_B8_A2		E5
U5.N2	Address bus	DDR2_B8_A3		G12
U5.N8	Address bus	DDR2_B8_A4		C4
U5.N3	Address bus	DDR2_B8_A5		D10
U5.N7	Address bus	DDR2_B8_A6		D5
U5.P2	Address bus	DDR2_B8_A7		B4
U5.P8	Address bus	DDR2_B8_A8		A5
U5.P3	Address bus	DDR2_B8_A9		C9
U5.M2	Address bus	DDR2_B8_A10		E10

Table 2–38. DDR2 Bank 8 Pin Assignments, Signal Names and Functions (Part 2 of 2)

Board Reference	Description	Schematic Signal Name	I/O Standard	Cyclone III LS Device Pin Number
U5.P7	Address bus	DDR2_B8_A11	1.8-V SSTL Class I	B5
U5.R2	Address bus	DDR2_B8_A12		A2
U5.R8	Address bus	DDR2_B8_A13		A4
U5.R3	Address bus	DDR2_B8_A14		A3
U5.R7	Address bus	DDR2_B8_A15		D4
U5.L2	Bank address bus	DDR2_B8_BA0		D11
U5.L3	Bank address bus	DDR2_B8_BA1		D9
U5.L1	Bank address bus	DDR2_B8_BA2		C13
U5.L7	Column address select	DDR2_B8_CASn		D6
U5.K2	Clock enable	DDR2_B8_CKE		G9
U5.L8	Chip select rank 0	DDR2_B8_CSn		E7
U5.K9	Termination enable rank 0	DDR2_B8_ODT		F8
U5.K7	Row address select	DDR2_B8_RASn		C8
U5.K3	Write enable	DDR2_B8_WEn		E8
U5.J8	Clock P	DDR2_B8_CLK_P	Differential 1.8-V SSTL Class I	B8
U5.K8	Clock N	DDR2_B8_CLK_N		A8
U5.F3	Write mask byte lane 2	DDR2_DM2	1.8-V SSTL Class I	D8
U5.B3	Write mask byte lane 3	DDR2_DM3		A9
U5.G8	Data bus byte lane 2	DDR2_DQ16		B11
U5.G2	Data bus byte lane 2	DDR2_DQ17		C12
U5.H7	Data bus byte lane 2	DDR2_DQ18		G10
U5.H3	Data bus byte lane 2	DDR2_DQ19		C11
U5.H1	Data bus byte lane 2	DDR2_DQ20		A6
U5.H9	Data bus byte lane 2	DDR2_DQ21		A7
U5.F1	Data bus byte lane 2	DDR2_DQ22		D12
U5.F9	Data bus byte lane 2	DDR2_DQ23		F10
U5.C8	Data bus byte lane 3	DDR2_DQ24		E14
U5.C2	Data bus byte lane 3	DDR2_DQ25		B12
U5.D7	Data bus byte lane 3	DDR2_DQ26		G14
U5.D3	Data bus byte lane 3	DDR2_DQ27		A10
U5.D1	Data bus byte lane 3	DDR2_DQ28		A12
U5.D9	Data bus byte lane 3	DDR2_DQ29		F14
U5.B1	Data bus byte lane 3	DDR2_DQ30		D14
U5.B9	Data bus byte lane 3	DDR2_DQ31		D13
U5.F7	Data strobe P byte lane 2	DDR2_DQS2		G13
U5.B7	Data strobe P byte lane 3	DDR2_DQS3		A11

Table 2–39 lists the DDR2 component references and manufacturing information.

Table 2–39. DDR2 Component References and Manufacturing Information

Board Reference	Description	Manufacturer	Manufacturing Part Number	Manufacturer Website
U5 and U6	8 M × 16 × 4 banks, 512 Mbit, 667 Mbps, CL5	Micron	MT47H32M16HR-3:F	www.micron.com

SSRAM

The SSRAM device consists of a single standard synchronous SRAM, providing 2 Mbyte with a 36-bit data bus. This device is part of the shared FSM bus which connects to the flash memory, SRAM, and MAX II CPLD EPM2210 System Controller.

The device speed is 200 MHz single-data-rate. There is no minimum speed for this device. The theoretical bandwidth of this 32-bit memory interface is 6.4 Gbps for continuous bursts. The read latency for any address is two clocks, in which at 200 MHz, the latency is 10 ns and at 50 MHz, the latency is 40 ns. The write latency is one clock.

Table 2–40 lists the SSRAM pin assignments, signal names, and functions. The signal names and types are relative to the Cyclone III LS device in terms of I/O setting and direction.

Table 2–40. SSRAM Pin Assignments, Schematic Signal Names, and Functions (Part 1 of 3)

Board Reference	Description	Schematic Signal Name	I/O Standard	Cyclone III LS Device Pin Number
U14.R6	Address bus	FSM_A2	2.5-V	AA17
U14.P6	Address bus	FSM_A3		AE12
U14.A2	Address bus	FSM_A4		AF21
U14.A10	Address bus	FSM_A5		AH2
U14.B2	Address bus	FSM_A6		AB12
U14.B10	Address bus	FSM_A7		AG24
U14.N6	Address bus	FSM_A8		AE25
U14.P3	Address bus	FSM_A9		AH21
U14.P4	Address bus	FSM_A10		AD25
U14.P8	Address bus	FSM_A11		AC9
U14.P9	Address bus	FSM_A12		AF4
U14.P10	Address bus	FSM_A13		AE10
U14.P11	Address bus	FSM_A14		AH26
U14.R3	Address bus	FSM_A15		AG22
U14.R4	Address bus	FSM_A16		AF12
U14.R8	Address bus	FSM_A17		AE19
U14.R9	Address bus	FSM_A18		AA9
U14.R10	Address bus	FSM_A19		AE6
U14.R11	Address bus	FSM_A20		AG18
U14.B1	Address bus	FSM_A21		AE11

Table 2–40. SSRAM Pin Assignments, Schematic Signal Names, and Functions (Part 2 of 3)

Board Reference	Description	Schematic Signal Name	I/O Standard	Cyclone III LS Device Pin Number
U14.A1	Address bus	FSM_A22	2.5-V	AB16
U14.B11	Address bus	FSM_A23		AE13
U14.C10	Address bus	FSM_A24		AG11
U14.P2	Address bus	FSM_A25		AE9
U14.J10	Data bus	FSM_D0		AH9
U14.J11	Data bus	FSM_D1		AH24
U14.K10	Data bus	FSM_D2		AF25
U14.K11	Data bus	FSM_D3		AE5
U14.L10	Data bus	FSM_D4		AB11
U14.L11	Data bus	FSM_D5		AD24
U14.M10	Data bus	FSM_D6		AF9
U14.M11	Data bus	FSM_D7		AE7
U14.D10	Data bus	FSM_D8		AE23
U14.D11	Data bus	FSM_D9		AF15
U14.E10	Data bus	FSM_D10		AD17
U14.E11	Data bus	FSM_D11		AF20
U14.F10	Data bus	FSM_D12		AH25
U14.F11	Data bus	FSM_D13		AE18
U14.G10	Data bus	FSM_D14		AD6
U14.G11	Data bus	FSM_D15		AG20
U14.D1	Data bus	FSM_D16		AH20
U14.D2	Data bus	FSM_D17		AH18
U14.E1	Data bus	FSM_D18		AF8
U14.E2	Data bus	FSM_D19		AE20
U14.F1	Data bus	FSM_D20		AB19
U14.F2	Data bus	FSM_D21		AB10
U14.G1	Data bus	FSM_D22		AC17
U14.G2	Data bus	FSM_D23		AD10
U14.J1	Data bus	FSM_D24		AG9
U14.J2	Data bus	FSM_D25		AE21
U14.K1	Data bus	FSM_D26		AD22
U14.K2	Data bus	FSM_D27		AH23
U14.L1	Data bus	FSM_D28		AG5
U14.L2	Data bus	FSM_D29		AB9
U14.M1	Data bus	FSM_D30		AD9
U14.M2	Data bus	FSM_D31		AD16
U14.A8	Address status controller	SRAM_ADSCn		AH19
U14.B9	Address status processor	SRAM_ADSPn		AB18
U14.A9	Address valid	SRAM_ADVn		AB20

Table 2–40. SSRAM Pin Assignments, Schematic Signal Names, and Functions (Part 3 of 3)

Board Reference	Description	Schematic Signal Name	I/O Standard	Cyclone III LS Device Pin Number
U14.A7	Byte write enable	SRAM_BWEn	2.5-V	AH8
U14.B5	Byte lane 0 write enable	SRAM_BWn0		AC12
U14.A5	Byte lane 1 write enable	SRAM_BWn1		AH11
U14.A4	Byte lane 2 write enable	SRAM_BWn2		AH4
U14.B4	Byte lane 3 write enable	SRAM_BWn3		AE22
U14.B3	Chip enable	SRAM_CE2		—
U14.A6	Chip enable	SRAM_CE3n		—
U14.A3	Chip enable	SRAM_CEn		AH10
U14.B6	Clock	SRAM_CLK		AG25
U14.N11	Data bus parity byte lane 0	SRAM_DQP0		AD19
U14.C11	Data bus parity byte lane 1	SRAM_DQP1		AF22
U14.C1	Data bus parity byte lane 2	SRAM_DQP2		AE8
U14.N1	Data bus parity byte lane 3	SRAM_DQP3		AE17
U14.B7	Global write enable	SRAM_GWn		AC19
U14.R1	Mode	SRAM_MODE		—
U14.B8	Output enable	SRAM_OEn		AB13
U14.H11	Sleep	SRAM_ZZ		AH14

Table 2–41 lists the SSRAM component reference and manufacturing information.

Table 2–41. SSRAM Component Reference and Manufacturing Information

Board Reference	Description	Manufacturer	Manufacturing Part Number	Manufacturer Website
U14	Standard Synchronous Pipelined SCD, 512 K × 36, 200 MHz	ISSI Inc.	IS61VPS51236A-250B3	www.issi.com

Flash

The flash interface consists of a single synchronous flash memory device, providing 64 Mbyte with a 16-bit data bus. This device is part of the shared FSM bus which connects to the flash memory, SRAM, and MAX II CPLD EPM2210 System Controller.

There are two 256-Mbyte die per package with A(25) low selecting the lower die and A(25) high selecting the upper die. The parameter blocks are 32 K and main blocks are 128 K. The parameters of this device are located at both the top and bottom of the address space.

This 16-bit data memory interface can sustain burst read operations at up to 52 MHz for a throughput of 832 Mbps. The write performance is 125 µs for a single word and 440 µs for a 32-word buffer. The erase time is 400 ms for a 32 K parameter block and 1200 ms for a 128 K main block.

Table 2–42 lists the flash pin assignments, signal names, and functions. The signal names and types are relative to the Cyclone III LS device in terms of I/O setting and direction.

Table 2–42. Flash Pin Assignments, Schematic Signal Names, and Functions (Part 1 of 2)

Board Reference	Description	Schematic Signal Name	I/O Standard	Cyclone III LS Device Pin Number
U9.F6	Address valid	FLASH_ADVn		AF18
U9.B4	Chip enable	FLASH_CEn		AH22
U9.E6	Clock	FLASH_CLK		AH6
U9.F8	Output enable	FLASH_OEn		AD7
U9.F7	Ready	FLASH_RDYBSYn		V4
U9.D4	Reset	FLASH_RESETn		AH5
U9.G8	Write enable	FLASH_WEn		AH17
U9.C6	Address valid	FLASH_WPn		—
U9.A1	Address bus	FSM_A1		AD14
U9.B1	Address bus	FSM_A2		AA17
U9.C1	Address bus	FSM_A3		AE12
U9.D1	Address bus	FSM_A4		AF21
U9.D2	Address bus	FSM_A5		AH2
U9.A2	Address bus	FSM_A6		AB12
U9.C2	Address bus	FSM_A7		AG24
U9.A3	Address bus	FSM_A8		AE25
U9.B3	Address bus	FSM_A9		AH21
U9.C3	Address bus	FSM_A10	2.5-V	AD25
U9.D3	Address bus	FSM_A11		AC9
U9.C4	Address bus	FSM_A12		AF4
U9.A5	Address bus	FSM_A13		AE10
U9.B5	Address bus	FSM_A14		AH26
U9.C5	Address bus	FSM_A15		AG22
U9.D7	Address bus	FSM_A16		AF12
U9.D8	Address bus	FSM_A17		AE19
U9.A7	Address bus	FSM_A18		AA9
U9.B7	Address bus	FSM_A19		AE6
U9.C7	Address bus	FSM_A20		AG18
U9.C8	Address bus	FSM_A21		AE11
U9.A8	Address bus	FSM_A22		AB16
U9.G1	Address bus	FSM_A23		AE13
U9.H8	Address bus	FSM_A24		AG11
U9.B6	Address bus (die select)	FSM_A25		AE9
U9.F2	Data bus	FSM_D0		AH9
U9.E2	Data bus	FSM_D1		AH24

Table 2–42. Flash Pin Assignments, Schematic Signal Names, and Functions (Part 2 of 2)

Board Reference	Description	Schematic Signal Name	I/O Standard	Cyclone III LS Device Pin Number
U9.G3	Data bus	FSM_D2	2.5-V	AF25
U9.E4	Data bus	FSM_D3		AE5
U9.E5	Data bus	FSM_D4		AB11
U9.G5	Data bus	FSM_D5		AD24
U9.G6	Data bus	FSM_D6		AF9
U9.H7	Data bus	FSM_D7		AE7
U9.E1	Data bus	FSM_D8		AE23
U9.E3	Data bus	FSM_D9		AF15
U9.F3	Data bus	FSM_D10		AD17
U9.F4	Data bus	FSM_D11		AF20
U9.F5	Data bus	FSM_D12		AH25
U9.H5	Data bus	FSM_D13		AE18
U9.G7	Data bus	FSM_D14		AD6
U9.E7	Data bus	FSM_D15		AG20

Table 2–43 lists the flash component reference and manufacturing information.

Table 2–43. Flash Component Reference and Manufacturing Information

Board Reference	Description	Manufacturer	Manufacturing Part Number	Manufacturer Website
U9	512 Mbyte Synchronous Flash	Numonyx	PC48F4400P0VB00	www.numonyx.com

EEPROM

A 32-Kbit I²C serial EEPROM is accessible from the Cyclone III LS device. The EEPROM speed is between 100 KHz and 400 KHz.

Table 2–44 lists the EEPROM pin assignments, signal names, and functions. The signal names and types are relative to the Cyclone III LS device in terms of I/O setting and direction.

Table 2–44. EEPROM Pin Assignments, Schematic Signal Names, and Functions

Board Reference	Description	Schematic Signal Name	I/O Standard	Cyclone III LS Device Pin Number
U21.6	EEPROM serial clock	EEPROM_SCL	2.5-V	AA3
U21.5	EEPROM serial data	EEPROM_SDA		AH3

Table 2–43 lists the flash component reference and manufacturing information.

Table 2–45. EEPROM Component Reference and Manufacturing Information

Board Reference	Description	Manufacturer	Manufacturing Part Number	Manufacturer Website
U21	32 Kbit I²C Serial EEPROM	Microchip Technology	24LC32Ax-I/SN	www.microchip.com

Power Supply

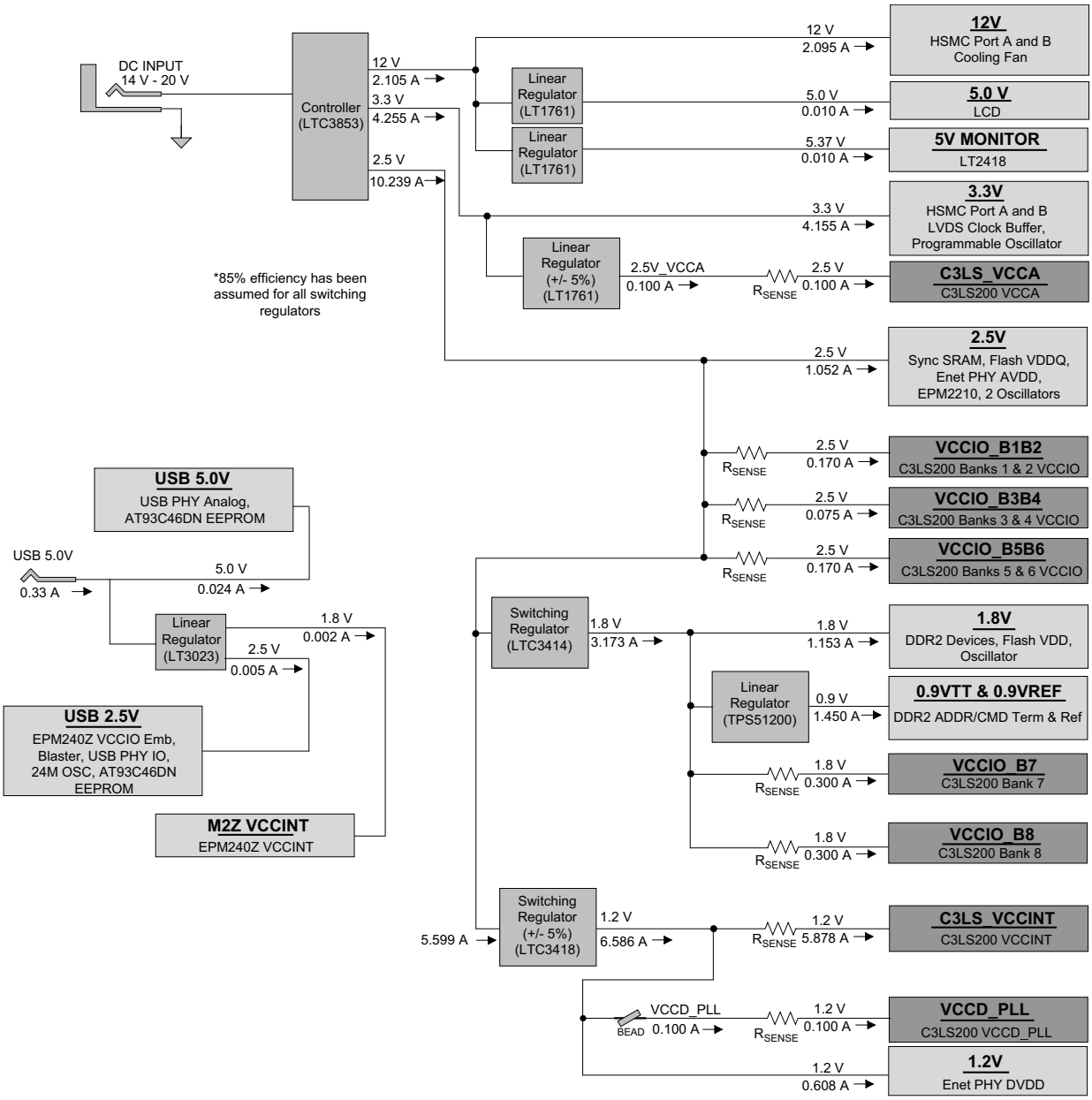
The development board's power is provided through a laptop style DC power input. The input voltage must be in the range of 14 V to 20 V. The DC voltage is then stepped down to various power rails used by the components on the board and installed into the HSMC connectors.

An on-board multi-channel analog-to-digital converter (ADC) is used to measure both the voltage and current for several specific board rails. The power utilization is displayed using a GUI that can graph power consumption versus time.

Power Distribution System

Figure 2–10 shows the power distribution system on the development board. Regulator inefficiencies and sharing are reflected in the currents shown, which are conservative absolute maximum levels.

Figure 2–10. Power Distribution System



Power Measurement

There are eight power supply rails which have on-board voltage and current sense capabilities. These 8-channel differential 24-bit ADC devices and rails are split from the primary supply plane by a low-value sense resistor for the ADC to measure voltage and current. A SPI bus connects these ADC devices to the MAX II CPLD EPM2210 System Controller as well as the Cyclone III LS FPGA.

Figure 2–11 shows the block diagram for the power measurement circuitry.

Figure 2–11. Power Measurement Circuit

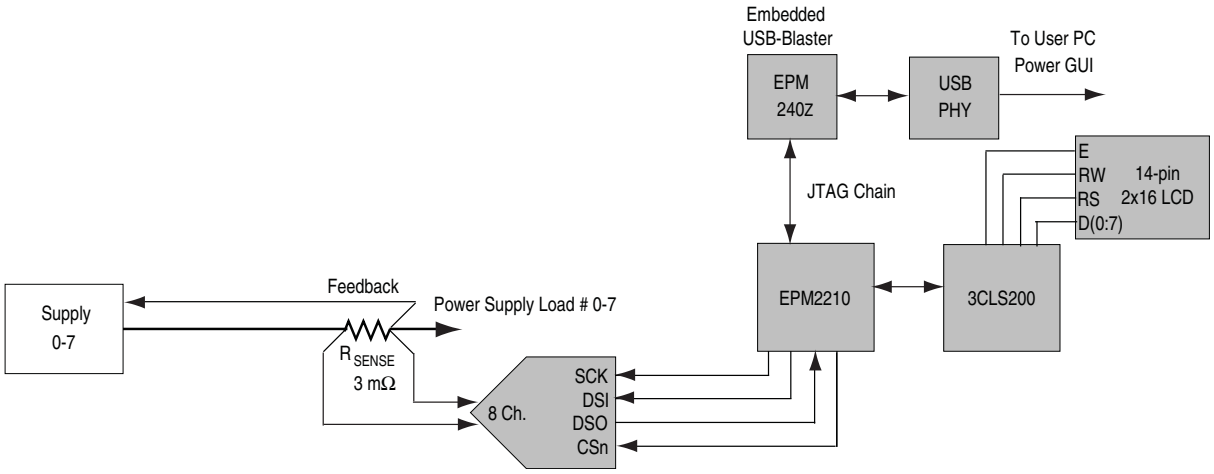


Table 2–46 lists the targeted rails. The schematic signal name column specifies the name of the rail being measured and the device pin column specifies the devices attached to the rail. If no subnet is named, the power is the total output power for that voltage.

Table 2–46. Power Rails Measurement Based on the Rail Selected in the Power GUI

Switch	Schematic Signal Name	Voltage (V)	Device Pin	Description
1	VCCIO_B1B2	2.5	VCCIO1	FPGA I/O power bank 1 (HSMB)
			VCCIO2	FPGA I/O power bank 2 (HSMB, flash)
2	VCCIO_B3B4	2.5	VCCIO3	FPGA I/O power bank 3 (MAX II, SSRAM, flash, FSM, Ethernet, user I/O)
			VCCIO4	FPGA I/O power bank 4 (MAX II, SSRAM, flash, FSM, Ethernet)
3	VCCIO_B5B6	2.5	VCCIO5	FPGA I/O power bank 5 (HSMA)
			VCCIO6	FPGA I/O power bank 6 (HSMA)
4	VCCIO_B7	1.8	VCCIO7	FPGA I/O power bank 7 (DDR2, user I/O)
5	VCCIO_B8	1.8	VCCIO8	FPGA I/O power bank 8 (DDR2, user I/O)
6	C3LS_VCCINT	1.2	VCCINT	FPGA core power
7	VCCD_PLL	1.2	VCCD_PLL	FPGA PLL digital power
8	C3LS_VCCA	2.5	VCCA	FPGA PLL analog power

Table 2–47 lists the power measurement ADC component reference and manufacturing information.

Table 2–47. Power Measurement ADC Component Reference and Manufacturing Information

Board Reference	Description	Manufacturer	Manufacturing Part Number	Manufacturer Website
U1	8-channel differential 24-bit ADC	Linear Technology	LTC2418CGN#PBF	www.linear.com

Statement of China-RoHS Compliance

Table 2–48 lists hazardous substances included with the kit.

Table 2–48. Table of Hazardous Substances' Name and Concentration *Notes (1), (2)*

Part Name	Lead (Pb)	Cadmium (Cd)	Hexavalent Chromium (Cr6+)	Mercury (Hg)	Polybrominated biphenyls (PBB)	Polybrominated diphenyl Ethers (PBDE)
Cyclone III LS FPGA development board	X*	0	0	0	0	0
16-V power supply	0	0	0	0	0	0
Type A-B USB cable	0	0	0	0	0	0
User guide	0	0	0	0	0	0

Notes to Table 2–48:

(1) 0 indicates that the concentration of the hazardous substance in all homogeneous materials in the parts is below the relevant threshold of the SJ/T11363-2006 standard.

(2) X* indicates that the concentration of the hazardous substance of at least one of all homogeneous materials in the parts is above the relevant threshold of the SJ/T11363-2006 standard, but it is exempted by EU RoHS.

Revision History

The following table displays the revision history for this reference manual.

Date and Document Version	Changes Made	Summary of Changes
October 2009 v1.0	Initial release.	—

How to Contact Altera

For the most up-to-date information about Altera products, refer to the following table.

Contact *(Note 1)*	Contact Method	Address
Technical support	Website	www.altera.com/support
Technical training	Website	www.altera.com/training
	Email	custrain@altera.com
Product literature	Website	www.altera.com/literature
Non-technical support (General)	Email	nacomp@altera.com
(Software Licensing)	Email	authorization@altera.com

Note to Table:

(1) You can also contact your local Altera sales office or sales representative.

Typographic Conventions

This document uses the typographic conventions shown in the following table.

Visual Cue	Meaning
Bold Type with Initial Capital Letters	Indicates command names, dialog box titles, dialog box options, and other GUI labels. For example, **Save As** dialog box.
bold type	Indicates directory names, project names, disk drive names, file names, file name extensions, and software utility names. For example, **\qdesigns** directory, **d:** drive, and **chiptrip.gdf** file.
Italic Type with Initial Capital Letters	Indicates document titles. For example, *AN 519: Design Guidelines.*
Italic type	Indicates variables. For example, *n* + 1. Variable names are enclosed in angle brackets (< >). For example, *<file name>* and *<project name>***.pof** file.
Initial Capital Letters	Indicates keyboard keys and menu names. For example, Delete key and the Options menu.
"Subheading Title"	Quotation marks indicate references to sections in a document and titles of Quartus II Help topics. For example, "Typographic Conventions."
`Courier type`	Indicates signal, port, register, bit, block, and primitive names. For example, `data1`, `tdi`, and `input`. Active-low signals are denoted by suffix `n`. For example, `resetn`. Indicates command line commands and anything that must be typed exactly as it appears. For example, `c:\qdesigns\tutorial\chiptrip.gdf`. Also indicates sections of an actual file, such as a Report File, references to parts of files (for example, the AHDL keyword `SUBDESIGN`), and logic function names (for example, `TRI`).
1., 2., 3., and a., b., c., and so on.	Numbered steps indicate a list of items when the sequence of the items is important, such as the steps listed in a procedure.
■ ■	Bullets indicate a list of items when the sequence of the items is not important.
	The hand points to information that requires special attention.
	A caution calls attention to a condition or possible situation that can damage or destroy the product or your work.
	A warning calls attention to a condition or possible situation that can cause you injury.
	The angled arrow instructs you to press Enter.
	The feet direct you to more information about a particular topic.