VIPER37

VIPerPlus family: fixed frequency offline converter

Datasheet - production data

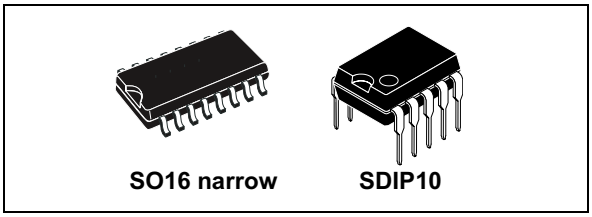
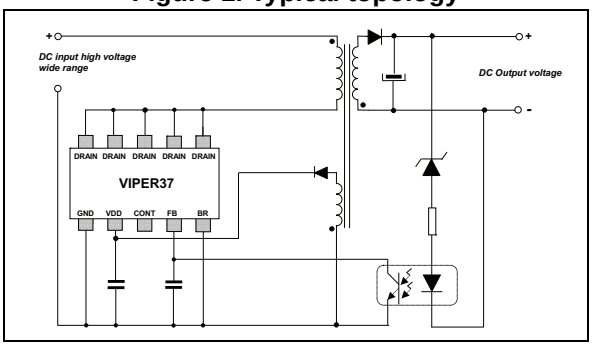


Figure 1. Typical topology



Features

- 800 V avalanche-rugged power MOSFET allowing ultra wide range input V_{ac} to be achieved
- PWM operation with adjustable limiting current
- 30 mW standby power at 265 V_{ac}
- Operating frequency:
  - 60 kHz (L type), 115 kHz (H type)
- Frequency jittering for low EMC
- Output overvoltage protection
- High primary current protection (2nd OCP)
- Input undervoltage setting (brownout)
- Onboard soft-start
- Safe auto-restart after a fault condition
- Hysteretic thermal shutdown

Applications

- SMPS for set-top boxes, DVD players and recorders, white goods
- Auxiliary power supply for consumer and home equipment
- ATX auxiliary power supply
- Low / medium power AC-DC adapters

Description

This device is an offline converter with an 800 V rugged power section, a PWM control, two levels of overcurrent protection, overvoltage and overload protection, hysteretic thermal protection, soft-start, and safe auto-restart after the removal of any fault condition. Burst mode operation and very low device consumption help to meet the standby energy saving regulations. Advance frequency jittering reduces EMI filter costs. Brownout function protects the switch mode power supply when the rectified input voltage level is below the normal minimum level specified for the system. The high voltage startup circuit is embedded in the device.

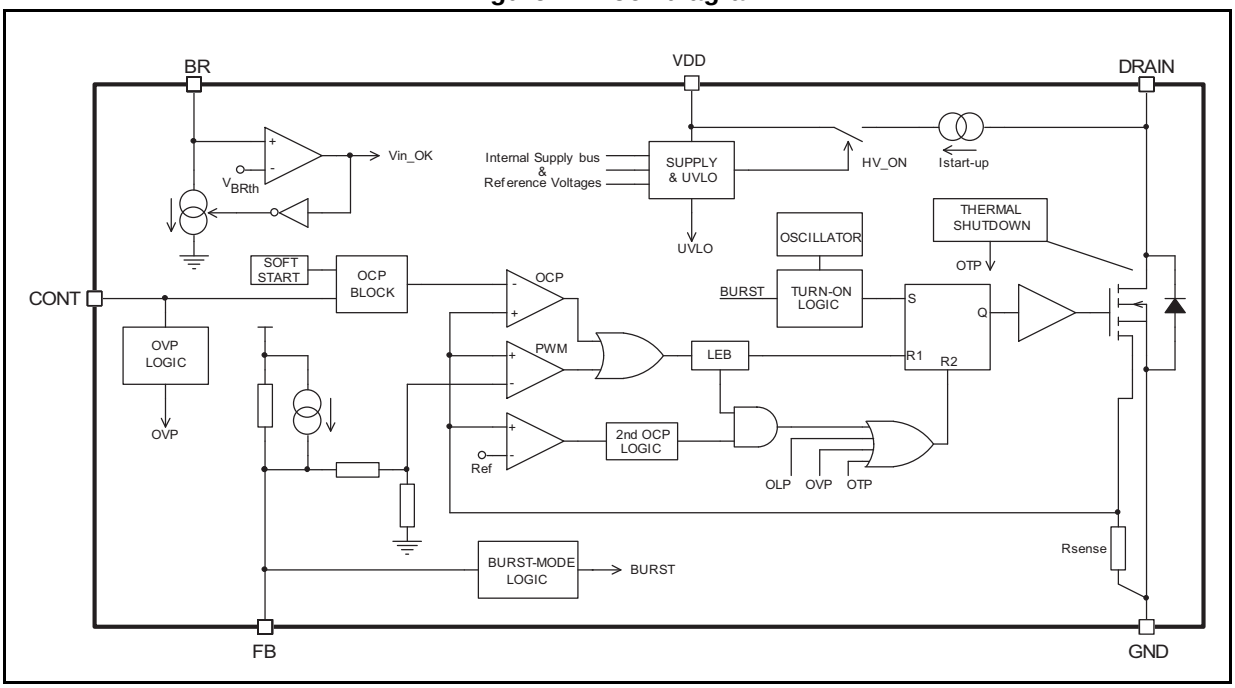
Table 1. Device summary

Order code	Package	Packing
VIPER37LE	SDIP10	Tube
VIPER37HE		
VIPER37HD	SO16 narrow	
VIPER37LD		
VIPER37HDTR		Tape and reel
VIPER37LDTR		

Contents

1 Block diagram

Figure 2. Block diagram



2 Typical power

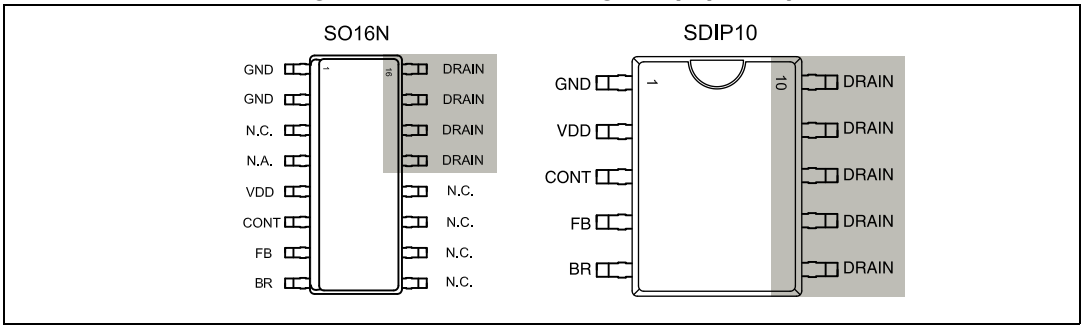
Table 2. Typical power

Part number	230 V_{AC}		85-265 V_{AC}	
	Adapter(1)	Open frame(2)	Adapter(1)	Open frame(2)
VIPER37	18 W	20 W	13 W	15 W

1. Typical continuous power in non-ventilated enclosed adapter measured at 50 °C ambient.
2. Maximum practical continuous power in an open frame design at 50 °C ambient, with adequate heatsinking.

3 Pin settings

Figure 3. Connection diagram (top view)



Note: The copper area for heat dissipation must be designed under the DRAIN pins.

Table 3. Pin description

Pin n. SO16N	Name	Function
1...2	GND	This pin represents the device ground and the source of the power section.
3	N.C.	Not connected.
4	N.A.	Not available for user. This pin is mechanically connected to the controller die pad of the frame. In order to improve the noise immunity, is highly recommended connect it to GND (pin 1-2).
5	VDD	Supply voltage of the control section. This pin also provides the charging current of the external capacitor during start-up time.
6	CONT	Control pin. The following functions can be selected: 1. current limit set point adjustment. The internal set default value of the cycle-by-cycle current limit can be reduced by connecting to ground an external resistor. 2. output voltage monitoring. A voltage exceeding V_{OVP} threshold (see *Table 8 on page 8*) shuts the IC down reducing the device consumption. This function is strobed and digitally filtered for high noise immunity.
7	FB	Control input for duty cycle control. Internal current generator provides bias current for loop regulation. A voltage below the threshold V_{FBbm} activates the burst-mode operation. A level close to the threshold V_{FBlin} means that we are approaching the cycle-by-cycle over-current set point.
8	BR	Brownout protection input with hysteresis. A voltage below the threshold V_{BRth} shuts down (not latch) the device and lowers the power consumption. Device operation restarts as the voltage exceeds the threshold $V_{BRth} + V_{BRhyst}$. It can be connected to ground when not used.
9...12	N.C.	Not connected.
13...16	DRAIN	High voltage drain pin. The built-in high voltage switched start-up bias current is drawn from this pin too. Pins connected to the metal frame to facilitate heat dissipation.

4 Electrical data

4.1 Maximum ratings

Table 4. Absolute maximum ratings

Symbol	Parameter	Value		Unit
		Min.	Max.	
V_{DRAIN}	Drain-to-source (ground) voltage		800	V
E_{AV}	Repetitive avalanche energy (limited by T_J = 150 °C)		5	mJ
I_{AR}	Repetitive avalanche current (limited by T_J = 150 °C)		1.5	A
I_{DRAIN}	Pulse drain current		3	A
V_{CONT}	Control input pin voltage	-0.3	6	V
V_{FB}	Feedback voltage	-0.3	5.5	V
V_{BR}	Brownout input pin voltage	-0.3	5	V
V_{DD}	Supply voltage (I_{DD} = 25 mA)	-0.3	Self limited	V
I_{DD}	Input current		25	mA
P_{TOT}	Power dissipation at T_A < 60 °C		1.5	W
T_J	Operating junction temperature range	-40	150	°C
T_{STG}	Storage temperature	-55	150	°C

4.2 Thermal data

Table 5. Thermal data

Symbol	Parameter	Max. value		Unit
		SO16N	SDIP10	
R_{thJP}	Thermal resistance junction pin (Dissipated power = 1 W)	35	35	°C/W
R_{thJA}	Thermal resistance junction ambient (Dissipated power = 1 W)	110	100	°C/W
R_{thJA}	Thermal resistance junction ambient (1) (Dissipated power = 1 W)	80	85	°C/W

1. When mounted on a standard single side FR4 board with 100 mm^2 (0.155 sq. in.) of Cu (35 µm thick).

4.3 Electrical characteristics

(T_J = -25 to 125 °C, V_{DD} = 14 V[a]; unless otherwise specified).

Table 6. Power section

Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
V_{BVDSS}	Breakdown voltage	I_{DRAIN} = 1 mA, V_{FB} = GND T_J = 25 °C	800			V
I_{OFF}	OFF state drain current	V_{DRAIN} = max. rating, V_{FB} = GND, T_J = 25 °C			60	µA
$R_{DS(on)}$	Drain-source on state resistance	I_{DRAIN} = 0.4 A, V_{FB} = 3 V, V_{BR} = GND, T_J = 25 °C			4.5	Ω
		I_{DRAIN} = 0.4 A, V_{FB} = 3 V, V_{BR} = GND, T_J = 125 °C			9	Ω
C_{OSS}	Effective (energy related) output capacitance	V_{DRAIN} = 0 to 640 V, T_J = 25 °C		17		pF

Table 7. Supply section

Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
Voltage						
V_{DRAIN_START}	Drain-source start voltage		60	80	100	V
I_{DDch}	Startup charging current	V_{DRAIN} = 120 V V_{BR} = GND V_{FB} = GND V_{DD} = 4 V	-2	-3	-4	mA
		V_{DRAIN} = 120 V V_{BR} = GND V_{FB} = GND V_{DD} = 5 V after fault	-0.4	-0.6	-0.8	mA
V_{DD}	Operating voltage range	After turn-on	8.5		23.5	V
$V_{DDclamp}$	V_{DD} clamp voltage	I_{DD} = 20 mA	23.5			V
V_{DDon}	V_{DD} startup threshold	V_{DRAIN} = 120 V V_{BR} = GND V_{FB} = GND	13	14	15	V
V_{DDoff}	V_{DD} undervoltage shutdown threshold		7.5	8	8.5	V
$V_{DD(RESTART)}$	V_{DD} restart voltage threshold		4	4.5	5	V

a. Adjust V_{DD} above V_{DDon} startup threshold before setting to 14 V.

Table 7. Supply section (continued)

Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
Current						
I_{DD0}	Operating supply current, not switching	V_{FB} = GND, F_{SW} = 0 kHz, V_{BR} = GND, V_{DD} = 10 V			0.9	mA
I_{DD1}	Operating supply current, switching	V_{DRAIN} = 120 V, F_{SW} = 60 kHz			2.5	mA
		V_{DRAIN} = 120 V, F_{SW} = 115 kHz			3.5	mA
I_{DD_FAULT}	Operating supply current, with protection tripping	V_{DD} = 10 V			400	µA
I_{DD_OFF}	Operating supply current with $V_{DD} < V_{DD\_OFF}$	V_{DD} = 7 V			270	µA

Table 8. Controller section

Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
Feedback pin						
V_{FBolp}	Overload shutdown threshold		4.5	4.8	5.2	V
V_{FBlin}	Linear dynamics upper limit		3.2	3.5	3.7	V
V_{FBbm}	Burst mode threshold	Voltage falling		0.6		V
$V_{FBbmhys}$	Burst mode hysteresis	Voltage rising		100		mV
I_{FB}	Feedback sourced current	V_{FB} = 0.3 V	-150	-200	-280	µA
		3.3 V < V_{FB} < 4.8 V		-3		µA
$R_{FB(DYN)}$	Dynamic resistance	V_{FB} < 3.3 V	14		21	kΩ
H_{FB}	$\Delta V_{FB} / \Delta I_D$		0.5		2	V/A
CONT pin						
V_{CONT_l}	Low level clamp voltage	I_{CONT} = -100 µA		0.5		V
V_{CONT_h}	High level clamp voltage	I_{CONT} = 1 mA	5	5.5	6	V
Current limitation						
I_{Dlim}	Max. drain current limitation	V_{FB} = 4 V, I_{CONT} = -10 µA T_J = 25 °C	0.95	1	1.05	A
t_{SS}	Soft-start time			8.5		ms
T_{ON_MIN}	Minimum turn-on time		220	400	480	ns
td	Propagation delay	(1)		100		ns
t_{LEB}	Leading edge blanking	(1)		300		ns
I_{D_BM}	Peak drain current during burst mode	V_{FB} = 0.6 V		160		mA

Table 8. Controller section (continued)

Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
Oscillator section						
F_{OSC}	VIPER37L	V_{DD} = operating voltage range, V_{FB} = 1 V	54	60	66	kHz
	VIPER37H		103	115	127	kHz
FD	Modulation depth	VIPER37L		±4		kHz
		VIPER37H		±8		kHz
FM	Modulation frequency			250		Hz
D_{MAX}	Maximum duty cycle		70		80	%
Overcurrent protection (2nd OCP)						
I_{DMAX}	Second overcurrent threshold			1.7		A
Overvoltage protection						
V_{OVP}	Overvoltage protection threshold		2.7	3	3.3	V
T_{STROBE}	Overvoltage protection strobe time			2.2		us
Brownout protection						
V_{BRth}	Brownout threshold	Voltage falling	0.41	0.45	0.49	V
V_{BRhyst}	Voltage hysteresis above V_{BRth}	Voltage rising		50		mV
I_{BRhyst}	Current hysteresis		7		12	µA
$V_{BRclamp}$	Clamp voltage	I_{BR} = 250 µA		3		V
V_{DIS}	Brownout disable voltage		50		150	mV
Thermal shutdown						
T_{SD}	Thermal shutdown temperature	(1)	150	160		°C
T_{HYST}	Thermal shutdown hysteresis	(1)		30		°C

1. Specification assured by design, characterization and statistical correlation.

Figure 4. Minimum turn-on time test circuit

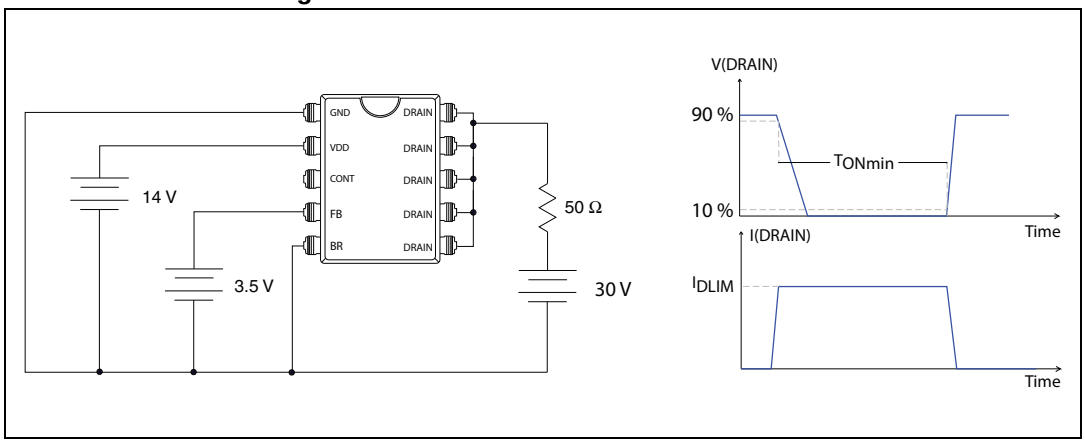


Figure 5. Brownout threshold test circuits

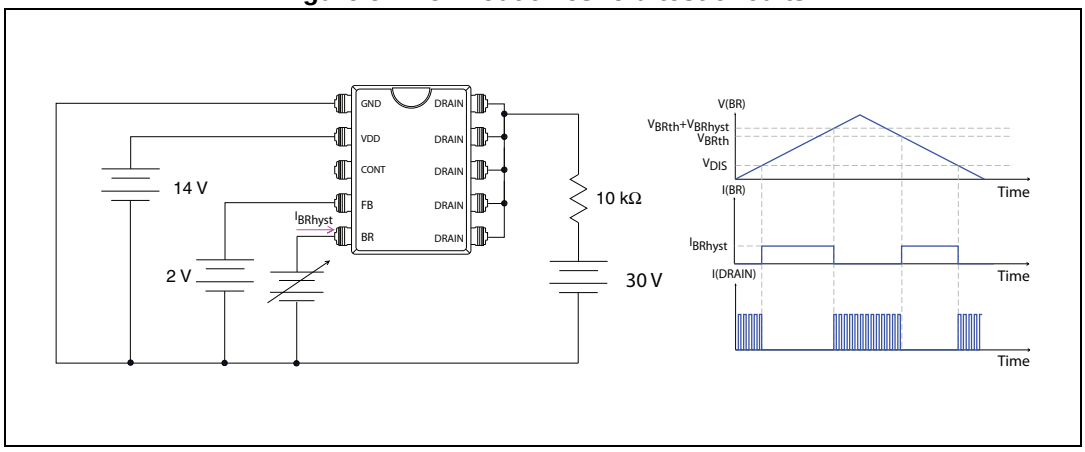
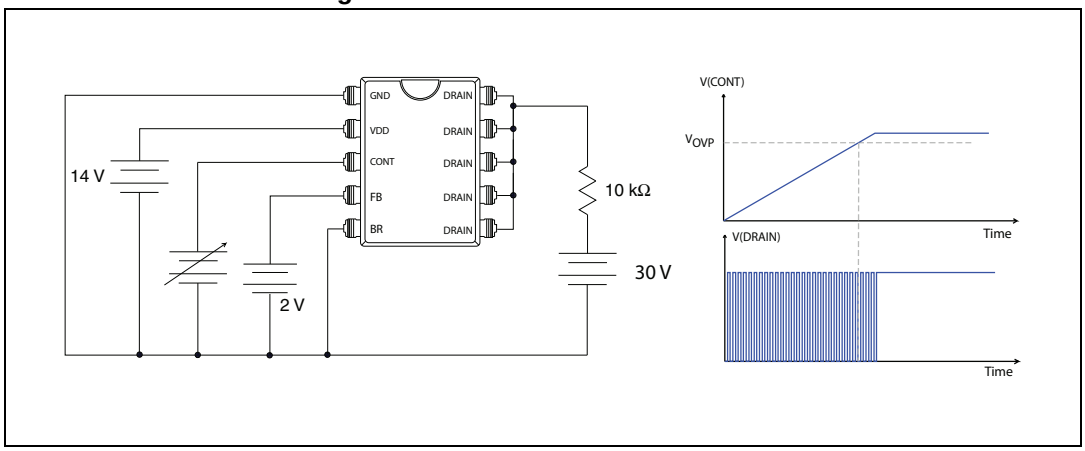


Figure 6. OVP threshold test circuits



Note: Adjust V_{DD} above V_{DDon} startup threshold before setting to 14 V.

5 Typical electrical characteristics

Figure 7. Current limit vs. T_J

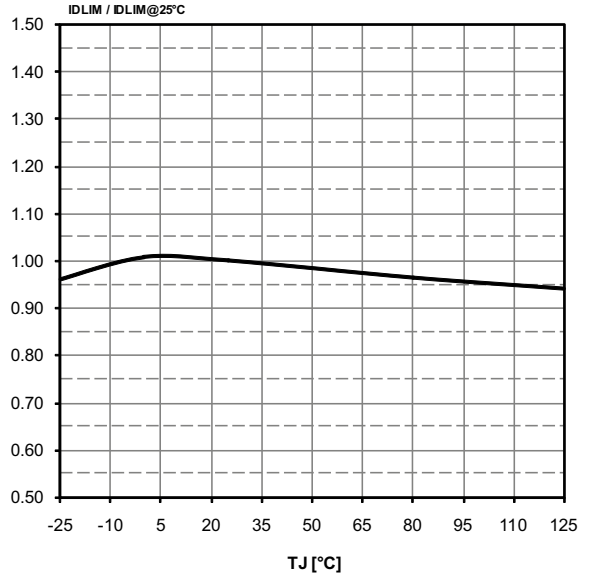


Figure 8. Switching frequency vs. T_J

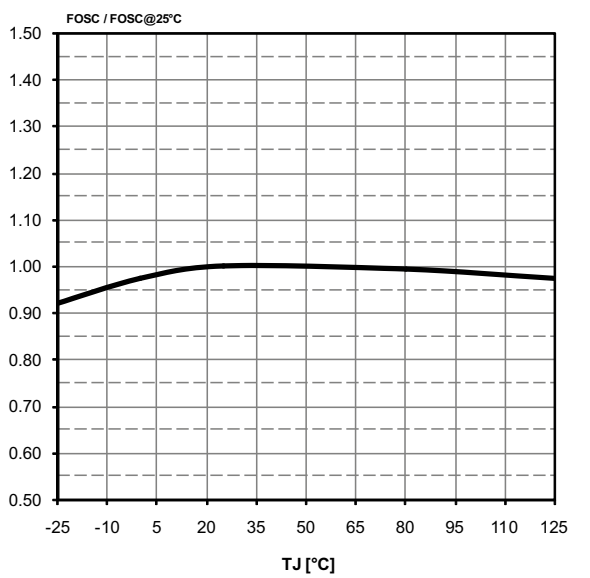


Figure 9. Drain start voltage vs. T_J

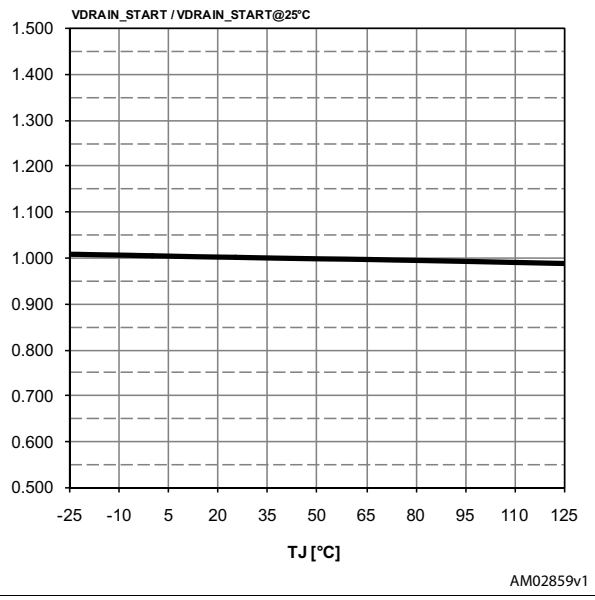


Figure 10. HFB vs. T_J

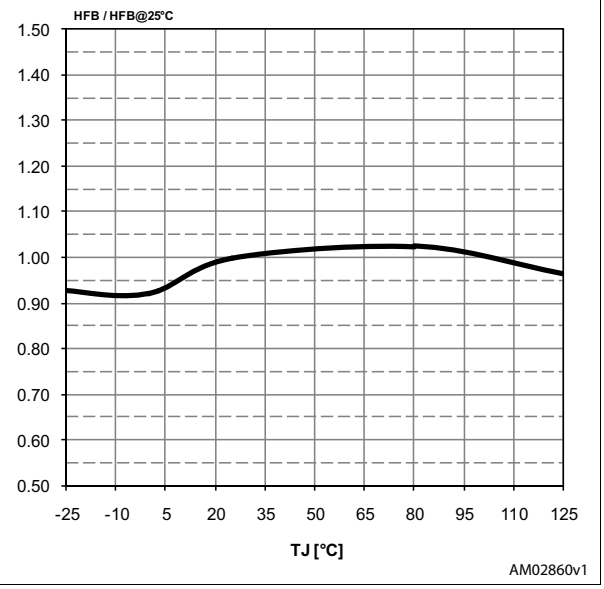


Figure 11. Brownout threshold vs. T_J

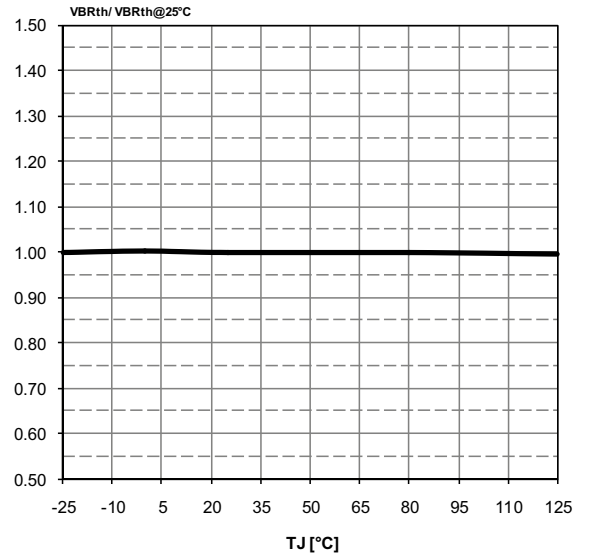


Figure 12. Brownout hysteresis vs. T_J

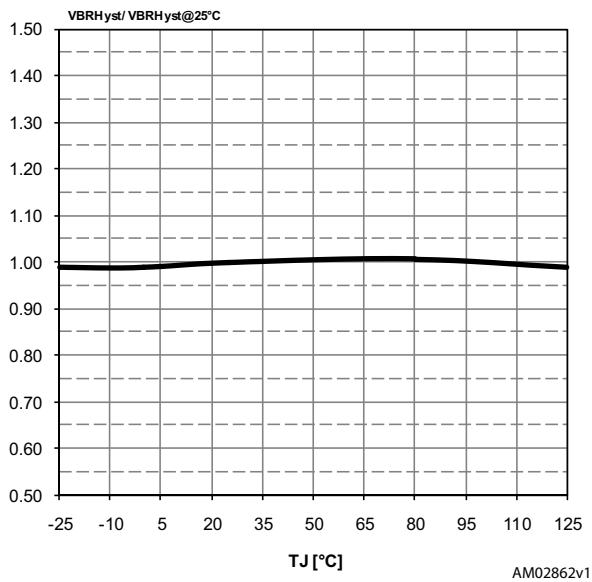


Figure 13. Brownout hysteresis current vs. T_J

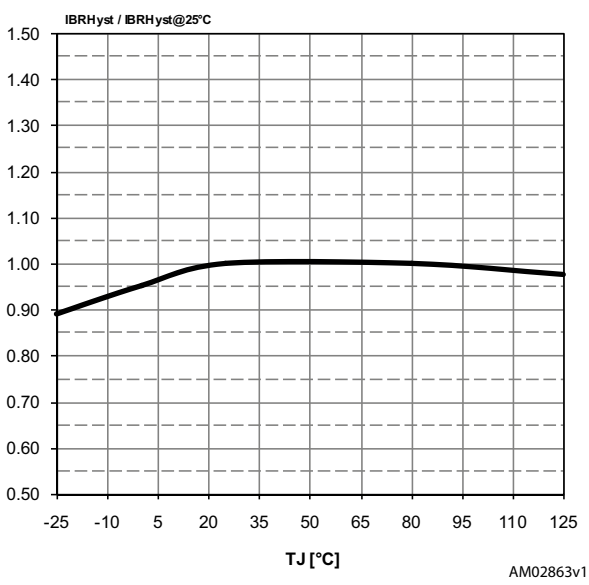


Figure 14. Operating supply current (not switching) vs. T_J

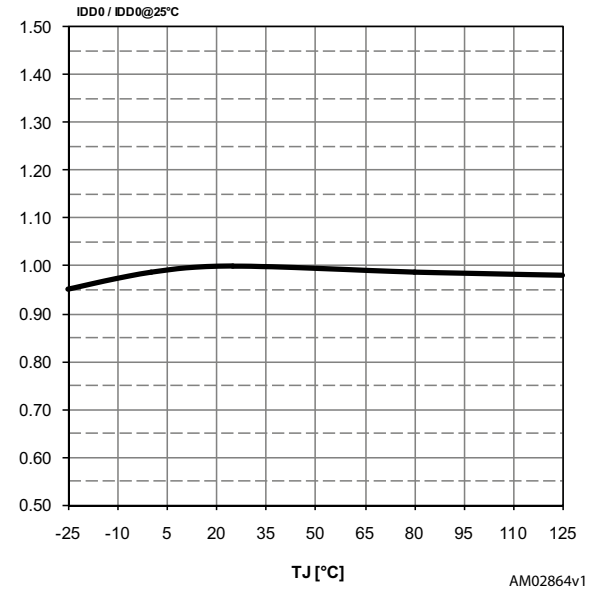


Figure 15. Operating supply current (switching) vs. T_J

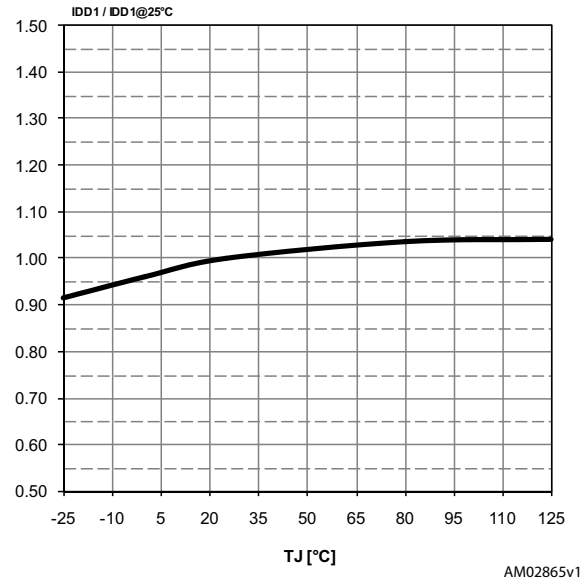


Figure 16. Current limit vs. R_{LIM}

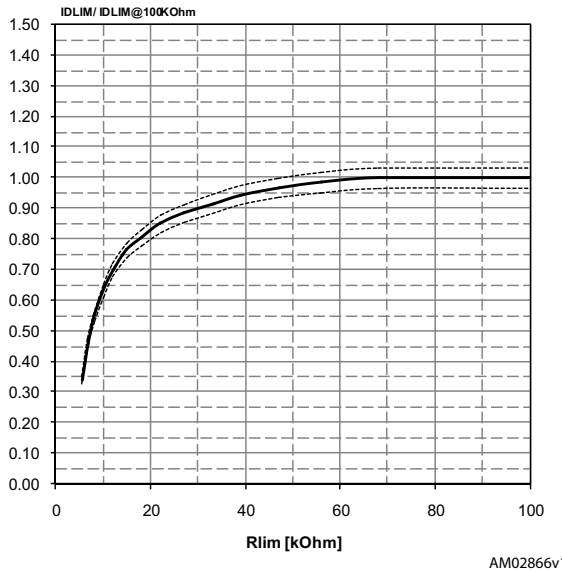


Figure 17. Power MOSFET ON resistance vs. T_J

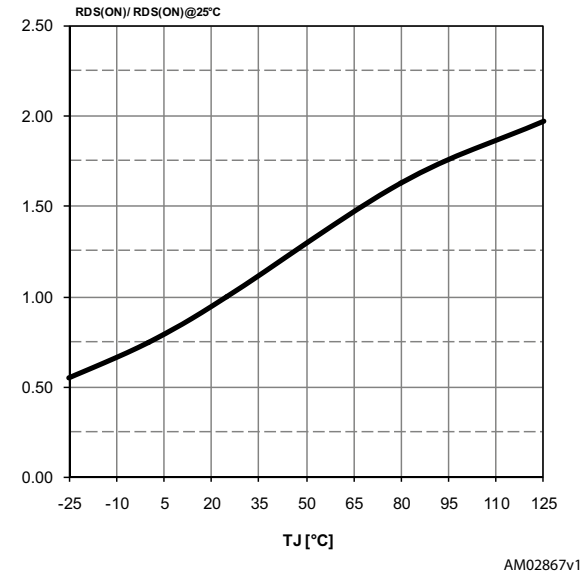


Figure 18. Power MOSFET breakdown voltage vs. T_J

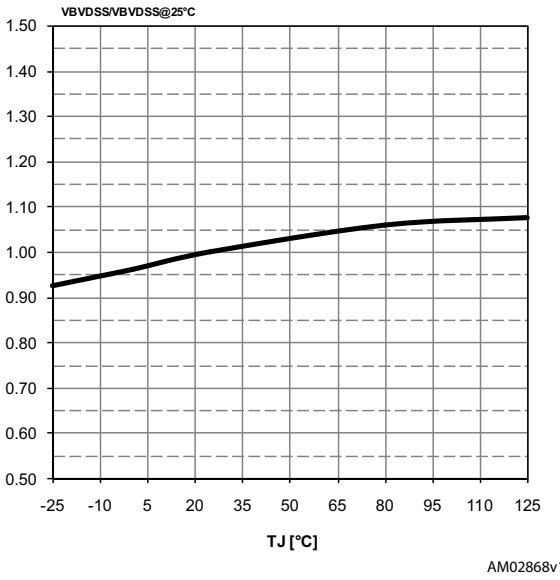
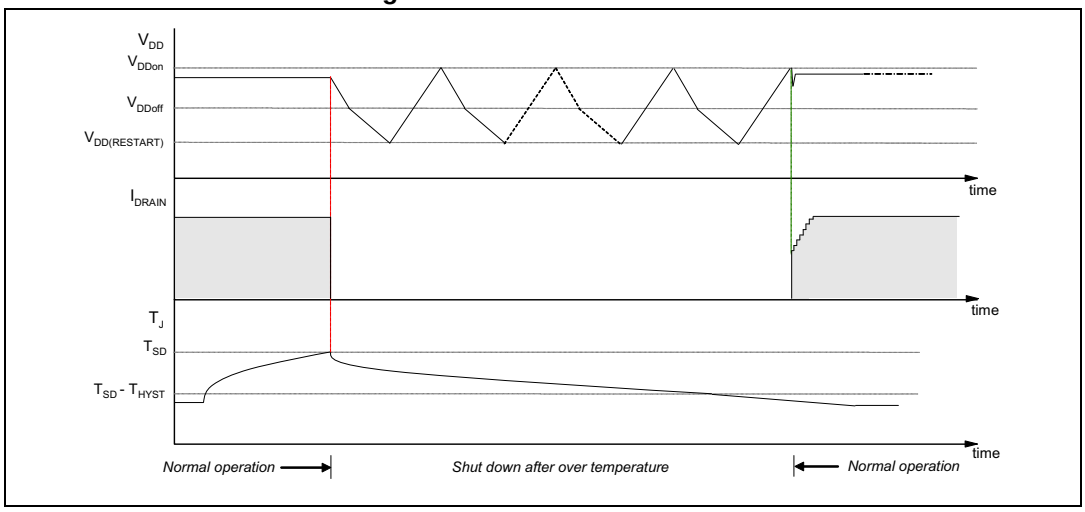


Figure 19. Thermal shutdown



6 Typical circuit

Figure 20. Min-features flyback application

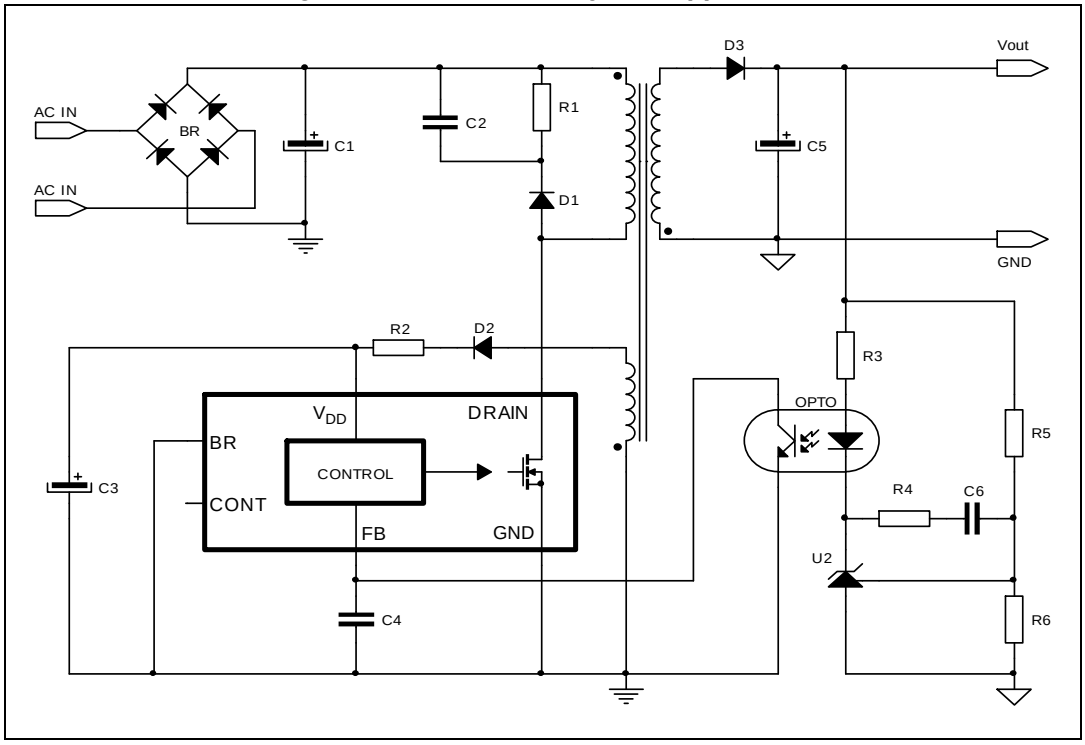
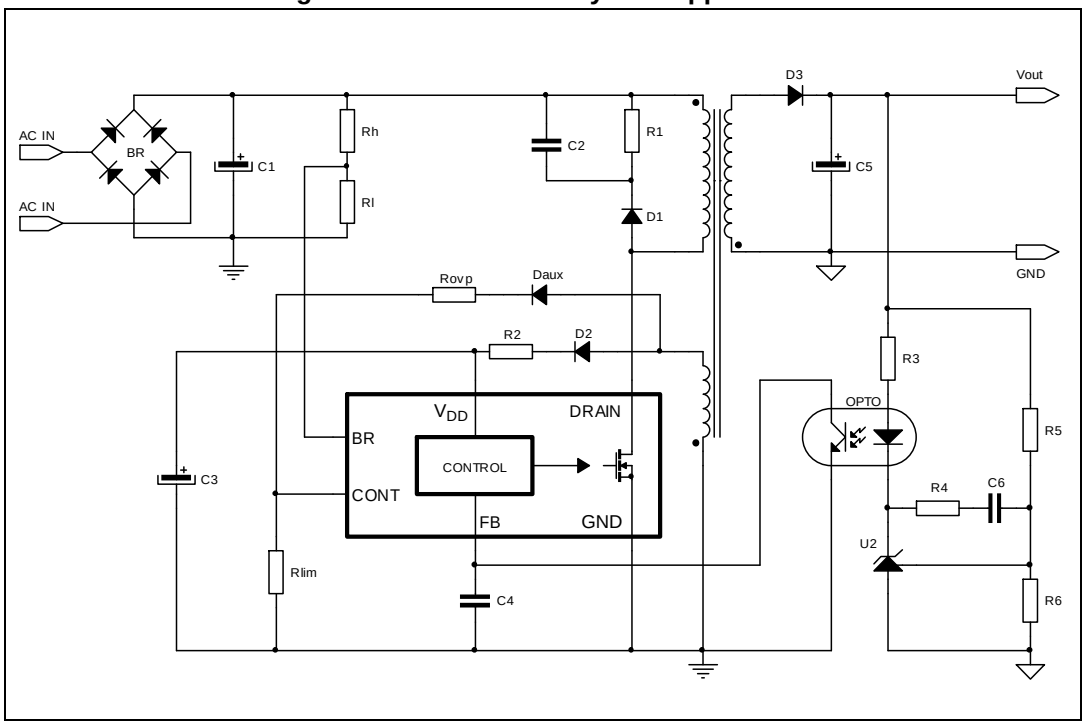


Figure 21. Full-features flyback application



7 Efficiency performances for a typical flyback converter

The efficiency of the converter has been measured in different load and line voltage conditions. In accordance with the ENERGY STAR® average active mode testing efficiency method, the efficiency measurements have been performed at 25%, 50% and 75% and 100% of the rated output power, at both 115 V_{AC} and 230 V_{AC}.

Table 9. Power supply efficiency, V_{OUT} = 5 V, V_{IN} = 115 V_{AC}

%Load	Iout [A]	Vout [V]	Pout [W]	Pin [W]	Efficiency [%]
25%	0.75	5.04	3.78	4.83	78.26%
50%	1.5	5.04	7.56	9.72	77.78%
75%	2.25	5.04	11.34	14.84	76.42%
100%	3	5.04	15.12	20.04	75.45%
Average efficiency					76.97%

Table 10. Power supply efficiency, V_{OUT}= 5 V, V_{IN} = 230 V_{AC}

%Load	Iout [A]	Vout [V]	Pout [W]	Pin [W]	Efficiency [%]
25%	0.75	5.04	3.78	5.01	75.45%
50%	1.5	5.04	7.56	9.76	77.46%
75%	2.25	5.04	11.34	14.67	77.30%
100%	3	5.03	15.09	19.59	77.03%
Average efficiency					76.81%

Figure 22. Power supply consumption at light output loads, V_{OUT}=5 V

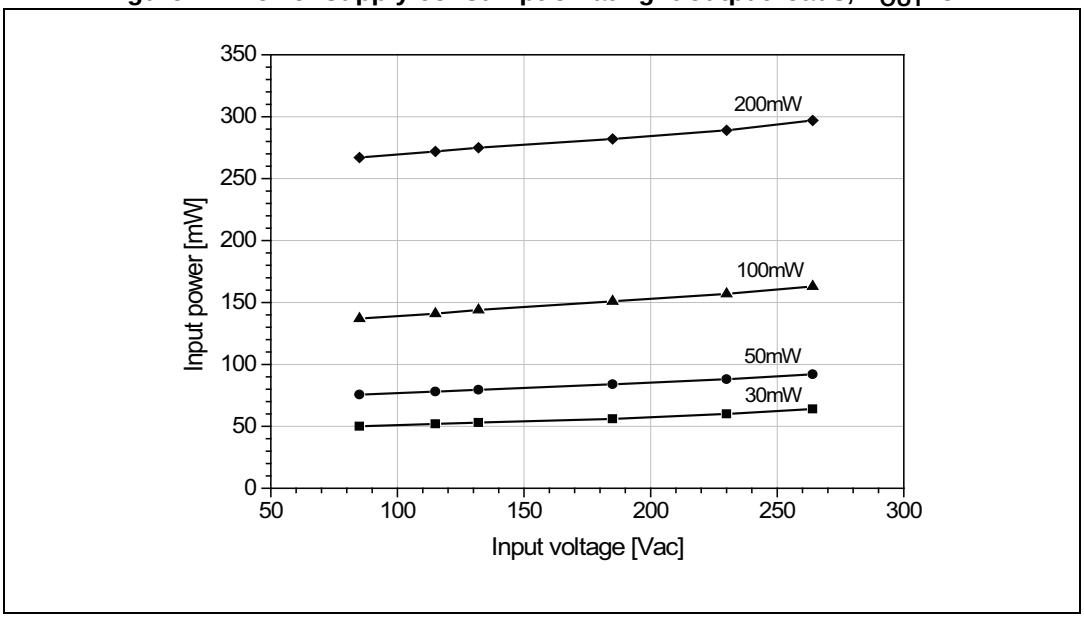
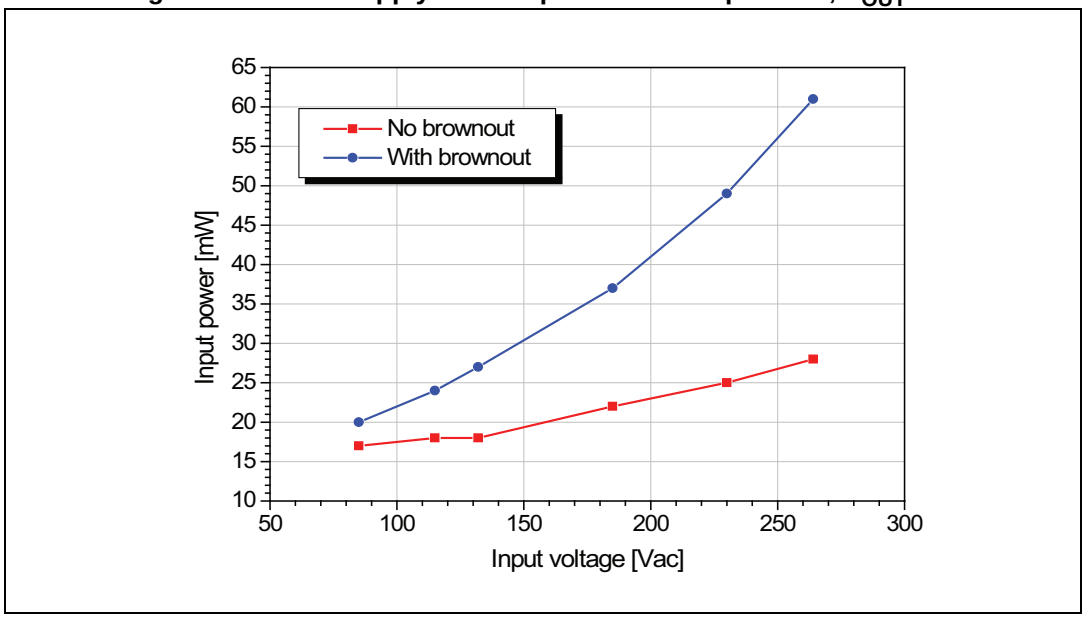


Figure 23. Power supply consumption at no output load, V_{OUT}=5 V



8 Operation description

The device is a high-performance low-voltage PWM controller chip with an 800 V avalanche rugged power section.

The controller includes: the oscillator with jittering feature, the startup circuits with soft-start feature, the PWM logic, the current limit circuit with adjustable set point, the second overcurrent circuit, the burst mode management, the brownout circuit, the UVLO circuit, the auto-restart circuit, and the thermal protection circuit.

The current limit set-point is set by the CONT pin. The burst mode operation guarantees high performance in standby mode and helps to accomplish the energy saving norm.

All the fault protections are built in auto-restart mode with very low repetition rate to prevent the IC overheating.

8.1 Power section and gate driver

The power section is implemented with an avalanche ruggedness N-channel MOSFET, which guarantees safe operation within the specified energy rating as well as high dv/dt capability. The power section has a B_{VDSS} of 800 V min. and a typical $R_{DS(on)}$ of 4.5 Ω at 25 °C.

The integrated SenseFET structure allows a virtually loss-less current sensing.

The gate driver is designed to supply a controlled gate current during both turn-on and turn-off in order to minimize common mode EMI. Under UVLO conditions an internal pull-down circuit holds the gate low in order to ensure that the power section cannot be turned on accidentally.

8.2 High voltage startup generator

The HV current generator is supplied through the DRAIN pin and is enabled only if the input bulk capacitor voltage is higher than the V_{DRAIN_START} threshold, 80 V_{DC} (typical). When the HV current generator is ON, the I_{DDch} current (3 mA typical value) is delivered to the capacitor on the V_{DD} pin. In the case of auto-restart mode after a fault event, the I_{DDch} current is reduced to 0.6 mA, in order to have a slow duty cycle during the restart phase.

8.3 Power-up and soft-start

If the input voltage rises up to the device start threshold V_{DRAIN_START}, the V_{DD} voltage begins to grow due to the I_{DDch} current (see *Table 7*) coming from the internal high voltage startup circuit. If the V_{DD} voltage reaches the V_{DDon} threshold (see *Table 7*), the Power MOSFET starts switching and the HV current generator is turned off (see *Figure 25*).

The IC is powered by the energy stored in the capacitor on the V_{DD} pin, C_{VDD}, until the self-supply circuit (typically an auxiliary winding of the transformer and a steering diode) develops a voltage high enough to sustain the operation.

The C_{VDD} capacitor must be sized correctly in order to avoid fast discharge and keep the needed voltage value higher than the V_{DDoff} threshold. In fact, a too low capacitance value could terminate the switching operation before the controller receives any energy from the auxiliary winding.

The following formula can be used for the V_{DD} capacitor calculation:

Equation 1

$$C_{VDD} = \frac{I_{DDch} \times t_{SSaux}}{V_{DDon} - V_{DDoff}}$$

The t_{SSaux} is the time needed for the steady-state of the auxiliary voltage. This time is estimated by the applicator according to the output stage configurations (transformer, output capacitances, etc.).

During the converter startup time, the drain current limitation is progressively increased to the maximum value. In this way the stress on the secondary diode is considerably reduced. It also helps to prevent transformer saturation. The soft-start time lasts 8.5 ms and the feature is implemented for every attempt of the startup converter or after a fault.

Figure 24. I_{DD} current during startup and burst mode

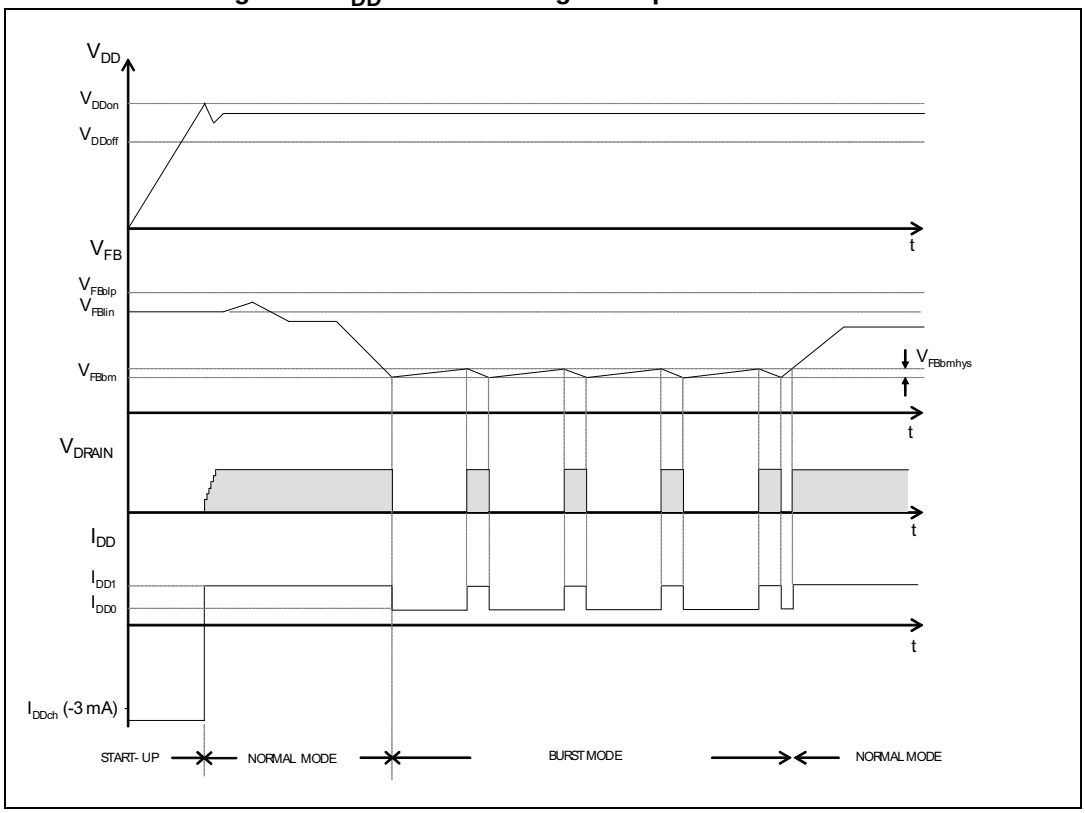


Figure 25. Timing diagram: normal power-up and power-down sequences

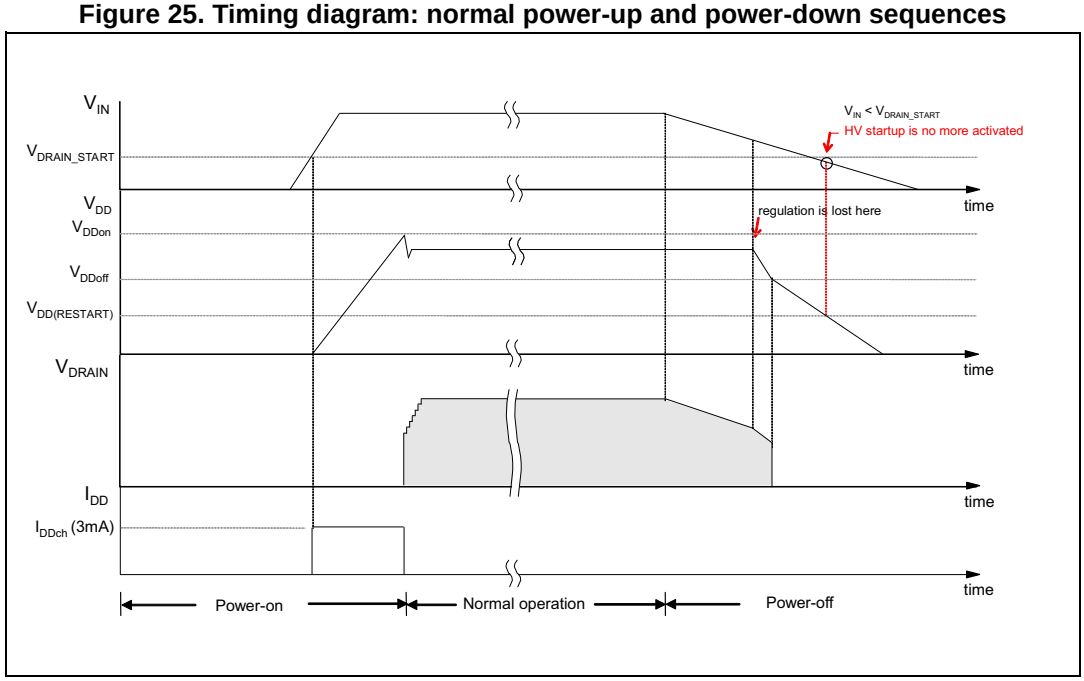
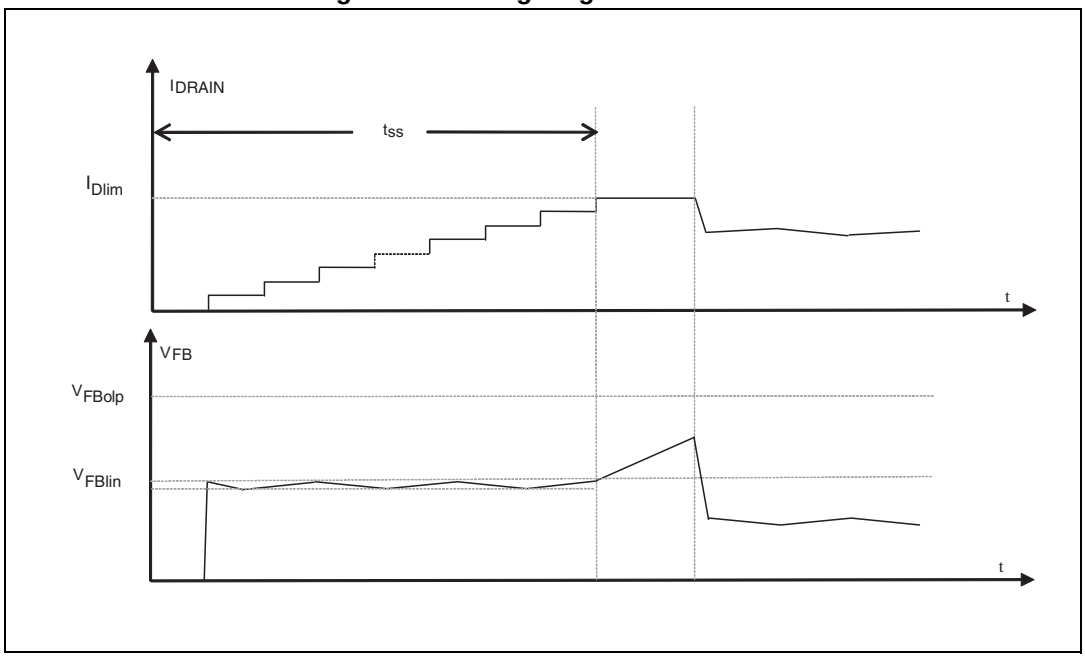


Figure 26. Timing diagram: soft-start



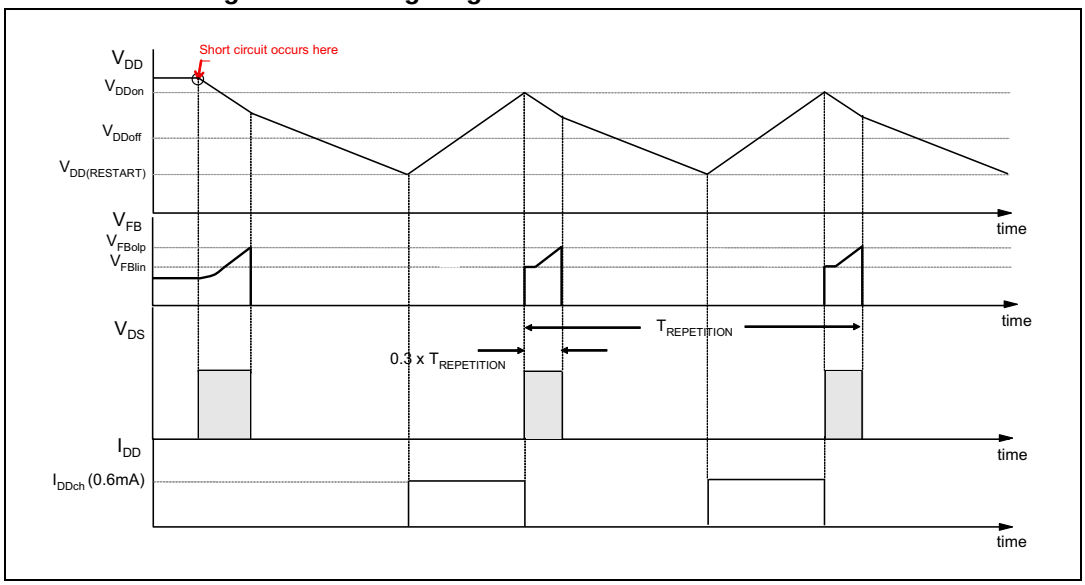
8.4 Power down operation

At converter power down, the system loses regulation as soon as the input voltage is so low that the peak current limitation is reached. The V_{DD} voltage drops and when it falls below the V_{DDoff} threshold (see *Table 7*) the Power MOSFET is switched OFF, the energy transfers to the IC interrupted and consequently the V_{DD} voltages decrease, *Figure 25*. Later, if the V_{IN} is lower than V_{DRAIN_START} (see *Table 7*), the startup sequence is inhibited and the power down completed. This feature is useful to prevent the converter's restart attempts and ensures monotonic output voltage decay during the system power down.

8.5 Auto-restart operation

If, after a converter power down, the V_{IN} is higher than $V_{DRAIN\_START,}$ the startup sequence is not inhibited and is activated only when the V_{DD} voltage drops below the $V_{DD(RESTART)}$ threshold (see *Table 7*). This means that the HV startup current generator restarts the V_{DD} capacitor charging only when the V_{DD} voltage drops below $V_{DD(RESTART)}$. The scenario described above is, for instance, a power down because of a fault condition. After a fault condition, the charging current I_{DDch} is 0.6 mA (typ.) instead of the 3 mA (typ.) of a normal startup converter phase. This feature, together with the low $V_{DD(RESTART)}$ threshold, ensures that, after a fault, the restart attempts of the IC have a very long repetition rate and the converter works safely with extremely low power throughput. *Figure 27* shows the IC behavior after a short-circuit event.

Figure 27. Timing diagram: behavior after short-circuit



8.6 Oscillator

The switching frequency is internally fixed to 60 kHz or 115 kHz. In both cases the switching frequency is modulated by approximately ±4 kHz (60 kHz version) or ±8 kHz (115 kHz version) at a 250 Hz (typ.) rate, so that the resulting spread-spectrum action distributes the energy of each harmonic of the switching frequency over a number of side-band harmonics having the same energy on the whole but smaller amplitudes.

8.7 Current mode conversion with adjustable current limit set point

This device is a current mode converter: the drain current is sensed and converted into voltage that is applied to the non-inverting pin of the PWM comparator. This voltage is compared with the one on the feedback pin through a voltage divider on a cycle-by-cycle basis.

The device has a default current limit value, I_{Dlim}, that the user can adjust according to the electrical specifications, through the R_{LIM} resistor connected to the CONT pin (see *Figure 16*).

The CONT pin has a minimum current sunk, needed to activate the I_{Dlim} adjustment: without R_{LIM} or with high R_{LIM} (i.e. 100 kΩ), the current limit is fixed to the default value (see I_{Dlim}, *Table 8*).

8.8 Overvoltage protection (OVP)

The device can monitor the converter output voltage. This operation is done by the CONT pin during Power MOSFET OFF-time, when the voltage generated by the auxiliary winding tracks the converter's output voltage, through turn ratio $\frac{N_{AUX}}{N_{SEC}}$ (see *Figure 28*).

In order to perform the output voltage monitor, the CONT pin must be connected to the aux. winding through a resistor divider made up of R_{LIM} and R_{OVP} (see *Figure 21* or *Figure 29*). If the voltage applied to the CONT pin exceeds the internal reference V_{OVP} (see *Table 8*) for four consecutive times, the controller recognizes an overvoltage condition. This special feature uses an internal counter; that is to reduce sensitivity to noise and prevent the latch from being erroneously activated (see *Figure 28*). The counter is reset every time the OVP signal is not triggered in one oscillator cycle.

Referring to *Figure 21*, the resistors' divider ratio k_{OVP} is given by:

Equation 2

$$k_{OVP} = \frac{V_{OVP}}{\frac{N_{AUX}}{N_{SEC}} \cdot (V_{OUTOVP} + V_{DSEC}) - V_{DAUX}}$$

Equation 3

$$k_{OVP} = \frac{R_{LIM}}{R_{LIM} + R_{OVP}}$$

where:

- V_{OVP} is the OVP threshold (see *Table 9*)
- $V_{OUT\ OVP}$ is the converter output voltage value to activate the OVP set by the user
- N_{AUX} is the auxiliary winding turns
- N_{SEC} is the secondary winding turns
- V_{DSEC} is the secondary diode forward voltage
- V_{DAUX} is the auxiliary diode forward voltage
- R_{OVP} together with R_{LIM} make up the output voltage divider.

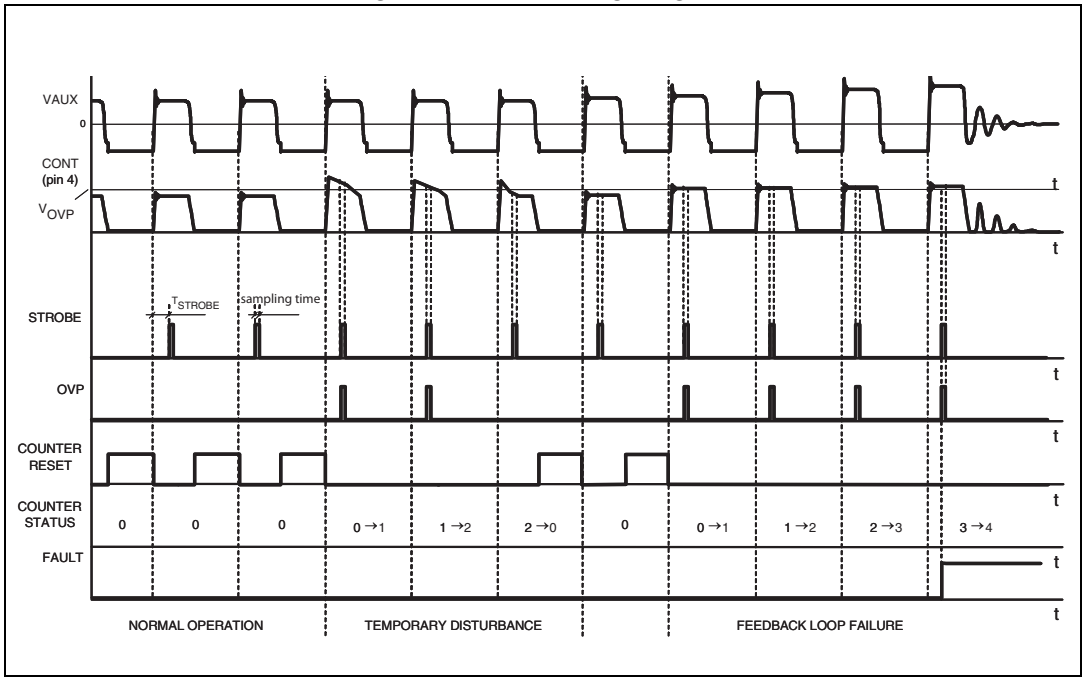
Then, once the $R_{LIM\ value\ is}$ fixed, according to the desired I_{Dlim}, the R_{OVP} can be calculated by:

Equation 4

$$R_{OVP} = R_{LIM} \times \frac{1 - k_{OVP}}{k_{OVP}}$$

The resistor values are such that the current sourced and sunk by the CONT pin are within the rated capability of the internal clamp.

Figure 28. OVP timing diagram



8.9 About the CONT pin

Referring to *Figure 29*, the features below can be implemented through the CONT pin:

1. Current limit set point
2. Overvoltage protection on the converter output voltage

Table 11, referring to *Figure 29*, lists the external resistance combinations needed to activate one or more of the CONT pin functions.

Figure 29. CONT pin configuration

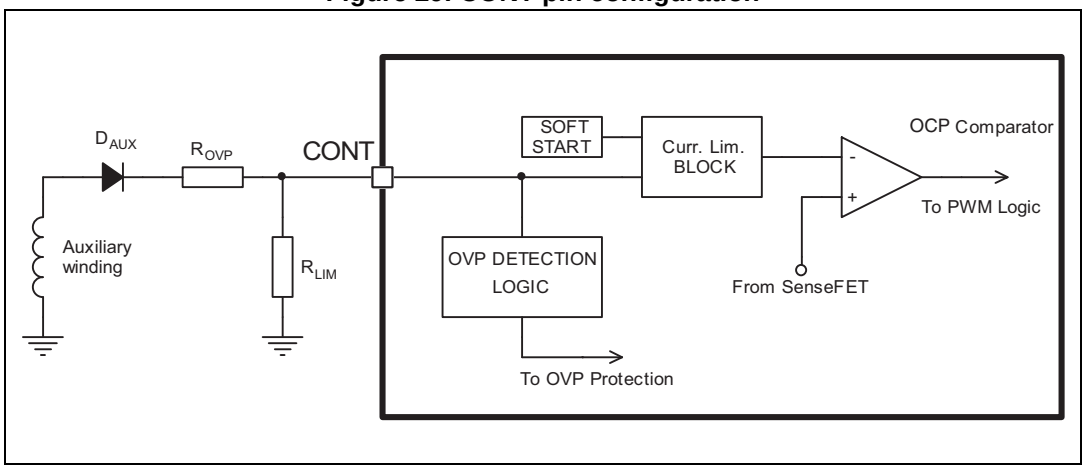


Table 11. CONT pin configurations

Function / component	R_{LIM} (1)	R_{OVP}	D_{AUX}
I_{Dlim} reduction	See *Figure 16*	No	No
OVP	≥ *80 kΩ*	See *Equation 4*	Yes
I_{Dlim} reduction + OVP	See *Figure 16*	See *Equation 4*	Yes

1. R_{LIM} must be fixed before R_{OVP}.

8.10 Feedback and overload protection (OLP)

The device is a current mode converter: the feedback pin controls the PWM operation, controls the burst mode, and actives the overload protection. *Figure 30* and *Figure 31* show the internal current mode structure.

With the feedback pin voltage between V_{FBbm} and V_{FBlin}, (see *Table 8*) the drain current is sensed and converted into voltage that is applied to the non-inverting pin of the PWM comparator.

This voltage is compared with the one on the feedback pin through a voltage divider on a cycle-by-cycle basis. When these two voltages are equal, the PWM logic orders the switch-off of the Power MOSFET. The drain current is always limited to the I_{Dlim} value.

In case of overload, the feedback pin increases in reaction to this event and when it goes higher than V_{FBlin}, the PWM comparator is disabled and the drain current is limited to I_{Dlim} by the OCP comparator, see *Figure 2*.

When the feedback pin voltage reaches the threshold V_{FBlin}, an internal current generator starts to charge the feedback capacitor (C_{FB}) and when the feedback voltage reaches the V_{FBolp} threshold, the converter is turned off and the startup phase is activated with a reduced value of I_{DDch} to 0.6 mA, see *Table 7*.

During the first startup phase of the converter, after the soft-start time (t_{SS}), the output voltage may force the feedback pin voltage to rise up to the V_{FBolp} threshold that switches off the converter itself.

To avoid this event, the appropriate feedback network must be selected according to the output load. Moreover, the feedback network fixes the compensation loop stability. *Figure 30* and *Figure 31* show the two different feedback networks.

The time from the overload detection (VFB = V_{FBlin}) to the device shutdown (VFB = V_{FBolp}) can be set by the C_{FB} value (see *Figure 30* and *Figure 31*), using the formula:

Equation 5

$$T_{OLP-delay} = C_{FB} \times \frac{V_{FBolp} - V_{FBlin}}{I_{FB}}$$

where I_{FB} is the value, reported in *Table 8*, when the FB voltage is between V_{FBlin} and V_{FBolp}.

In *Figure 30*, the capacitor connected to the FB pin (C_{FB}) is part of the compensation circuit as well as being necessary to activate the overload protection.

After the startup time, t_{SS}, during which the feedback voltage is fixed at V_{FBlin}, the output capacitor may not be at its nominal value and the controller interprets this situation as an overload condition. In this case, the OLP delay helps to avoid an incorrect device shutdown during the startup phase.

Owing to the above considerations, the OLP delay time must be long enough to bypass the initial output voltage transient and check the overload condition only when the output voltage is in steady-state. The output transient time depends on the value of the output capacitor and on the load.

When the value of the C_{FB} capacitor calculated for the loop stability is too low and cannot ensure enough OLP delay, an alternative compensation network can be used, shown in *Figure 31*.

Using this alternative compensation network, two poles (f_{PFB}, f_{PFB1}) and one zero (f_{ZFB}) are introduced by the capacitors C_{FB} and C_{FB1} and the resistor R_{FB1}.

The capacitor C_{FB} introduces a pole (f_{PFB}) at a higher frequency than f_{ZB} and f_{PFB1}. This pole is usually used to compensate the high frequency zero due to the ESR (equivalent series resistor) of the output capacitance of the flyback converter.

The mathematical expressions of these poles and zero frequency, considering the scheme in *Figure 31*, are reported by the equations below:

Equation 6

$$f_{ZFB} = \frac{1}{2 \cdot \pi \cdot C_{FB1} \cdot R_{FB1}}$$

Equation 7

$$f_{PFB} = \frac{R_{FB(DYN)} + R_{FB1}}{2 \cdot \pi \cdot C_{FB} \cdot \left(R_{FB(DYN)} \cdot R_{FB1}\right)}$$

Equation 8

$$f_{PFB1} = \frac{1}{2 \cdot \pi \cdot C_{FB1} \cdot \left(R_{FB1} + R_{FB(DYN)}\right)}$$

$R_{FB(DYN)}$ is the dynamic resistance seen by the FB pin.

The C_{FB1} capacitor fixes the OLP delay and usually C_{FB1} results much higher than C_{FB}. *Equation 5* can still be used to calculate the OLP delay time but C_{FB1} must be considered instead of C_{FB}. Using the alternative compensation network, the user can satisfy, in all cases, the loop stability and the correct OLP delay time alike.

Figure 30. FB pin configuration 1

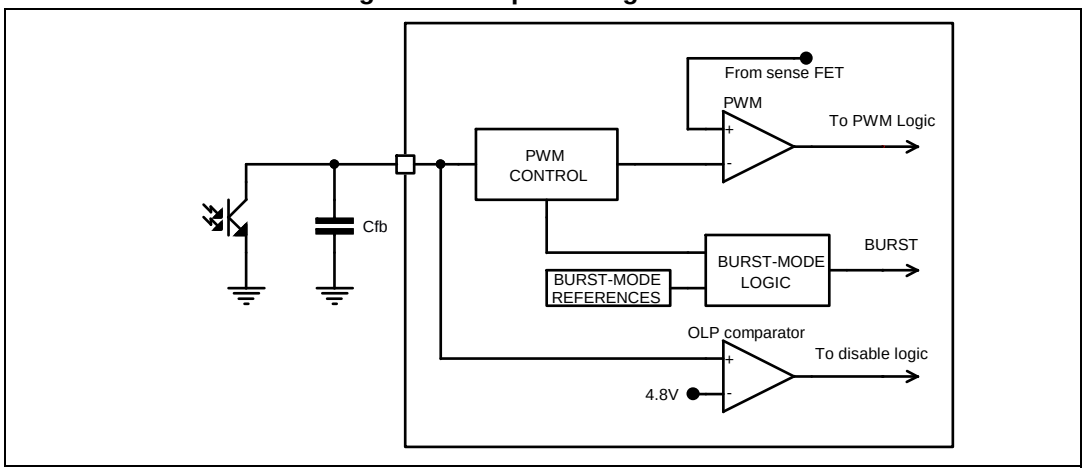
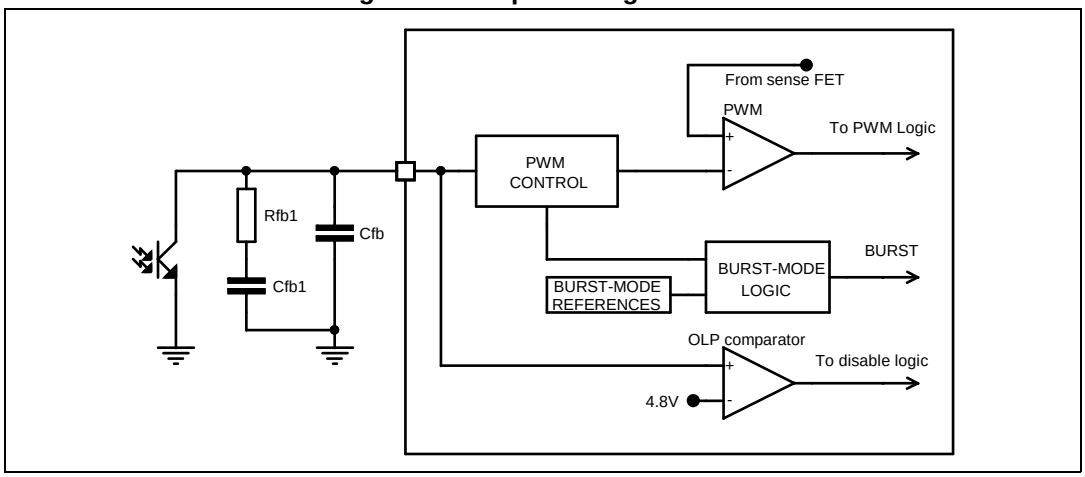


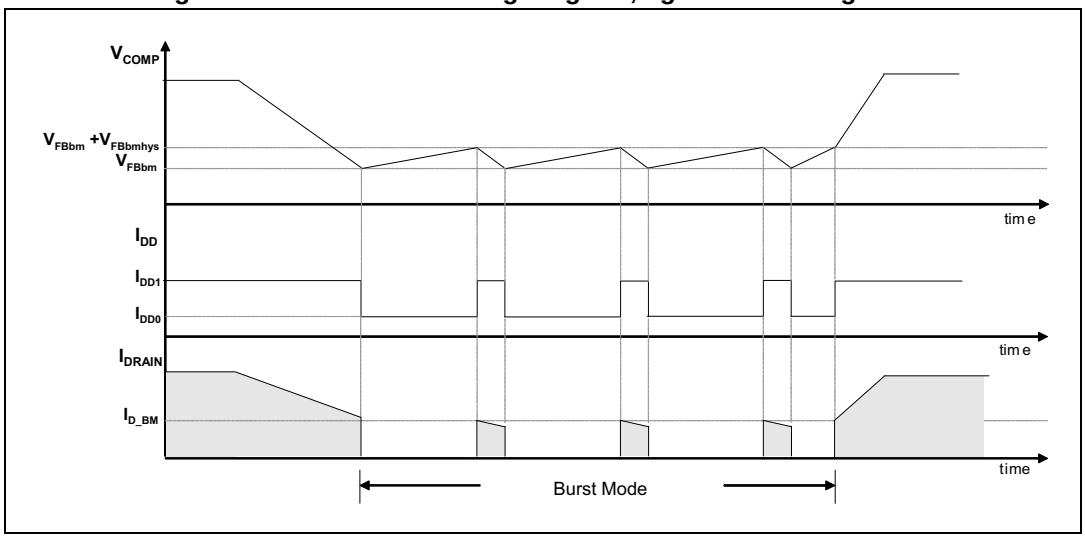
Figure 31. FB pin configuration 2



8.11 Burst mode operation at no load or very light load

When the load decreases, the feedback loop reacts by lowering the feedback pin voltage. If it falls below the burst mode threshold, V_{FBbm}, the Power MOSFET is no longer allowed to be switched on. After the MOSFET stops, as a result of the feedback reaction to the energy delivery stop, the feedback pin voltage increases and when it exceeds the level, V_{FBbm} + $V_{FBbmhys}$, the power MOSFET starts switching again. The burst mode thresholds are reported in *Table 8* and *Figure 32* shows this behavior. Depending on the output load, the power alternates between periods of time in which the Power MOSFET is switching and is enabled, with periods of time when the Power MOSFET is not switching; this working mode is called burst mode. The power delivered to the output during switching periods exceeds the load power demands; the excess of power is balanced from the non-switching period where no power is processed. The advantage of burst mode operation is an average switching frequency much lower then the normal operation working frequency, up to a few hundred hertz, minimizing all frequency related losses. During burst mode the drain current peak is clamped to the level, I_{D_BM}, reported in *Table 8*.

Figure 32. Burst mode timing diagram, light load management



8.12 Brownout protection

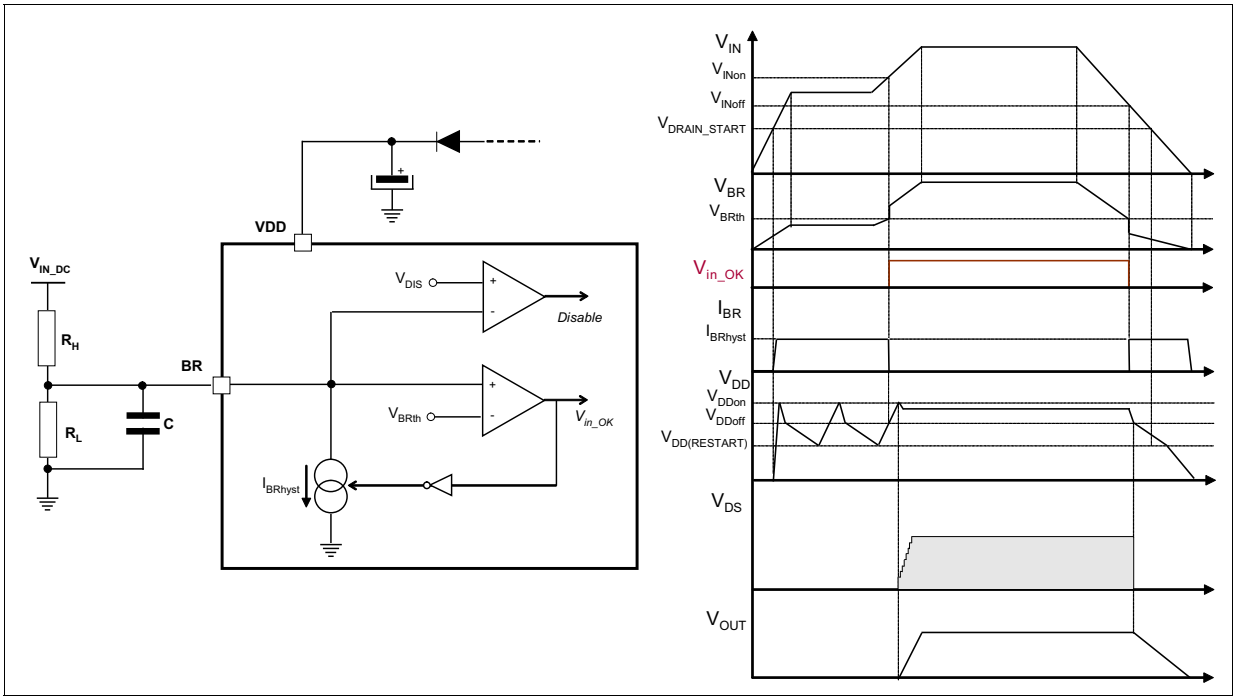
Brownout protection is a not-latched shutdown function activated when a condition of mains undervoltage is detected.

The brownout comparator is internally referenced to V_{BRth}, *Table 8*, and disables the PWM if the voltage applied at the BR pin is below this internal reference. Under this condition the Power MOSFET is turned off. Until the brownout condition is present, the VDD voltage continuously oscillates between the V_{DDon} and the UVLO thresholds, as shown in the timing diagram of *Figure 33*. A voltage hysteresis is present to improve the noise immunity.

The switching operation is restarted as the voltage on the pin is above the reference plus the previously mentioned voltage hysteresis, see *Figure 5*.

The brownout comparator is provided also with a current hysteresis, I_{BRhyst}. The user must set the rectified input voltage above which the Power MOSFET starts switching after brownout event, V_{INon}, and the rectified input voltage below which the Power MOSFET is switched off, V_{INoff}. Thanks to the I_{BRhyst}, see *Table 8*, these two thresholds can be set separately.

Figure 33. Brownout protection: BR external setting and timing diagram



When the V_{INon} and the V_{INoff} levels are fixed, with reference to *Figure 33*, the following relationships can be established for the calculation of the resistors R_H and R_L:

Equation 9

$$R_L = -\frac{V_{BRhyst}}{I_{BRhyst}} + \frac{V_{INon} - V_{INoff} - V_{BRhyst}}{V_{INoff} - V_{BRth}} \times \frac{V_{BRth}}{I_{BRhyst}}$$

Equation 10

$$R_H = \frac{V_{INon} - V_{INoff} - V_{BRhyst}}{I_{BRhyst}} \times \frac{R_L}{R_L + \frac{V_{BRhyst}}{I_{BRhyst}}}$$

For a proper operation of this function, $V_{IN\ on}$ must be less than the peak voltage at minimum mains and $V_{IN\ off}$ less than the minimum voltage on the input bulk capacitor at minimum mains and maximum load.

The BR pin is a high impedance input connected to high value resistors, it is therefore prone to pick up noise, which might alter the OFF threshold when the converter operates or creates an undesired switch-off of the device during ESD tests.

It is possible to bypass the pin to ground with a small film capacitor (e.g. 1-10 nF) to prevent any malfunctioning of this kind.

If the brownout function is not used, the BR pin must be connected to GND, ensuring that the voltage is lower than the minimum V_{DIS} threshold (50 mV), see *Table 8*.

In order to enable the brownout function, the BR pin voltage must be higher than the maximum V_{DIS} threshold (150 mV), see *Table 8*.

8.13 2nd level overcurrent protection and hiccup mode

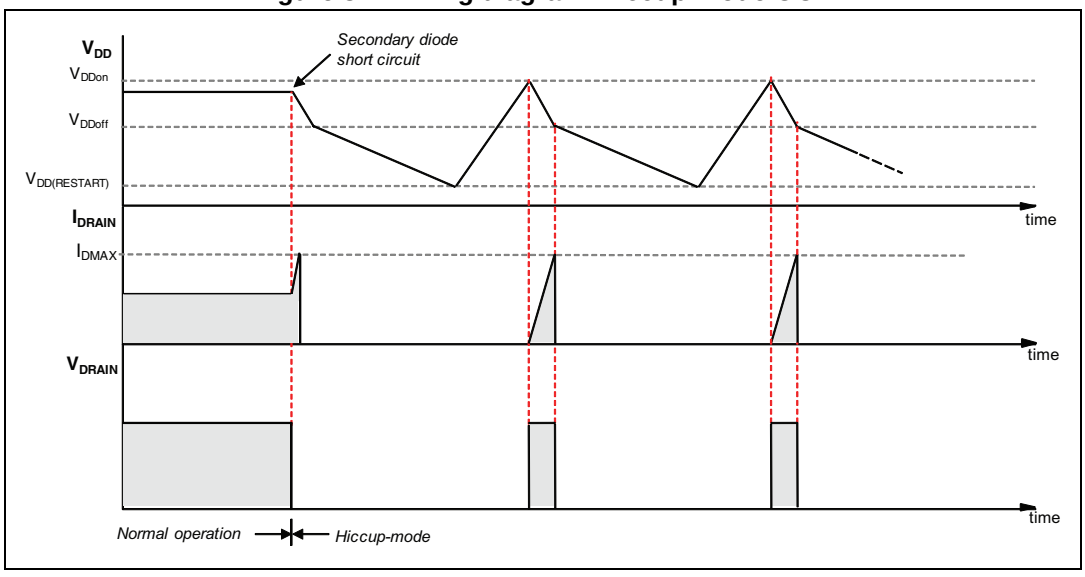
The device is protected against short-circuit of the secondary rectifier, short-circuit on the secondary winding, or a hard-saturation of the flyback transformer. Such an anomalous condition is invoked when the drain current exceeds the threshold I_{DMAX} (see *Table 8*).

To distinguish a real malfunction from a disturbance (e.g. induced during ESD tests) a “warning state” is entered after the first signal trip. If, in the subsequent switching cycle, the signal is not tripped, a temporary disturbance is assumed and the protection logic is reset in its idle state; otherwise, if the I_{DMAX} threshold is exceeded for two consecutive switching cycles, a real malfunction is assumed and the Power MOSFET is turned off.

The shutdown condition is latched as long as the device is supplied. While it is disabled, no energy is transferred from the auxiliary winding; hence the voltage on the V_{DD} capacitor decays to the V_{DD} undervoltage threshold (V_{DDoff}), which clears the latch.

The startup HV current generator is still off, until the V_{DD} voltage goes below its restart voltage, $V_{DD(RESTART)}$. After this condition the V_{DD} capacitor is charged again by a 600 µA current, and the converter switching restarts if the V_{DDon} occurs. If the fault condition is not removed the device enters auto-restart mode. This behavior results in a low-frequency intermittent operation (hiccup-mode operation), with very low stress on the power circuit. See the timing diagram of *Figure 34*.

Figure 34. Timing diagram: hiccup-mode OCP



9 Package information

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK specifications, grade definitions and product status are available at: www.st.com. ECOPACK is an ST trademark.

9.1 SDIP10 package information

Figure 35. SDIP10 package outline

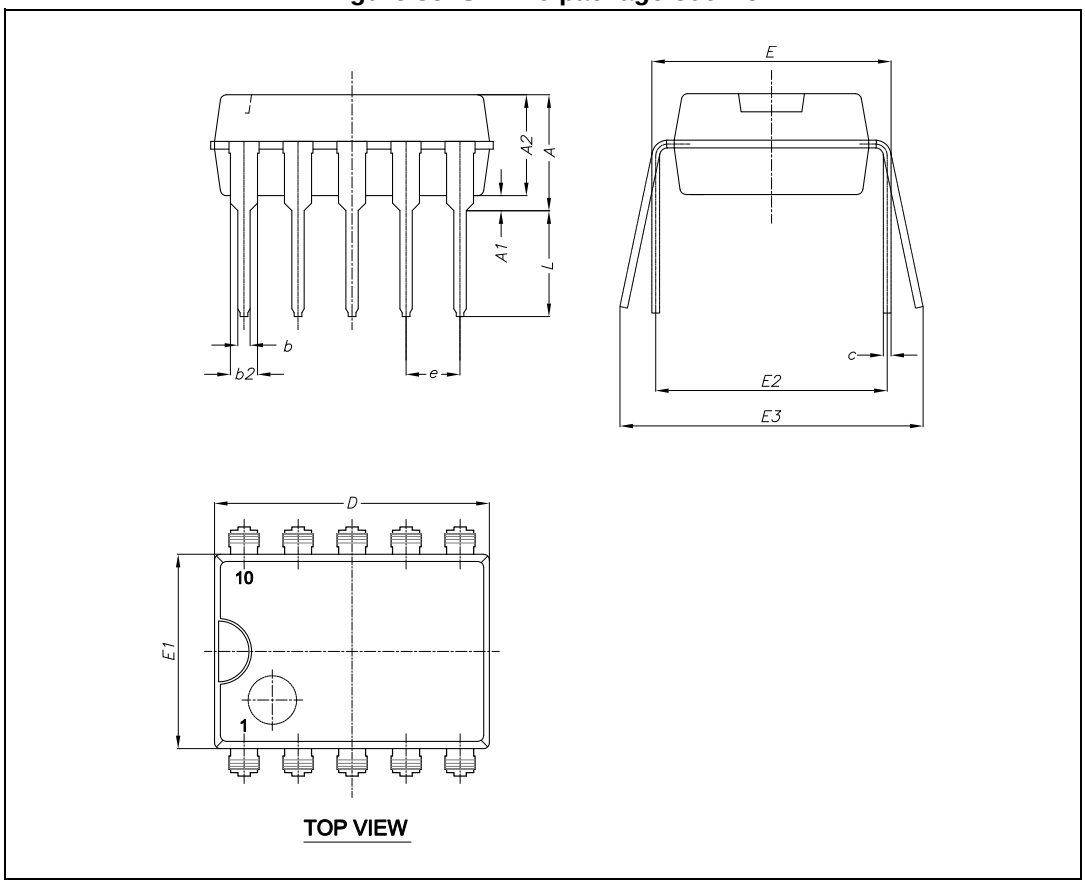


Table 12. SDIP10 mechanical data

Dim.	mm		
	Min.	Typ.	Max.
A			5.33
A1	0.38		
A2	2.92		4.95
b	0.36		0.56
b2	0.51		1.15
c	0.2		0.36
D	9.02		10.16
E	7.62		8.26
E1	6.1		7.11
E2		7.62	
E3			10.92
e		1.77	
L	2.92		3.81

9.2 SO16 narrow package information

Figure 36. SO16 narrow package outline

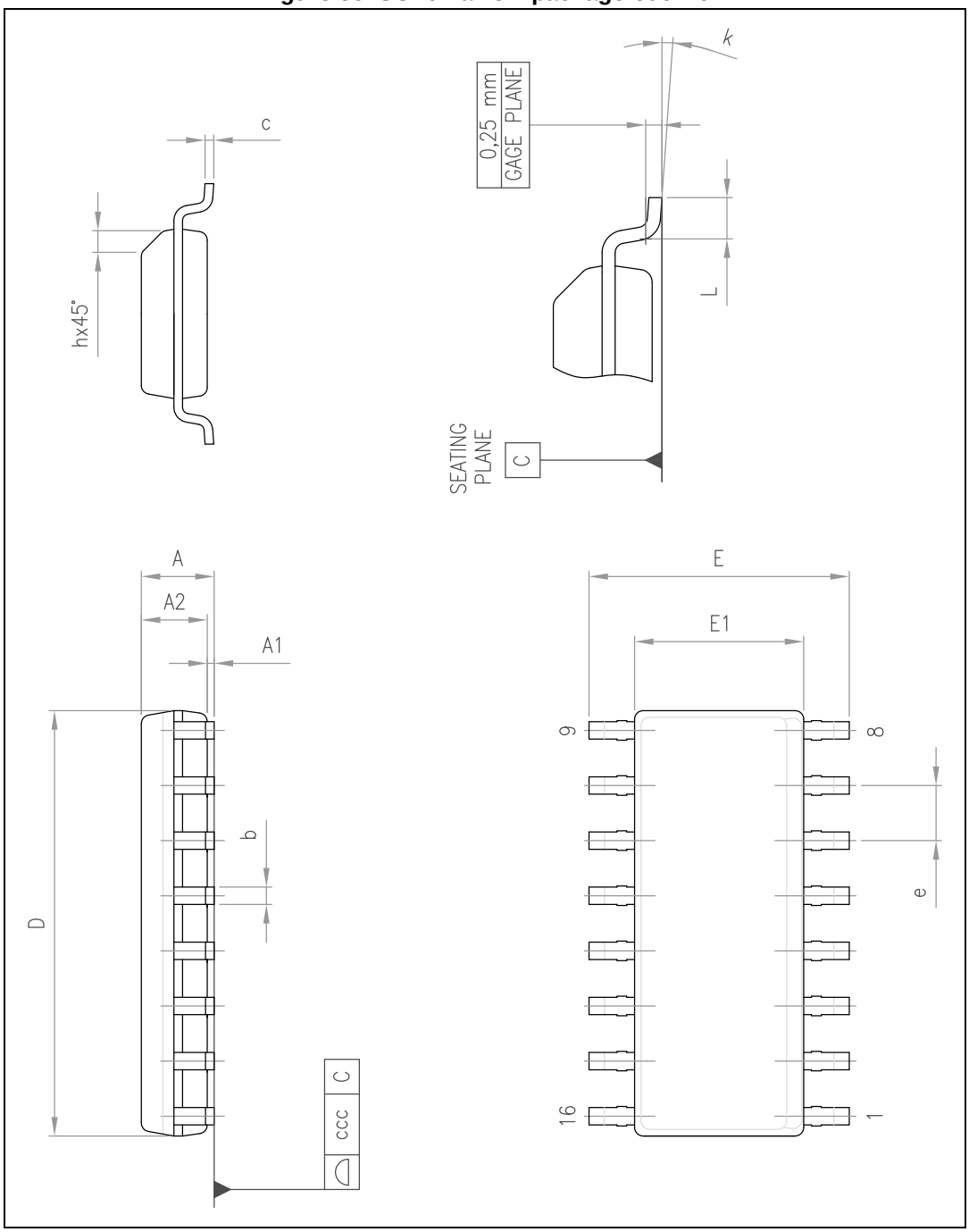


Table 13. SO16 narrow mechanical data

Dim.	mm		
	Min.	Typ.	Max.
A			1.75
A1	0.1		0.25
A2	1.25		
b	0.31		0.51
c	0.17		0.25
D	9.8	9.9	10
E	5.8	6	6.2
E1	3.8	3.9	4
e		1.27	
h	0.25		0.5
L	0.4		1.27
k	0		8
ccc			0.1

10 Revision history

Table 14. Document revision history

Date	Revision	Changes
17-Feb-2012	1	Initial release
20-May-2015	2	Added SO16 narrow package. Updated features in cover page. Updated *Table 1: Device summary*, *Table 2: Typical power*, *Table 3: Pin description*, *Section 4.3: Electrical characteristics*, *Figure 3: Connection diagram (top view)*. Modified the HFB parameter in *Table 8: Controller section*. Added *Section 9.2: SO16 narrow package information*. Minor text changes.
01-Jul-2015	3	Minor text changes.