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# FDP2532 / FDB2532

## N-Channel PowerTrench® MOSFET

150 V, 79 A, 16 mΩ

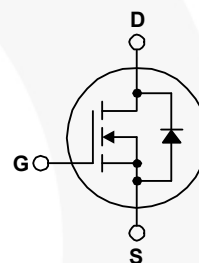
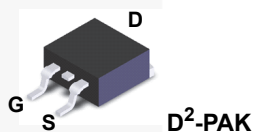
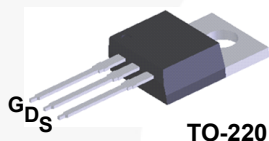
### Features

- $R_{DS(on)} = 14 \text{ m}\Omega$  (Typ.) @  $V_{GS} = 10 \text{ V}$ ,  $I_D = 33 \text{ A}$
- $Q_{G(tot)} = 82 \text{ nC}$  (Typ.) @  $V_{GS} = 10 \text{ V}$
- Low Miller Charge
- Low  $Q_{rr}$  Body Diode
- UIS Capability (Single Pulse and Repetitive Pulse)

### Applications

- Consumer Appliances
- Synchronous Rectification
- Battery Protection Circuit
- Motor drives and Uninterruptible Power Supplies
- Micro Solar Inverter

Formerly developmental type 82884



### MOSFET Maximum Ratings $T_C = 25^\circ\text{C}$ unless otherwise noted

Symbol	Parameter	FDP2532 / FDB2532	Unit
$V_{DSS}$	Drain to Source Voltage	150	V
$V_{GS}$	Gate to Source Voltage	$\pm 20$	V
$I_D$	Drain Current		
	Continuous ( $T_C = 25^\circ\text{C}$ , $V_{GS} = 10\text{V}$ )	79	A
	Continuous ( $T_C = 100^\circ\text{C}$ , $V_{GS} = 10\text{V}$ )	56	A
	Continuous ( $T_{amb} = 25^\circ\text{C}$ , $V_{GS} = 10\text{V}$ , $R_{\theta JA} = 43^\circ\text{C/W}$ )	8	A
	Pulsed	Figure 4	A
$E_{AS}$	Single Pulse Avalanche Energy (Note 1)	400	mJ
$P_D$	Power dissipation	310	W
	Derate above $25^\circ\text{C}$	2.07	W/ $^\circ\text{C}$
$T_J, T_{STG}$	Operating and Storage Temperature	-55 to 175	$^\circ\text{C}$

### Thermal Characteristics

$R_{\theta JC}$	Thermal Resistance Junction to Case, Max. TO-220, D²-PAK	0.61	$^\circ\text{C/W}$
$R_{\theta JA}$	Thermal Resistance Junction to Ambient, Max. TO-220, D²-PAK (Note 2)	62	$^\circ\text{C/W}$
$R_{\theta JA}$	Thermal Resistance Junction to Ambient D²-PAK, Max. 1in² copper pad area	43	$^\circ\text{C/W}$

## Package Marking and Ordering Information

Device Marking	Device	Package	Reel Size	Tape Width	Quantity
FDB2532	FDB2532	D <sup>2</sup> -PAK	330 mm	24 mm	800 units
FDP2532	FDP2532	TO-220	Tube	N/A	50 units

## Electrical Characteristics $T_C = 25^\circ\text{C}$ unless otherwise noted

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
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### Off Characteristics

$B_{VDSS}$	Drain to Source Breakdown Voltage	$I_D = 250\mu\text{A}, V_{GS} = 0\text{V}$	150	-	-	V
$I_{DSS}$	Zero Gate Voltage Drain Current	$V_{DS} = 120\text{V}$ $V_{GS} = 0\text{V}$ $T_C = 150^\circ\text{C}$	-	-	1	$\mu\text{A}$
$I_{GSS}$	Gate to Source Leakage Current	$V_{GS} = \pm 20\text{V}$	-	-	$\pm 100$	nA

### On Characteristics

$V_{GS(TH)}$	Gate to Source Threshold Voltage	$V_{GS} = V_{DS}, I_D = 250\mu\text{A}$	2	-	4	V
$r_{DS(ON)}$	Drain to Source On Resistance	$I_D = 33\text{A}, V_{GS} = 10\text{V}$	-	0.014	0.016	$\Omega$
		$I_D = 16\text{A}, V_{GS} = 6\text{V}$	-	0.016	0.024	
		$I_D = 33\text{A}, V_{GS} = 10\text{V}$ , $T_C = 175^\circ\text{C}$	-	0.040	0.048	

### Dynamic Characteristics

$C_{ISS}$	Input Capacitance	$V_{DS} = 25\text{V}, V_{GS} = 0\text{V}$ , $f = 1\text{MHz}$	-	5870	-	pF
$C_{OSS}$	Output Capacitance		-	615	-	pF
$C_{RSS}$	Reverse Transfer Capacitance		-	135	-	pF
$Q_{g(TOT)}$	Total Gate Charge at 10V	$V_{GS} = 0\text{V}$ to 10V	-	82	107	nC
$Q_{g(TH)}$	Threshold Gate Charge	$V_{GS} = 0\text{V}$ to 2V	-	11	14	nC
$Q_{gs}$	Gate to Source Gate Charge	$V_{DD} = 75\text{V}$ $I_D = 33\text{A}$ $I_g = 1.0\text{mA}$	-	23	-	nC
$Q_{gs2}$	Gate Charge Threshold to Plateau		-	13	-	nC
$Q_{gd}$	Gate to Drain "Miller" Charge		-	19	-	nC

### Resistive Switching Characteristics ( $V_{GS} = 10\text{V}$ )

$t_{ON}$	Turn-On Time	$V_{DD} = 75\text{V}, I_D = 33\text{A}$ $V_{GS} = 10\text{V}, R_{GS} = 3.6\Omega$	-	-	69	ns
$t_{d(ON)}$	Turn-On Delay Time		-	16	-	ns
$t_r$	Rise Time		-	30	-	ns
$t_{d(OFF)}$	Turn-Off Delay Time		-	39	-	ns
$t_f$	Fall Time		-	17	-	ns
$t_{OFF}$	Turn-Off Time		-	-	84	ns

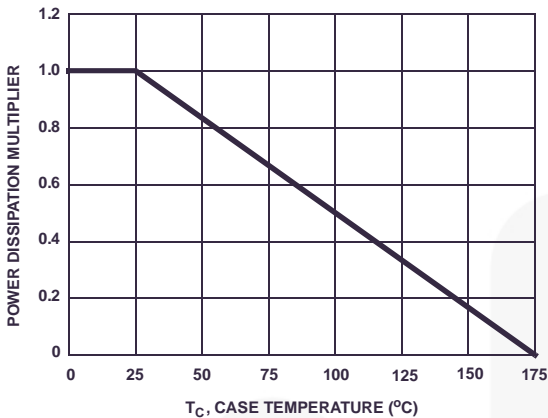
### Drain-Source Diode Characteristics

$V_{SD}$	Source to Drain Diode Voltage	$I_{SD} = 33\text{A}$	-	-	1.25	V
		$I_{SD} = 16\text{A}$	-	-	1.0	V
$t_{rr}$	Reverse Recovery Time	$I_{SD} = 33\text{A}, dI_{SD}/dt = 100\text{A}/\mu\text{s}$	-	-	105	ns
$Q_{RR}$	Reverse Recovery Charge	$I_{SD} = 33\text{A}, dI_{SD}/dt = 100\text{A}/\mu\text{s}$	-	-	327	nC

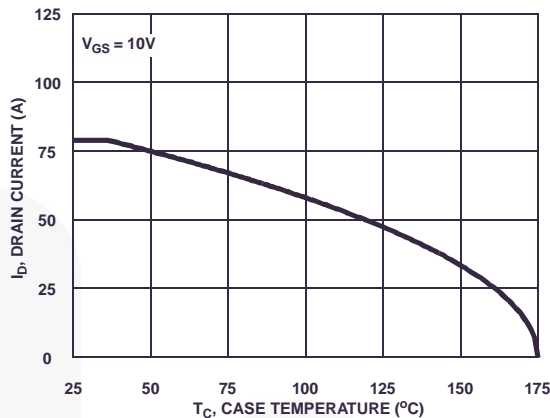
#### Notes:

- Starting  $T_J = 25^\circ\text{C}$ ,  $L = 0.5\text{mH}$ ,  $I_{AS} = 40\text{A}$ .
- Pulse Width = 100s

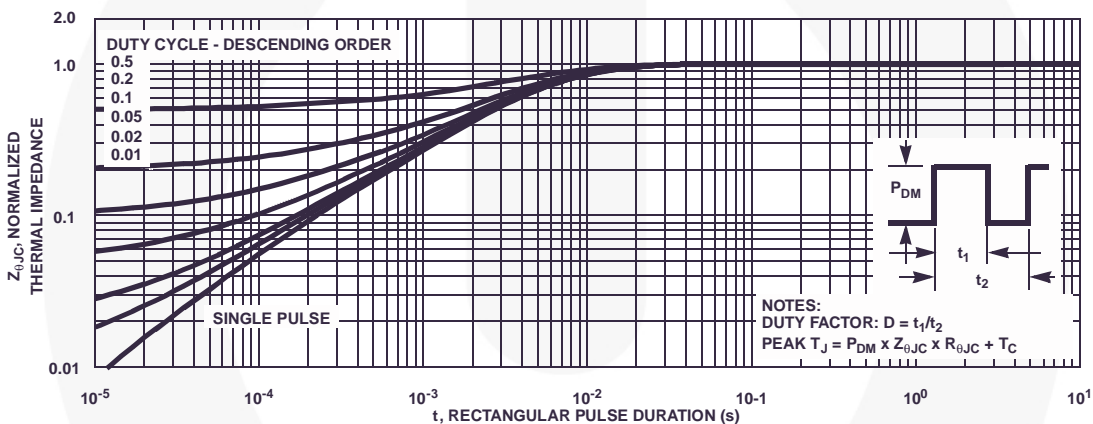
**Typical Characteristics**  $T_C = 25^\circ\text{C}$  unless otherwise noted



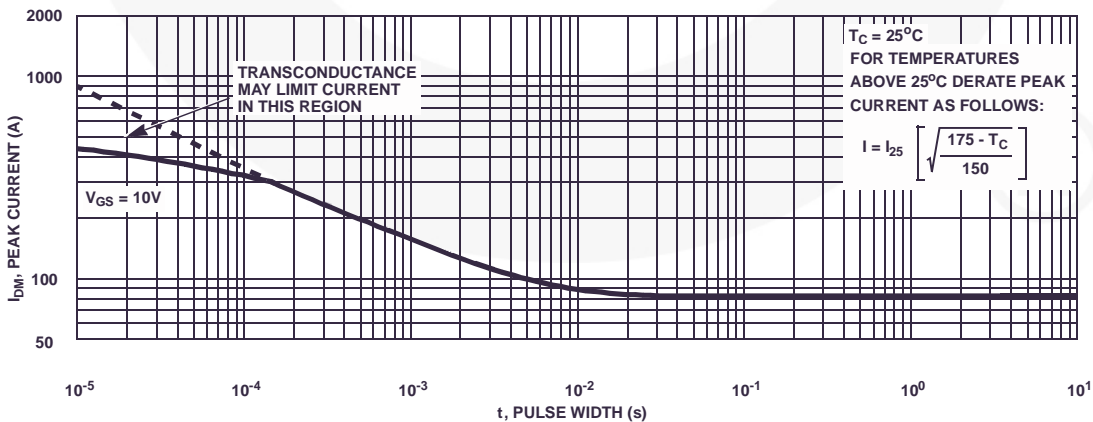
**Figure 1. Normalized Power Dissipation vs Ambient Temperature**



**Figure 2. Maximum Continuous Drain Current vs Case Temperature**

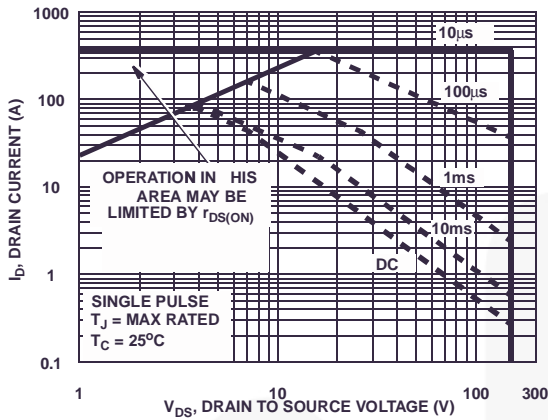


**Figure 3. Normalized Maximum Transient Thermal Impedance**

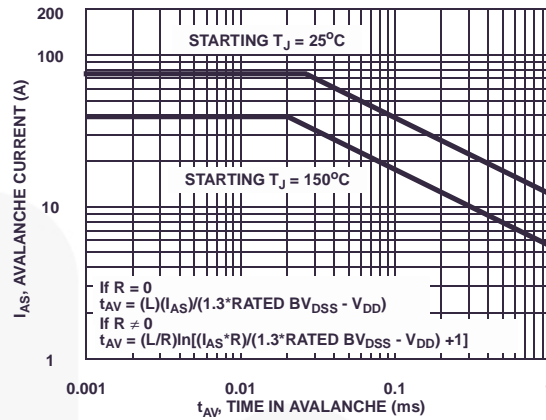


**Figure 4. Peak Current Capability**

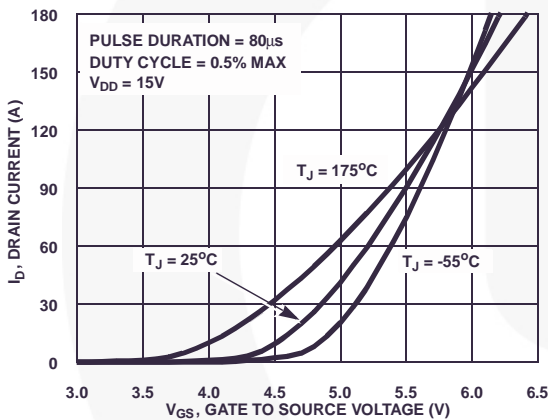
**Typical Characteristics**  $T_C = 25^\circ\text{C}$  unless otherwise noted



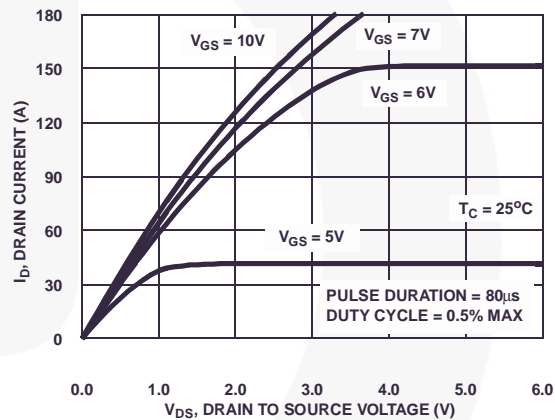
**Figure 5. Forward Bias Safe Operating Area**



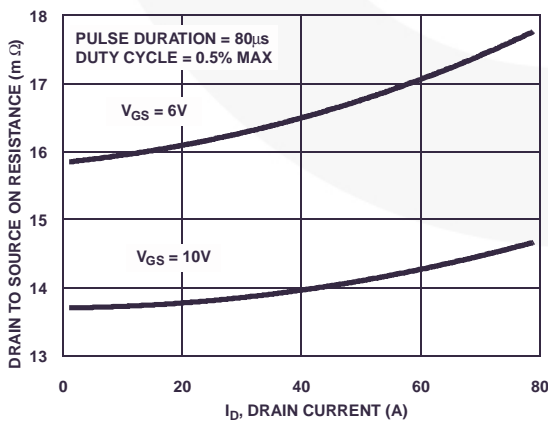
NOTE: Refer to Fairchild Application Notes AN7515 and AN7517  
**Figure 6. Unclamped Inductive Switching Capability**



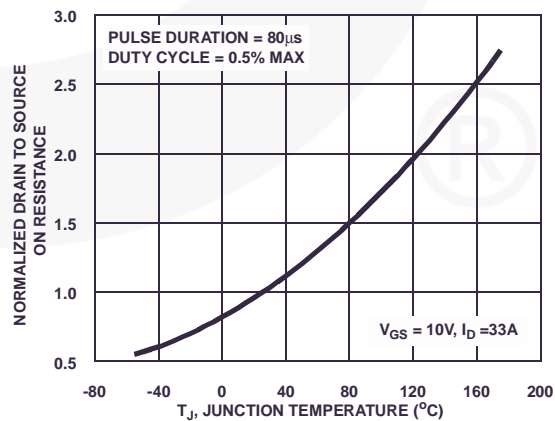
**Figure 7. Transfer Characteristics**



**Figure 8. Saturation Characteristics**

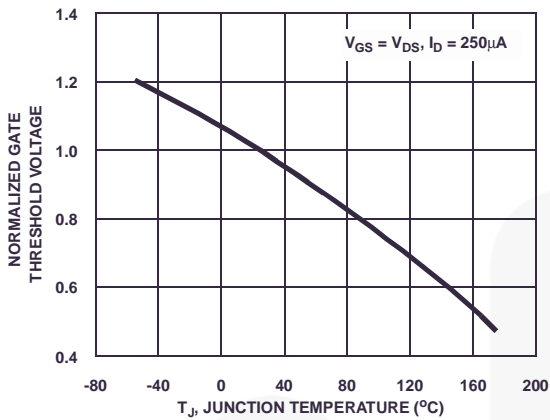


**Figure 9. Drain to Source On Resistance vs Drain Current**

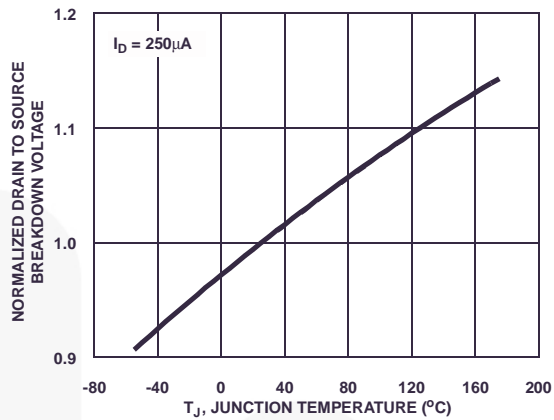


**Figure 10. Normalized Drain to Source On Resistance vs Junction Temperature**

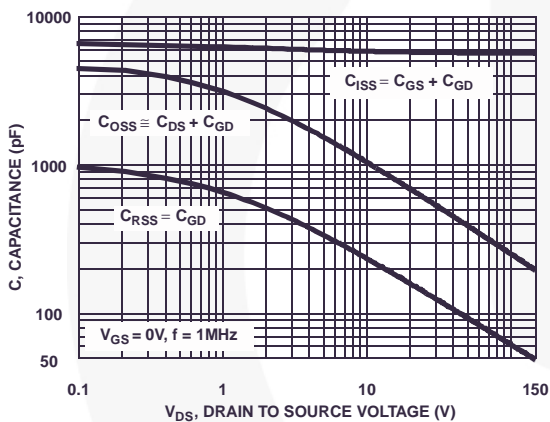
**Typical Characteristics**  $T_C = 25^\circ\text{C}$  unless otherwise noted



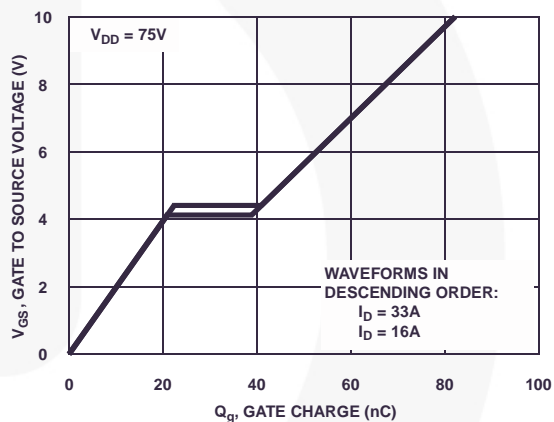
**Figure 11. Normalized Gate Threshold Voltage vs Junction Temperature**



**Figure 12. Normalized Drain to Source Breakdown Voltage vs Junction Temperature**



**Figure 13. Capacitance vs Drain to Source Voltage**



**Figure 14. Gate Charge Waveforms for Constant Gate Currents**

### Test Circuits and Waveforms

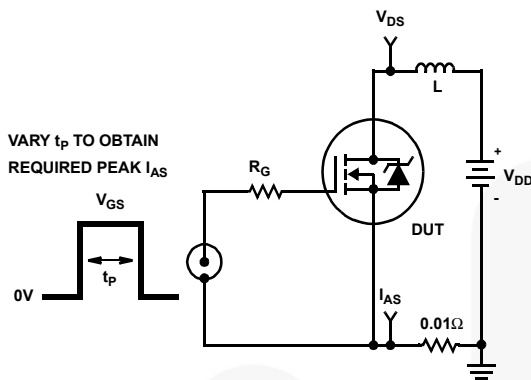


Figure 15. Unclamped Energy Test Circuit

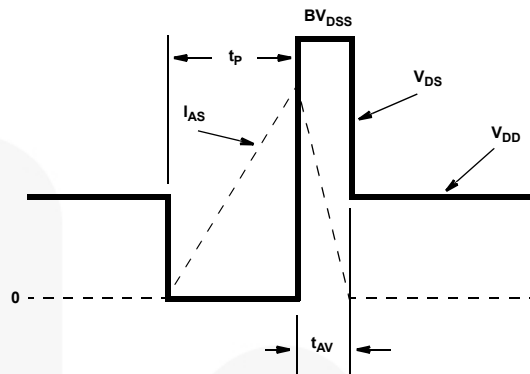


Figure 16. Unclamped Energy Waveforms

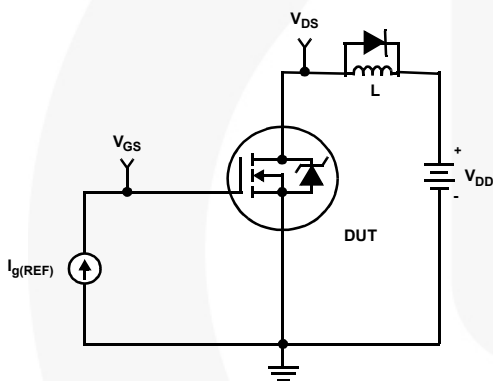


Figure 17. Gate Charge Test Circuit

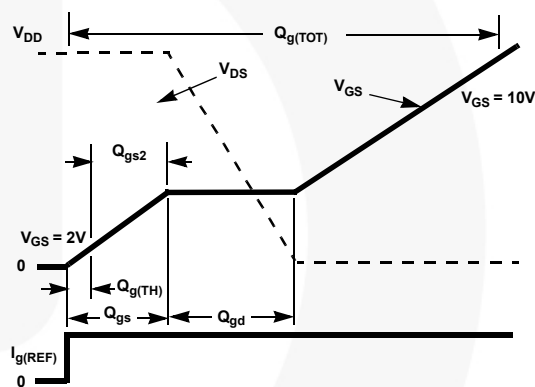


Figure 18. Gate Charge Waveforms

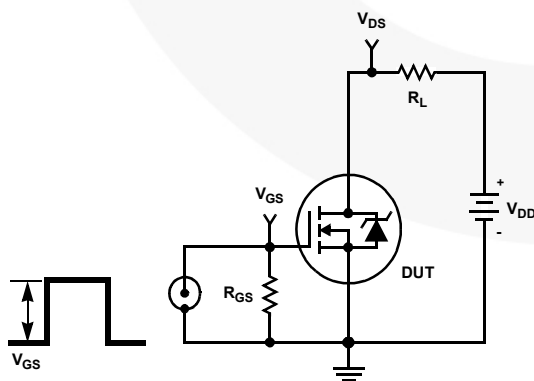


Figure 19. Switching Time Test Circuit

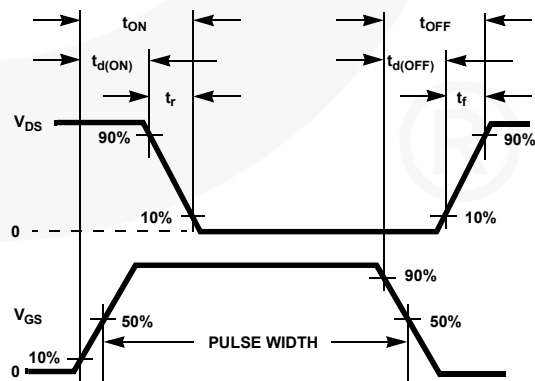


Figure 20. Switching Time Waveforms

### Thermal Resistance vs. Mounting Pad Area

The maximum rated junction temperature,  $T_{JM}$ , and the thermal resistance of the heat dissipating path determines the maximum allowable device power dissipation,  $P_{DM}$ , in an application. Therefore the application's ambient temperature,  $T_A$  ( $^{\circ}C$ ), and thermal resistance  $R_{\theta JA}$  ( $^{\circ}C/W$ ) must be reviewed to ensure that  $T_{JM}$  is never exceeded. Equation 1 mathematically represents the relationship and serves as the basis for establishing the rating of the part.

$$P_{DM} = \frac{(T_{JM} - T_A)}{R_{\theta JA}} \quad (\text{EQ. 1})$$

In using surface mount devices such as the TO-263 package, the environment in which it is applied will have a significant influence on the part's current and maximum power dissipation ratings. Precise determination of  $P_{DM}$  is complex and influenced by many factors:

1. Mounting pad area onto which the device is attached and whether there is copper on one side or both sides of the board.
2. The number of copper layers and the thickness of the board.
3. The use of external heat sinks.
4. The use of thermal vias.
5. Air flow and board orientation.
6. For non steady state applications, the pulse width, the duty cycle and the transient thermal response of the part, the board and the environment they are in.

Fairchild provides thermal information to assist the designer's preliminary application evaluation. Figure 21 defines the  $R_{\theta JA}$  for the device as a function of the top copper (component side) area. This is for a horizontally positioned FR-4 board with 1oz copper after 1000 seconds of steady state power with no air flow. This graph provides the necessary information for calculation of the steady state junction temperature or power dissipation. Pulse applications can be evaluated using the Fairchild device Spice thermal model or manually utilizing the normalized maximum transient thermal impedance curve.

Thermal resistances corresponding to other copper areas can be obtained from Figure 21 or by calculation using Equation 2 or 3. Equation 2 is used for copper area defined in inches square and equation 3 is for area in centimeters square. The area, in square inches or square centimeters is the top copper area including the gate and source pads.

$$R_{\theta JA} = 26.51 + \frac{19.84}{(0.262 + Area)} \quad (\text{EQ. 2})$$

Area in Inches Squared

$$R_{\theta JA} = 26.51 + \frac{128}{(1.69 + Area)} \quad (\text{EQ. 3})$$

Area in Centimeters Squared

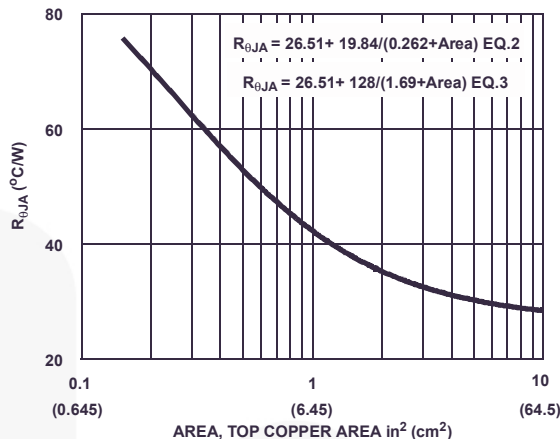


Figure 21. Thermal Resistance vs Mounting Pad Area



### PSPICE Electrical Model

.SUBCKT FDB2532 2 1 3; rev April 2002  
 CA 12 8 1.4e-9  
 CB 15 14 1.6e-9  
 CIN 6 8 5.61e-9

Dbody 7 5 DbodyMOD  
 Dbreak 5 11 DbreakMOD  
 Dplcap 10 5 DplcapMOD

Ebreak 11 7 17 18 159  
 Eds 14 8 5 8 1  
 Egs 13 8 6 8 1  
 Esg 6 10 6 8 1  
 Evthres 6 21 19 8 1  
 Evtemp 20 6 18 22 1

It 8 17 1

Lgate 1 9 9.56e-9  
 Ldrain 2 5 1.0e-9  
 Lsource 3 7 7.71e-9

RLgate 1 9 95.6  
 RLdrain 2 5 10  
 RLsource 3 7 77.1

Mmed 16 6 8 8 MmedMOD  
 Mstro 16 6 8 8 MstroMOD  
 Mweak 16 21 8 8 MweakMOD

Rbreak 17 18 RbreakMOD 1  
 Rdrain 50 16 RdrainMOD 9.6e-3  
 Rgate 9 20 1.01  
 RSLC1 5 51 RSLCMOD 1.0e-6  
 RSLC2 5 50 1.0e3  
 Rsource 8 7 RsourceMOD 3.0e-3  
 Rvthres 22 8 RvthresMOD 1  
 Rvtemp 18 19 RvtempMOD 1  
 S1a 6 12 13 8 S1AMOD  
 S1b 13 12 13 8 S1BMOD  
 S2a 6 15 14 13 S2AMOD  
 S2b 13 15 14 13 S2BMOD

Vbat 22 19 DC 1

ESLC 51 50 VALUE={ (V(5,51)/ABS(V(5,51))) \* (PWR(V(5,51)/(1e-6\*190),3)) }

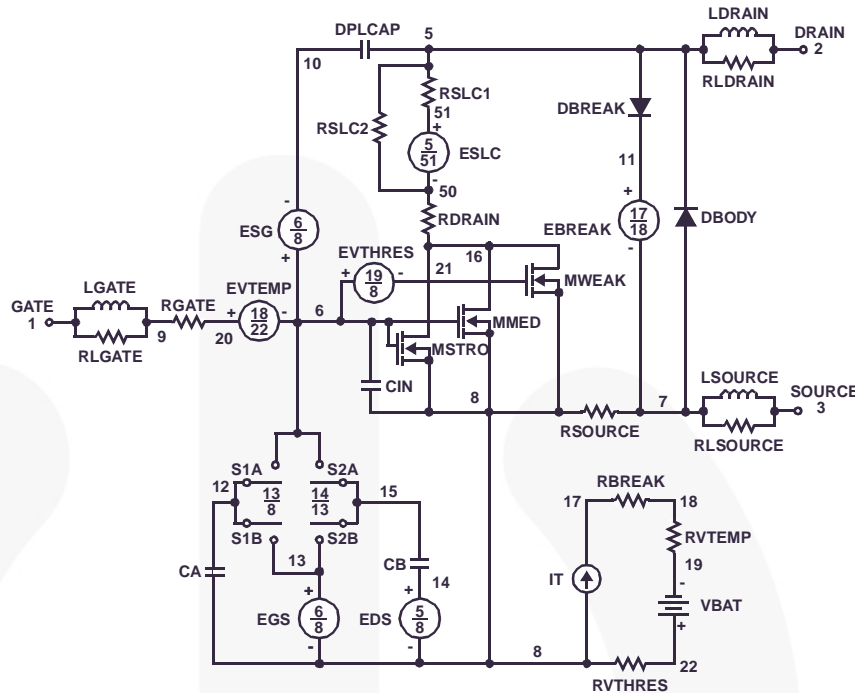
.MODEL DbodyMOD D (IS=6.0E-11 N=1.09 RS=2.3e-3 TRS1=3.0e-3 TRS2=1.0e-6  
 + CJO=3.9e-9 M=0.65 TT=4.8e-8 XTI=4.2)  
 .MODEL DbreakMOD D (RS=0.17 TRS1=3.0e-3 TRS2=-8.9e-6)  
 .MODEL DplcapMOD D (CJO=1.0e-9 IS=1.0e-30 N=10 M=0.6)  
 .MODEL MmedMOD NMOS (VTO=3.55 KP=10 IS=1e-30 N=10 TOX=1 L=1u W=1u RG=1.01)  
 .MODEL MstroMOD NMOS (VTO=4.2 KP=145 IS=1e-30 N=10 TOX=1 L=1u W=1u)  
 .MODEL MweakMOD NMOS (VTO=2.9 KP=0.05 IS=1e-30 N=10 TOX=1 L=1u W=1u RG=10.1 RS=0.1)

.MODEL RbreakMOD RES (TC1=1.1e-3 TC2=-9.0e-7)  
 .MODEL RdrainMOD RES (TC1=9.0e-3 TC2=3.5e-5)  
 .MODEL RSLCMOD RES (TC1=3.4e-3 TC2=1.5e-6)  
 .MODEL RsourceMOD RES (TC1=4.0e-3 TC2=1.0e-6)  
 .MODEL RvthresMOD RES (TC1=-4.1e-3 TC2=-1.4e-5)  
 .MODEL RvtempMOD RES (TC1=-4.0e-3 TC2=3.5e-6)

.MODEL S1AMOD VSWITCH (RON=1e-5 ROFF=0.1 VON=-6.0 VOFF=-4.0)  
 .MODEL S1BMOD VSWITCH (RON=1e-5 ROFF=0.1 VON=-4.0 VOFF=-6.0)  
 .MODEL S2AMOD VSWITCH (RON=1e-5 ROFF=0.1 VON=-1.4 VOFF=1.0)  
 .MODEL S2BMOD VSWITCH (RON=1e-5 ROFF=0.1 VON=1.0 VOFF=-1.4)

.ENDS

Note: For further discussion of the PSPICE model, consult **A New PSPICE Sub-Circuit for the Power MOSFET Featuring Global Temperature Options**; IEEE Power Electronics Specialist Conference Records, 1991, written by William J. Hepp and C. Frank Wheatley.





### SPICE Thermal Model

REV 26 February 2002

FDB2532

```
CTHERM1 TH 6 7.5e-3
CTHERM2 6 5 8.0e-3
CTHERM3 5 4 9.0e-3
CTHERM4 4 3 2.4e-2
CTHERM5 3 2 3.4e-2
CTHERM6 2 TL 6.5e-2
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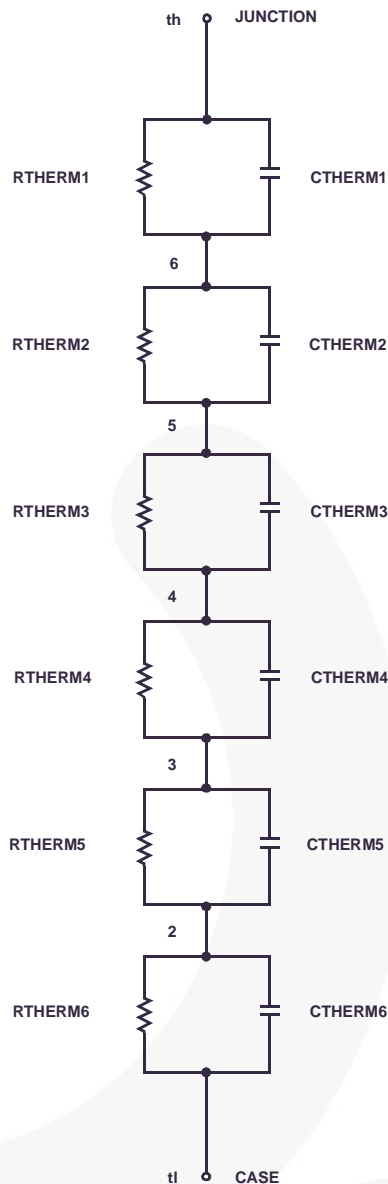
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RTHERM2 6 5 2.5e-3
RTHERM3 5 4 2.0e-2
RTHERM4 4 3 8.0e-2
RTHERM5 3 2 1.2e-1
RTHERM6 2 TL 1.3e-1
```

### SABER Thermal Model

SABER thermal model FDB2532  
 template thermal\_model th tl  
 thermal\_c th, tl

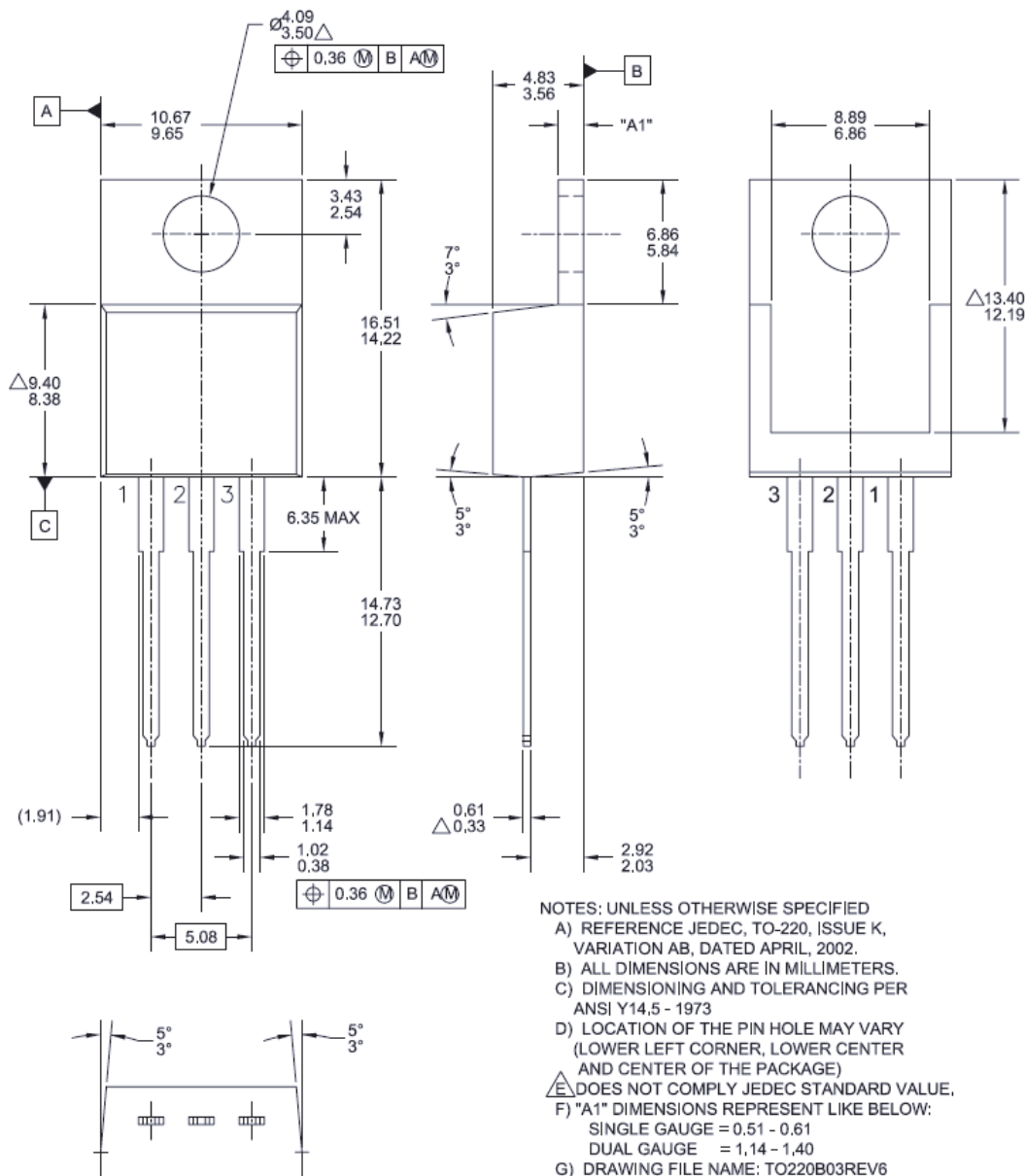
```
{
  ctherm.ctherm1 th 6 =7.5e-3
  ctherm.ctherm2 6 5 =8.0e-3
  ctherm.ctherm3 5 4 =9.0e-3
  ctherm.ctherm4 4 3 =2.4e-2
  ctherm.ctherm5 3 2 =3.4e-2
  ctherm.ctherm6 2 tl =6.5e-2
```

```
rrtherm.rtherm1 th 6 =3.1e-4
rtherm.rtherm2 6 5 =2.5e-3
rtherm.rtherm3 5 4 =2.0e-2
rtherm.rtherm4 4 3 =8.0e-2
rtherm.rtherm5 3 2 =1.2e-1
rtherm.rtherm6 2 tl =1.3e-1
}
```



## Mechanical Dimensions

### TO-220 3L



**Figure 22. TO-220, Molded, 3Lead, Jeduc Variation AB**

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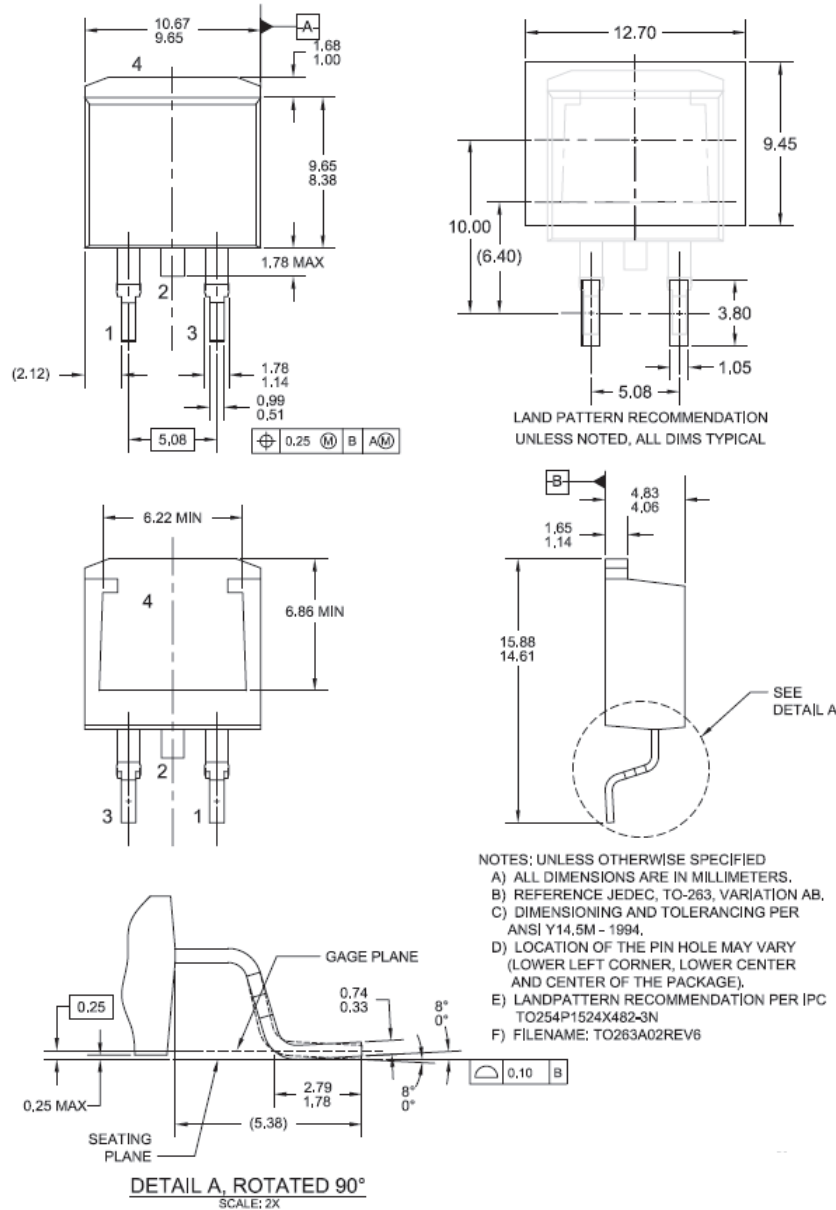
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[http://www.fairchildsemi.com/package/packageDetails.html?id=PN\\_TT220-003](http://www.fairchildsemi.com/package/packageDetails.html?id=PN_TT220-003)

Dimension in Millimeters

**Mechanical Dimensions**

**TO-263 2L (D<sup>2</sup>PAK)**



**Figure 23. 2LD, TO263, Surface Mount**

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Dimension in Millimeters



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