Unit: mm

#### TOSHIBA Diode Silicon Epitaxial Planar Type

# **1SS193**

#### Ultra High Speed Switching Application

• AEC-Q101 Qualified (Note1)

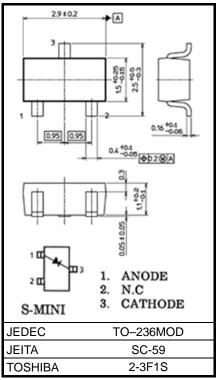
• Small package : SC-59

• Low forward voltage :  $V_F(3) = 0.9V$  (typ.) • Fast reverse recovery time:  $t_{rr} = 1.6ns$  (typ.) • Small total capacitance :  $C_T = 0.9pF$  (typ.)

Note1: For detail information, please contact to our sales.

### Absolute Maximum Ratings (Ta = 25°C)

Characteristic	Symbol	Rating	Unit	
Maximum (peak) reverse voltage	V <sub>RM</sub>	85	V	
Reverse voltage	VR	80	V	
Maximum (peak) forward current	I <sub>FM</sub>	300	mA	
Average forward current	Io	100	mA	
Surge current (10ms)	IFSM	2	Α	
Power dissipation	Р	150	mW	
Junction temperature	Tj	150	°C	
Storage temperature range	T <sub>stg</sub>	-55 to 150	°C	



Weight: 12 mg (typ.)

Note: Using continuously under heavy loads (e.g. the application of high temperature/current/voltage and the significant change in temperature, etc.) may cause this product to decrease in the reliability significantly even if the operating conditions (i.e. operating temperature/current/voltage, etc.) are within the absolute maximum ratings.

Please design the appropriate reliability upon reviewing the Toshiba Semiconductor Reliability Handbook ("Handling Precautions"/"Derating Concept and Methods") and individual reliability data (i.e. reliability test report and estimated failure rate, etc).

#### **Electrical Characteristics (Ta = 25°C)**

Characteristic	Symbol	Test Condition	Min	Тур.	Max	Unit
Forward voltage	VF (1)	I <sub>F</sub> =1mA	_	0.60	_	V
	VF (2)	I <sub>F</sub> = 10mA	_	0.72	_	
	VF (3)	I <sub>F</sub> = 100mA	_	0.90	1.20	
Reverse current	I <sub>R (1)</sub>	V <sub>R</sub> = 30V	_	_	0.1	μА
	I <sub>R (2)</sub>	V <sub>R</sub> = 80V	_	_	0.5	
Total capacitance	Ст	$V_R = 0 V, f = 1MH_Z$	_	0.9	3.0	pF
Reverse recovery time	t <sub>rr</sub>	I <sub>F</sub> = 10mA (Fig.1)	_	1.6	4.0	ns

Start of commercial production 1982-05

## Marking

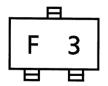
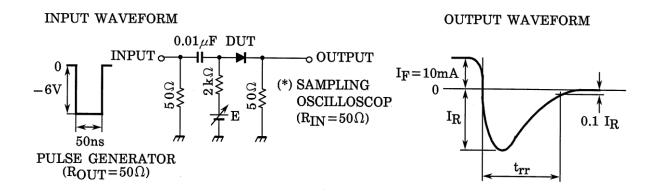
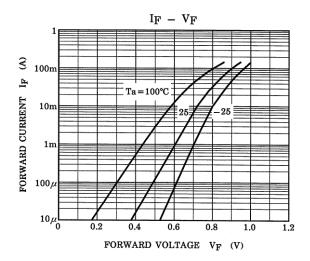
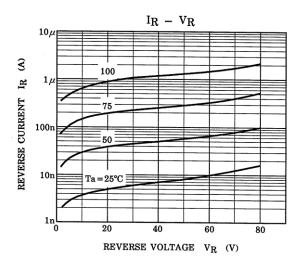


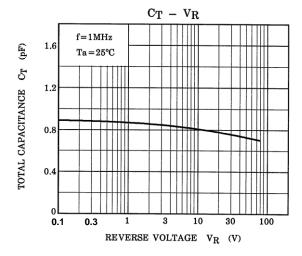
Fig.1 Reverse recovery time (trr) test circuit

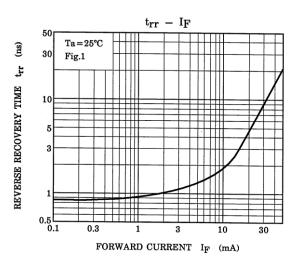


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