

+3.3V Programmable LVDS Transmitter 18-Bit Flat Panel Display Link-87.5 MHz

Check for Samples: [DS90C365A](#)

FEATURES

- Pin-to-pin compatible to DS90C363, DS90C363A and DS90C365
- No special start-up sequence required between clock/data and /PD pins. Input signals (clock and data) can be applied either before or after the device is powered.
- Support Spread Spectrum Clocking up to 100kHz frequency modulation & deviations of $\pm 2.5\%$ center spread or -5% down spread.
- “Input Clock Detection” feature will pull all LVDS pairs to logic low when input clock is missing and when /PD pin is logic high.
- 18 to 87.5 MHz shift clock support
- Tx power consumption < 146 mW (typ) at 87.5 MHz Grayscale
- Tx Power-down mode < 37 uW (typ)
- Supports VGA, SVGA, XGA, SXGA (dual pixel), SXGA+ (dual pixel), UXGA (dual pixel).
- Narrow bus reduces cable size and cost
- Up to 1.785 Gbps throughput
- Up to 223.125 Megabytes/sec bandwidth
- 345 mV (typ) swing LVDS devices for low EMI
- PLL requires no external components
- Compliant to TIA/EIA-644 LVDS standard
- Low profile 48-lead TSSOP package

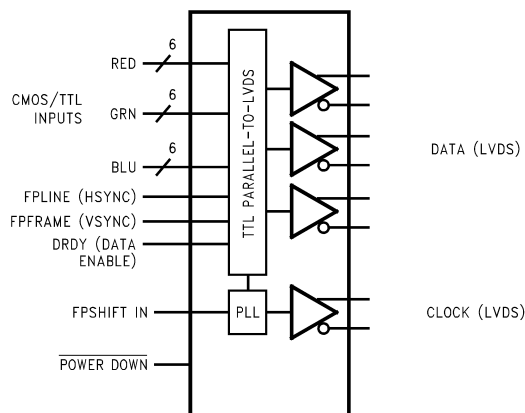
DESCRIPTION

The DS90C365A is a pin to pin compatible replacement for DS90C363, DS90C363A and DS90C365. The DS90C365A has additional features and improvements making it an ideal replacement for DS90C363, DS90C363A and DS90C365. family of LVDS Transmitters.

The DS90C365A transmitter converts 21 bits of LVCMOS/LVTTL data into four LVDS (Low Voltage Differential Signaling) data streams. A phase-locked transmit clock is transmitted in parallel with the data streams over the fourth LVDS link. Every cycle of the transmit clock 21 bits RGB of input data are sampled and transmitted. At a transmit clock frequency of 87.5 MHz, 21 bits of RGB data and 3 bits of LCD timing and control data (FPLINE, FPFRAME, DRDY) are transmitted at a rate of 612.5 Mbps per LVDS data channel. Using a 87.5 MHz clock, the data throughput is 229.687 Mbytes/sec. This transmitter can be programmed for Rising edge strobe or Falling edge strobe through a dedicated pin. A Rising edge or Falling edge strobe transmitter will interoperate with a Falling edge strobe FPDLink Receiver without any translation logic.

This chipset is an ideal means to solve EMI and cable size problems associated with wide, high-speed TTL interfaces with added Spread Spectrum Clocking support..

Block Diagram



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These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

Absolute Maximum Ratings⁽¹⁾

Supply Voltage (V_{CC})		-0.3V to +4V
CMOS/TTL Input Voltage		-0.5V to ($V_{CC} + 0.3$)V
LVDS Driver Output Voltage		-0.3V to ($V_{CC} + 0.3$)V
LVDS Output Short Circuit Duration		Continuous
Junction Temperature		+150°C
Storage Temperature		-65°C to +150°C
Lead Temperature (Soldering, 4 seconds)		+260°C
Maximum Package Power Dissipation Capacity at 25°C, TSSOP Package		1.98W
Package Derating		16 mW/°C above +25°C
ESD Rating	HBM, 1.5k Ω , 100pF	7kV
	EIAJ, 0 Ω , 200 pF	500V
Latch Up Tolerance at 25°C		\pm 100mA

(1) "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be verified. They are not meant to imply that the device should be operated at these limits. The tables of "Electrical Characteristics" specify conditions for device operation.

Recommended Operating Conditions

	Min	Nom	Max	Unit
Supply Voltage (V_{CC})	3.0	3.3	3.6	V
Operating Free Air Temperature (T_A)	-10	+25	+70	°C
Supply Noise Voltage (V_{CC})			200	mV _{PP}
TxCLKIN frequency	18		85	MHz

Electrical Characteristics⁽¹⁾

Over recommended operating supply and temperature ranges unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ ⁽²⁾	Max	Unit
LVCMOS/LVTTL DC SPECIFICATIONS						
V_{IH}	High Level Input Voltage		2.0		V_{CC}	V
V_{IL}	Low Level Input Voltage		0		0.8	V
V_{CL}	Input Clamp Voltage	$I_{CL} = -18$ mA		-0.79	-1.5	V
I_{IN}	Input Current	$V_{IN} = 0.4$ V, 2.5V or V_{CC}		+1.8	+10	μ A
		$V_{IN} =$ GND	-10	0		μ A
LVDS DC SPECIFICATIONS						
V_{OD}	Differential Output Voltage	$R_L = 100\Omega$	250	345	450	mV
ΔV_{OD}	Change in V_{OD} between complimentary output states				35	mV
V_{OS}	Offset Voltage ⁽³⁾		1.13	1.25	1.38	V
ΔV_{OS}	Change in V_{OS} between complimentary output states				35	mV
I_{OS}	Output Short Circuit Current	$V_{OUT} = 0$ V, $R_L = 100\Omega$		-3.5	-5	mA
I_{OZ}	Output TRI-STATE [®] Current	Power Down = 0V, $V_{OUT} = 0$ V or V_{CC}		\pm 1	\pm 10	μ A

(1) Current into device pins is defined as positive. Current out of device pins is defined as negative. Voltages are referenced to ground unless otherwise specified (except V_{OD} and ΔV_{OD}).

(2) Typical values are given for $V_{CC} = 3.3$ V and $T_A = +25^\circ$ C unless specified otherwise.

(3) V_{OS} previously referred as V_{CM} .

Electrical Characteristics⁽¹⁾ (continued)

Over recommended operating supply and temperature ranges unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ ⁽²⁾	Max	Unit
TRANSMITTER SUPPLY CURRENT						
ICCTW	Transmitter Supply Current, Worst Case	$R_L = 100\Omega$, $C_L = 5\text{ pF}$, Worst Case Pattern (Figure 1, Figure 3) "Typ" values are given for $V_{CC} = 3.6\text{V}$ and $T_A = +25^\circ\text{C}$, "Max" values are given for $V_{CC} = 3.6\text{V}$ and $T_A = -10^\circ\text{C}$	f = 25MHz	29	40	mA
			f = 40 MHz	34	45	mA
			f = 65 MHz	42	55	mA
			f = 87.5 MHz	48	60	mA
ICCTG	Transmitter Supply Current, 16 Grayscale	$R_L = 100\Omega$, $C_L = 5\text{ pF}$, 16 Grayscale Pattern (Figure 2, Figure 3) "Typ" values are given for $V_{CC} = 3.6\text{V}$ and $T_A = +25^\circ\text{C}$, "Max" values are given for $V_{CC} = 3.6\text{V}$ and $T_A = -10^\circ\text{C}$	f = 25 MHz	28	40	mA
			f = 40 MHz	32	45	mA
			f = 65 MHz	39	50	mA
			f = 87.5 MHz	44	56	mA
ICCTZ	Transmitter Supply Current, Power Down	Power Down = Low, Driver Outputs in TRI-STATE [®] under Power Down Mode		11	150	μA

Recommended Transmitter Input Characteristics

Over recommended operating supply and temperature ranges unless otherwise specified

Symbol	Parameter	Min	Typ	Max	Unit
TCIT	TxCLK IN Transition Time (Figure 5)	1.0		6.0	ns
TCIP	TxCLK IN Period (Figure 6)	11.76	T	50	ns
TCIH	TxCLK IN High Time (Figure 6)	0.35T	0.5T	0.65T	ns
TCIL	TxCLK IN Low Time (Figure 6)	0.35T	0.5T	0.65T	ns
TXIT	TxIN, and /PD pin Transition Time	1.5		6.0	ns
TXPD	Minimum pulse width for PWR DOWN pin signal	1			us

Transmitter Switching Characteristics

Over recommended operating supply and temperature ranges unless otherwise specified

Symbol	Parameter	Min	Typ	Max	Unit	
LLHT	LVDS Low-to-High Transition Time (Figure 4)		0.75	1.4	ns	
LHLT	LVDS High-to-Low Transition Time (Figure 4)		0.75	1.4	ns	
TPPos0	Transmitter Output Pulse Position (Figure 12) ⁽¹⁾	f = 25MHz	-0.45	0	+0.45	ns
TPPos1	Transmitter Output Pulse Position		5.26	5.71	6.16	ns
TPPos2	Transmitter Output Pulse Position		10.98	11.43	11.88	ns
TPPos3	Transmitter Output Pulse Position		16.69	17.14	17.59	ns
TPPos4	Transmitter Output Pulse Position		22.41	22.86	23.31	ns
TPPos5	Transmitter Output Pulse Position		28.12	28.57	29.02	ns
TPPos6	Transmitter Output Pulse Position		33.84	34.29	34.74	ns

(1) The Minimum and Maximum Limits are based on statistical analysis of the device performance over process, voltage, and temperature ranges. This parameter is functionality tested only on Automatic Test Equipment (ATE).

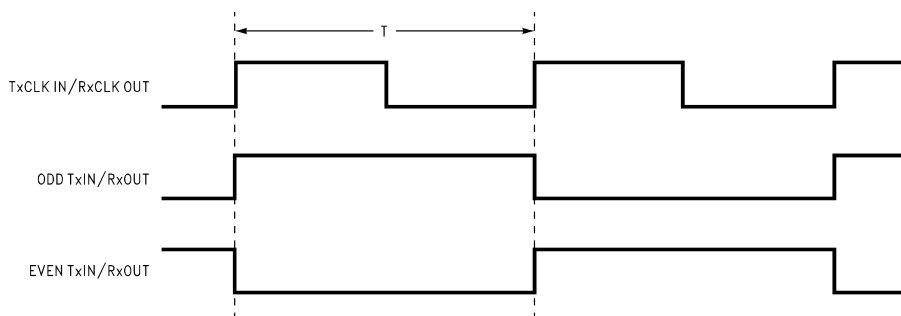
Transmitter Switching Characteristics (continued)

Over recommended operating supply and temperature ranges unless otherwise specified

Symbol	Parameter		Min	Typ	Max	Unit
TPPos0	Transmitter Output Pulse Position (Figure 12) ⁽¹⁾	f = 40 MHz	-0.25	0	+0.25	ns
TPPos1	Transmitter Output Pulse Position		3.32	3.57	3.82	ns
TPPos2	Transmitter Output Pulse Position		6.89	7.14	7.39	ns
TPPos3	Transmitter Output Pulse Position		10.46	10.71	10.96	ns
TPPos4	Transmitter Output Pulse Position		14.04	14.29	14.54	ns
TPPos5	Transmitter Output Pulse Position		17.61	17.86	18.11	ns
TPPos6	Transmitter Output Pulse Position		21.18	21.43	21.68	ns
TPPos0	Transmitter Output Pulse Position (Figure 12) ⁽¹⁾	f = 65 MHz	-0.20	0	+0.20	ns
TPPos1	Transmitter Output Pulse Position		2.00	2.20	2.40	ns
TPPos2	Transmitter Output Pulse Position for Bit 2		4.20	4.40	4.60	ns
TPPos3	Transmitter Output Pulse Position for Bit 3		6.39	6.59	6.79	ns
TPPos4	Transmitter Output Pulse Position		8.59	8.79	8.99	ns
TPPos5	Transmitter Output Pulse Position		10.79	10.99	11.19	ns
TPPos6	Transmitter Output Pulse Position		12.99	13.19	13.39	ns
TPPos0	Transmitter Output Pulse Position (Figure 12) ⁽¹⁾	f = 87.5 MHz	-0.20	0	+0.20	ns
TPPos1	Transmitter Output Pulse Position		1.48	1.68	1.88	ns
TPPos2	Transmitter Output Pulse Position		3.16	3.36	3.56	ns
TPPos3	Transmitter Output Pulse Position		4.84	5.04	5.24	ns
TPPos4	Transmitter Output Pulse Position		6.52	6.72	6.92	ns
TPPos5	Transmitter Output Pulse Position		8.20	8.40	8.60	ns
TPPos6	Transmitter Output Pulse Position		9.88	10.08	10.28	ns
TSTC	Required TxIN Setup to TxCLK IN (Figure 6) at 85MHz		2.5			ns
THTC	Required TxIN Hold to TxCLK IN (Figure 6) at 87.5 MHz		0.5			ns
TCCD	TxCLK IN to TxCLK OUT Delay. Measure from TxCLK IN edge to immediately crossing point of differential TxCLK OUT by following the positive TxCLK OUT. 50% duty cycle input clock is assumed. (Figure 7)	T _A = -10°C, and 85MHz for "Min" T _A = 70°C, and 25MHz for "Max", V _{CC} = 3.6V, R _{FB} pin = VCC	3.086		7.211	ns
	Measure from TxCLK IN edge to immediately crossing point of differential TxCLK OUT by following the positive TxCLK OUT. 50% duty cycle input clock is assumed. (Figure 8)	T _A = -10°C, and 85MHz for "Min" T _A = 70°C, and 25MHz for "Max", V _{CC} = 3.6V, R _{FB} pin = GND	2.868		6.062	ns
SSCG	Spread Spectrum Clock support; Modulation frequency with a linear profile. ⁽²⁾	f = 25 MHz		100kHz ± 2.5%/-5%		
		f = 40 MHz		100kHz ± 2.5%/-5%		
		f = 65 MHz		100kHz ± 2.5%/-5%		
		f = 87.5 MHz		100kHz ± 2.5%/-5%		
TPLLS	Transmitter Phase Lock Loop Set (Figure 9)				10	ms
TPDD	Transmitter Power Down Delay (Figure 11)				100	ns

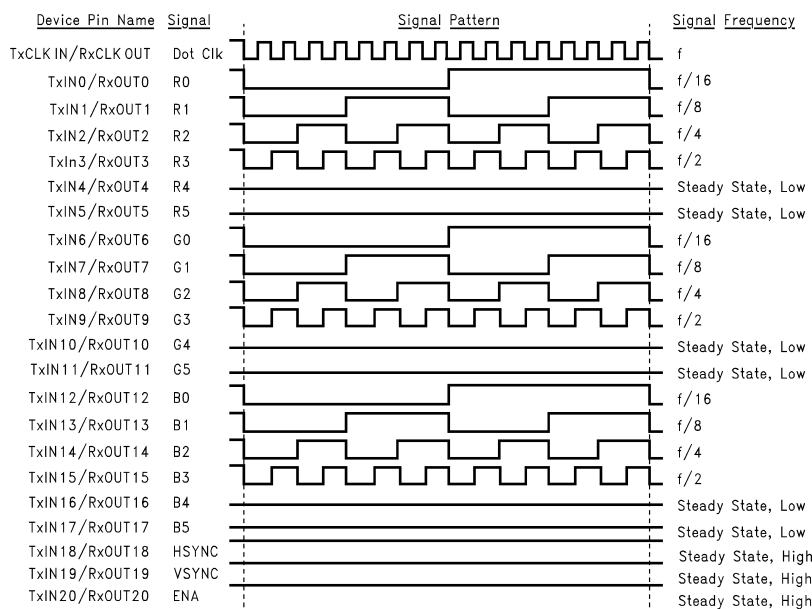
(2) Care must be taken to ensure TSTC and THTC are met so input data are sampling correctly. This SSCG parameter only shows the performance of tracking Spread Spectrum Clock applied to TxCLK IN pin, and reflects the result on TxCLKOUT+ and TxCLKOUT- pins.

AC Timing Diagrams



- A. The worst case test pattern produces a maximum toggling of digital circuits, LVDS I/O and LVCMOS/LVTTL I/O.
- B. [Figure 1](#) and [Figure 2](#) show a falling edge data strobe (TxCLK IN/RxCLK OUT).

Figure 1. "Worst Case" Test Pattern



- A. The 16 grayscale test pattern tests device power consumption for a "typical" LCD display pattern. The test pattern approximates signal switching needed to produce groups of 16 vertical stripes across the display.
- B. [Figure 1](#) and [Figure 2](#) show a falling edge data strobe (TxCLK IN/RxCLK OUT).
- C. Recommended pin to signal mapping. Customer may choose to define differently.

Figure 2. "16 Grayscale" Test Pattern - DS90C365A

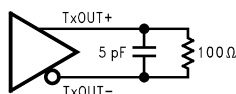


Figure 3. DS90C365A (Transmitter) LVDS Output Load. 5pF is showed as board loading

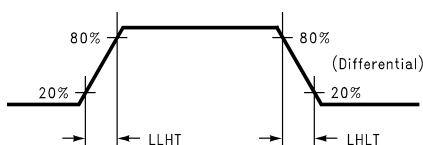


Figure 4. DS90C365A (Transmitter) LVDS Transition Times

AC Timing Diagrams (continued)

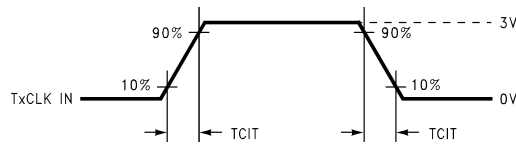


Figure 5. DS90C365A (Transmitter) Input Clock Transition Time

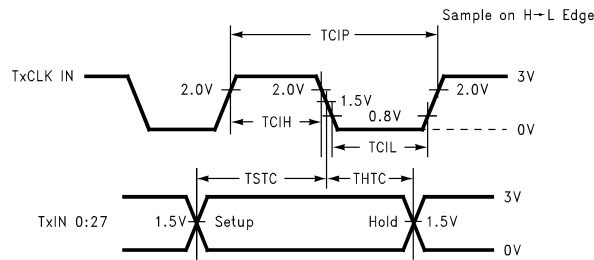


Figure 6. DS90C365A (Transmitter) Setup/Hold and High/Low Times with R_FB pin = GND (Falling Edge Strobe)

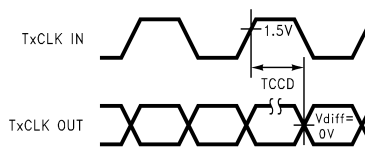


Figure 7. DS90C365A (Transmitter) Clock In to Clock Out Delay with R_FB pin = VCC

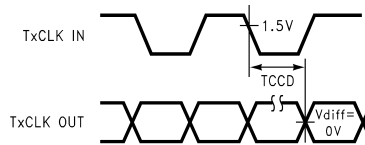


Figure 8. DS90C365A (Transmitter) Clock In to Clock Out Delay with R_FB pin = GND

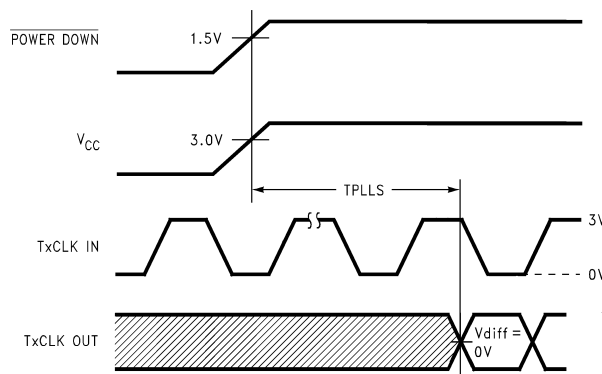


Figure 9. DS90C365A (Transmitter) Phase Lock Loop Set Time

AC Timing Diagrams (continued)

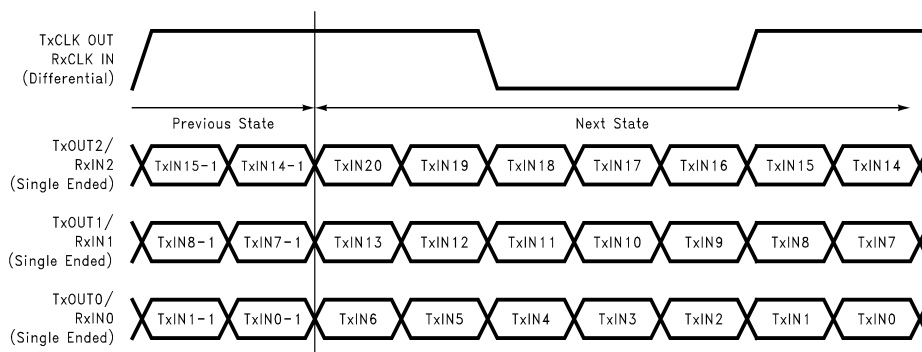


Figure 10. 21 Parallel TTL Data Inputs Mapped to LVDS Outputs - DS90C365A

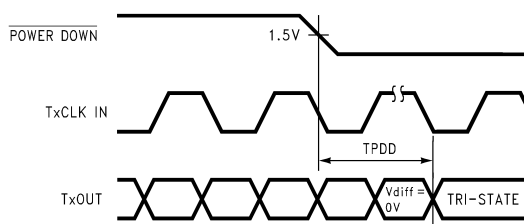


Figure 11. Transmitter Power Down Delay

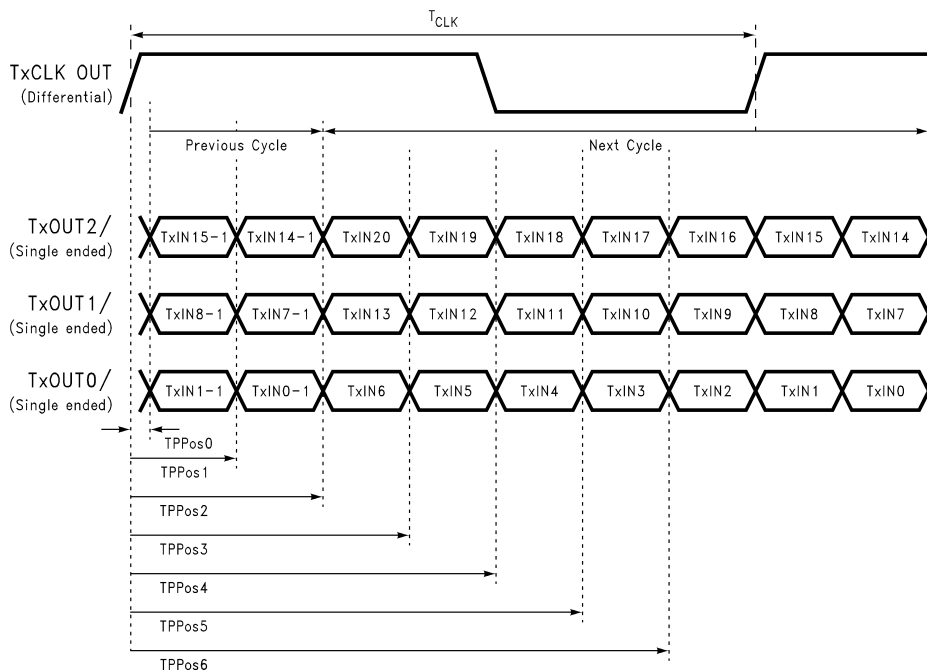


Figure 12. Transmitter LVDS Output Pulse Position Measurement - DS90C365A

PIN DESCRIPTIONS

DS90C365A DGG0048A (TSSOP) Package Pin Descriptions — FPD Link Transmitter

Pin Name	I/O	No.	Description
TxIN	I	21	LVTTL level input. This includes: 6 Red, 6 Green, 6 Blue, and 3 control lines—FPLINE, FPFRAME and DRDY (also referred to as HSYNC, VSYNC, Data Enable).
TxOUT+	O	3	Positive LVDS differential data output.
TxOUT-	O	3	Negative LVDS differential data output.
TxCLKIN	I	1	LVTTL level clock input. Pin name TxCLK IN.
R_FB	I	1	LVTTL level programmable strobe select (See Table 1).
TxCLK OUT+	O	1	Positive LVDS differential clock output.
TxCLK OUT-	O	1	Negative LVDS differential clock output.
PWR DOWN	I	1	LVTTL level input. When asserted (low input) TRI-STATES the outputs, ensuring low current at power down.
V _{CC}	I	3	Power supply pins for LVTTL inputs.
GND	I	5	Ground pins for LVTTL inputs.
PLL V _{CC}	I	1	Power supply pin for PLL.
PLL GND	I	2	Ground pins for PLL.
LVDS V _{CC}	I	1	Power supply pin for LVDS outputs.
LVDS GND	I	3	Ground pins for LVDS outputs.
NC		1	No connect

APPLICATIONS INFORMATION

The DS90C365A is backward compatible with the DS90C365, DS90C363A, DS90C363 in TSSOP 48-lead package, and it is a pin-for-pin replacements.

This device DS90C365A also features reduced variation of the TCCD parameter which is important for dual pixel applications. See AN-1084([SNLA001](#))

This device may also be used as a replacement for the DS90CF563 (5V, 65MHz) and DS90CF561 (5V, 40MHz) FPD-Link Transmitters with certain considerations/modifications:

1. Change 5V power supply to 3.3V. Provide this 3.3V supply to the V_{CC}, LVDS V_{CC} and PLL V_{CC} of the transmitter.
2. The DS90C365A transmitter input and control inputs accept 3.3V LVTTL/LVCMOS levels. They are not 5V tolerant.
3. To implement a falling edge device for the DS90C365A, the R_FB pin may be tied to ground OR left unconnected (an internal pull-down resistor biases this pin low). Biasing this pin to V_{CC} implements a rising edge device.

TRANSMITTER INPUT PINS

The TxIN and control input pins are compatible with LVCMOS and LVTTL levels. These pins are not 5V tolerant.

TRANSMITTER INPUT CLOCK/DATA SEQUENCING

Unlike the DS90C365, DS90C(F)383A/363A, the DS90C365A does not require any special requirement for sequencing of the input clock/data and PD (PowerDown) signal. The DS90C365A offers a more robust input sequencing feature where the input clock/data can be inserted after the release of the PD signal. In the case where the clock/data is stopped and reapplied, such as changing video mode within Graphics Controller, it is not necessary to cycle the PD signal. However, there are in certain cases where the PD may need to be asserted during these mode changes. In cases where the source (Graphics Source) may be supplying an unstable clock or spurious noisy clock output to the LVDS transmitter, the LVDS Transmitter may attempt to lock onto this unstable clock signal but is unable to do so due the instability or quality of the clock source. The PD signal in

these cases should then be asserted once a stable clock is applied to the LVDS transmitter. Asserting the PWR DOWN pin will effectively place the device in reset and disable the PLL, enabling the LVDS Transmitter into a power saving standby mode. However, it is still generally a good practice to assert the PWR DOWN pin or reset the LVDS transmitter whenever the clock/data is stopped and reapplied but it is not mandatory for the DS90C365A.

SPREAD SPECTRUM CLOCK SUPPORT

The DS90C365A can support Spread Spectrum Clocking signal type inputs. The DS90C365A outputs will accurately track Spread Spectrum Clock/Data inputs with modulation frequencies of up to 100kHz (max.) with either center spread of $\pm 2.5\%$ or down spread -5% deviations.

POWER SOURCES SEQUENCE

In typical applications, it is recommended to have V_{CC}, LVDS V_{CC} and PLL V_{CC} from the same power source with three separate de-coupling bypass capacitor groups. There is no requirement on which VCC entering the device first.

Pin Diagram for TSSOP Package

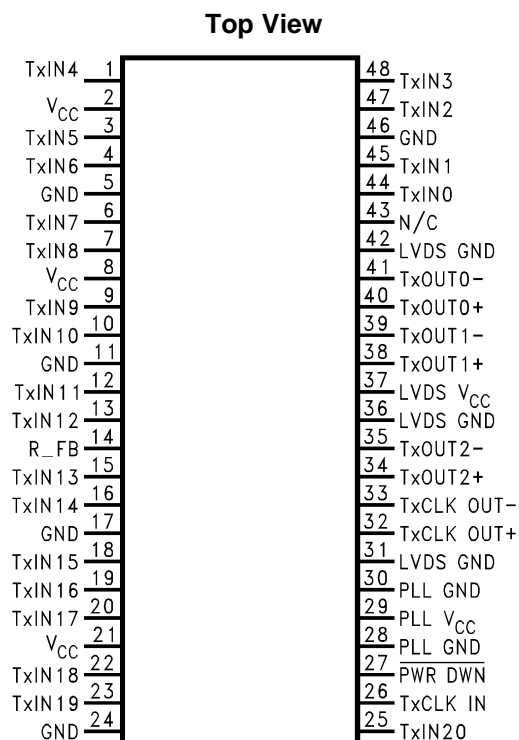


Figure 13. Order Number DS90C365AMT DGG0048A Package

Typical Application

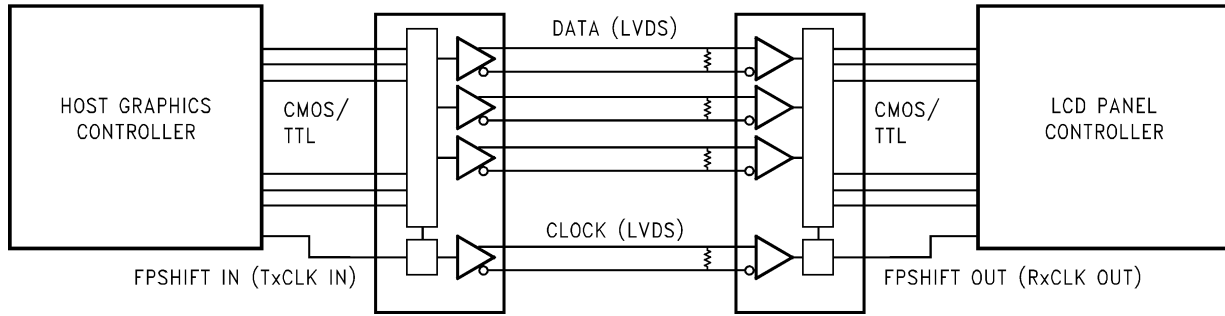


Table 1. Truth Table – Programmable Transmitter (DS90C365A)

Pin	Condition	Strobe Status
R_FB	R_FB = V _{CC}	Rising edge strobe
R_FB	R_FB = GND or NC	Falling edge strobe

REVISION HISTORY

Changes from Revision H (April 2013) to Revision I	Page
<hr/> <ul style="list-style-type: none">• Changed layout of National Data Sheet to TI format	<hr/> 10

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
DS90C365AMT/NOPB	ACTIVE	TSSOP	DGG	48	38	RoHS & Green	SN	Level-2-260C-1 YEAR	-10 to 70	DS90C365AMT	Samples
DS90C365AMTX/NOPB	ACTIVE	TSSOP	DGG	48	1000	RoHS & Green	SN	Level-2-260C-1 YEAR	-10 to 70	DS90C365AMT	Samples

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBsolete: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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TAPE AND REEL INFORMATION



QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

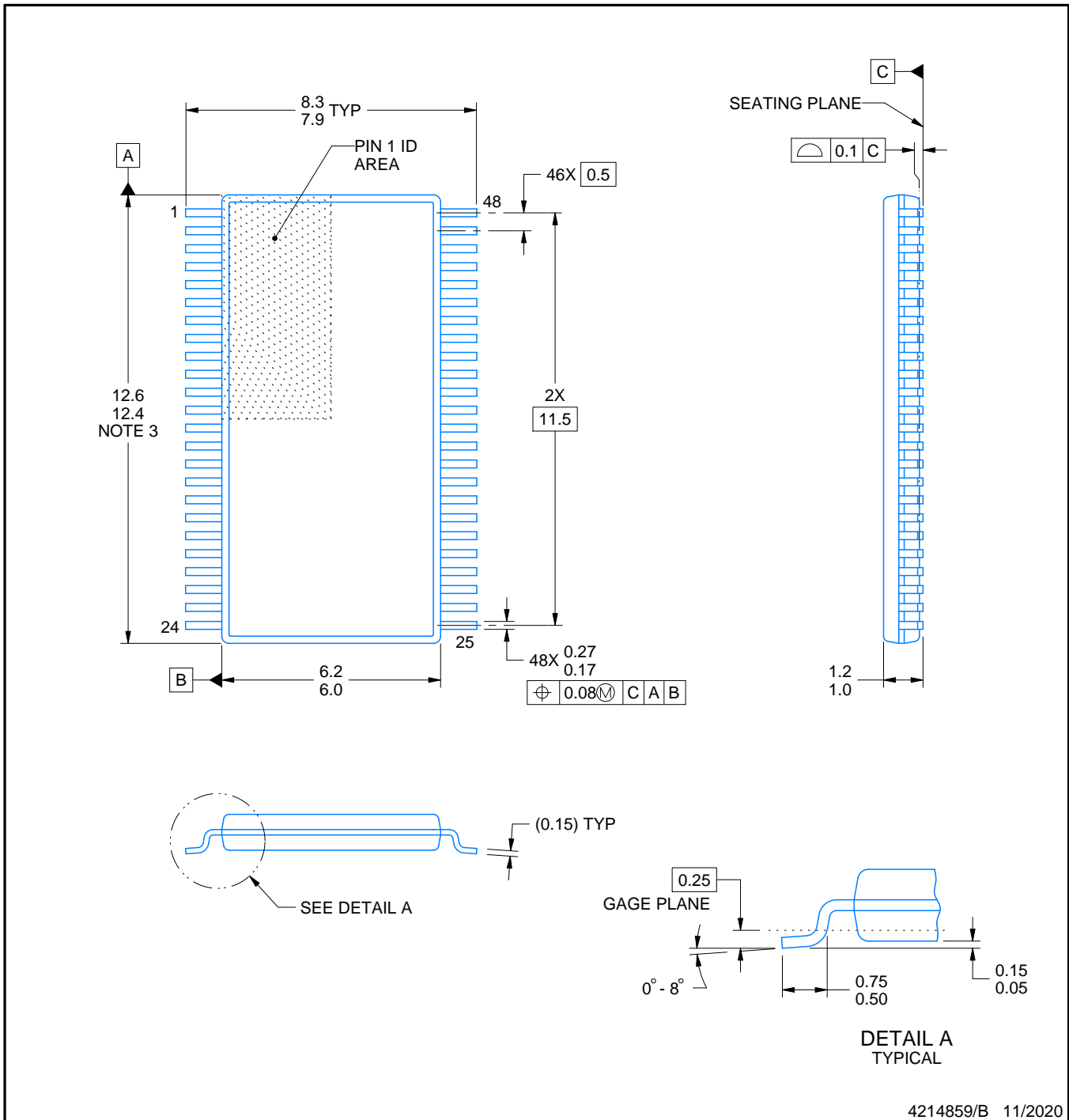
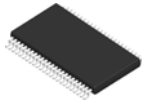
Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
DS90C365AMTX/NOPB	TSSOP	DGG	48	1000	330.0	24.4	8.6	13.2	1.6	12.0	24.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
DS90C365AMTX/NOPB	TSSOP	DGG	48	1000	367.0	367.0	45.0



4214859/B 11/2020

NOTES:

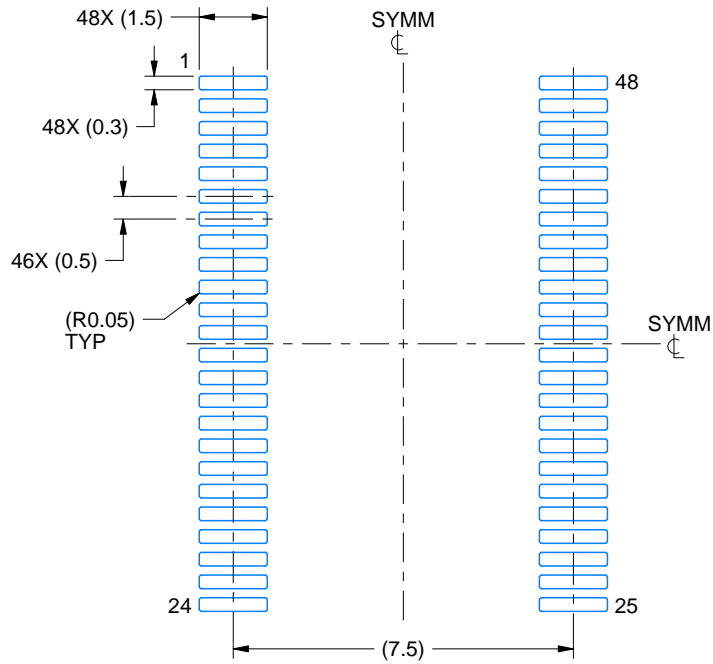
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. Reference JEDEC registration MO-153.

EXAMPLE BOARD LAYOUT

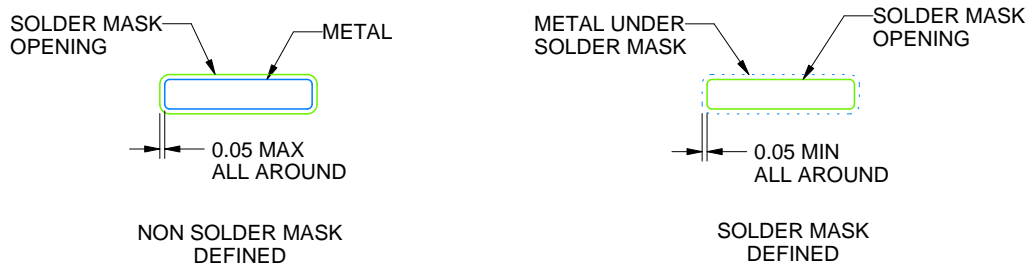
DGG0048A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



LAND PATTERN EXAMPLE
SCALE:6X



SOLDER MASK DETAILS

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NOTES: (continued)

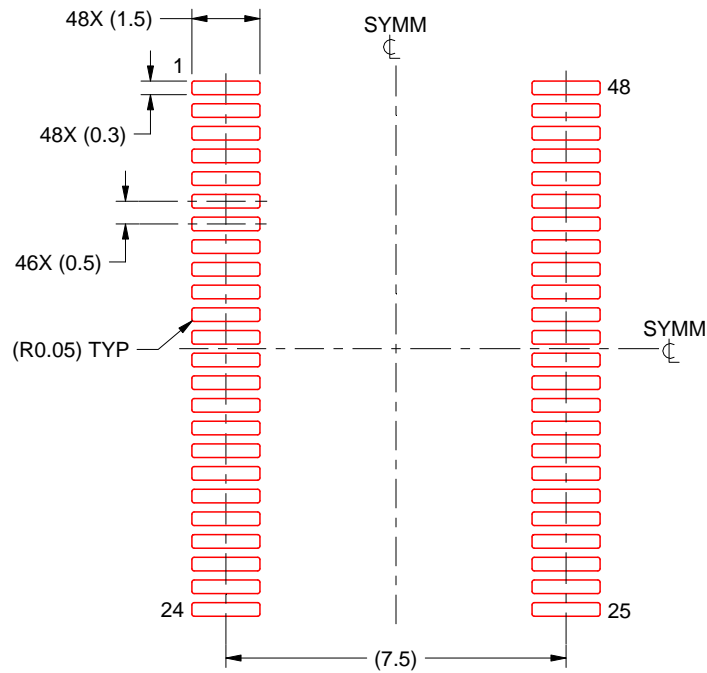
- 5. Publication IPC-7351 may have alternate designs.
- 6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

DGG0048A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:6X

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NOTES: (continued)

7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
8. Board assembly site may have different recommendations for stencil design.

DGG (R-PDSO-G**)

PLASTIC SMALL-OUTLINE PACKAGE

48 PINS SHOWN



- NOTES: A. All linear dimensions are in millimeters.
 B. This drawing is subject to change without notice.
 C. Body dimensions do not include mold protrusion not to exceed 0,15.
 D. Falls within JEDEC MO-153

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