MOSFET – Power, Dual N-Channel, for 1-Cell Lithium-ion Battery Protection

12 V, 3.2 mΩ, 27 A

EFC8811R

This Power MOSFET features a low on−state resistance. This device is suitable for applications such as power switches of portable machines. Best suited for 1−cell lithium−ion battery applications.

Features

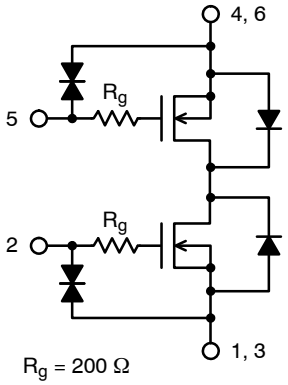
- 2.5 V Drive
- 2 kV ESD HBM
- Common−Drain Type
- ESD Diode−Protected Gate
- Pb−Free, Halogen Free and RoHS Compliance

Applications

- 1−Cell Lithium−ion Battery Charging and Discharging Switch

V_{SSS}	$R_{SS(on)}$ MAX	I_S MAX
12 V	3.2 mΩ @ 4.5 V	27 A
	3.2 mΩ @ 4.0 V	
	3.2 mΩ @ 3.8 V	
	4.4 mΩ @ 3.1 V	
	6.3 mΩ @ 2.5 V	

ELECTRICAL CONNECTION N−Channel



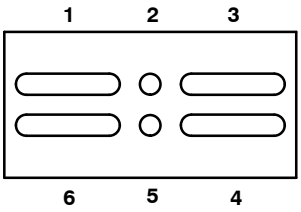
R_g = 200 Ω

CSP6, 1.77x3.54/ EFCP3517−6DGH−020 CASE 568AL

MARKING DIAGRAM

ML = Device Code
Y = Year of Production
M = Month of Assembly Operation
ZZ = Assembly Lot Number

PIN CONNECTIONS



1: Source1
2: Gate1
3: Source1
4: Source2
5: Gate2
6: Source2

ORDERING INFORMATION

See detailed ordering and shipping information on page 2 of this data sheet.

SPECIFICATIONS

ABSOLUTE MAXIMUM RATINGS (T_A = 25°C)

Parameter	Symbol	Value	Unit
Source to Source Voltage	V_{SSS}	12	V
Gate to Source Voltage	V_{GSS}	±8	V
Source Current (DC)	I_S	27	A
Source Current (Pulse) PW ≤ 100 μs, Duty Cycle ≤ 1%	I_{SP}	100	A
Total Dissipation Surface mounted on ceramic substrate (5000 mm² x 0.8 mm)	P_T	2.5	W
Junction Temperature	T_j	150	°C
Storage Temperature	T_{stg}	−55 to +150	°C

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

THERMAL RESISTANCE RATINGS

Parameter	Symbol	Value	Unit
Junction to Ambient Surface mounted on ceramic substrate (5000 mm² x 0.8 mm)	$R_{\theta JA}$	50	°C/W

ELECTRICAL CHARACTERISTICS (T_A = 25°C)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Source to Source Breakdown Voltage	$V_{(BR)SSS}$	I_S = 1 mA, V_{GS} = 0 V (Test Circuit 1)	12	–	–	V
Zero−Gate Voltage Source Current	I_{SSS}	V_{SS} = 10 V, V_{GS} = 0 V (Test Circuit 1)	–	–	1	μA
Gate to Source Leakage Current	I_{GSS}	V_{GS} = ±8 V, V_{SS} = 0 V (Test Circuit 2)	–	–	±1	μA
Gate Threshold Voltage	V_{GS}(th)	V_{SS} = 6 V, I_S = 1 mA (Test Circuit 3)	0.5	–	1.3	V
Forward Transconductance	g_{FS}	V_{SS} = 6 V, I_S = 3 A (Test Circuit 4)	–	19	–	S
Static Source to Source On−State Resistance	$R_{SS(on)}1$	I_S = 5 A, V_{GS} = 4.5 V (Test Circuit 5)	1.8	2.3	3.2	mΩ
	$R_{SS(on)}2$	I_S = 5 A, V_{GS} = 4.0 V (Test Circuit 5)	1.9	2.4	3.2	mΩ
	$R_{SS(on)}3$	I_S = 5 A, V_{GS} = 3.8 V (Test Circuit 5)	2.0	2.6	3.2	mΩ
	$R_{SS(on)}4$	I_S = 5 A, V_{GS} = 3.1 V (Test Circuit 5)	2.1	3.3	4.4	mΩ
	$R_{SS(on)}5$	I_S = 5 A, V_{GS} = 2.5 V (Test Circuit 5)	2.7	4.0	6.3	mΩ
Turn−ON Delay Time	$t_{d(on)}$	V_{SS} = 6 V, V_{GS} = 4.5 V, I_S = 3 A (Test Circuit 6)	–	80	–	ns
Rise Time	t_r		–	570	–	ns
Turn−OFF Delay Time	$t_{d(off)}$		–	38,000	–	ns
Fall Time	t_f		–	17,700	–	ns
Total Gate Charge	Q_g	V_{SS} = 6 V, V_{GS} = 4.5 V, I_S = 27 A (Test Circuit 7)	–	100	–	nC
Forward Source to Source Voltage	$V_{F(S-S)}$	I_S = 3 A, V_{GS} = 0 V (Test Circuit 8)	–	0.75	1.2	V

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

ORDERING INFORMATION

Device	Marking	Package	Shipping (Qty / Packing)†
EFC8811R−TF	ML	CSP6, 1.77 × 3.54 EFCP3517−6DGH−020 (Pb−Free / Halogen Free)	5,000 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

TEST CIRCUITS ARE EXAMPLE OF MEASURING FET1 SIDE

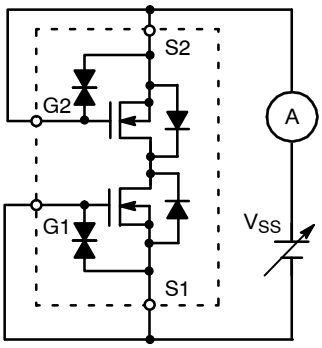
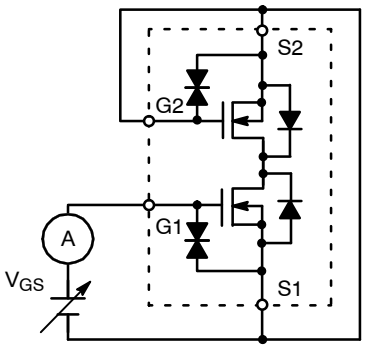
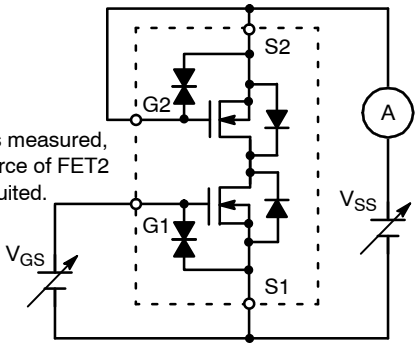


Figure 1. Test Circuit 1 – V_{SSS}/I_{SSS}



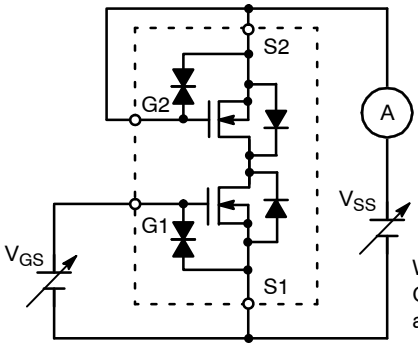
When FET1 is measured, Gate and Source of FET2 are short−circuited.

Figure 2. Test Circuit 2 – I_{GSS}



When FET1 is measured, Gate and Source of FET2 are short−circuited.

Figure 3. Test Circuit 3 – $V_{GS}(th)$



When FET1 is measured, Gate and Source of FET2 are short−circuited.

Figure 4. Test Circuit 4 – g_{FS}

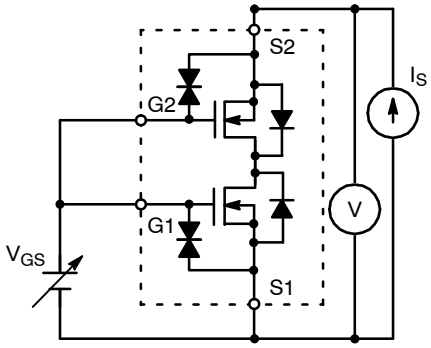
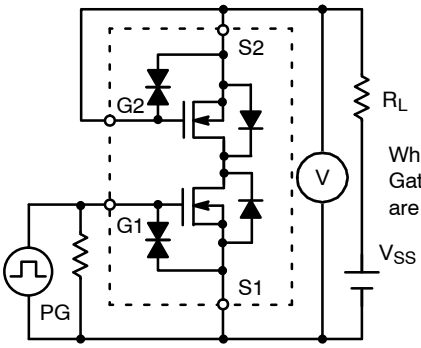
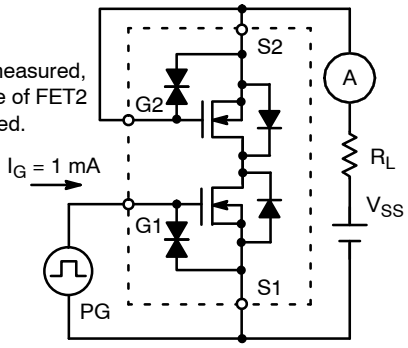


Figure 5. Test Circuit 5 – $R_{SS(on)}$



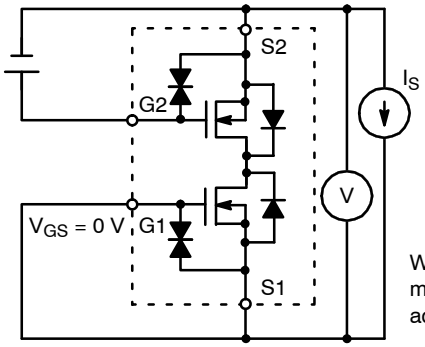
When FET1 is measured, Gate and Source of FET2 are short−circuited.

Figure 6. Test Circuit 6 – $t_{d(on)}$, t_r, $t_{d(off)}$, t_f



When FET1 is measured, Gate and Source of FET2 are short−circuited.

Figure 7. Test Circuit 7 – Q_g



When FET1 is measured, +4.5 V is added to V_{GS} of FET2.

Figure 8. Test Circuit 8 – $V_{F(S-S)}$

NOTE: When FET2 is measured, the position of FET1 and FET2 is switched.

TYPICAL CHARACTERISTICS

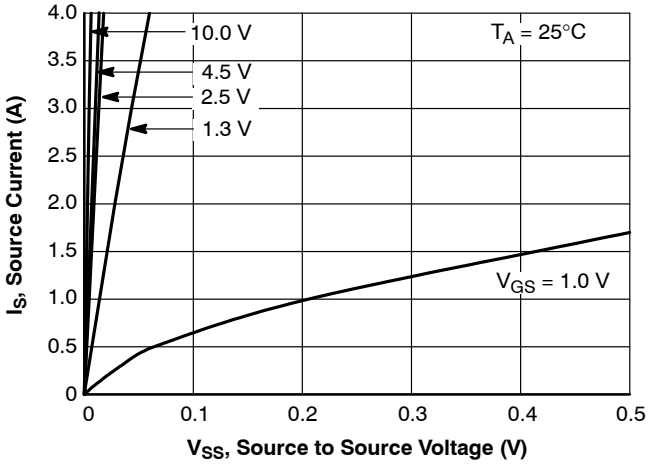


Figure 9. I_S – V_{SS}

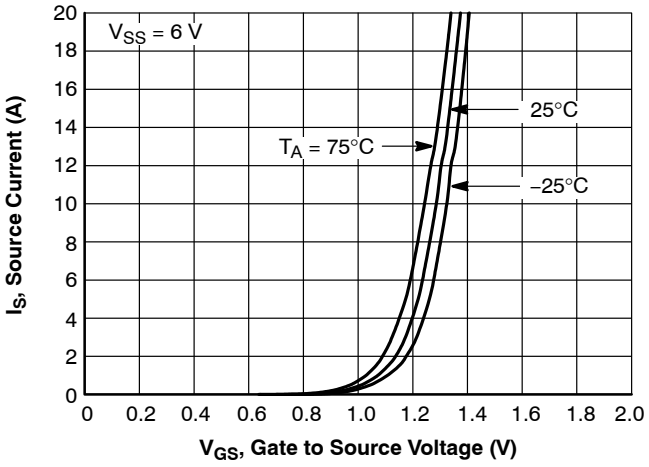


Figure 10. I_S – V_{GS}

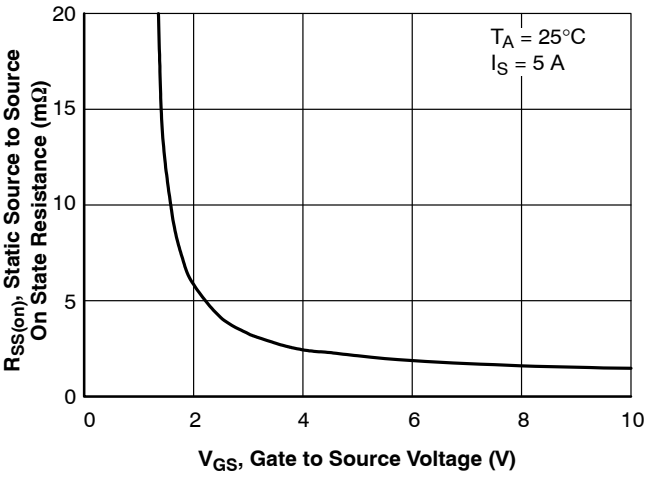


Figure 11. $R_{SS(on)}$ – V_{GS}

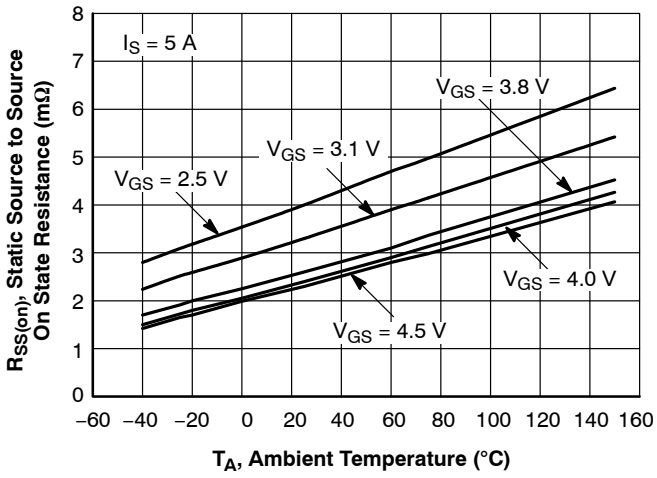


Figure 12. $R_{SS(on)}$ – T_A

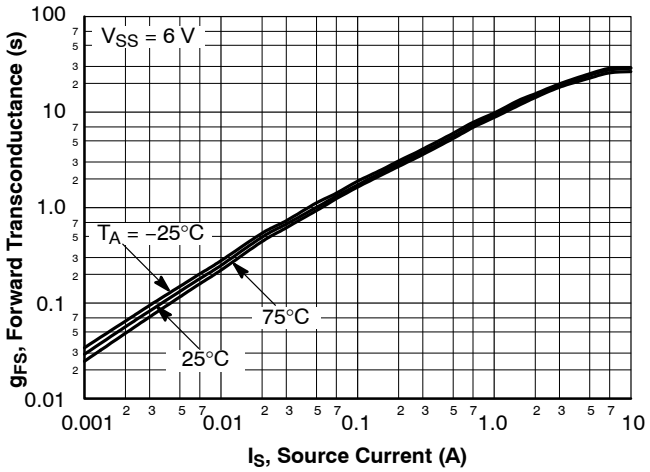


Figure 13. g_{FS} – I_S

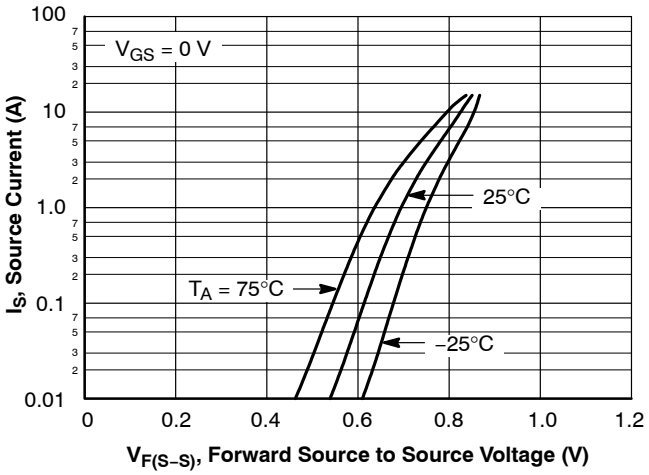


Figure 14. I_S – $V_{F(S-S)}$

TYPICAL CHARACTERISTICS (Continued)

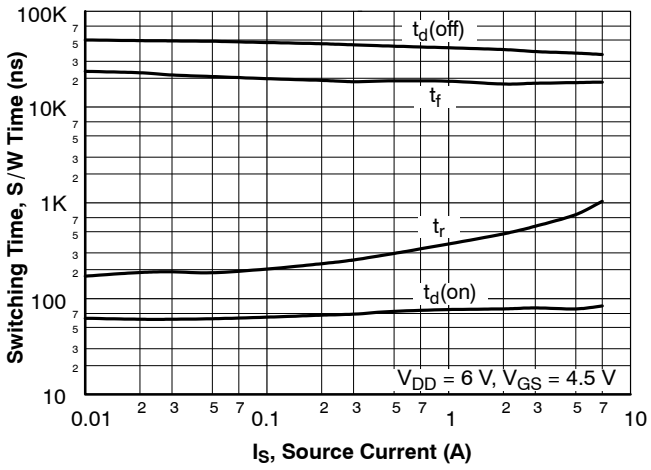


Figure 15. S/W Time – I_S

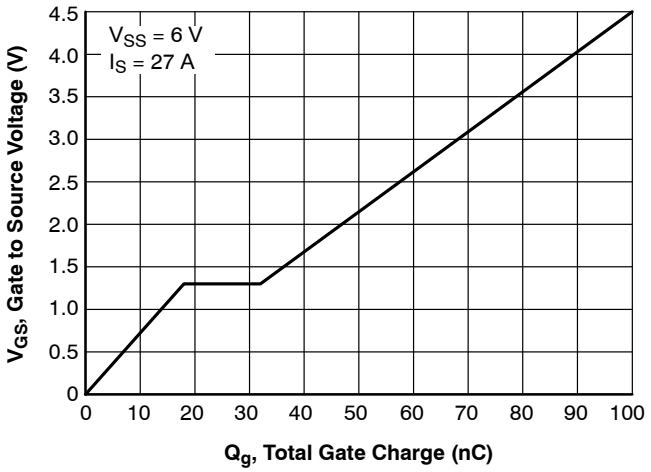


Figure 16. V_{GS} – Q_g

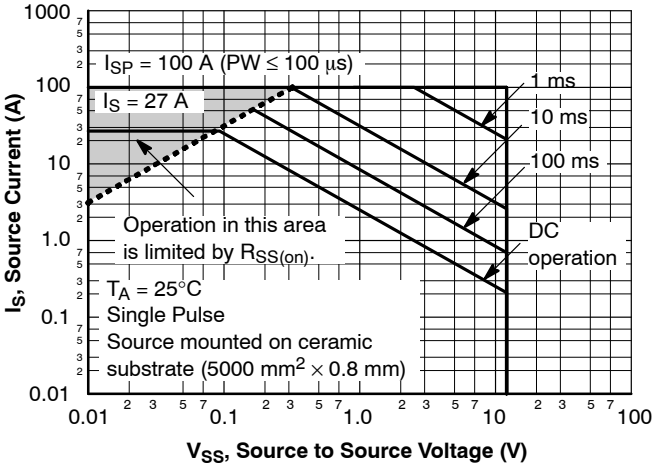


Figure 17. SOA

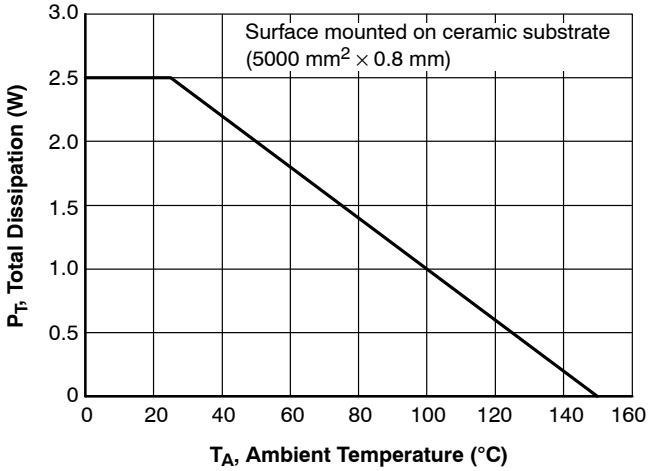


Figure 18. P_T – T_A

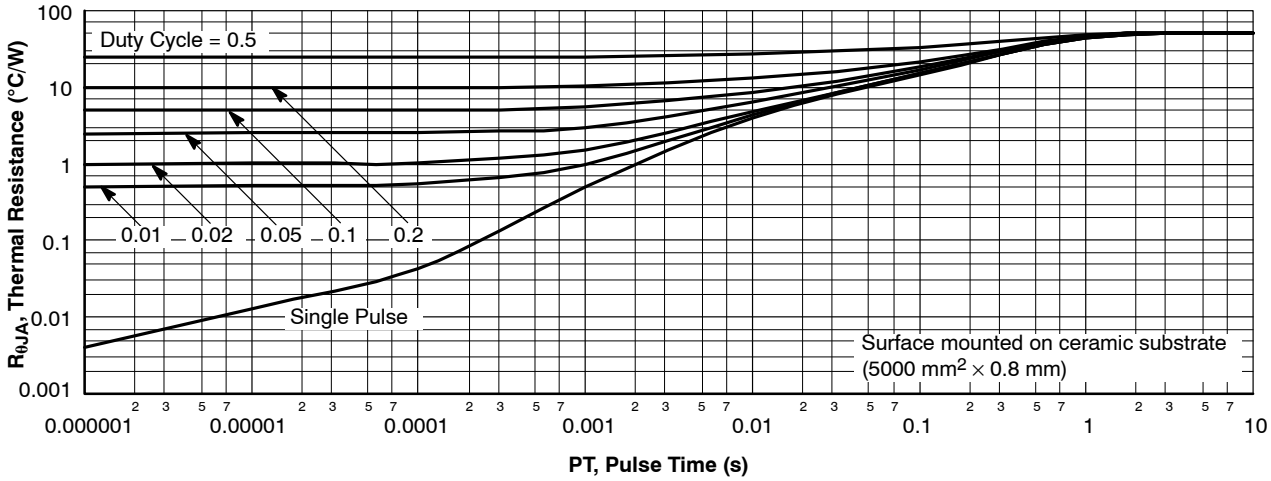


Figure 19. $R_{\theta JA}$ – Pulse Time

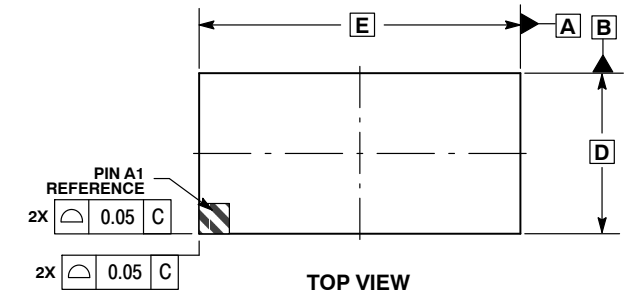
MECHANICAL CASE OUTLINE
PACKAGE DIMENSIONS

ON Semiconductor®

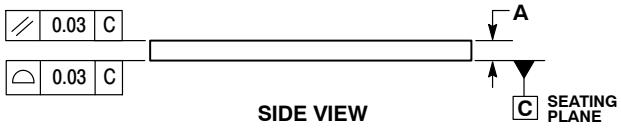
SCALE 4:1

CSP6, 1.77x3.54 / EFCP3517−6DGH−020
CASE 568AL
ISSUE O

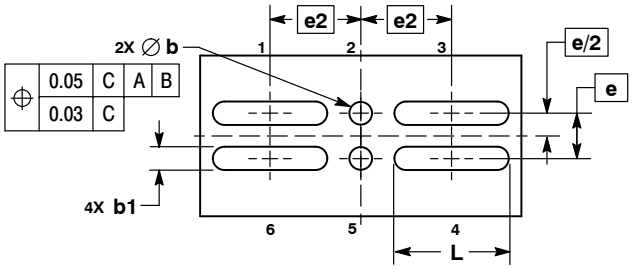
DATE 23 OCT 2013



TOP VIEW



SIDE VIEW

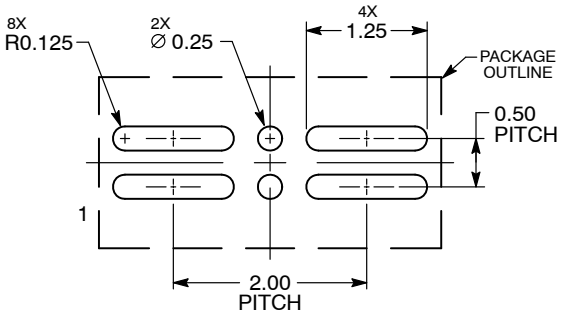


BOTTOM VIEW

NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.

DIM	MILLIMETERS MIN	MAX
A	−−−	0.22
b	0.22	0.28
b1	0.22	0.28
D	1.77 BSC	
E	3.54 BSC	
e	0.50 BSC	
e2	1.00 BSC	
L	1.22	1.28

RECOMMENDED SOLDERING FOOTPRINT*



DIMENSIONS: MILLIMETERS

*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

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