

Operational Amplifiers

Low Noise Operational Amplifiers

BA8522Rxxx

General Description

BA8522Rxxx are low noise operational amplifiers of high voltage gain. It excels especially in input referred noise voltage ($9 \text{ nV}/\sqrt{\text{Hz}}$), total harmonic distortion (0.002%) and operating voltage range ($\pm 2\text{V}$ to $\pm 16\text{V}$) and it is the most suitable operational amplifier with audio equipment.

Features

- High Voltage Gain
- Low Input Referred Noise Voltage
- Low Total Harmonic Distortion
- Low Input Offset Voltage
- Wide Operating Supply Voltage
- Wide Operating Temperature Range

Application

- Audio Application
- Consumer Equipment
- Active Filter

Key Specifications

- Operating Supply Voltage (split supply): $\pm 2\text{V}$ to $\pm 16\text{V}$
- Temperature Range: -40°C to $+105^\circ\text{C}$
- Input Offset Voltage: $\pm 1.5\text{mV}(\text{Max})$
- Slew Rate: $3\text{V}/\mu\text{s}(\text{Typ})$
- Total Harmonic Distortion: $0.002\%(\text{Typ})$
- Input Referred Noise Voltage: $9 \text{ nV}/\sqrt{\text{Hz}}(\text{Typ})$

Packages

	W(Typ) x D(Typ) x H(Max)
SOP8	5.00mm x 6.20mm x 1.71mm
SSOP-B8	3.00mm x 6.40mm x 1.35mm
MSOP8	2.90mm x 4.00mm x 0.90mm

Simplified Schematic

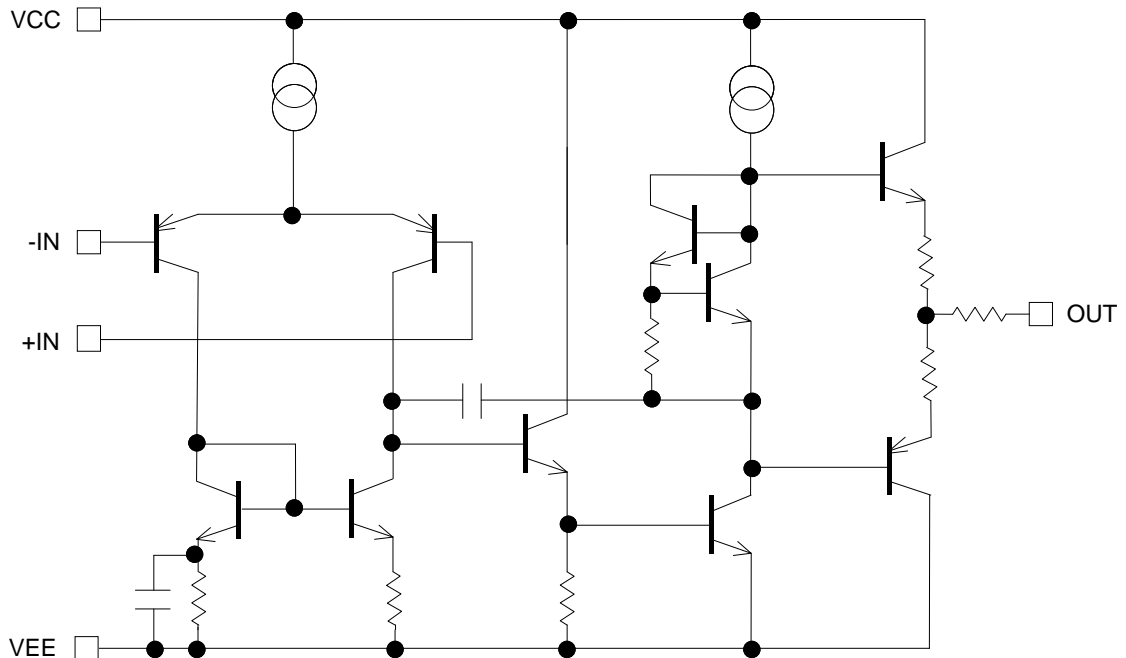
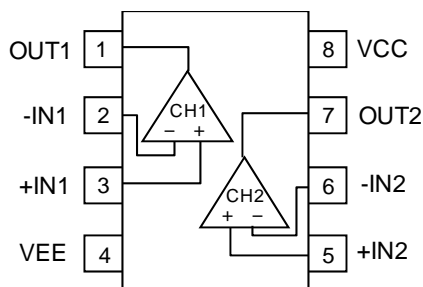


Figure 1. Simplified schematic (1 channel only)

○Product structure : Silicon monolithic integrated circuit ○This product has no designed protection against radioactive rays

Pin Configuration

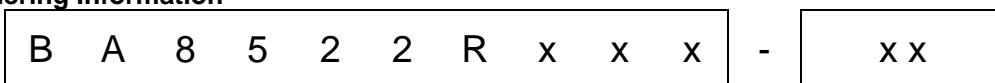
BA8522RF : SOP8
 BA8522RFV : SSOP-B8
 BA8522RFVM : MSOP8



Pin No.	Pin Name
1	OUT1
2	-IN1
3	+IN1
4	VEE
5	+IN2
6	-IN2
7	OUT2
8	VCC

Package		
SOP8	SSOP-B8	MSOP8
BA8522RF	BA8522RFV	BA8522RFVM

Ordering Information



Part Number BA8522Rxxx	Package F : SOP8 FV : SSOP-B8 FVM : MSOP8	Packaging and Forming Specification E2: Embossed tape and reel (SOP8/SSOP-B8) TR: Embossed tape and reel (MSOP8)
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Line-up

T _{opr}	Operating Supply Voltage (split supply)	Supply Current (Typ)	Slew Rate (Typ)	Package		Orderable Part Number
-40°C to +105°C	±2.0V to ±16.0V	5.5mA	3V/μs	SOP8	Reel of 2500	BA8522RF-E2
				SSOP-B8	Reel of 2500	BA8522RFV-E2
				MSOP8	Reel of 3000	BA8522RFVM-TR

Absolute Maximum Ratings ($T_A=25^\circ\text{C}$)

Parameter	Symbol	Ratings	Unit
Supply Voltage	VCC-VEE	+36	V
Power Dissipation	P _D	SOP8	0.69 ^(Note 1,4)
		SSOP-B8	0.62 ^(Note 2,4)
		MSOP8	0.59 ^(Note 3,4)
Differential Input Voltage ^(Note 5)	V _{ID}	+36	V
Input Common-mode Voltage Range	V _{ICM}	(VEE-0.3) to VEE+36	V
Input Current ^(Note 6)	I _I	-10	mA
Operating Supply Voltage	V _{opr}	±2 to ±16 (+4 to +32)	V
Output Current	I _{OUT}	±50	mA
Operating Temperature	T _{opr}	-40 to +105	°C
Storage Temperature	T _{stg}	55 to +150	°C
Maximum Junction Temperature	T _{Jmax}	+150	°C

(Note 1) To use at temperature above $T_A=25^\circ\text{C}$ reduce 5.5mW/°C.

(Note 2) To use at temperature above $T_A=25^\circ\text{C}$ reduce 5.0mW/°C.

(Note 3) To use at temperature above $T_A=25^\circ\text{C}$ reduce 4.7mW/°C.

(Note 4) Mounted on a FR4 glass epoxy PCB 70mm×70mm×1.6mm (copper foil area less than 3%).

(Note 5) The voltage difference between inverting input and non-inverting input is the differential input voltage. Then input terminal voltage is set to more than VEE.

(Note 6) Excessive input current will flow if a differential input voltage in excess of approximately ±0.6V is applied between the input unless some limiting resistance is used.

Caution: Operating the IC over the absolute maximum ratings may damage the IC. The damage can either be a short circuit between pins or an open circuit between pins and the internal circuitry. Therefore, it is important to consider circuit protection measures, such as adding a fuse, in case the IC is operated over the absolute maximum ratings.

Electrical Characteristics

○ BA8522Rxxx (Unless otherwise specified VCC=+15V, VEE=-15V, T_A=25°C)

Parameter	Symbol	Limits			Unit	Condition
		Min	Typ	Max		
Input Offset Voltage ^(Note 7)	V _{IO}	-	0.1	1.5	mV	-
Input Offset Voltage drift ^(Note 7)	V _{IO} /ΔT	-	2	-	μV/°C	-
Input Offset Current ^(Note 7)	I _{IO}	-	5	200	nA	-
Input Bias Current ^(Note 8)	I _B	-	50	500	nA	-
Supply Current	I _{CC}	-	5.5	9	mA	R _L =∞, All Op-Amps, +IN=0V
Maximum Output Voltage	V _{OM}	±12	±13.5	-	V	R _L ≥ 10kΩ
		±10.5	±11	-	V	R _L ≥ 2kΩ
Large Signal Voltage Gain	A _V	86	110	-	dB	R _L ≥ 10kΩ, OUT=±10V
Input Common-mode Voltage Range	V _{ICM}	±12	±14	-	V	-
Common-mode Rejection Ratio	CMRR	70	90	-	dB	-
Power Supply Rejection Ratio	PSRR	76.5	90	-	dB	-
Channel Separation	CS	-	105	-	dB	A _V =40dB, f=1kHz OUT=1Vrms
Slew Rate	SR	-	3	-	V/μs	R _L =2kΩ, C _L =100pF
Gain Bandwidth	GBW	-	6	-	MHz	f=500kHz
Input Referred Noise Voltage	V _N	-	1.2	-	μVrms	A _V =40dB, R _S =100Ω DIN-AUDIO
		-	9	-	nV/√Hz	A _V =40dB, R _S =100Ω, f=1kHz
Total Harmonic Distortion + Noise	THD+N	-	0.002	-	%	A _V =20dB, OUT=5Vrms f=1kHz, 80kHz-LPF
Channel Separation	CS	-	100	-	dB	OUT=0.5Vrms, f=1kHz A _V =40dB, Input referred

(Note 7) Absolute value

(Note 8) Current direction: Since first input stage is composed with PNP transistor, input bias current flows out of IC.

Description of Electrical Characteristics

Described below are descriptions of the relevant electrical terms used in this datasheet. Items and symbols used are also shown. Note that item name and symbol and their meaning may differ from those on another manufacturer's document or general document.

1. Absolute maximum ratings

Absolute maximum rating items indicate the condition which must not be exceeded. Application of voltage in excess of absolute maximum rating or use out of absolute maximum rated temperature environment may cause deterioration of characteristics.

- (1) Supply Voltage (VCC/VEE)
Indicates the maximum voltage that can be applied between the positive VCC terminal and VEE terminal without deterioration or destruction of characteristics of internal circuit.
- (2) Differential Input Voltage (V_{ID})
Indicates the maximum voltage that can be applied between non-inverting and inverting terminals without damaging the IC.
- (3) Input Common-mode Voltage Range (V_{ICM})
Indicates the maximum voltage that can be applied to the non-inverting and inverting terminals without deterioration or destruction of electrical characteristics. Input common-mode voltage range of the maximum ratings does not assure normal operation of IC. For normal operation, use the IC within the input common-mode voltage range characteristics.
- (4) Power Dissipation (P_D)
Indicates the power that can be consumed by the IC when mounted on a specific board at the ambient temperature 25°C (normal temperature). As for package product, P_D is determined by the temperature that can be permitted by the IC in the package (maximum junction temperature) and the thermal resistance of the package.

2. Electrical characteristics item

- (1) Input Offset Voltage (V_{IO})
Indicates the voltage difference between non-inverting terminal and inverting terminals. It can be translated into the input voltage difference required for setting the output voltage at 0 V.
- (2) Input Offset Voltage Drift ($\Delta V_{IO}/\Delta T$)
Denotes the ratio of the input offset voltage fluctuation to the ambient temperature fluctuation.
- (3) Input Offset Current (I_{IO})
Indicates the difference of input bias current between the non-inverting and inverting terminals.
- (4) Input Bias Current (I_B)
Indicates the current that flows into or out of the input terminal. It is defined by the average of input bias currents at the non-inverting and inverting terminals.
- (5) Supply Current (I_{CC})
Indicates the current that flows within the IC under specified no-load conditions.
- (6) Output Saturation Voltage (V_{OM})
Signifies the voltage range that can be output under specific output conditions.
- (7) Large Signal Voltage Gain (A_V)
Indicates the amplifying rate (gain) of output voltage against the voltage difference between non-inverting terminal and inverting terminal. It is normally the amplifying rate (gain) with reference to DC voltage.
 $A_v = (\text{Output Voltage}) / (\text{Differential Input Voltage})$
- (8) Input Common-mode Voltage Range (V_{ICM})
Indicates the input voltage range where IC normally operates.
- (9) Common-mode Rejection Ratio (CMRR)
Indicates the ratio of fluctuation of input offset voltage when the input common mode voltage is changed. It is normally the fluctuation of DC.
 $CMRR = (\text{Change of Input common-mode voltage}) / (\text{Input offset fluctuation})$
- (10) Power Supply Rejection Ratio (PSRR)
Indicates the ratio of fluctuation of input offset voltage when supply voltage is changed. It is normally the fluctuation of DC.
 $PSRR = (\text{Change of power supply voltage}) / (\text{Input offset fluctuation})$
- (11) Channel Separation (CS)
Indicates the fluctuation in the output voltage of the driven channel with reference to the change of output voltage of the channel which is not driven.
- (12) Slew Rate (SR)
Indicates the ratio of the change in output voltage with time when a step input signal is applied.
- (13) Gain Bandwidth (GBW)
The product of the open-loop voltage gain and the frequency at which the voltage gain decreases 6dB/octave.
- (14) Input Referred Noise Voltage (V_N)
Indicates a noise voltage generated inside the operational amplifier equivalent by ideal voltage source connected in series with input terminal.

- (15) Total Harmonic Distortion + Noise (THD+N)
Indicates the fluctuation of input offset voltage or that of output voltage with reference to the change of output voltage of driven channel.

Typical Performance Curves

○ BA8522Rxxx

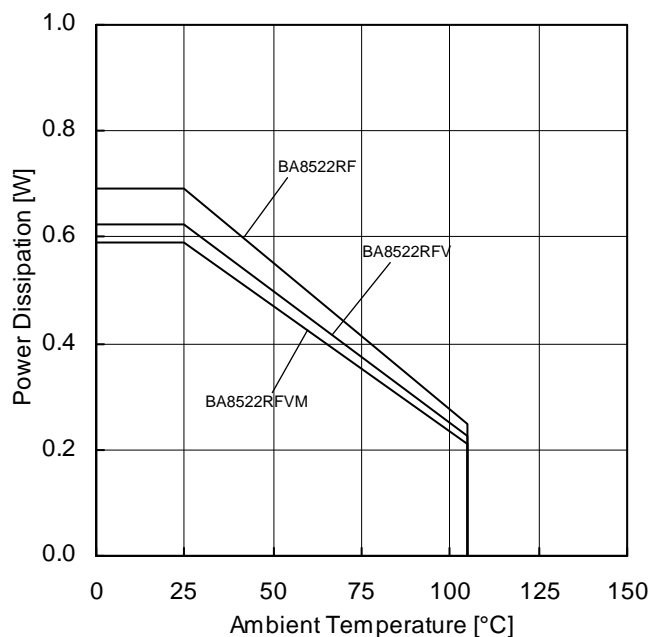


Figure 2.
Power Dissipation vs Ambient Temperature
(Derating Curve)

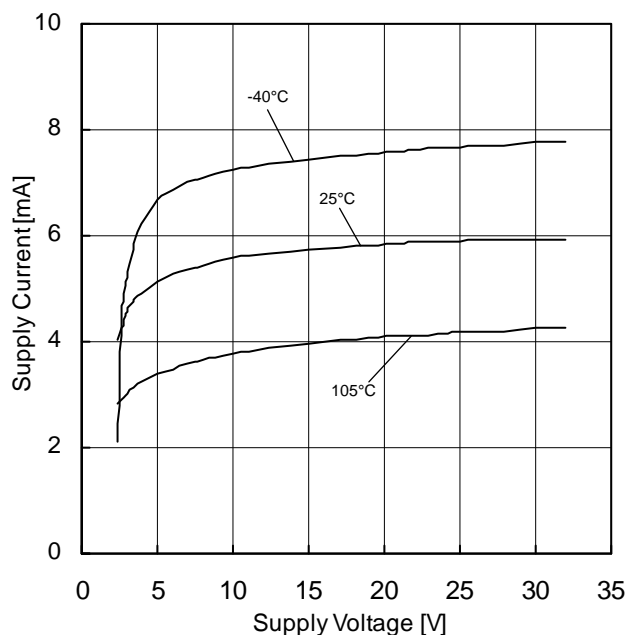


Figure 3.
Supply Current vs Supply Voltage

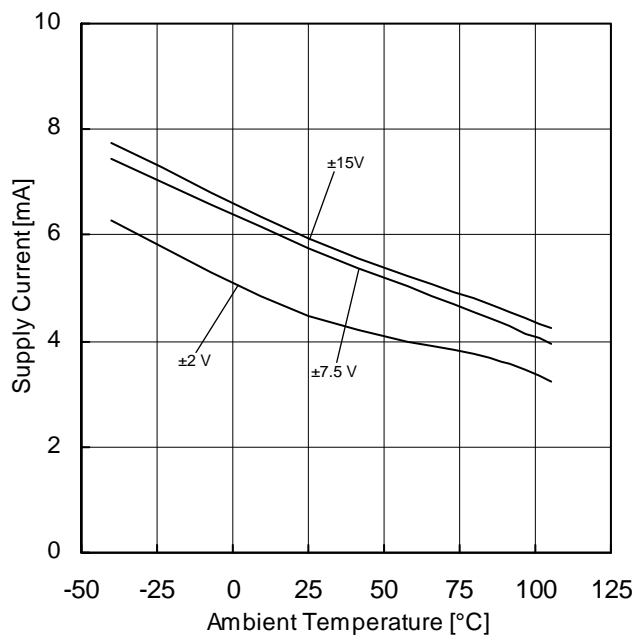


Figure 4.
Supply Current vs Ambient Temperature

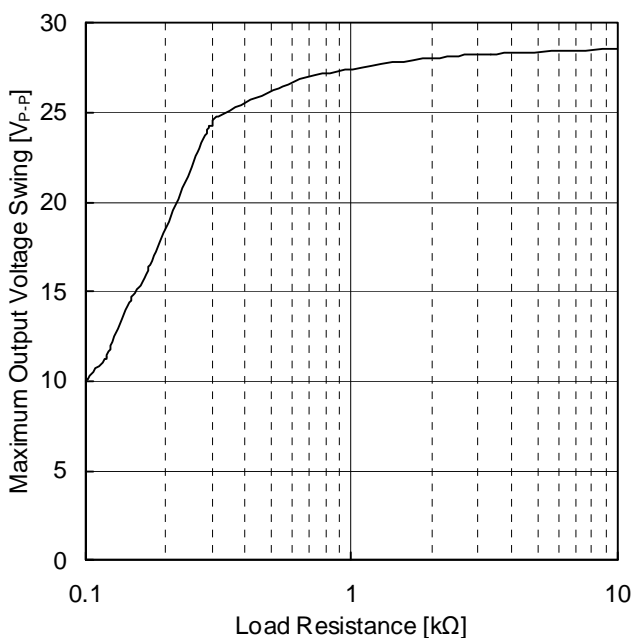


Figure 5.
Maximum Output Voltage Swing vs Load Resistance
(VCC/VEE=+15V/-15V, TA=25°C)

(*) The above data is measurement value of typical sample, it is not guaranteed.

Typical Performance Curves - continued

○ BA8522Rxxx

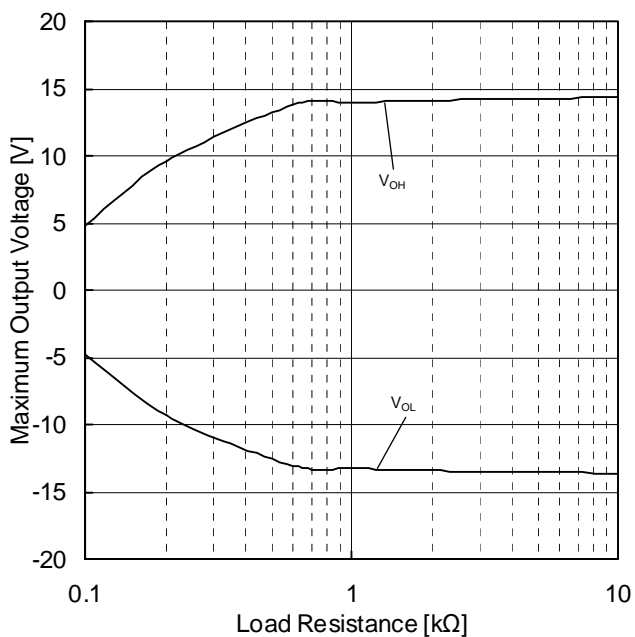


Figure 6.
Maximum Output Voltage vs Load Resistance
(VCC/VEE=+15V/-15V, T_A=25°C)

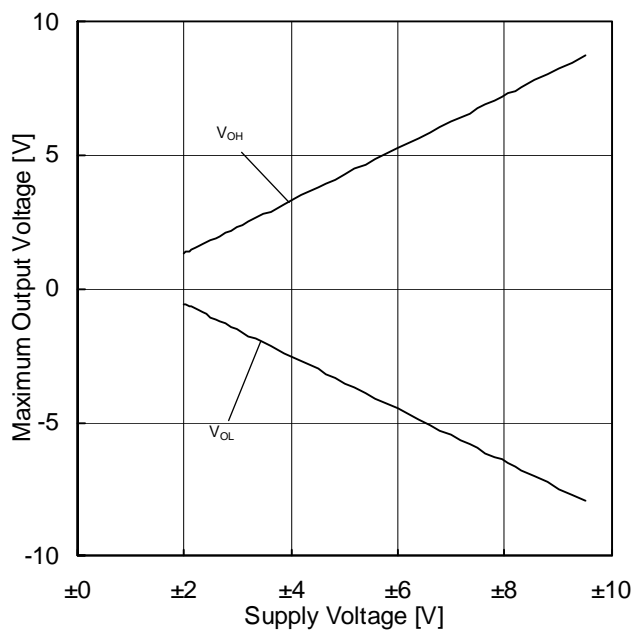


Figure 7.
Maximum Output Voltage vs Supply Voltage
(R_L=2kΩ, T_A=25°C)

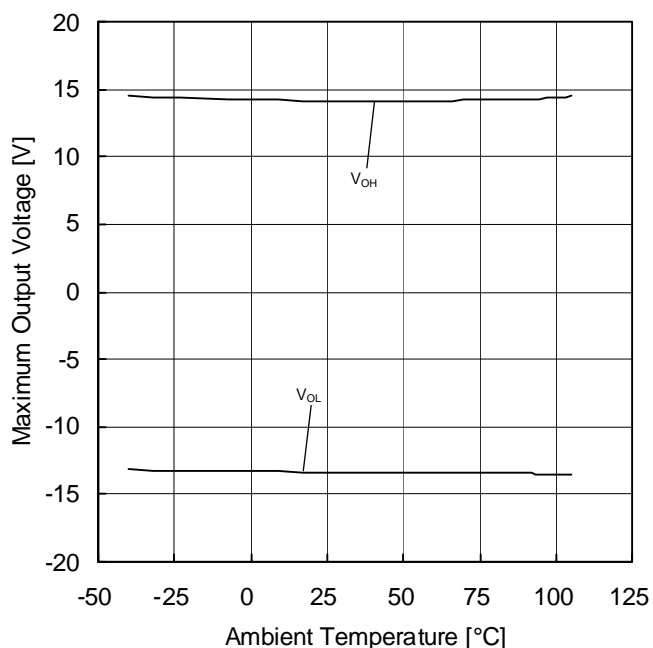


Figure 8.
Maximum Output Voltage vs Ambient Temperature
(VCC/VEE=+15V/-15V, R_L=2kΩ)

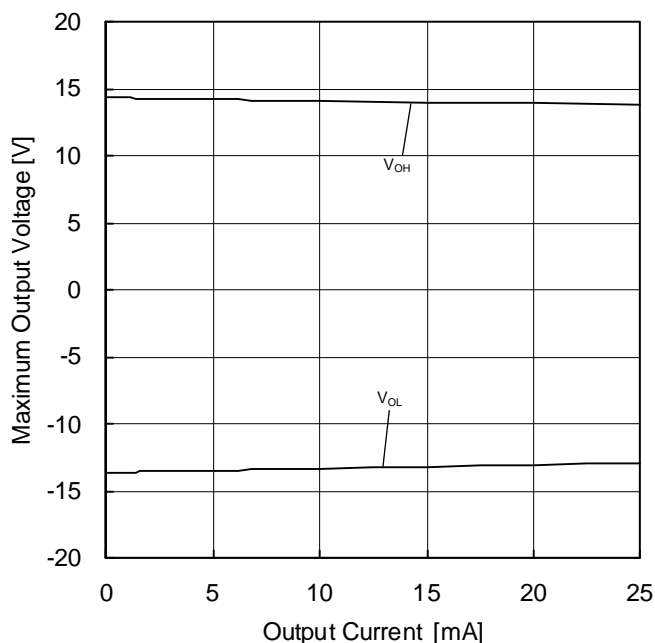


Figure 9.
Maximum Output Voltage vs Output Current
(VCC/VEE=+15V/-15V, T_A=25°C)

(*) The above data is measurement value of typical sample, it is not guaranteed.

Typical Performance Curves - continued

○ BA8522Rxxx

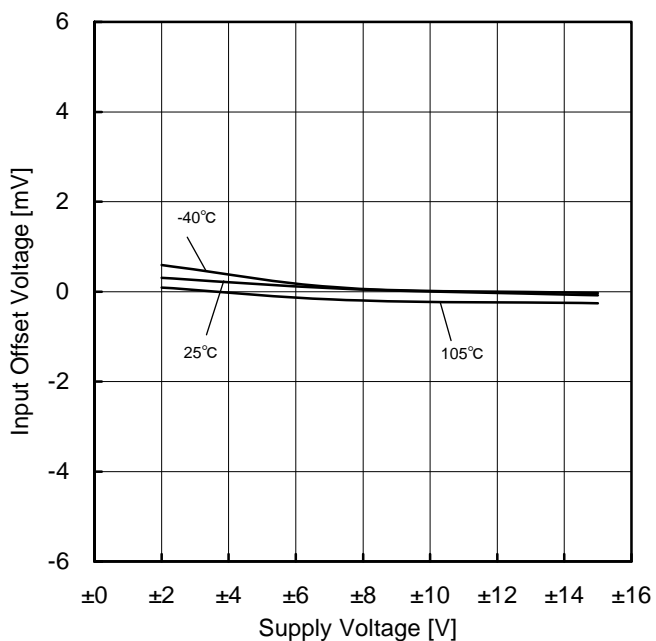


Figure 10.
Input Offset Voltage vs Supply Voltage
($V_{ICM}=0V, E_K=0V$)

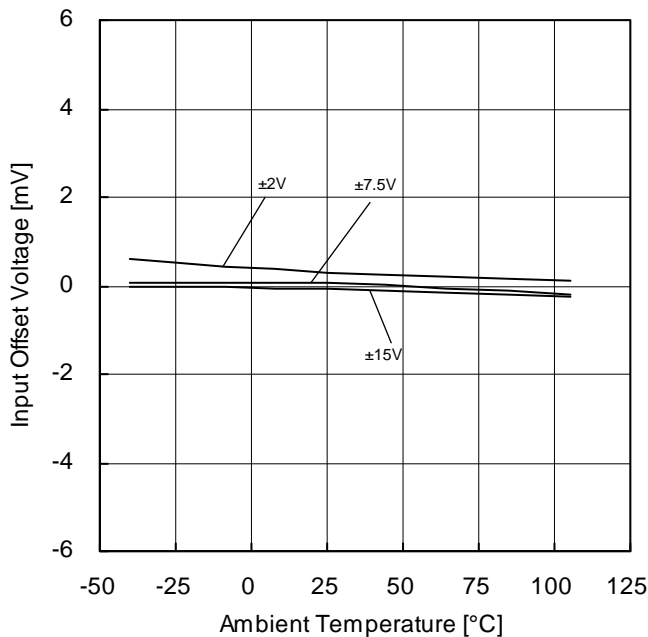


Figure 11.
Input Offset Voltage vs Ambient Temperature
($V_{ICM}=0V, E_K=0V$)

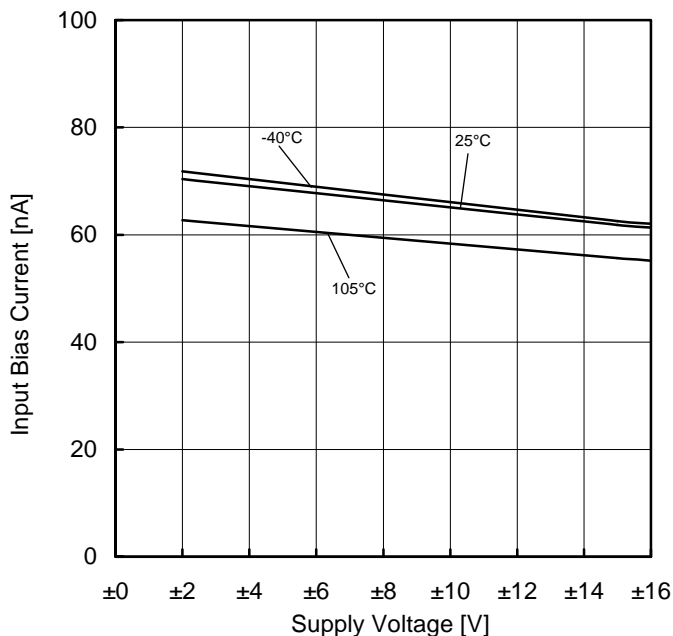


Figure 12.
Input Bias Current vs Supply Voltage
($V_{ICM}=0V, E_K=0V$)

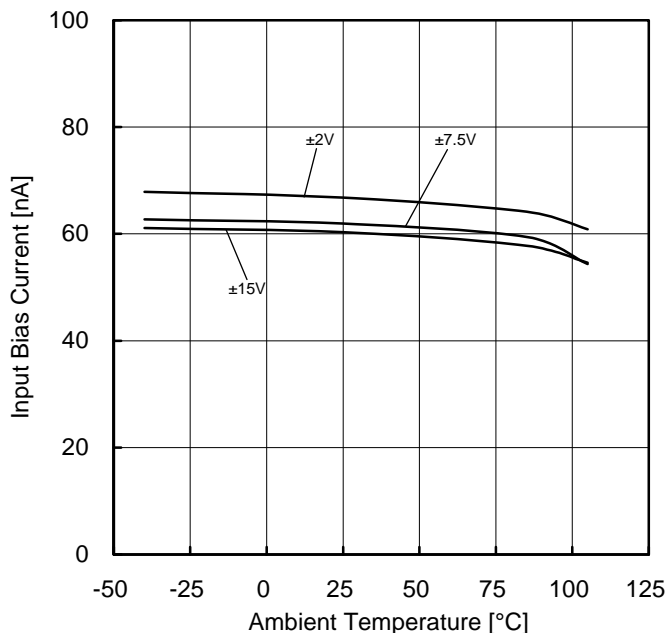


Figure 13.
Input Bias Current vs Ambient Temperature
($V_{ICM}=0V, E_K=0V$)

(*) The above data is measurement value of typical sample, it is not guaranteed.

Typical Performance Curves - continued

○ BA8522Rxxx

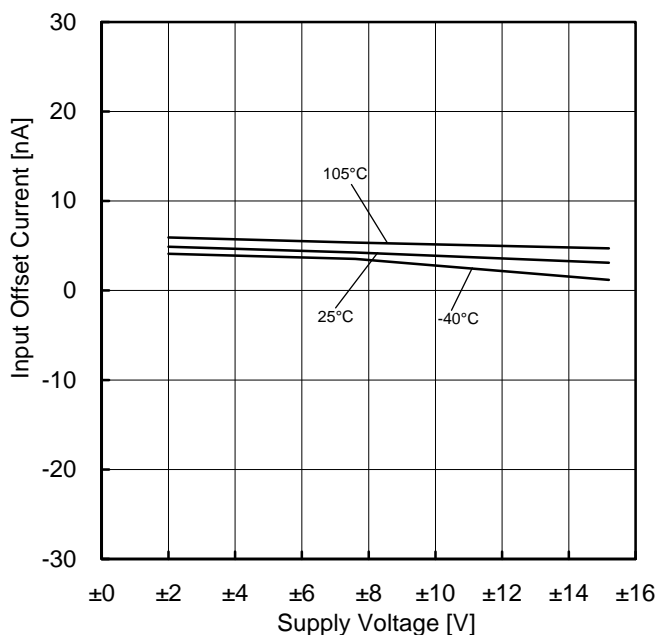


Figure 14.
Input Offset Current vs Supply Voltage
($V_{ICM}=0V$, $E_K=0V$)

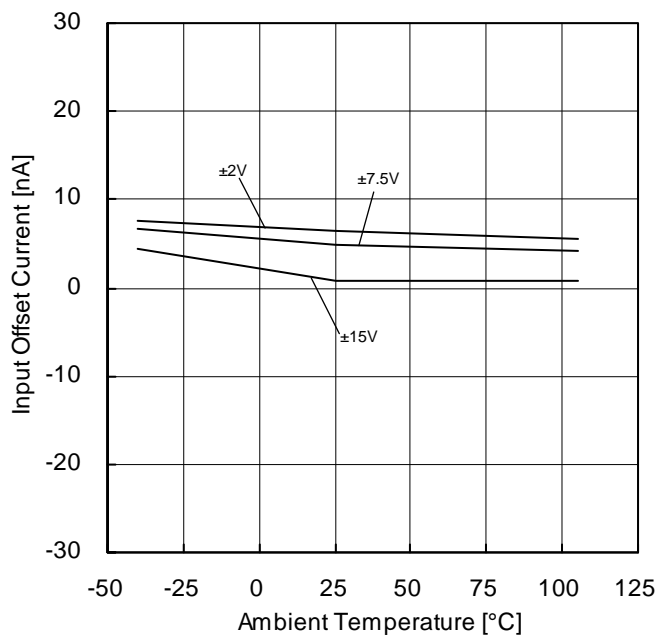


Figure 15.
Input Offset Current vs Ambient Temperature
($V_{ICM}=0V$, $E_K=0V$)

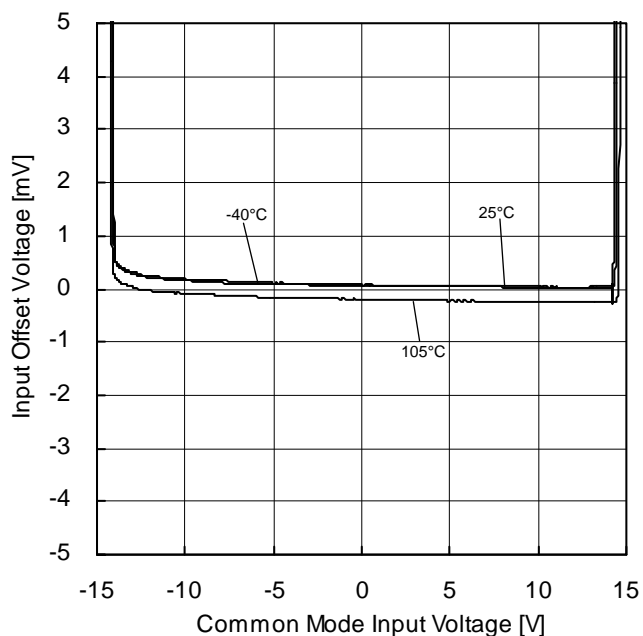


Figure 16.
Input Offset Voltage vs Common Mode Input Voltage
($V_{CC}=8V$, $E_K=-4V$)

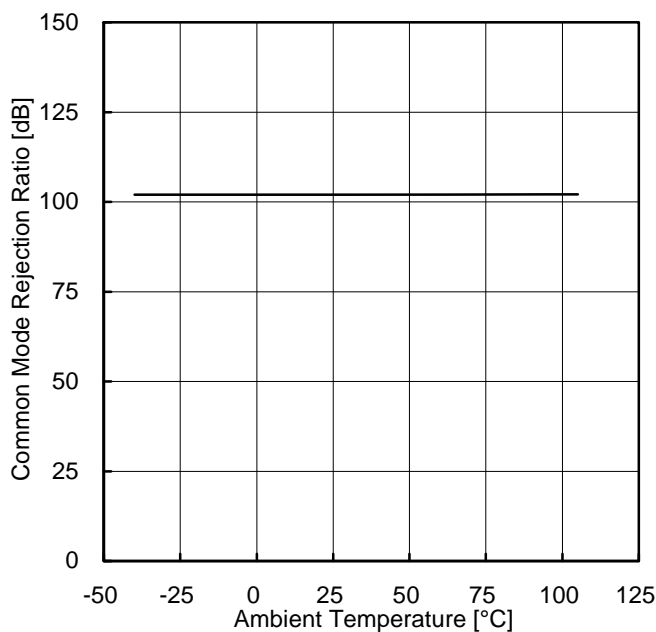


Figure 17.
Common Mode Rejection Ratio vs Ambient Temperature
($V_{CC}/V_{EE}=+15V/-15V$, $V_{ICM}=-12V$ to $+12V$)

(*) The above data is measurement value of typical sample, it is not guaranteed.

Typical Performance Curves - continued

○ BA8522Rxxx

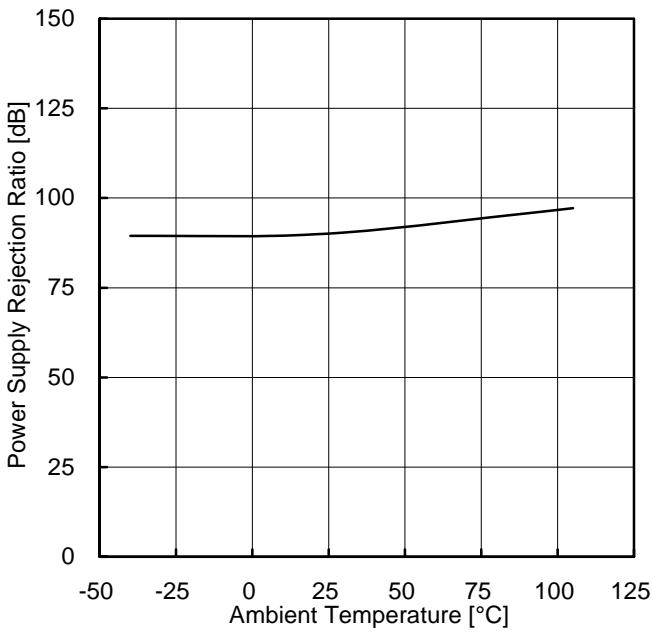


Figure 18.
Power Supply Rejection Ratio vs Ambient Temperature
(VCC/VEE=+2V/-2V to +15V/-15V)

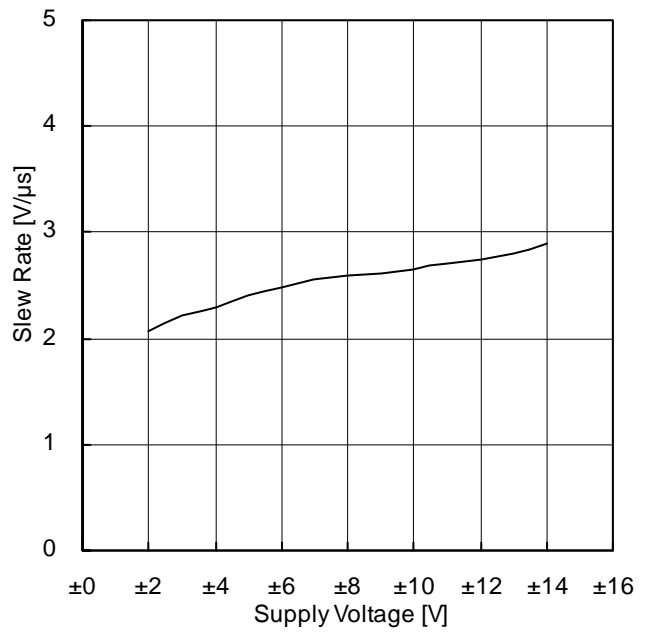


Figure 19.
Slew Rate vs Supply Voltage
(C_L=100pF, R_L=2kΩ, T_A=25°C)

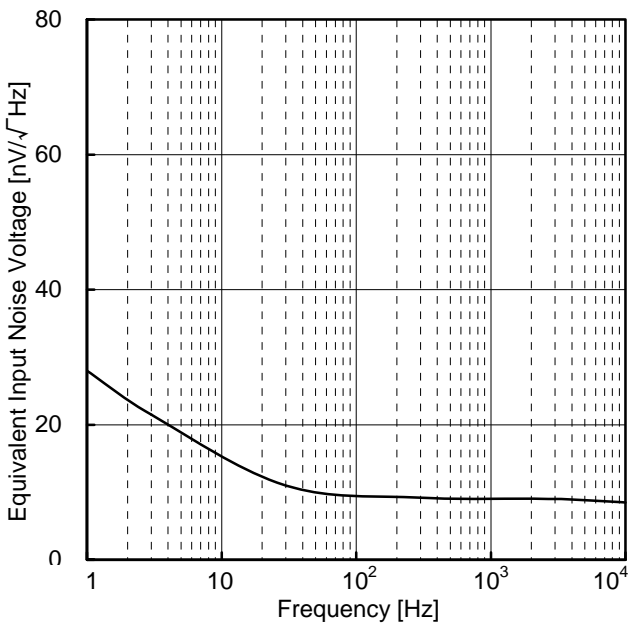


Figure 20.
Equivalent Input Noise Voltage vs Frequency
(VCC/VEE=+15V/-15V, R_S=100Ω, T_A=25°C)

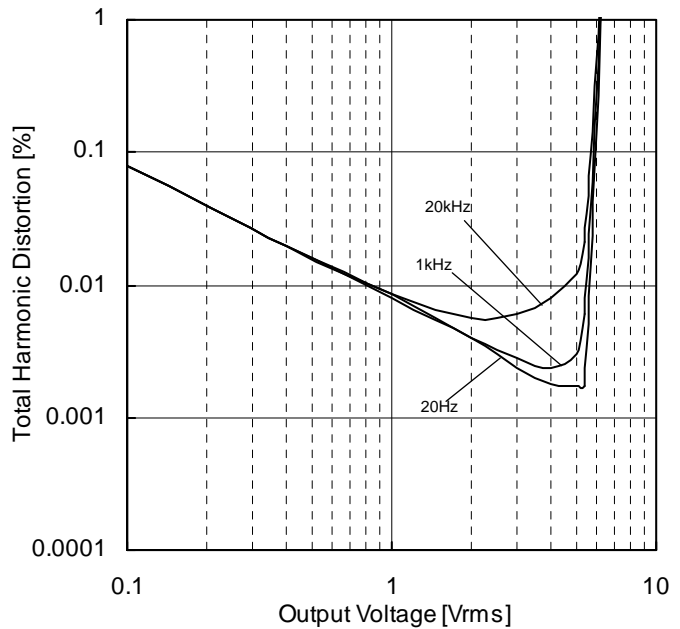


Figure 21.
Total Harmonic Distortion vs Output Voltage
(VCC/VEE=+15V/-15V, A_v=20dB, R_L=2kΩ, 80kHz-LPF, T_A=25°C)

(*) The above data is measurement value of typical sample, it is not guaranteed.

Typical Performance Curves - continued

○ BA8522Rxxx

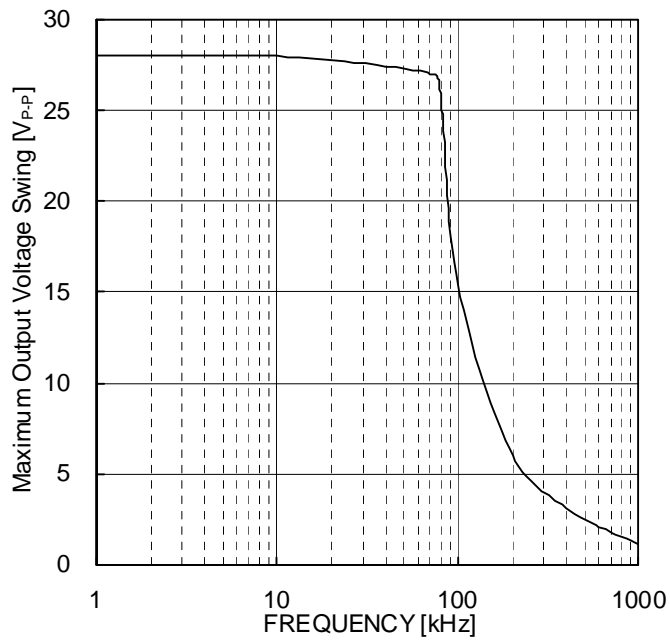


Figure 22.
Maximum Output Voltage Swing vs Frequency
(VCC/VEE=+15V/-15V, R_L=2kΩ, T_A=25°C)

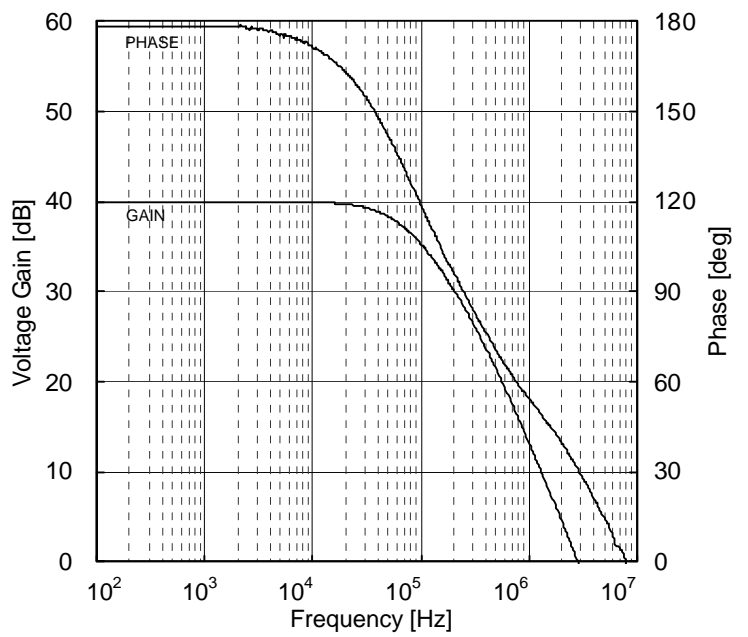


Figure 23.
Voltage Gain · Phase vs Frequency
(VCC/VEE=+15V/-15V, A_v=40dB, R_L=2kΩ, T_A=25°C)

(*) The above data is measurement value of typical sample, it is not guaranteed.

Application Information
NULL method condition for Test Circuit 1

VCC, VEE, E_K, V_{ICM} Unit: V

Parameter	V _F	SW1	SW2	SW3	VCC	VEE	E _K	V _{ICM}	Calculation
Input Offset Voltage	V _{F1}	ON	ON	OFF	15	-15	0	0	1
Input Offset Current	V _{F2}	OFF	OFF	OFF	15	-15	0	0	2
Input Bias Current	V _{F3}	OFF	ON	OFF	15	-15	0	0	3
	V _{F4}	ON	OFF						
Large Signal Voltage Gain	V _{F5}	ON	ON	ON	15	-15	10	0	4
	V _{F6}				15	-15	-10	0	
Common-Mode Rejection Ratio (Input Common-Mode Voltage Range)	V _{F7}	ON	ON	OFF	15	-15	0	-12	5
	V _{F8}				15	-15	0	12	
Power Supply Rejection Ratio	V _{F9}	ON	ON	OFF	2	-2	0	0	6
	V _{F10}				16	-16	0	0	

- Calculation -

1. Input Offset Voltage (V_{IO})

$$V_{IO} = \frac{|V_{F1}|}{1 + R_F/R_S} \quad [V]$$

2. Input Offset Current (I_{IO})

$$I_{IO} = \frac{|V_{F2} - V_{F1}|}{R_i \times (1 + R_F/R_S)} \quad [A]$$

3. Input Bias Current (I_B)

$$I_B = \frac{|V_{F4} - V_{F3}|}{2 \times R_i \times (1 + R_F/R_S)} \quad [A]$$

4. Large Signal Voltage Gain (A_v)

$$A_v = 20 \text{Log} \frac{\Delta E_K \times (1 + R_F/R_S)}{|V_{F6} - V_{F5}|} \quad [\text{dB}]$$

5. Common-mode Rejection Ratio (CMRR)

$$\text{CMRR} = 20 \text{Log} \frac{\Delta V_{ICM} \times (1 + R_F/R_S)}{|V_{F8} - V_{F7}|} \quad [\text{dB}]$$

6. Power supply rejection ratio (PSRR)

$$\text{PSRR} = 20 \text{Log} \frac{\Delta V_{CC} \times (1 + R_F/R_S)}{|V_{F10} - V_{F9}|} \quad [\text{dB}]$$

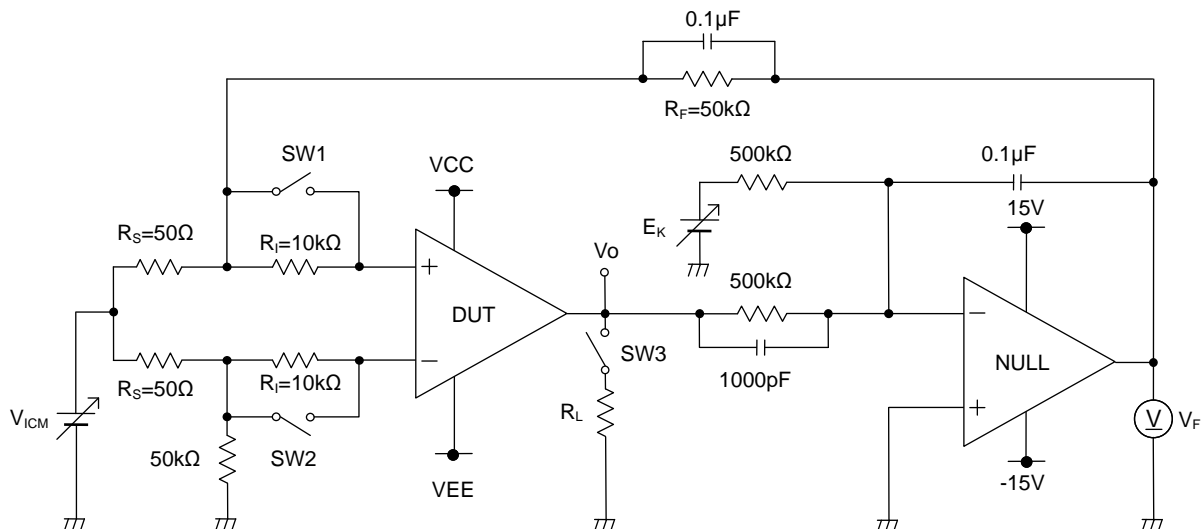


Figure 24. Test circuit1 (one channel only)

Switch Condition for Test Circuit 2

SW No.	SW1	SW2	SW3	SW4	SW5	SW6	SW7	SW8	SW9	SW10	SW11	SW12
Supply Current	OFF	OFF	OFF	ON	OFF	ON	OFF	OFF	OFF	OFF	OFF	OFF
Maximum Output Voltage	OFF	OFF	ON	OFF	OFF	OFF	ON	OFF	ON	OFF	OFF	ON
Slew Rate	OFF	OFF	OFF	ON	OFF	OFF	OFF	ON	ON	ON	OFF	OFF
Gain Bandwidth	OFF	ON	OFF	OFF	ON	ON	OFF	OFF	ON	ON	ON	OFF
Input Referred Noise Voltage	ON	OFF	OFF	OFF	ON	ON	OFF	OFF	OFF	OFF	ON	OFF

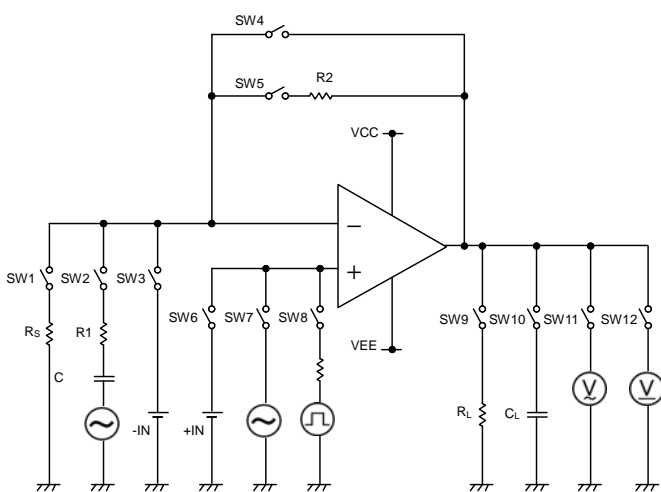


Figure 25. Test Circuit 2 (each channel)

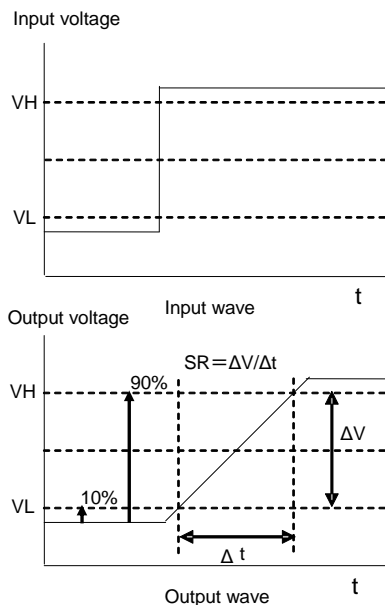


Figure 26. Slew Rate Input Waveform

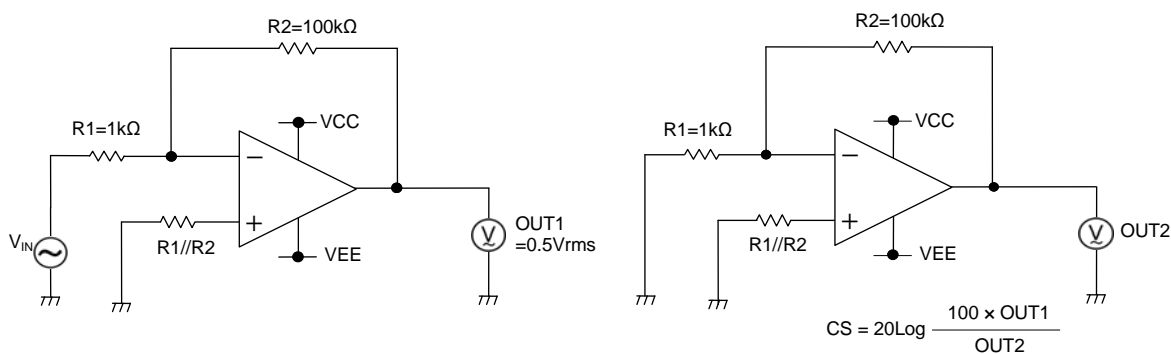


Figure 27. Test Circuit 3(Channel Separation)

Power Dissipation

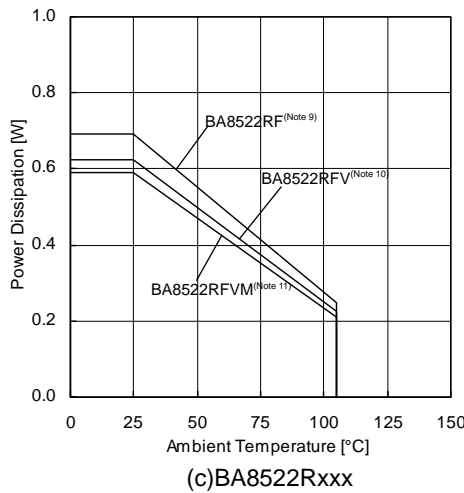
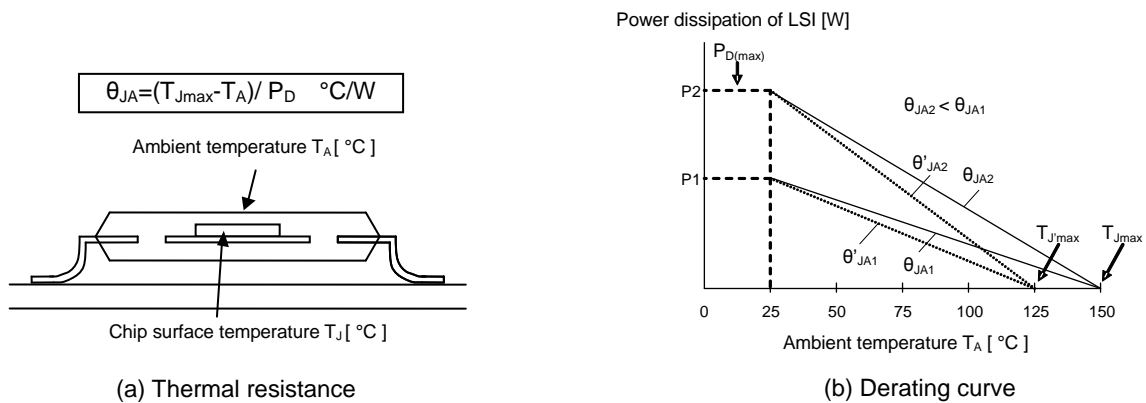
Power dissipation (total loss) indicates the power that the IC can consume at $T_A=25^\circ\text{C}$ (normal temperature). As the IC consumes power, it heats up, causing its temperature to be higher than the ambient temperature. The allowable temperature that the IC can accept is limited. This depends on the circuit configuration, manufacturing process, and consumable power.

Power dissipation is determined by the allowable temperature within the IC (maximum junction temperature) and the thermal resistance of the package used (heat dissipation capability). Maximum junction temperature is typically equal to the maximum storage temperature. The heat generated through the consumption of power by the IC radiates from the mold resin or lead frame of the package. Thermal resistance, represented by the symbol θ_{JA} $^\circ\text{C}/\text{W}$, indicates this heat dissipation capability. Similarly, the temperature of an IC inside its package can be estimated by thermal resistance.

Figure 28(a) shows the model of the thermal resistance of a package. The equation below shows how to compute for the Thermal resistance (θ_{JA}), given the ambient temperature (T_A), maximum junction temperature (T_{Jmax}), and power dissipation (P_D).

$$\theta_{JA} = (T_{Jmax} - T_A) / P_D \quad ^\circ\text{C}/\text{W}$$

The Derating curve in Figure 28(b) indicates the power that the IC can consume with reference to ambient temperature. Power consumption of the IC begins to attenuate at certain temperatures. This gradient is determined by Thermal resistance (θ_{JA}), which depends on the chip size, power consumption, package, ambient temperature, package condition, wind velocity, etc. This may also vary even when the same of package is used. Thermal reduction curve indicates a reference value measured at a specified condition. Figure 28(c) shows an example of the derating curve for BA8522Rxxx.



(Note 9)	(Note 10)	(Note 11)	Unit
5.5	5.0	4.7	mW/°C

When using the unit above $T_A=25^\circ\text{C}$, subtract the value above per degree $^\circ\text{C}$.
 Permissible dissipation is the value when FR4 glass epoxy board 70mm x70mm x1.6mm (copper foil area less than 3%) is mounted.

Figure 28. Thermal Resistance and Derating Curve

Examples of Circuit

○Voltage Follower

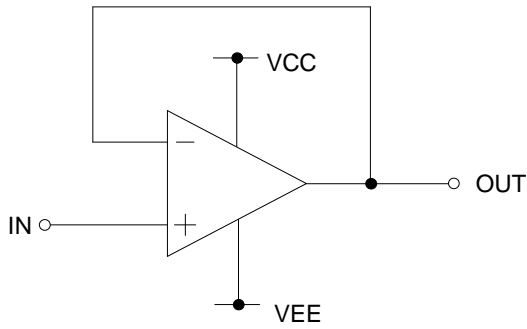


Figure 29. Voltage Follower Circuit

Voltage gain is 0dB.

Using this circuit, the output voltage (OUT) is configured to be equal to the input voltage (IN). This circuit also stabilizes the output voltage (OUT) due to high input impedance and low output impedance. Computation for output voltage (OUT) is shown below.

$$OUT=IN$$

○Inverting Amplifier

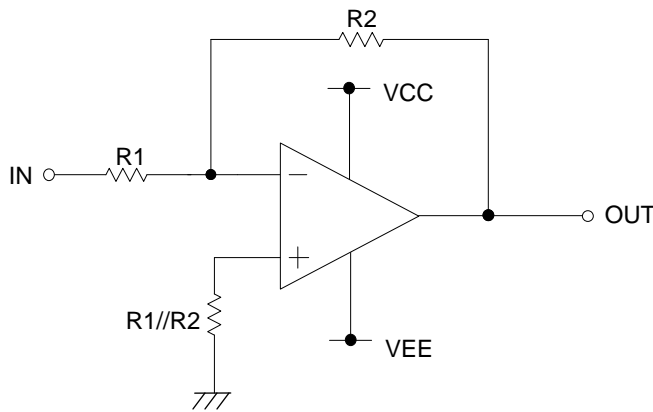


Figure 30. Inverting Amplifier Circuit

For inverting amplifier, input voltage (IN) is amplified by a voltage gain and depends on the ratio of R1 and R2. The out-of-phase output voltage is shown in the next expression

$$OUT=-\left(\frac{R2}{R1}\right) \cdot IN$$

This circuit has input impedance equal to R1.

○Non-inverting Amplifier

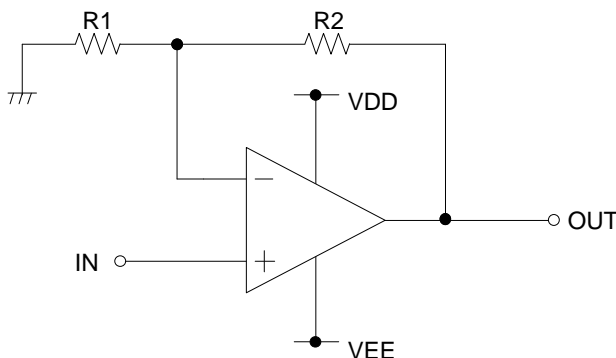


Figure 31. Non-inverting Amplifier Circuit

For non-inverting amplifier, input voltage (IN) is amplified by a voltage gain, which depends on the ratio of R1 and R2. The output voltage (OUT) is in-phase with the input voltage (IN) and is shown in the next expression.

$$OUT=\left(1 + \frac{R2}{R1}\right) \cdot IN$$

Effectively, this circuit has high input impedance since its input side is the same as that of the operational amplifier.

Operational Notes

1. Reverse Connection of Power Supply

Connecting the power supply in reverse polarity can damage the IC. Take precautions against reverse polarity when connecting the power supply, such as mounting an external diode between the power supply and the IC's power supply pins.

2. Power Supply Lines

Design the PCB layout pattern to provide low impedance supply lines. Separate the ground and supply lines of the digital and analog blocks to prevent noise in the ground and supply lines of the digital block from affecting the analog block. Furthermore, connect a capacitor to ground at all power supply pins. Consider the effect of temperature and aging on the capacitance value when using electrolytic capacitors.

3. Ground Voltage

Ensure that no pins are at a voltage below that of the ground pin at any time, even during transient condition.

4. Ground Wiring Pattern

When using both small-signal and large-current ground traces, the two ground traces should be routed separately but connected to a single ground at the reference point of the application board to avoid fluctuations in the small-signal ground caused by large currents. Also ensure that the ground traces of external components do not cause variations on the ground voltage. The ground lines must be as short and thick as possible to reduce line impedance.

5. Thermal Consideration

Should by any chance the power dissipation rating be exceeded the rise in temperature of the chip may result in deterioration of the properties of the chip. The absolute maximum rating of the P_D stated in this specification is when the IC is mounted on a 70mm x 70mm x 1.6mm glass epoxy board. In case of exceeding this absolute maximum rating, increase the board size and copper area to prevent exceeding the P_D rating.

6. Recommended Operating Conditions

These conditions represent a range within which the expected characteristics of the IC can be approximately obtained. The electrical characteristics are guaranteed under the conditions of each parameter.

7. Inrush Current

When power is first supplied to the IC, it is possible that the internal logic may be unstable and inrush current may flow instantaneously due to the internal powering sequence and delays, especially if the IC has more than one power supply. Therefore, give special consideration to power coupling capacitance, power wiring, width of ground wiring, and routing of connections.

8. Operation Under Strong Electromagnetic Field

Operating the IC in the presence of a strong electromagnetic field may cause the IC to malfunction.

9. Testing on Application Boards

When testing the IC on an application board, connecting a capacitor directly to a low-impedance output pin may subject the IC to stress. Always discharge capacitors completely after each process or step. The IC's power supply should always be turned off completely before connecting or removing it from the test setup during the inspection process. To prevent damage from static discharge, ground the IC during assembly and use similar precautions during transport and storage.

10. Inter-pin Short and Mounting Errors

Ensure that the direction and position are correct when mounting the IC on the PCB. Incorrect mounting may result in damaging the IC. Avoid nearby pins being shorted to each other especially to ground, power supply and output pin. Inter-pin shorts could be due to many reasons such as metal particles, water droplets (in very humid environment) and unintentional solder bridge deposited in between pins during assembly to name a few.

11. Regarding the Input Pin of the IC

This monolithic IC contains P+ isolation and P substrate layers between adjacent elements in order to keep them isolated. P-N junctions are formed at the intersection of the P layers with the N layers of other elements, creating a parasitic diode or transistor. For example (refer to figure 32):

When $GND > Pin A$ and $GND > Pin B$, the P-N junction operates as a parasitic diode.

When $GND > Pin B$, the P-N junction operates as a parasitic transistor.

Operational Notes – continued

Parasitic diodes inevitably occur in the structure of the IC. The operation of parasitic diodes can result in mutual interference among circuits, operational faults, or physical damage. Therefore, conditions that cause these diodes to operate, such as applying a voltage lower than the GND voltage to an input pin (and thus to the P substrate) should be avoided.

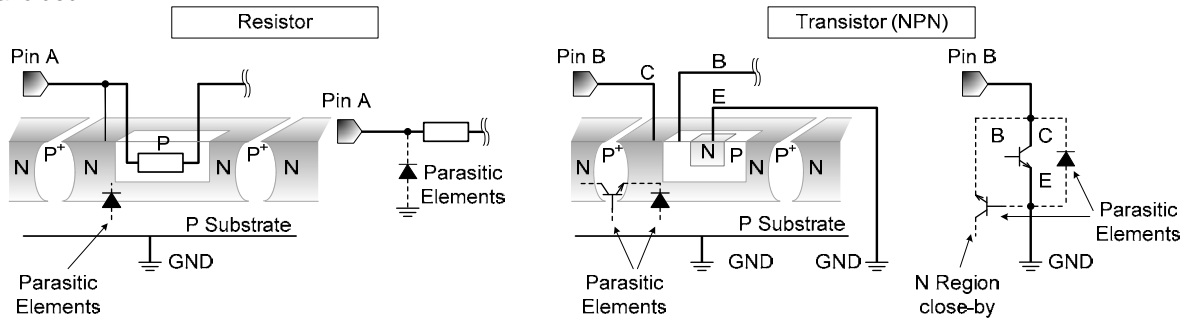


Figure 32. Example of monolithic IC structure

12. Unused circuits

When there are unused op-amps, it is recommended that they are connected as in Figure 33, setting the non-inverting input terminal to a potential within the in-phase input voltage range (V_{ICM}).

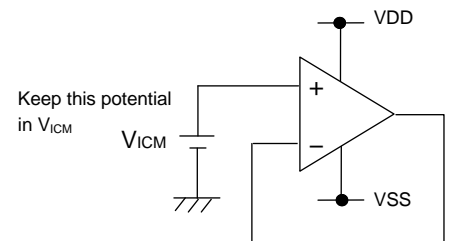


Figure 33. Example of Application Circuit for Unused Op-amp

13. Input Voltage

Applying VEE +36V to the input terminal is possible without causing deterioration of the electrical characteristics or destruction, regardless of the supply voltage. However, this does not ensure normal circuit operation. Please note that the circuit operates normally only when the input voltage is within the common mode input voltage range of the electric characteristics.

14. Power supply(single/dual)

The op-amp operates when the voltage supplied is between VCC and VEE. Therefore, the single supply op-amp can be used as dual supply op-amp as well.

15. Output capacitor

If a large capacitor is connected between the output pin and VEE pin, current from the charged capacitor will flow into the output pin and may destroy the IC when the VCC pin is shorted to ground or pulled down to 0V. Use a capacitor smaller than 0.1uF between output pin and VEE pin.

16. Oscillation by output capacitor

Please pay attention to the oscillation by output capacitor and in designing an application of negative feedback loop circuit with these ICs.

17. Short-circuit of Output Terminal

When output terminal and VCC or VEE terminal are shorted, excessive Output current may flow under some conditions, and heating may destroy IC. It is necessary to connect a resistor as shown in Figure 34. , thereby protecting against load shorting.

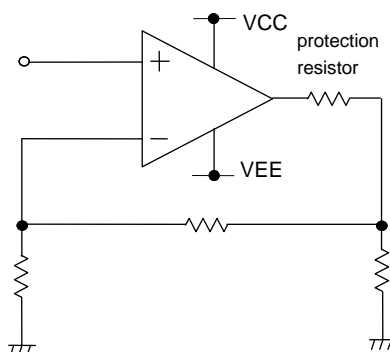
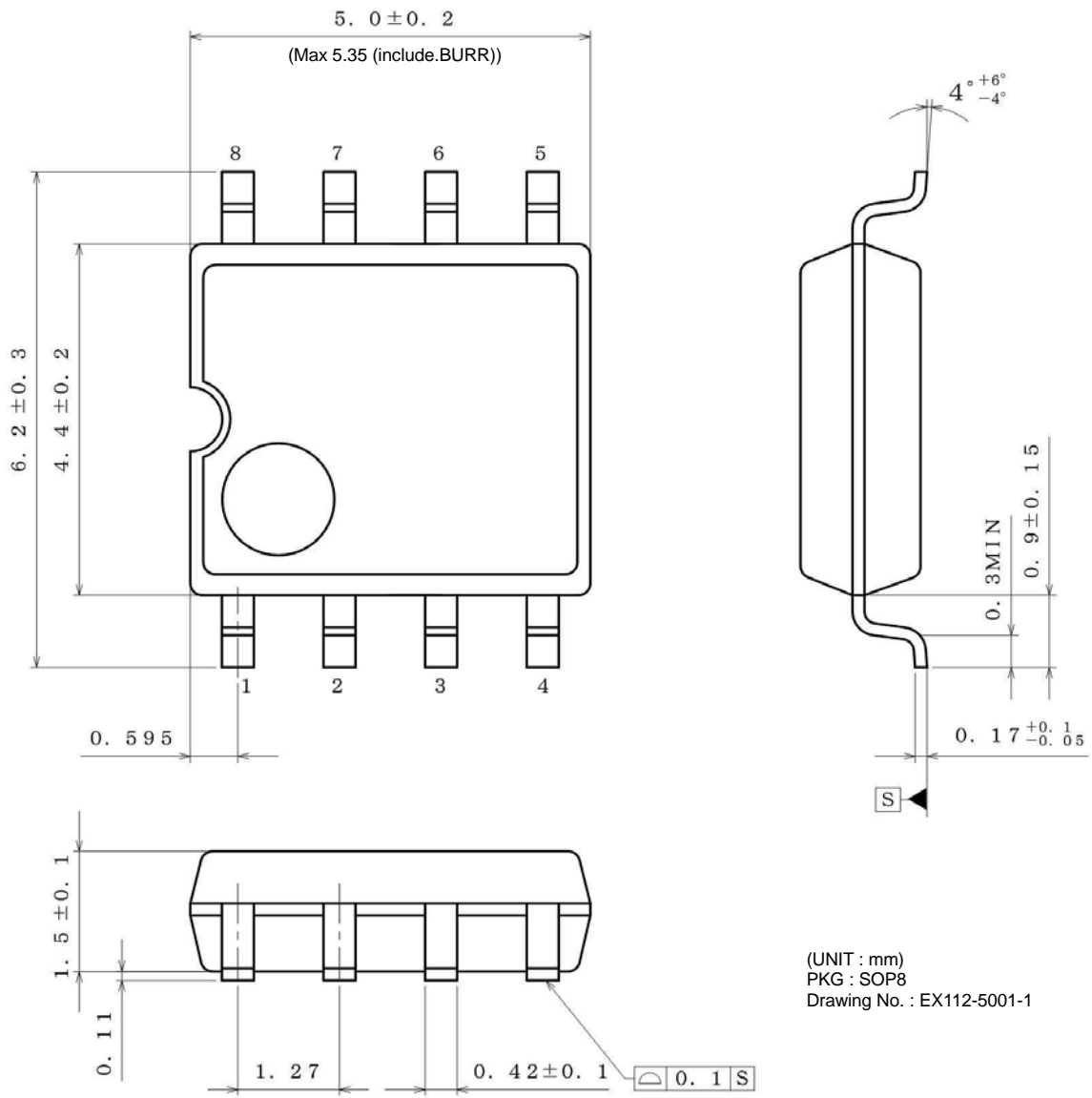


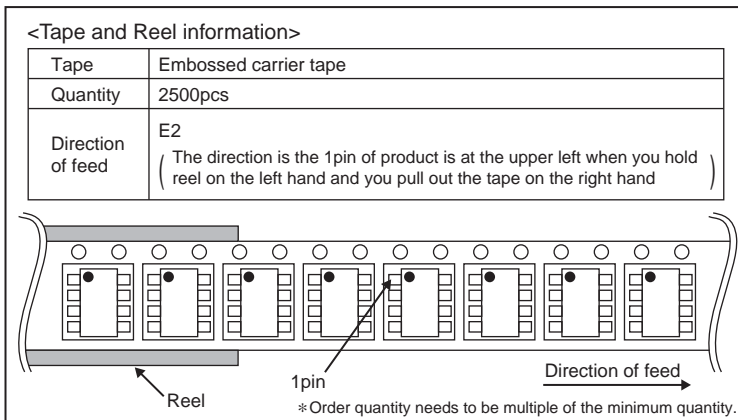
Figure 34. The Example of Output Short Protection

Physical Dimensions Tape and Reel Information

Package Name	SOP8
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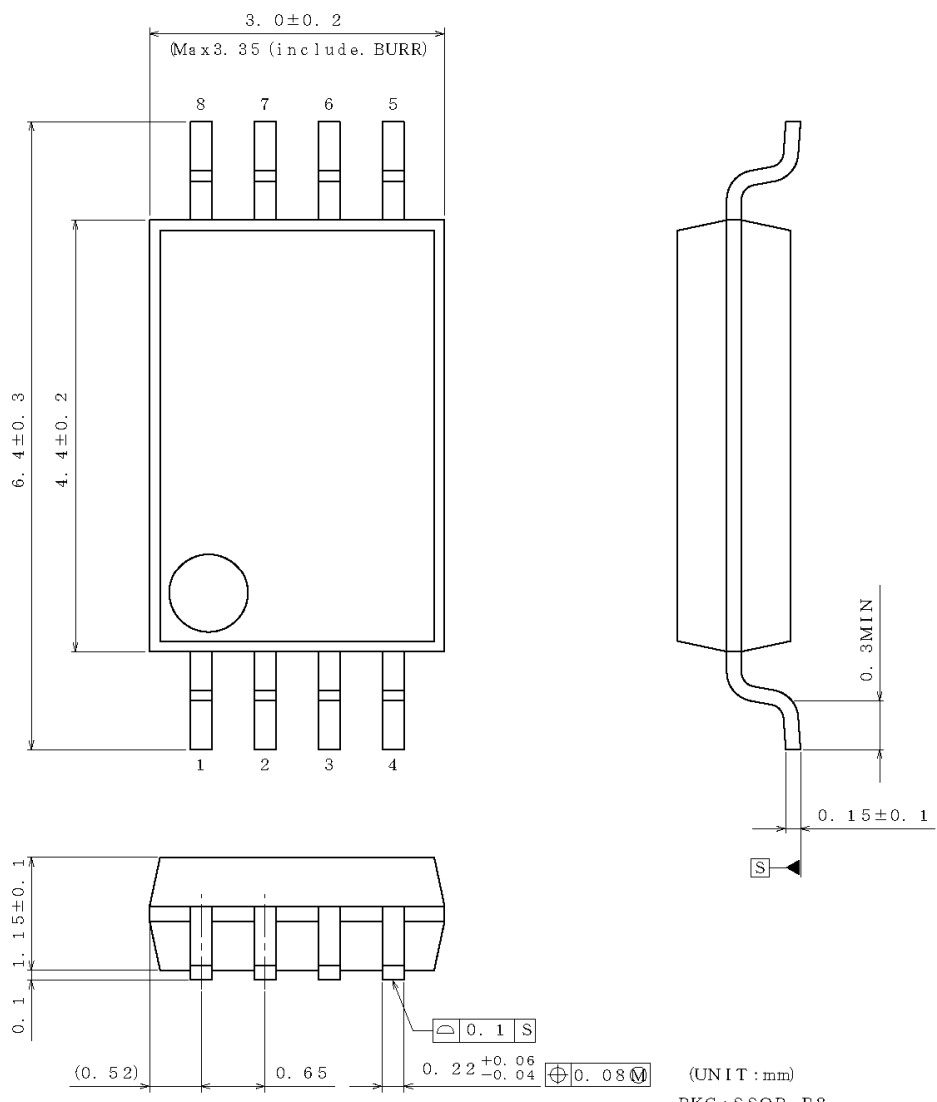


(UNIT : mm)
 PKG : SOP8
 Drawing No. : EX112-5001-1



Physical Dimension, Tape and Reel Information – continued

Package Name	SSOP-B8
--------------	---------



PKG : SSOP-B8
 Drawing No. EX151-5002

<Tape and Reel information>

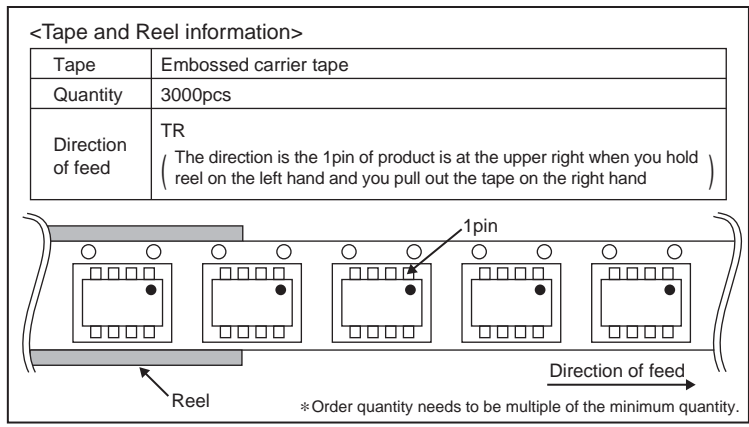
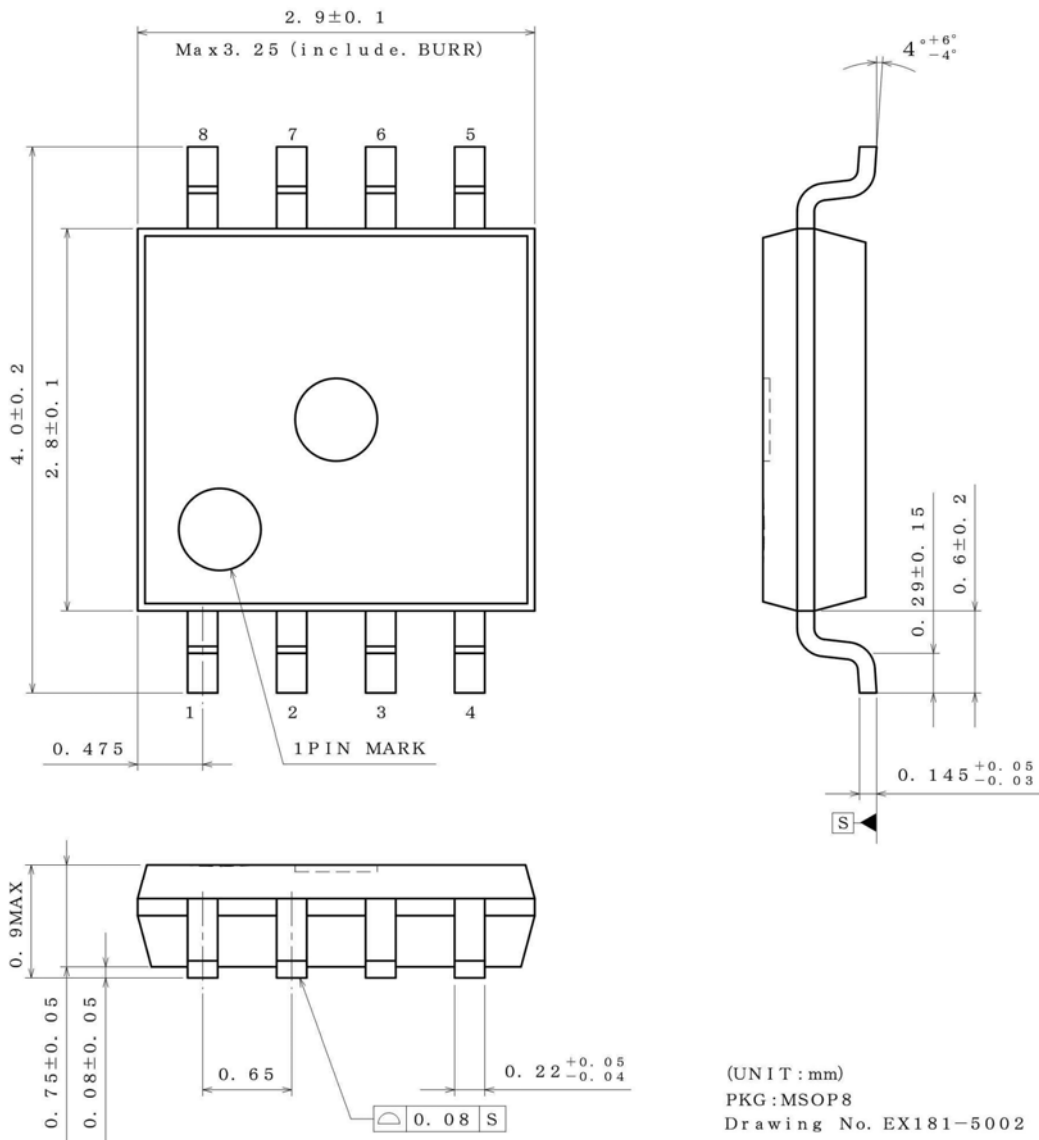
Tape	Embossed carrier tape
Quantity	2500pcs
Direction of feed	E2 (The direction is the 1pin of product is at the upper left when you hold reel on the left hand and you pull out the tape on the right hand)

Reel → 1pin → Direction of feed →

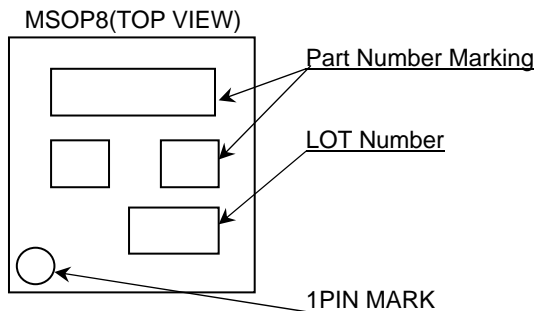
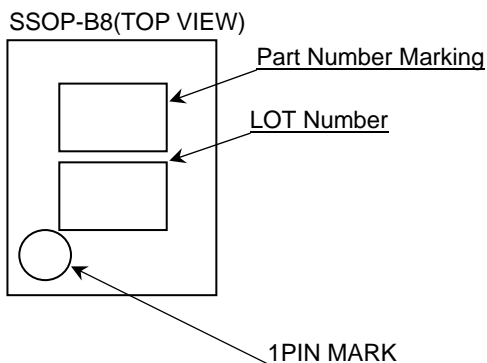
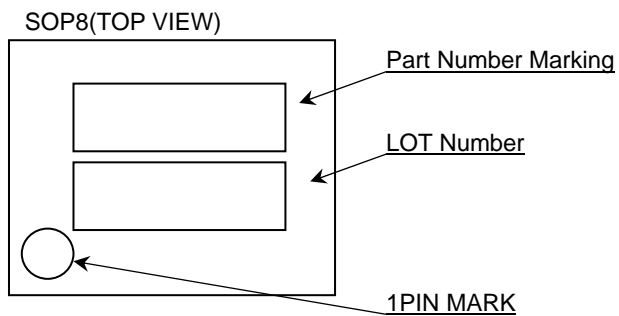
* Order quantity needs to be multiple of the minimum quantity.

Physical Dimension, Tape and Reel Information – continued

Package Name	MSOP8
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Marking Diagrams

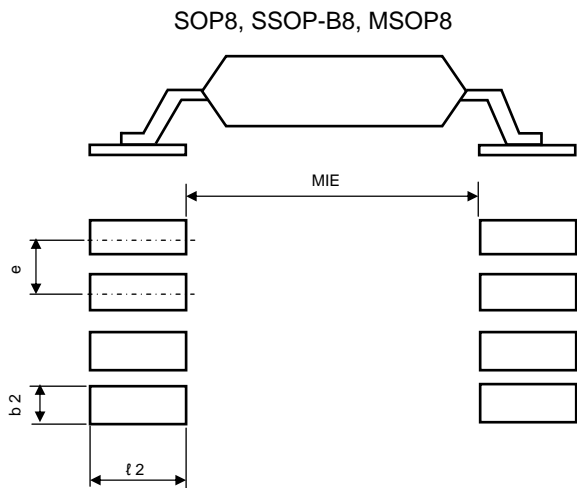


Product Name		Package Type	Marking
BA8522R	F	SOP8	8522R
	FV	SSOP-B8	
	FVM	MSOP8	

Land pattern data

All dimensions in mm

PKG	Land pitch e	Land space MIE	Land length $\geq l_2$	Land width b2
SOP8	1.27	4.60	1.10	0.76
SSOP-B8	0.65	4.60	1.20	0.35
MSOP8	0.65	2.62	0.99	0.35



Revision History

Date	Revision	Changes
13.Sep.2013	001	New Release

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JAPAN	USA	EU	CHINA
CLASS III	CLASS III	CLASS II b	CLASS III
CLASS IV		CLASS III	

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 - Use of the Products in places subject to dew condensation
- The Products are not subject to radiation-proof design.
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 - [d] the Products are exposed to high Electrostatic
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4. Use Products within the specified time after opening a humidity barrier bag. Baking is required before using Products of which storage time is exceeding the recommended storage time period.

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