1 nV/√Hz Low Noise Instrumentation Amplifier

Data Sheet

AD8429

FEATURES

- **Low noise**
  - **1 nV/√Hz input noise**
  - **45 nV/√Hz output noise**
- **High accuracy dc performance (AD8429BRZ)**
  - **90 dB CMRR minimum (G = 1)**
  - **50 µV maximum input offset voltage**
  - **0.02% maximum gain accuracy (G = 1)**
- **Excellent ac specifications**
  - **80 dB CMRR to 5 kHz (G = 1)**
  - **15 MHz bandwidth (G = 1)**
  - **1.2 MHz bandwidth (G = 100)**
  - **22 V/µs slew rate**
  - **THD: −130 dBc (1 kHz, G = 1)**
- **Versatile**
  - **±4 V to ±18 V dual supply**
  - **Gain set with a single resistor (G = 1 to 10,000)**
- **Temperature range for specified performance**
  - **−40°C to +125°C**

APPLICATIONS

Medical instrumentation
Precision data acquisition
Microphone preamplification
Vibration analysis

PIN CONNECTION DIAGRAM

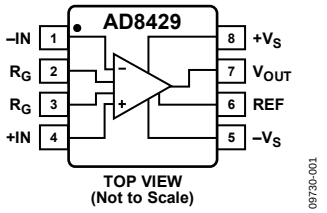

Figure 1.

GENERAL DESCRIPTION

The AD8429 is an ultralow noise, instrumentation amplifier designed for measuring extremely small signals over a wide temperature range (−40°C to +125°C).

The AD8429 excels at measuring tiny signals. It delivers ultralow input noise performance of 1 nV/√Hz. The high CMRR of the AD8429 prevents unwanted signals from corrupting the acquisition. The CMRR increases as the gain increases, offering high rejection when it is most needed. The high performance pin configuration of the AD8429 allows it to reliably maintain high CMRR at frequencies well beyond those of typical instrumentation amplifiers.

The AD8429 reliably amplifies fast changing signals. Its current feedback architecture provides high bandwidth at high gain, for example, 1.2 MHz at G = 100. The design includes circuitry to improve settling time after large input voltage transients. The AD8429 was designed for excellent distortion performance, allowing use in demanding applications such as vibration analysis.

Gain is set from 1 to 10,000 with a single resistor. A reference pin allows the user to offset the output voltage. This feature can be useful to shift the output level when interfacing to a single supply signal chain.

The AD8429 performance is specified over the extended industrial temperature range of −40°C to +125°C. It is available in an 8-lead plastic SOIC package.

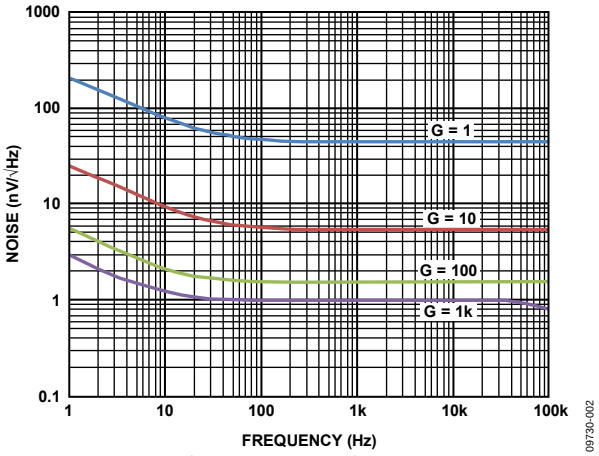

Figure 2. RTI Voltage Noise Spectral Density vs. Frequency

Rev. A **Document Feedback**

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AD8429* PRODUCT PAGE QUICK LINKS

Last Content Update: 02/23/2017

COMPARABLE PARTS

View a parametric search of comparable parts.

EVALUATION KITS

- AD62x, AD822x, AD842x Series InAmp Evaluation Board

DOCUMENTATION

Application Notes

- AN-1401: Instrumentation Amplifier Common-Mode Range: The Diamond Plot

Data Sheet

- AD8429: 1 nV/√Hz Low NoiseInstrumentation Amplifier Data Sheet

Technical Books

- A Designer's Guide to Instrumentation Amplifiers, 3rd Edition, 2006

TOOLS AND SIMULATIONS

- AD8429 SPICE Macro-Model

DESIGN RESOURCES

- AD8429 Material Declaration
- PCN-PDN Information
- Quality And Reliability
- Symbols and Footprints

DISCUSSIONS

View all AD8429 EngineerZone Discussions.

SAMPLE AND BUY

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Submit a technical question or find your regional support number.

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REVISION HISTORY

2/2017—Rev, 0 to Rev. A

Changes to Figure 2 ... 1
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4/2011—Revision 0: Initial Version

SPECIFICATIONS

V_S = ±15 V, V_{REF} = 0 V, T_A = 25°C, G = 1, R_L = 10 kΩ, unless otherwise noted.

Table 1.

Parameter	Test Conditions/Comments	A Grade Min	A Grade Typ	A Grade Max	B Grade Min	B Grade Typ	B Grade Max	Unit
COMMON-MODE REJECTION RATIO (CMRR)								
CMRR DC to 60 Hz with 1 kΩ Source Imbalance	V_{CM} = ±10 V							
G = 1		80			90			dB
G = 10		100			110			dB
G = 100		120			130			dB
G = 1000		134			140			dB
CMRR at 5 kHz	V_{CM} = ±10 V							
G = 1		76			80			dB
G = 10		90			90			dB
G = 100		90			90			dB
G = 1000		90			90			dB
VOLTAGE NOISE, RTI	V_{IN}+, V_{IN}− = 0 V							
Spectral Density[1]: 1 kHz								
Input Voltage Noise, e_{ni}				1.0			1.0	nV/√Hz
Output Voltage Noise, e_{no}				45			45	nV/√Hz
Peak to Peak: 0.1 Hz to 10 Hz								
G = 1			2			2		µV p-p
G = 1000			100			100		nV p-p
CURRENT NOISE								
Spectral Density: 1 kHz			1.5			1.5		pA/√Hz
Peak to Peak: 0.1 Hz to 10 Hz			100			100		pA p-p
VOLTAGE OFFSET[2]								
Input Offset, V_{OSI}				150			50	µV
Average TC			0.1	1		0.1	0.3	µV/°C
Output Offset, V_{OSO}				1000			500	µV
Average TC			3	10		3	10	µV/°C
Offset RTI vs. Supply (PSR)	V_S = ±5 V to ±15 V							
G = 1		90			100			dB
G = 10		110			120			dB
G = 100		130			130			dB
G = 1000		130			130			dB
INPUT CURRENT	V_{IN}+, V_{IN}− = 0 V							
Input Bias Current				300			150	nA
Average TC			250			250		pA/°C
Input Offset Current				100			30	nA
Average TC			15			15		pA/°C
DYNAMIC RESPONSE								
Small Signal Bandwidth: −3 dB								
G = 1			15			15		MHz
G = 10			4			4		MHz
G = 100			1.2			1.2		MHz
G = 1000			0.15			0.15		MHz

Parameter	Test Conditions/Comments	A Grade			B Grade			Unit
		Min	Typ	Max	Min	Typ	Max	
Settling Time 0.01%	10 V step							
G = 1			0.75			0.75		µs
G = 10			0.65			0.65		µs
G = 100			0.85			0.85		µs
G = 1000			5			5		µs
Settling Time 0.001%	10 V step							
G = 1			0.9			0.9		µs
G = 10			0.9			0.9		µs
G = 100			1.2			1.2		µs
G = 1000			7			7		µs
Slew Rate								
G = 1 to 100			22			22		V/µs
THD	First five harmonics, f = 1 kHz, R_L = 2 kΩ, V_{OUT} = 10 V p-p							
G = 1			−130			−130		dBc
G = 10			−116			−116		dBc
G = 100			−113			−113		dBc
G = 1000			−111			−111		dBc
THD + N	f = 1 kHz, R_L = 2 kΩ, V_{OUT} = 10 V p-p							
G = 100			0.0005			0.0005		%
GAIN[3]	G = 1 + (6 kΩ/R_G)							
Gain Range		1		10000	1		10000	V/V
Gain Error	V_{OUT} = ±10 V							
G = 1				0.05			0.02	%
G > 1				0.3			0.15	%
Gain Nonlinearity	V_{OUT} = −10 V to +10 V							
G = 1 to 1000	R_L = 10 kΩ		2			2		ppm
Gain vs. Temperature								
G = 1			2	5		2	5	ppm/°C
G > 1				−100			−100	ppm/°C
INPUT								
Impedance (Pin to Ground)[4]			1.5‖3			1.5‖3		GΩ‖pF
Input Operating Voltage Range[5]	V_S = ±4 V to ±18 V	$-V_S$ + 2.8		$+V_S$ − 2.5	$-V_S$ + 2.8		$+V_S$ − 2.5	V
OUTPUT								
Output Swing	R_L = 2 kΩ	$-V_S$ + 1.8		+Vs − 1.2	$-V_S$ + 1.8		+Vs − 1.2	V
Over Temperature		$-V_S$ + 1.9		+Vs − 1.3	$-V_S$ + 1.9		+Vs − 1.3	V
Output Swing	R_L = 10 kΩ	$-V_S$ + 1.7		+Vs − 1.1	$-V_S$ + 1.7		+Vs − 1.1	V
Over Temperature		$-V_S$ + 1.8		+Vs − 1.2	$-V_S$ + 1.8		+Vs − 1.2	V
Short-Circuit Current			35			35		mA
REFERENCE INPUT								
R_{IN}			10			10		kΩ
I_{IN}	V_{IN}+, V_{IN}− = 0 V		70			70		µA
Voltage Range		$-V_S$		$+V_S$				V
Reference Gain to Output			1			1		V/V
Reference Gain Error			0.01	0.05		0.01	0.05	%

Parameter	Test Conditions/Comments	A Grade			B Grade			Unit
		Min	Typ	Max	Min	Typ	Max	
POWER SUPPLY								
Operating Range		±4		±18	±4		±18	V
Quiescent Current			6.7	7		6.7	7	mA
	T = 125°C			9			9	mA
TEMPERATURE RANGE								
For Specified Performance		−40		+125	−40		+125	°C

[1] Total voltage noise = $\sqrt{(e_{ni}^2 + (e_{no}/G)^2 + e_{RG}^2)}$. See the Theory of Operation section for more information.
[2] Total RTI $V_{OS} = (V_{OSI}) + (V_{OSO}/G)$.
[3] These specifications do not include the tolerance of the external gain setting resistor, R_G. For G > 1, add R_G errors to the specifications given in this table.
[4] Differential and common-mode input impedance can be calculated from the pin impedance: $Z_{DIFF} = 2(Z_{PIN})$; $Z_{CM} = Z_{PIN}/2$.
[5] Input voltage range of the AD8429 input stage only. The input range can depend on the common-mode voltage, differential voltage, gain, and reference voltage. See the Input Voltage Range section for more details.

ABSOLUTE MAXIMUM RATINGS

Table 2.

Parameter	Rating
Supply Voltage	±18 V
Output Short-Circuit Current Duration	Indefinite
Maximum Voltage at –IN, +IN[1]	$\pm V_S$
Differential Input Voltage[1]	
Gain ≤ 4	$\pm V_S$
4 > Gain > 50	±50 V/gain
Gain ≥ 50	±1 V
Maximum Voltage at REF	$\pm V_S$
Storage Temperature Range	−65°C to +150°C
Specified Temperature Range	−40°C to +125°C
Maximum Junction Temperature	140°C
ESD	
Human Body Model	3.0 kV
Charge Device Model	1.5 kV
Machine Model	0.2 kV

[1] For voltages beyond these limits, use input protection resistors. See the Theory of Operation section for more information.

Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

THERMAL RESISTANCE

θ_{JA} is specified for a device in free air using a 4-layer JEDEC printed circuit board (PCB).

Table 3.

Package	θ_{JA}	Unit
8-Lead SOIC	121	°C/W

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

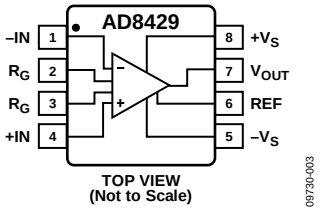

Figure 3. Pin Configuration

Table 4. Pin Function Descriptions

Pin No.	Mnemonic	Description
1	–IN	Negative Input Terminal.
2, 3	R_G	Gain Setting Terminals. Place resistor across the R_G pins to set the gain. G = 1 + (6 kΩ/R_G).
4	+IN	Positive Input Terminal.
5	$-V_S$	Negative Power Supply Terminal.
6	REF	Reference Voltage Terminal. Drive this terminal with a low impedance voltage source to level shift the output.
7	V_{OUT}	Output Terminal.
8	$+V_S$	Positive Power Supply Terminal.

TYPICAL PERFORMANCE CHARACTERISTICS

T = 25°C, V_S = ±15, V_{REF} = 0, R_L = 10 kΩ, unless otherwise noted.

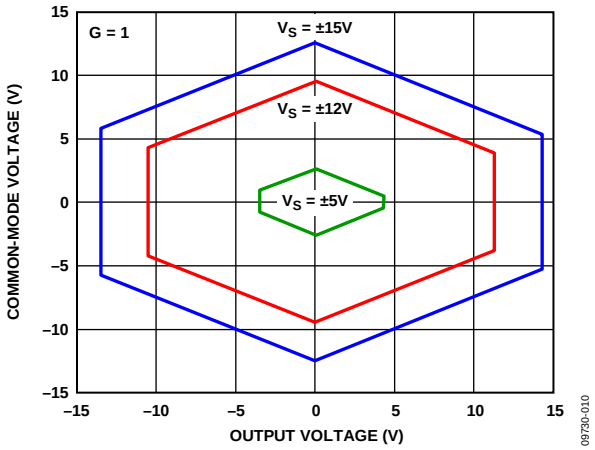

Figure 4. Input Common-Mode Voltage vs. Output Voltage, Dual Supply, V_S = ±5 V, ±12 V, ±15 V (G = 1)

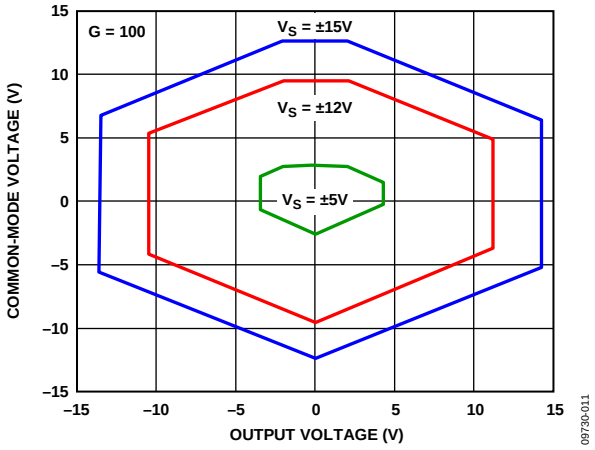

Figure 5. Input Common-Mode Voltage vs. Output Voltage, Dual Supply, V_S = ±5 V, ±12 V, ±15 V (G = 100)

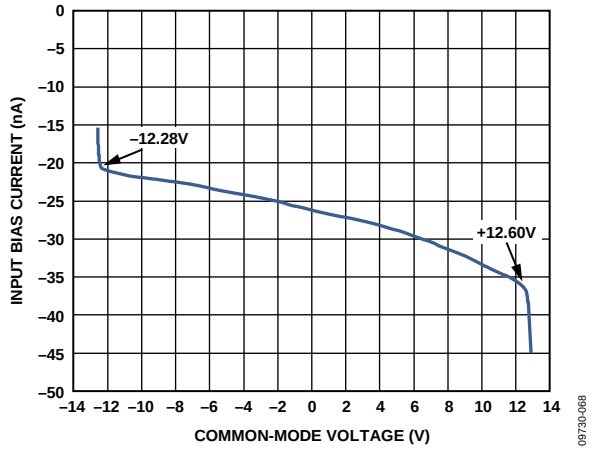

Figure 6. Input Bias Current vs. Common-Mode Voltage

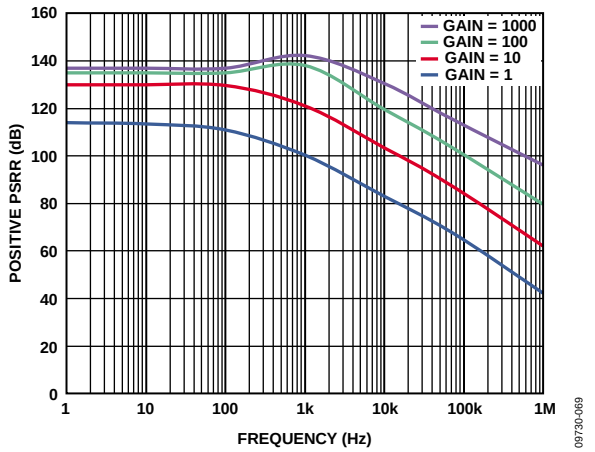

Figure 7. Positive PSRR vs. Frequency

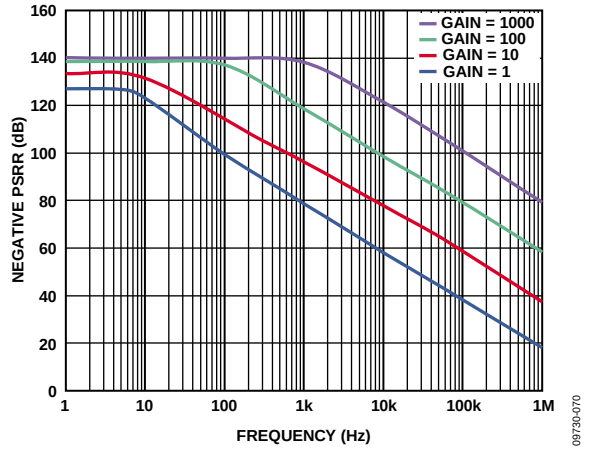

Figure 8. Negative PSRR vs. Frequency

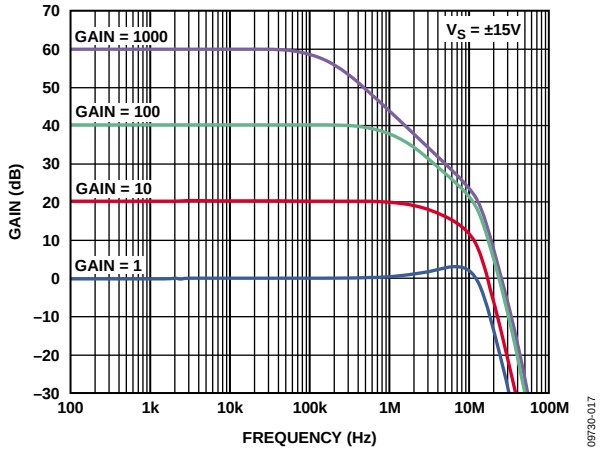

Figure 9. Gain vs. Frequency

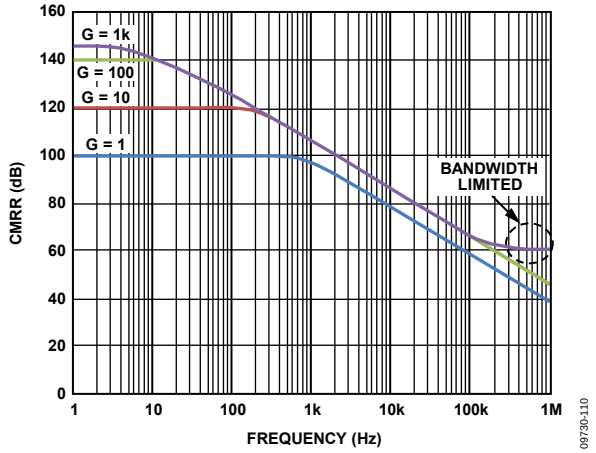

Figure 10. CMRR vs. Frequency

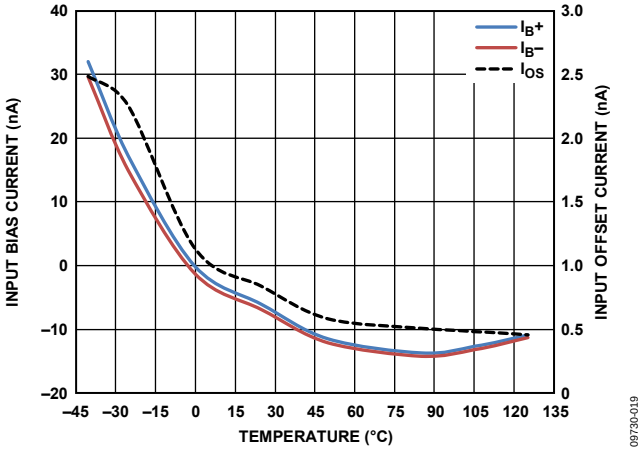

Figure 13. Input Bias Current and Input Offset Current vs. Temperature

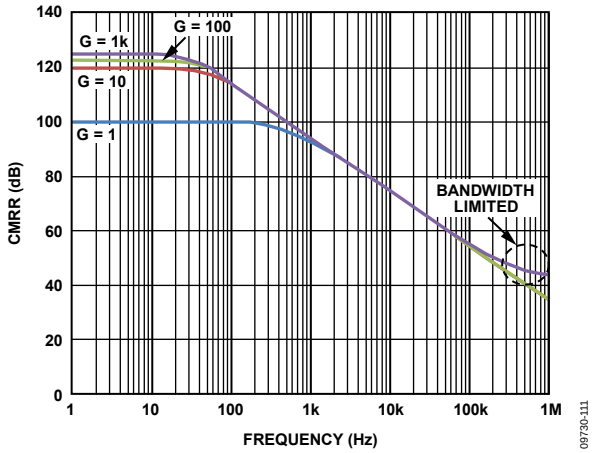

Figure 11. CMRR vs. Frequency, 1 kΩ Source Imbalance

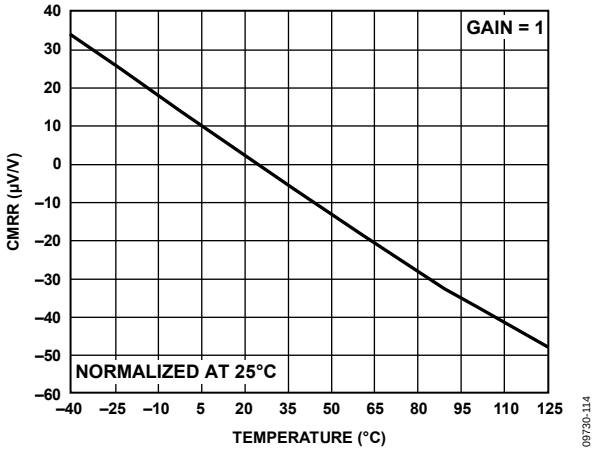

Figure 14. CMRR vs. Temperature (G = 1), Normalized at 25°C

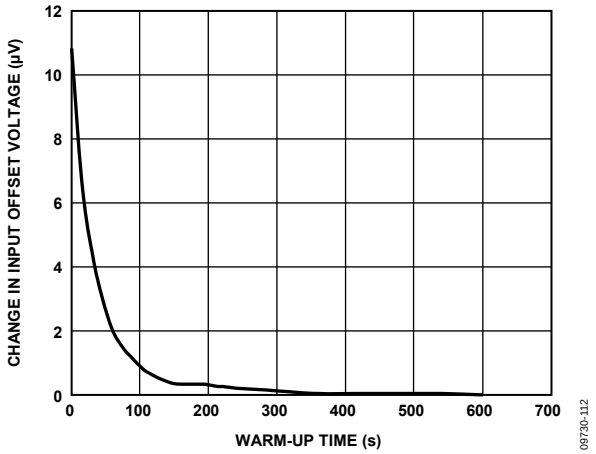

Figure 12. Change in Input Offset Voltage (V_{OSI}) vs. Warm-Up Time

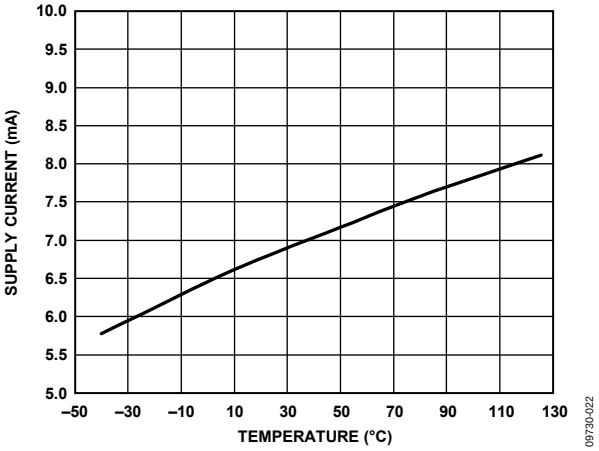

Figure 15. Supply Current vs. Temperature (G = 1)

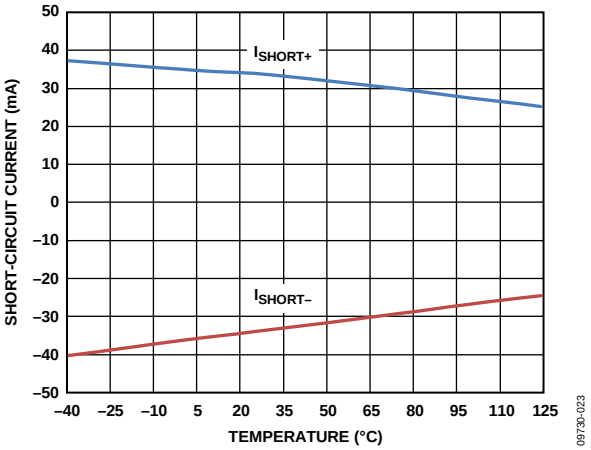

Figure 16. Short-Circuit Current vs. Temperature (G = 1)

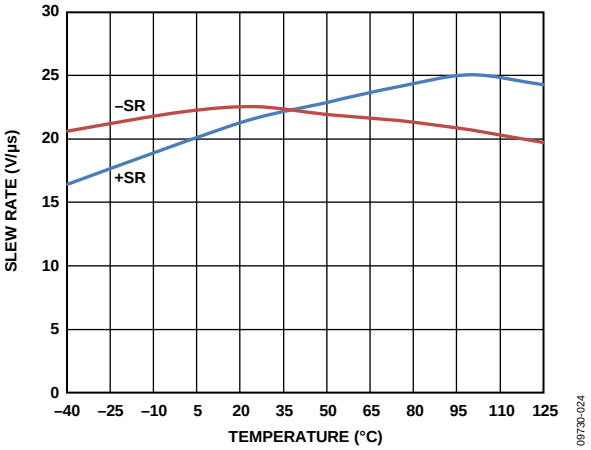

Figure 17. Slew Rate vs. Temperature, V_S = ±15 V (G = 1)

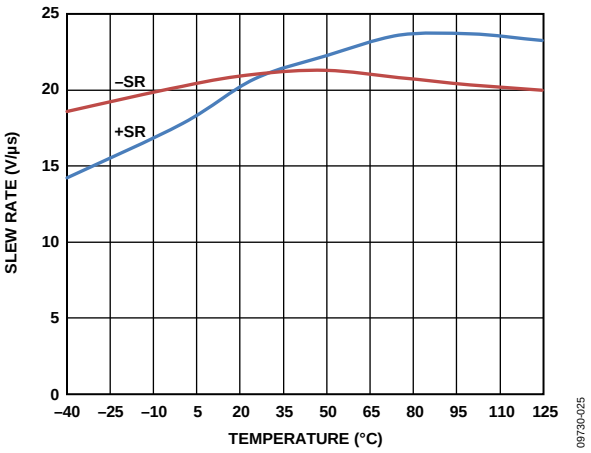

Figure 18. Slew Rate vs. Temperature, V_S = ±5 V (G = 1)

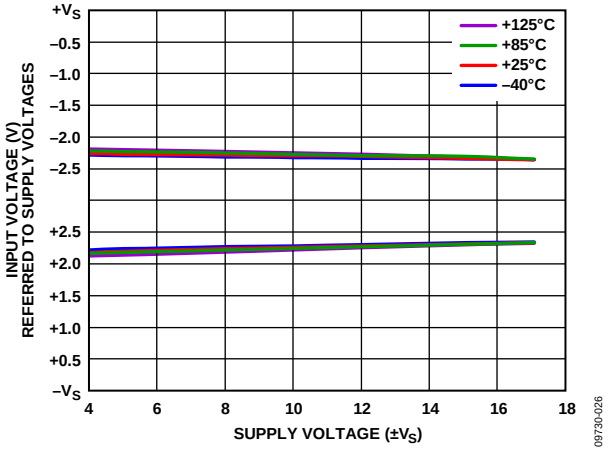

Figure 19. Input Voltage Limit vs. Supply Voltage

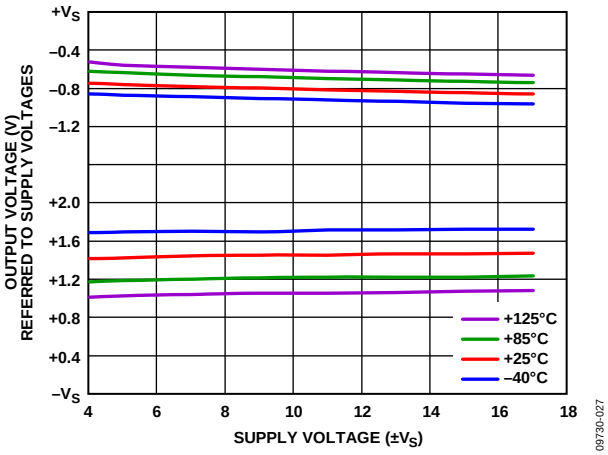

Figure 20. Output Voltage Swing vs. Supply Voltage, R_L = 10 kΩ

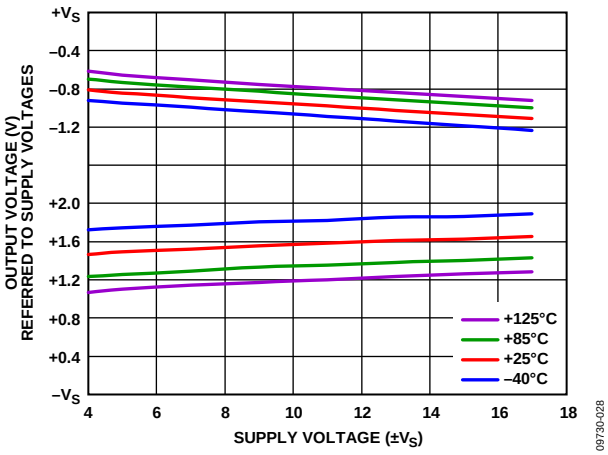

Figure 21. Output Voltage Swing vs. Supply Voltage, R_L = 2 kΩ

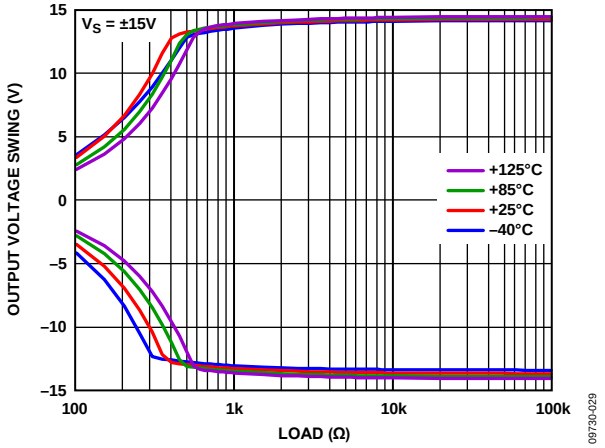

Figure 22. Output Voltage Swing vs. Load Resistance

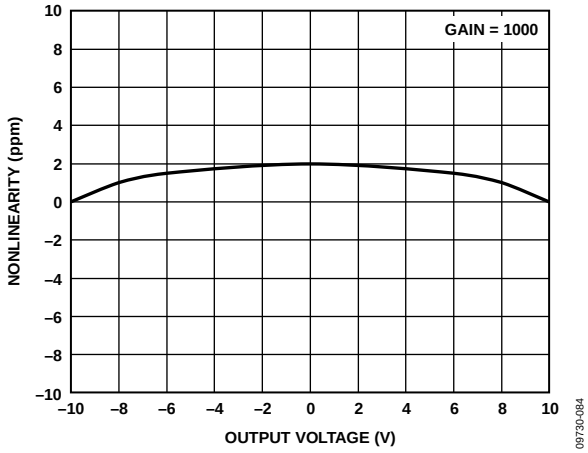

Figure 25. Gain Nonlinearity (G = 1000), R_L = 10 kΩ

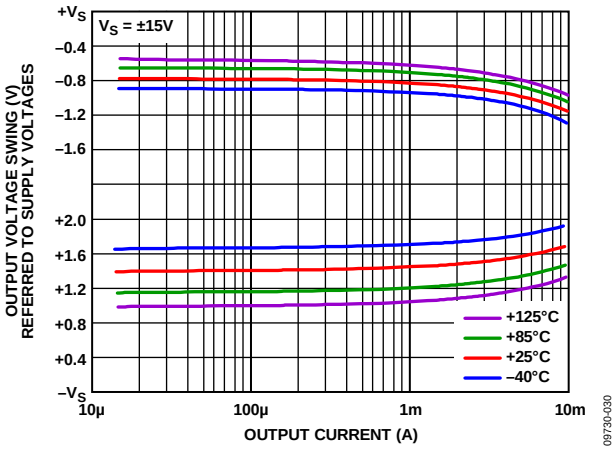

Figure 23. Output Voltage Swing vs. Output Current

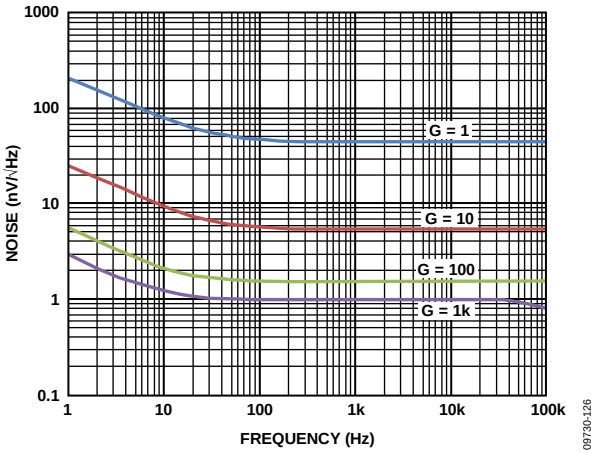

Figure 26. RTI Voltage Noise Spectral Density vs. Frequency

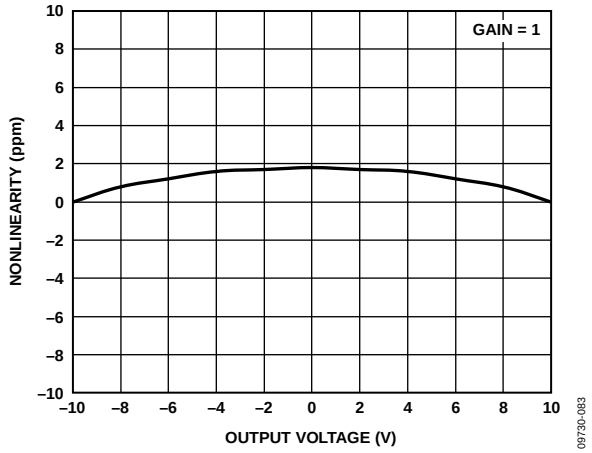

Figure 24. Gain Nonlinearity (G = 1), R_L = 10 kΩ

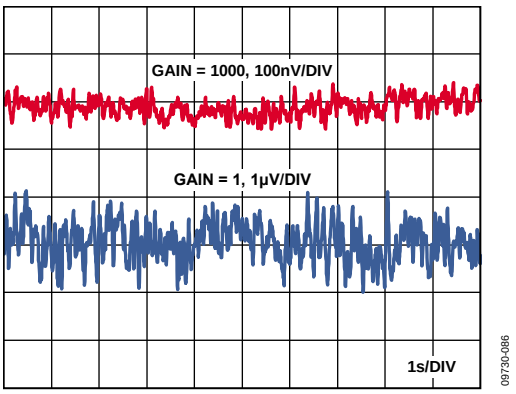

Figure 27. 0.1 Hz to 10 Hz RTI Voltage Noise (G = 1, G = 1000)

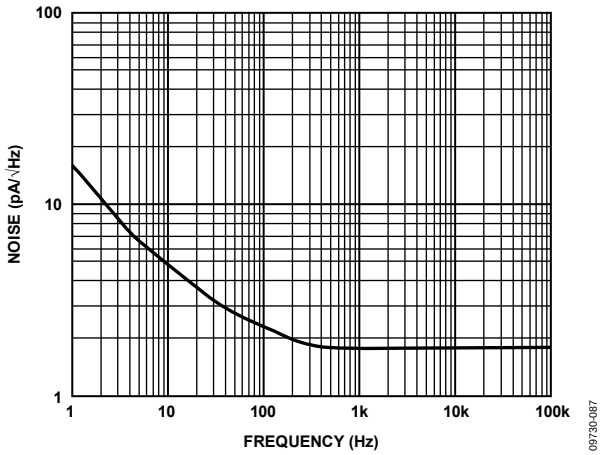

Figure 28. Current Noise Spectral Density vs. Frequency

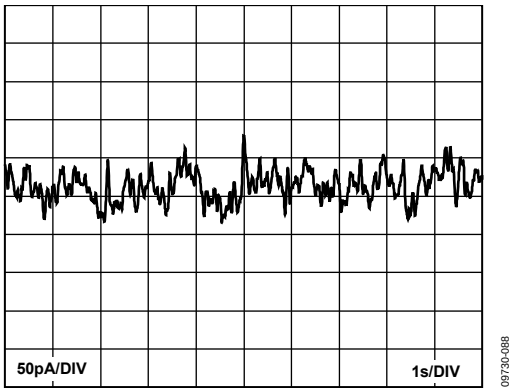

Figure 29. 0.1 Hz to 10 Hz Current Noise

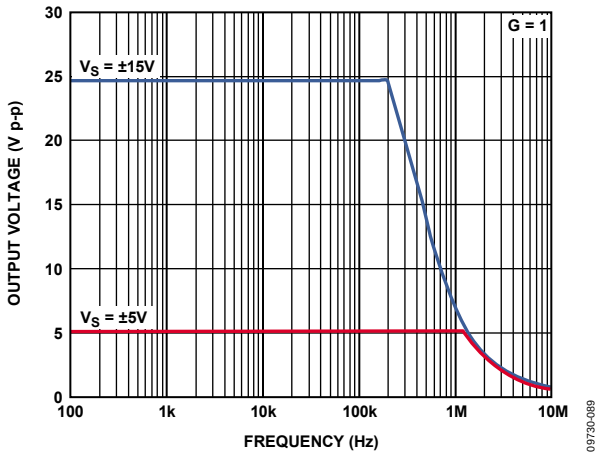

Figure 30. Large Signal Frequency Response

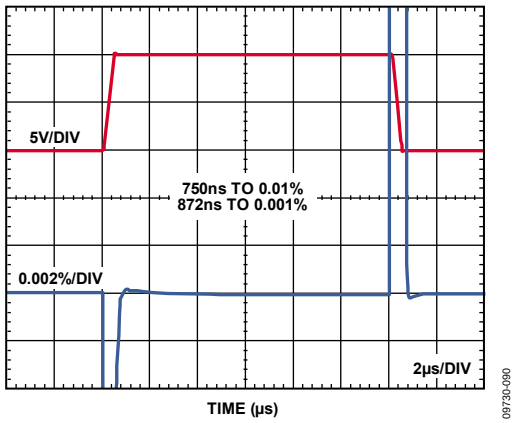

Figure 31. Large Signal Pulse Response and Settling Time (G = 1), 10 V Step, V_S = ±15 V

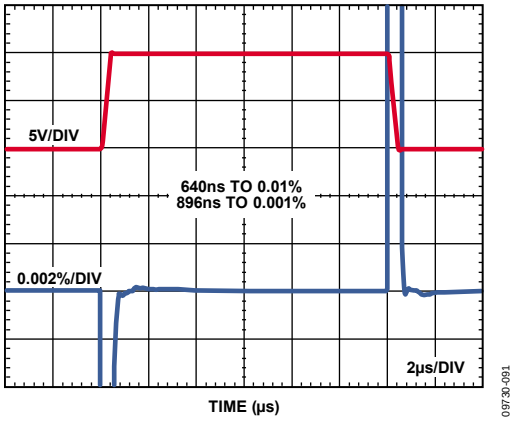

Figure 32. Large Signal Pulse Response and Settling Time (G = 10), 10 V Step, V_S = ±15 V

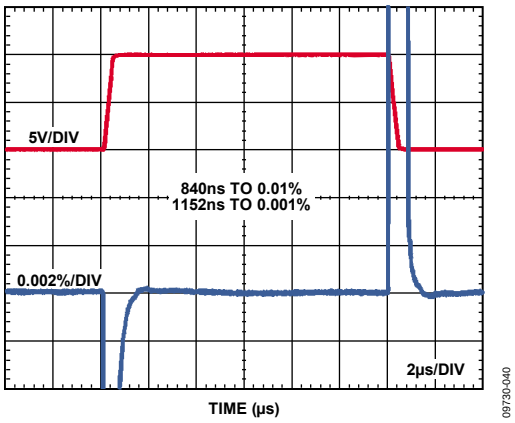

Figure 33. Large Signal Pulse Response and Settling Time (G = 100), 10 V Step, V_S = ±15 V

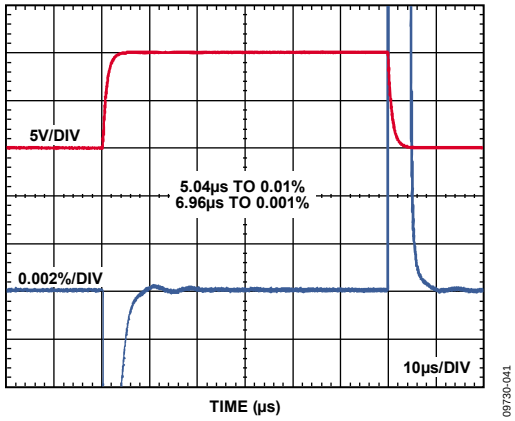

Figure 34. Large Signal Pulse Response and Settling Time (G = 1000), 10 V Step, V_S = ±15 V

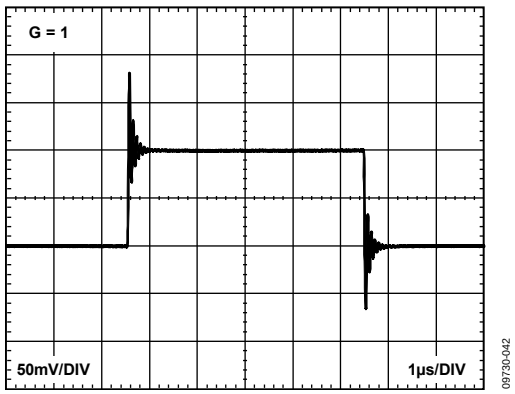

Figure 35. Small Signal Response (G = 1), R_L = 10 kΩ, C_L = 100 pF

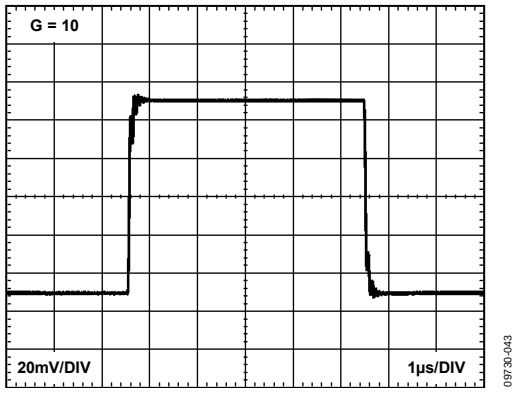

Figure 36. Small Signal Response (G = 10), R_L = 10 kΩ, C_L = 100 pF

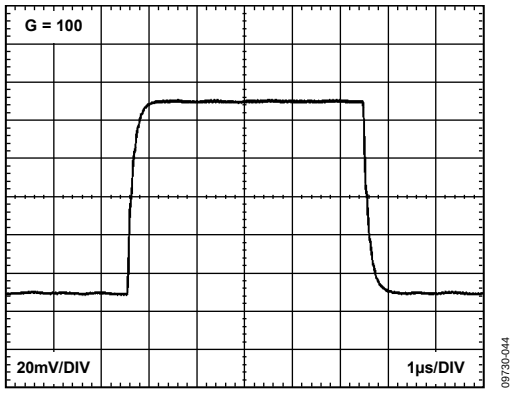

Figure 37. Small Signal Response (G = 100), R_L = 10 kΩ, C_L = 100 pF

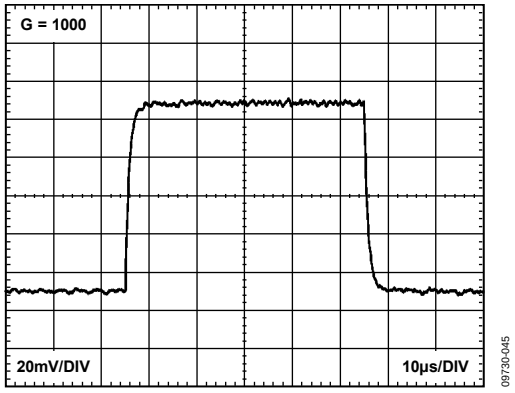

Figure 38. Small Signal Response (G = 1000), R_L = 10 kΩ, C_L = 100 pF

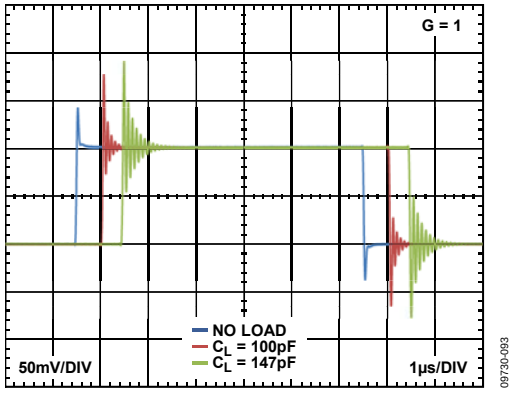

Figure 39. Small Signal Response with Various Capacitive Loads (G = 1), R_L = Infinity

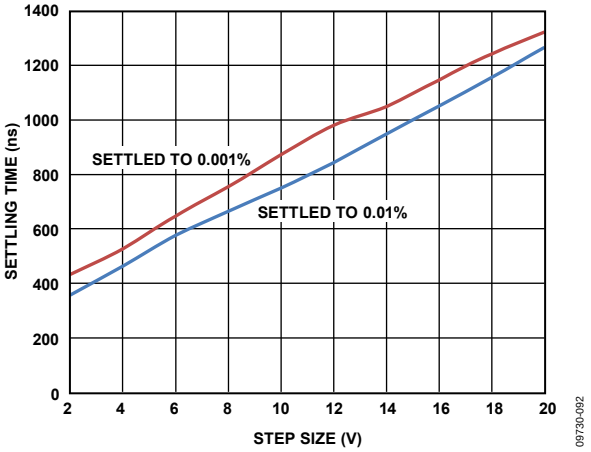

Figure 40. Settling Time vs. Step Size (G = 1)

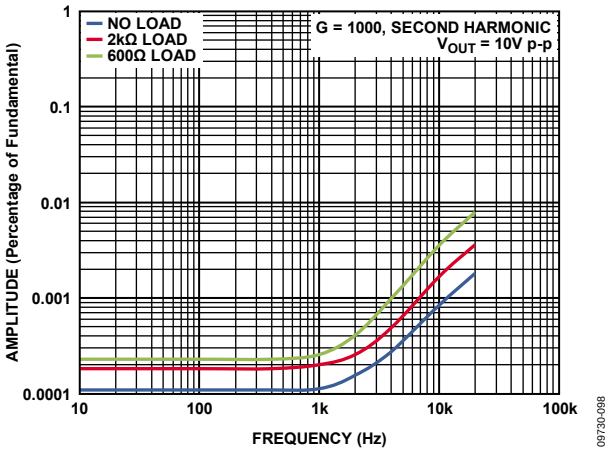

Figure 43. Second Harmonic Distortion vs. Frequency (G = 1000)

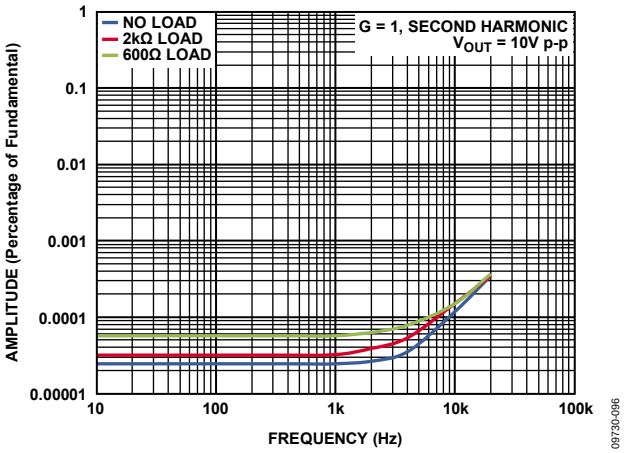

Figure 41. Second Harmonic Distortion vs. Frequency (G = 1)

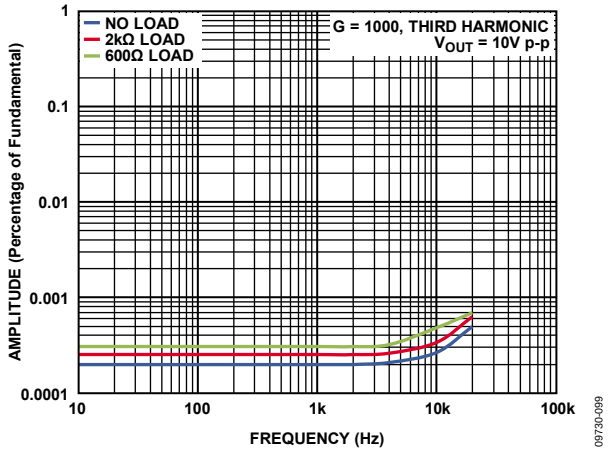

Figure 44. Third Harmonic Distortion vs. Frequency (G = 1000)

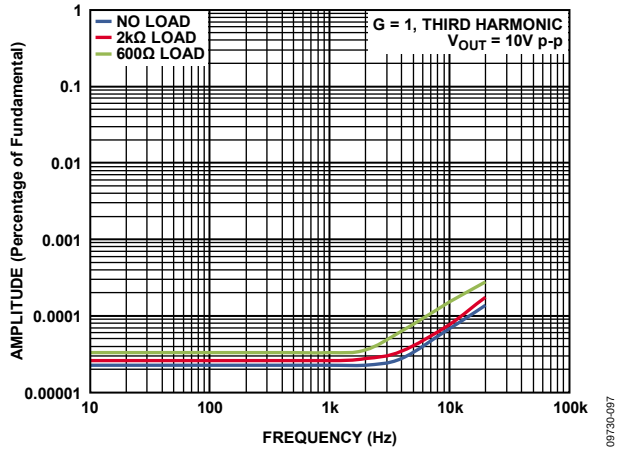

Figure 42. Third Harmonic Distortion vs. Frequency (G = 1)

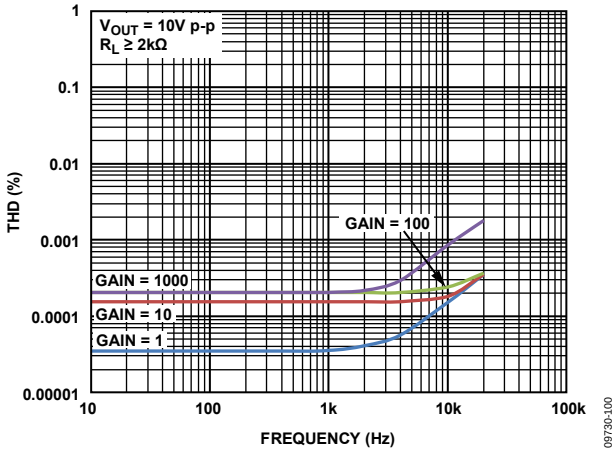

Figure 45. THD vs. Frequency

THEORY OF OPERATION

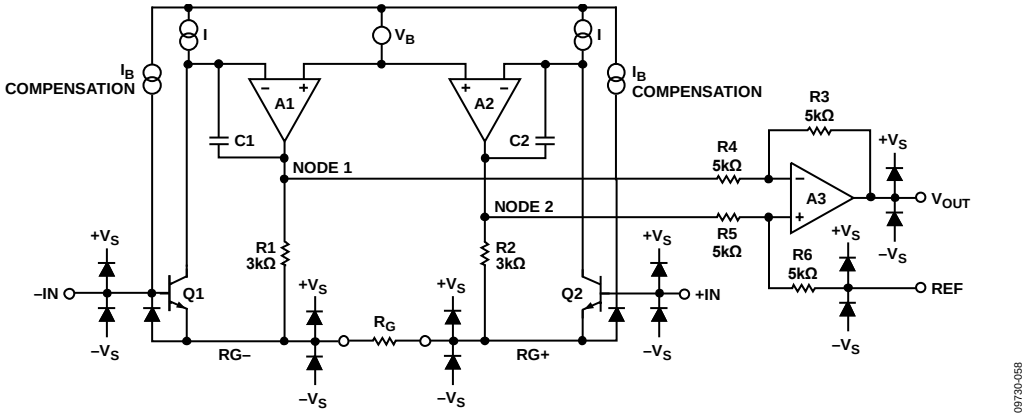

Figure 46. Simplified Schematic

ARCHITECTURE

The AD8429 is based on the classic 3-op-amp topology. This topology has two stages: a preamplifier to provide differential amplification followed by a difference amplifier that removes the common-mode voltage and provides additional amplification. Figure 46 shows a simplified schematic of the AD8429.

The first stage works as follows. To keep its two inputs matched, Amplifier A1 must keep the collector of Q1 at a constant voltage. It does this by forcing RG– to be a precise diode drop from –IN. Similarly, A2 forces RG+ to be a constant diode drop from +IN. Therefore, a replica of the differential input voltage is placed across the gain setting resistor, R_G. The current that flows through this resistance must also flow through the R1 and R2 resistors, creating a gained differential signal between the A2 and A1 outputs.

The second stage is a G = 1 difference amplifier, composed of Amplifier A3 and the R3 through R6 resistors. This stage removes the common-mode signal from the amplified differential signal.

The transfer function of the AD8429 is

$$V_{OUT} = G \times (V_{IN+} - V_{IN-}) + V_{REF}$$

where:

$$G = 1 + \frac{6\,\text{k}\Omega}{R_G}$$

GAIN SELECTION

Placing a resistor across the R_G terminals sets the gain of the AD8429, which can be calculated by referring to Table 5 or by using the following gain equation:

$$R_G = \frac{6\,\text{k}\Omega}{G-1}$$

Table 5. Gains Achieved Using 1% Resistors

1% Standard Table Value of R_G	Calculated Gain
6.04 kΩ	1.993
1.5 kΩ	5.000
665 Ω	10.02
316 Ω	19.99
121 Ω	50.59
60.4 Ω	100.3
30.1 Ω	200.3
12.1 Ω	496.9
6.04 Ω	994.4
3.01 Ω	1994

The AD8429 defaults to G = 1 when no gain resistor is used. Add the tolerance and gain drift of the R_G resistor to the specifications of the AD8429 to determine the total gain accuracy of the system. When the gain resistor is not used, gain error and gain drift are minimal.

R_G Power Dissipation

The AD8429 duplicates the differential voltage across its inputs onto the R_G resistor. Choose an R_G resistor size sufficient to handle the expected power dissipation.

REFERENCE TERMINAL

The output voltage of the AD8429 is developed with respect to the potential on the reference terminal. This is useful when the output signal must be offset to a precise midsupply level. For example, a voltage source can be tied to the REF pin to level shift the output, allowing the AD8429 to drive a single-supply ADC. The REF pin is protected with ESD diodes and should not exceed either $+V_S$ or $-V_S$ by more than 0.3 V.

For best performance, maintain a source impedance to the REF terminal that is well below 1 Ω. As shown in Figure 46, the reference terminal, REF, is at one end of a 5 kΩ resistor. Additional impedance at the REF terminal adds to this 5 kΩ resistor and results in amplification of the signal connected to the positive input. The amplification from the additional R_{REF} can be calculated as follows:

$$2(5\ k\Omega + R_{REF})/(10\ k\Omega + R_{REF})$$

Only the positive signal path is amplified; the negative path is unaffected. This uneven amplification degrades CMRR.

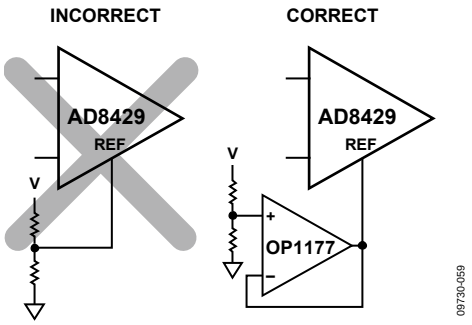

Figure 47. Driving the Reference Pin

INPUT VOLTAGE RANGE

Figure 4 and Figure 5 show the allowable common-mode input voltage ranges for various output voltages and supply voltages. The 3-op-amp architecture of the AD8429 applies gain in the first stage before removing common-mode voltage with the difference amplifier stage. Internal nodes between the first and second stages (Node 1 and Node 2 in Figure 46) experience a combination of a gained signal, a common-mode signal, and a diode drop. This combined signal can be limited by the voltage supplies even when the individual input and output signals are not limited.

LAYOUT

To ensure optimum performance of the AD8429 at the PCB level, care must be taken in the design of the board layout. The pins of the AD8429 are arranged in a logical manner to aid in this task.

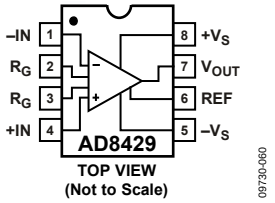

Figure 48. Pinout Diagram

Common-Mode Rejection Ratio over Frequency

Poor layout can cause some of the common-mode signals to be converted to differential signals before reaching the in-amp. Such conversions occur when one input path has a frequency response that is different from the other. To maintain high CMRR over frequency, closely match the input source impedance and capacitance of each path. Place additional source resistance in the input path (for example, for input protection) close to the in-amp inputs, which minimizes their interaction with parasitic capacitance from the PCB traces.

Parasitic capacitance at the gain setting pins can also affect CMRR over frequency. If the board design has a component at the gain setting pins (for example, a switch or jumper), choose a component such that the parasitic capacitance is as small as possible.

Power Supplies and Grounding

Use a stable dc voltage to power the instrumentation amplifier. Noise on the supply pins can adversely affect performance. See the PSRR performance curves in Figure 9 and Figure 10 for more information.

Place a 0.1 µF capacitor as close as possible to each supply pin. Because the length of the bypass capacitor leads is critical at high frequency, surface-mount capacitors are recommended. A parasitic inductance in the bypass ground trace works against the low impedance created by the bypass capacitor. As shown in Figure 49, a 10 µF capacitor can be used farther away from the device. For larger value capacitors, intended to be effective at lower frequencies, the current return path distance is less critical. In most cases, this capacitor can be shared by other precision integrated circuits.

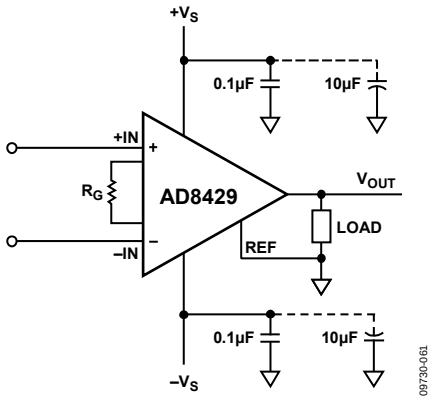

Figure 49. Supply Decoupling, REF, and Output Referred to Local Ground

A ground plane layer is helpful to reduce parasitic inductances. This minimizes voltage drops with changes in current. The area of the current path is directly proportional to the magnitude of parasitic inductances and, therefore, the impedance of the path at high frequency. Large changes in currents in an inductive decoupling path or ground return create unwanted effects, due to the coupling of such changes into the amplifier inputs.

Because load currents flow from the supplies, the load should be connected at the same physical location as the bypass capacitor grounds.

Reference Pin

The output voltage of the AD8429 is developed with respect to the potential on the reference terminal. Ensure that REF is tied to the appropriate local ground.

INPUT BIAS CURRENT RETURN PATH

The input bias current of the AD8429 must have a return path to ground. When using a floating source without a current return path, such as a thermocouple, create a current return path, as shown in Figure 50.

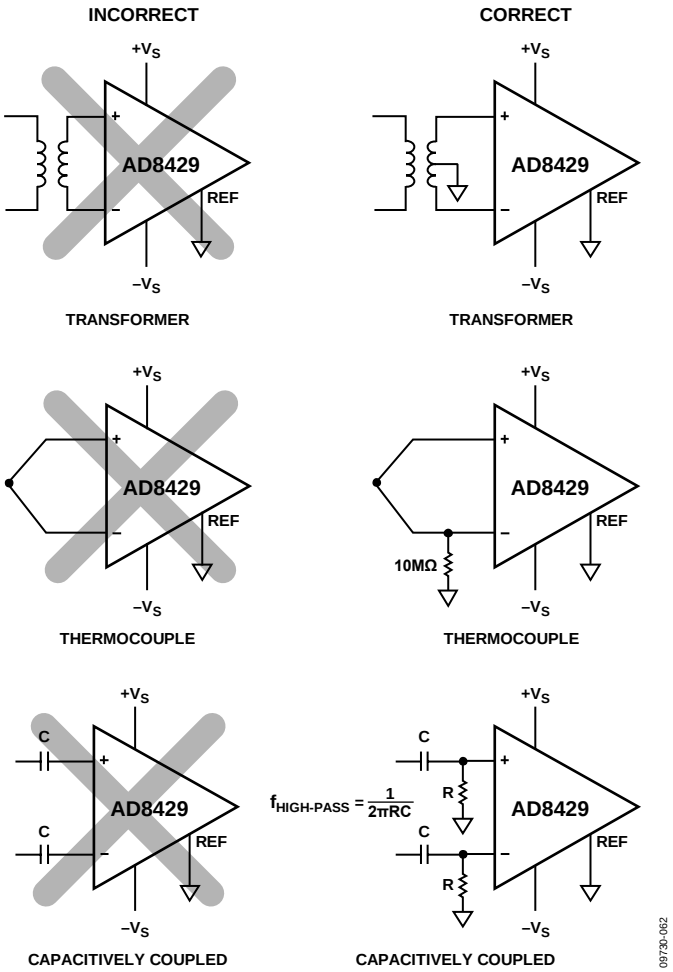

Figure 50. Creating an Input Bias Current Return Path

INPUT PROTECTION

Do not allow the inputs of the AD8429 to exceed the ratings stated in the Absolute Maximum Ratings section of this data sheet. If this cannot be done, protection circuitry can be added in front of the AD8429 to limit the current into the inputs to a maximum current, I_{MAX}.

Input Voltages Beyond the Rails

If voltages beyond the rails are expected, use an external resistor in series with each input to limit current during overload conditions. The limiting resistor at the input can be computed from

$$R_{PROTECT} \geq \frac{|V_{IN} - V_{SUPPLY}|}{I_{MAX}}$$

Noise sensitive applications may require a lower protection resistance. Low leakage diode clamps, such as the BAV199, can be used at the inputs to shunt current away from the AD8429 inputs, thereby allowing smaller protection resistor values. To ensure current flows primarily through the external protection diodes, place a small value resistor, such as a 33 Ω, between the diodes and the AD8429.

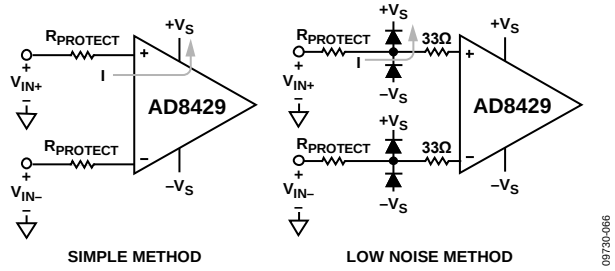

Figure 51. Protection for Voltages Beyond the Rails

Large Differential Input Voltage at High Gain

If large differential voltages at high gain are expected, use an external resistor in series with each input to limit current during overload conditions. The limiting resistor at each input can be computed by using the following equation:

$$R_{PROTECT} \geq \frac{1}{2}\left(\frac{|V_{DIFF}| - 1\text{V}}{I_{MAX}} - R_G\right)$$

Noise sensitive applications may require a lower protection resistance. Low leakage diode clamps, such as the BAV199, can be used across the inputs to shunt current away from the AD8429 inputs and, therefore, allow smaller protection resistor values.

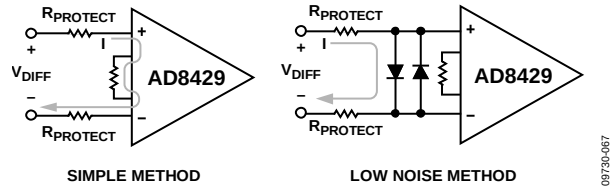

Figure 52. Protection for Large Differential Voltages

I_{MAX}

The maximum current into the AD8429 inputs, I_{MAX}, depends on time and temperature. At room temperature, the device can withstand a current of 10 mA for at least one day. This time is cumulative over the life of the device.

RADIO FREQUENCY INTERFERENCE (RFI)

RF rectification is often a problem when amplifiers are used in applications that have strong RF signals. The disturbance can appear as a small dc offset voltage. High frequency signals can be filtered with a low-pass RC network placed at the input of the instrumentation amplifier, as shown in Figure 53.

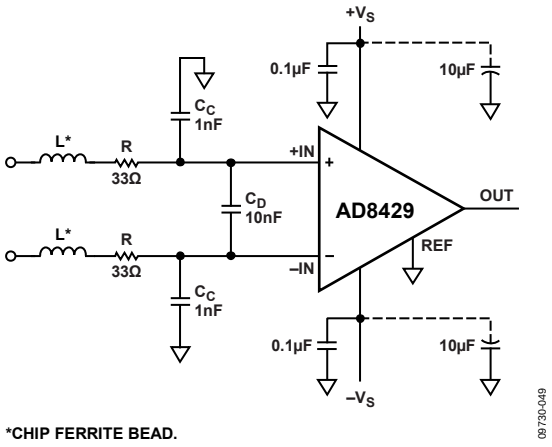

Figure 53. RFI Suppression

The filter limits the input signal bandwidth, according to the following relationship:

$$FilterFrequency_{DIFF} = \frac{1}{2\pi R(2C_D + C_C)}$$

$$FilterFrequency_{CM} = \frac{1}{2\pi RC_C}$$

where $C_D \geq 10\ C_C$.

C_D affects the difference signal, and C_C affects the common-mode signal. Choose values of R and C_C that minimize RFI. A mismatch between R × C_C at the positive input and R × C_C at the negative input degrades the CMRR of the AD8429. By using a value of C_D that is one magnitude larger than C_C, the effect of the mismatch is reduced, and performance is improved.

Resistors add noise; therefore, the choice of resistor and capacitor values depends on the desired tradeoff between noise, input impedance at high frequencies, and RFI immunity. The resistors used for the RFI filter can be the same as those used for input protection.

CALCULATING THE NOISE OF THE INPUT STAGE

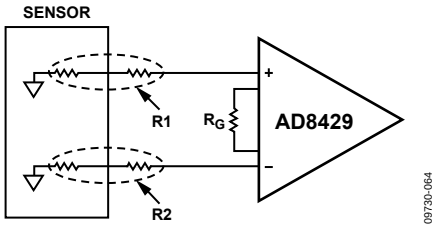

Figure 54. Source Resistance from Sensor and Protection Resistors

The total noise of the amplifier front end depends on much more than the 1 nV/√Hz specification of this data sheet. There are three main contributors: the source resistance, the voltage noise of the instrumentation amplifier, and the current noise of the instrumentation amplifier.

In the following calculations, noise is referred to the input (RTI). In other words, everything is calculated as if it appeared at the amplifier input. To calculate the noise referred to the amplifier output (RTO), simply multiply the RTI noise by the gain of the instrumentation amplifier.

Source Resistance Noise

Any sensor connected to the AD8429 has some output resistance. There may also be resistance placed in series with inputs for protection from either overvoltage or radio frequency interference. This combined resistance is labeled R1 and R2 in Figure 54. Any resistor, no matter how well made, has an intrinsic level of noise. This noise is proportional to the square root of the resistor value. At room temperature, the value is approximately equal to 4 nV/√Hz × √(resistor value in kΩ).

For example, assuming that the combined sensor and protection resistance on the positive input is 4 kΩ, and on the negative input is 1 kΩ, the total noise from the input resistance is

$$\sqrt{\left(4\times\sqrt{4}\right)^2 + \left(4\times\sqrt{1}\right)^2} = \sqrt{64+16} = 8.9\ \text{nV}/\sqrt{\text{Hz}}$$

Voltage Noise of the Instrumentation Amplifier

The voltage noise of the instrumentation amplifier is calculated using three parameters: the device input noise, output noise, and the R_G resistor noise. It is calculated as follows:

$$Total\ Voltage\ Noise = \sqrt{\left(Output\ Noise/G\right)^2 + \left(Input\ Noise\right)^2 + \left(Noise\ of\ R_G\ Resistor\right)^2}$$

For example, for a gain of 100, the gain resistor is 60.4 Ω. Therefore, the voltage noise of the in-amp is

$$\sqrt{(45/100)^2 + 1^2 + \left(4\times\sqrt{0.0604}\right)^2} = 1.5\ \text{nV}/\sqrt{\text{Hz}}$$

Current Noise of the Instrumentation Amplifier

Current noise is calculated by multiplying the source resistance by the current noise.

For example, if the R1 source resistance in Figure 54 is 4 kΩ, and the R2 source resistance is 1 kΩ, the total effect from the current noise is calculated as follows:

$$\sqrt{\left((4\times1.5)^2 + (1\times1.5)^2\right)} = 6.2\ \text{nV}/\sqrt{\text{Hz}}$$

Total Noise Density Calculation

To determine the total noise of the in-amp, referred to input, combine the source resistance noise, voltage noise, and current noise contribution by the sum of squares method.

For example, if the R1 source resistance in Figure 54 is 4 kΩ, the R2 source resistance is 1 kΩ, and the gain of the in-amps is 100, the total noise, referred to input, is

$$\sqrt{8.9^2 + 1.5^2 + 6.2^2} = 11.0\ \text{nV}/\sqrt{\text{Hz}}$$

OUTLINE DIMENSIONS

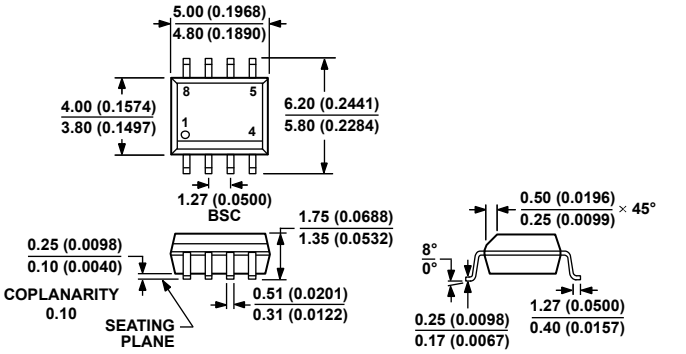

Figure 55. 8-Lead Standard Small Outline Package [SOIC_N]
Narrow Body
(R-8)
Dimensions shown in millimeters and (inches)

ORDERING GUIDE

Model[1]	Temperature Range	Package Description	Package Option
AD8429ARZ	−40°C to +125°C	8-Lead SOIC_N	R-8
AD8429ARZ-R7	−40°C to +125°C	8-Lead SOIC_N, 7″Tape and Reel	R-8
AD8429BRZ	−40°C to +125°C	8-Lead SOIC_N	R-8
AD8429BRZ-R7	−40°C to +125°C	8-Lead SOIC_N, 7″Tape and Reel	R-8

[1] Z = RoHS Compliant Part.

NOTES