Dual 100mA, Low Dropout, Low Noise, Micropower Regulator

FEATURES

- **Low Noise: 20μV$_{RMS}$ (10Hz to 100kHz)**
- **Low Quiescent Current: 20μA/Channel**
- **Wide Input Voltage Range: 1.8V to 20V**
- **Output Current: 100mA/Channel**
- **Very Low Shutdown Current: <0.1μA**
- **Low Dropout Voltage: 300mV at 100mA**
- Adjustable Output from 1.22V to 20V
- Stable with 1μF Output Capacitor
- Stable with Aluminum, Tantalum or Ceramic Capacitors
- Reverse Battery Protected
- No Reverse Current
- No Protection Diodes Needed
- Overcurrent and Overtemperature Protected
- Thermally Enhanced 10-Lead MSOP and DFN Packages

APPLICATIONS

- Cellular Phones
- Pagers
- Battery-Powered Systems
- Frequency Synthesizers
- Wireless Modems

DESCRIPTION

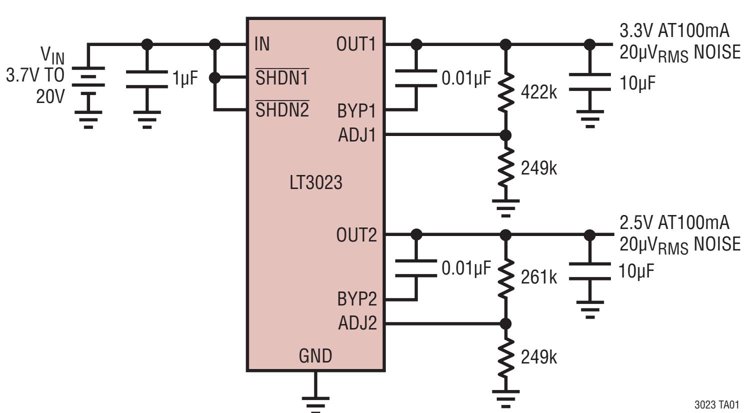
The LT®3023 is a dual, micropower, low noise, low dropout regulator. With an external 0.01μF bypass capacitor, output noise drops to 20μV$_{RMS}$ over a 10Hz to 100kHz bandwidth. Designed for use in battery-powered systems, the low 20μA quiescent current per channel makes it an ideal choice. In shutdown, quiescent current drops to less than 0.1μA. Shutdown control is independent for each channel, allowing for flexibility in power management. The device is capable of operating over an input voltage from 1.8V to 20V, and can supply 100mA of output current from each channel with a dropout voltage of 300mV. Quiescent current is well controlled in dropout.

The LT3023 regulator is stable with output capacitors as low as 1μF. Small ceramic capacitors can be used without the series resistance required by other regulators.

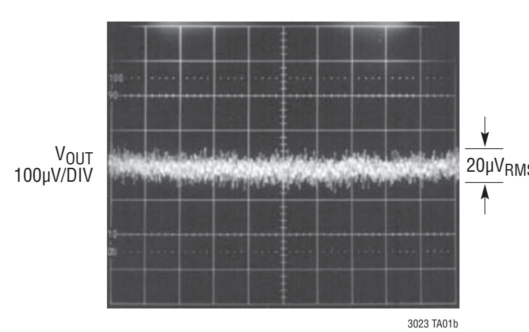
Internal protection circuitry includes reverse battery protection, current limiting, thermal limiting and reverse current protection. The device is available as an adjustable device with a 1.22V reference voltage. The LT3023 regulator is available in the thermally enhanced 10-lead MSOP and DFN packages.

TYPICAL APPLICATION

3.3V/2.5V Low Noise Regulators



10Hz to 100kHz Output Noise



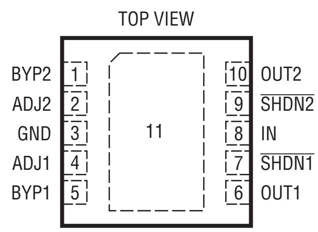
ABSOLUTE MAXIMUM RATINGS

(Note 1)

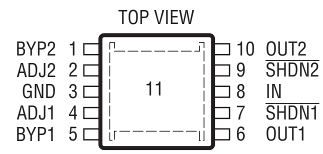
IN Pin Voltage .... ±20V
OUT1, OUT2 Pin Voltage .... ±20V
Input to Output Differential Voltage .... ±20V
ADJ1, ADJ2 Pin Voltage .... ±7V
BYP1, BYP2 Pin Voltage .... ±0.6V
$\overline{\text{SHDN1}}$, $\overline{\text{SHDN2}}$ Pin Voltage .... ±20V

Output Short-Circuit Duration .... Indefinite
Operating Junction Temperature Range
(Note 2) .... –40°C to 125°C
Storage Temperature Range .... –65°C to 150°C
Lead Temperature (Soldering, 10 sec) .... 300°C
(MSE package only)

PIN CONFIGURATION



DD PACKAGE
10-LEAD (3mm × 3mm) PLASTIC DFN
T_{JMAX} = 125°C, θ_{JA} = 40°C/W, θ_{JC} = 10°C/W
EXPOSED PAD (PIN 11) IS GND, MUST BE SOLDERED TO PCB



MSE PACKAGE
10-LEAD PLASTIC MSOP
T_{JMAX} = 150°C, θ_{JA} = 40°C/W, θ_{JC} = 10°C/W
EXPOSED PAD (PIN 11) IS GND, MUST BE SOLDERED TO PCB

ORDER INFORMATION

LEAD FREE FINISH	TAPE AND REEL	PART MARKING*	PACKAGE DESCRIPTION	TEMPERATURE RANGE
LT3023EDD#PBF	LT3023EDD#TRPBF	LAJA	10-Lead (3mm × 3mm) Plastic DFN	–40°C to 125°C
LT3023IDD#PBF	LT3023IDD#TRPBF	LAJA	10-Lead (3mm × 3mm) Plastic DFN	–40°C to 125°C
LT3023EMSE#PBF	LT3023EMSE#TRPBF	LTAHZ	10-Lead Plastic MSOP	–40°C to 125°C
LT3023IMSE#PBF	LT3023IMSE#TRPBF	LTAHZ	10-Lead Plastic MSOP	–40°C to 125°C
LEAD BASED FINISH	**TAPE AND REEL**	**PART MARKING***	**PACKAGE DESCRIPTION**	**TEMPERATURE RANGE**
LT3023EDD	LT3023EDD#TR	LAJA	10-Lead (3mm × 3mm) Plastic DFN	–40°C to 125°C
LT3023IDD	LT3023IDD#TR	LAJA	10-Lead (3mm × 3mm) Plastic DFN	–40°C to 125°C
LT3023EMSE	LT3023EMSE#TR	LTAHZ	10-Lead Plastic MSOP	–40°C to 125°C
LT3023IMSE	LT3023IMSE#TR	LTAHZ	10-Lead Plastic MSOP	–40°C to 125°C

Consult LTC Marketing for parts specified with wider operating temperature ranges. *The temperature grade is identified by a label on the shipping container.

For more information on lead free part marking, go to: http://www.linear.com/leadfree/
For more information on tape and reel specifications, go to: http://www.linear.com/tapeandreel/

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. (Note 2)

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Minimum Input Voltage (Notes 3, 11)	I_{LOAD} = 100mA	●		1.8	2.3	V
ADJ1, ADJ2 Pin Voltage (Note 3, 4)	V_{IN} = 2V, I_{LOAD} = 1mA 2.3V < V_{IN} < 20V, 1mA < I_{LOAD} < 100mA	 ●	1.205 1.190	1.220 1.220	1.235 1.250	V V

3023fa

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. (Note 2)

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Line Regulation (Note 3)	ΔV_{IN} = 2V to 20V, I_{LOAD} = 1mA	●		1	10	mV
Load Regulation (Note 3)	V_{IN} = 2.3V, ΔI_{LOAD} = 1mA to 100mA			1	12	mV
	V_{IN} = 2.3V, ΔI_{LOAD} = 1mA to 100mA	●			25	mV
Dropout Voltage $V_{IN} = V_{OUT(NOMINAL)}$ (Notes 5, 6, 11)	I_{LOAD} = 1mA			0.10	0.15	V
	I_{LOAD} = 1mA	●			0.19	V
	I_{LOAD} = 10mA			0.17	0.22	V
	I_{LOAD} = 10mA	●			0.29	V
	I_{LOAD} = 50mA			0.24	0.28	V
	I_{LOAD} = 50mA	●			0.38	V
	I_{LOAD} = 100mA			0.30	0.35	V
	I_{LOAD} = 100mA	●			0.45	V
GND Pin Current (Per Channel) $V_{IN} = V_{OUT(NOMINAL)}$ (Notes 5, 7)	I_{LOAD} = 0mA	●		20	45	µA
	I_{LOAD} = 1mA	●		55	100	µA
	I_{LOAD} = 10mA	●		230	400	µA
	I_{LOAD} = 50mA	●		1	2	mA
	I_{LOAD} = 100mA	●		2.2	4	mA
Output Voltage Noise	C_{OUT} = 10µF, C_{BYP} = 0.01µF, I_{LOAD} = 100mA, BW = 10Hz to 100kHz			20		μV_{RMS}
ADJ1/ADJ2 Pin Bias Current	(Notes 3, 8)			30	100	nA
Shutdown Threshold	V_{OUT} = Off to On	●		0.8	1.4	V
	V_{OUT} = On to Off	●	0.25	0.65		V
$\overline{SHDN1}/\overline{SHDN2}$ Pin Current (Note 9)	$V_{\overline{SHDN}}$ = 0V	●		0	0.5	µA
	$V_{\overline{SHDN}}$ = 20V	●		1	3	µA
Quiescent Current in Shutdown	V_{IN} = 6V, $V_{\overline{SHDN}}$ = 0V (Both $\overline{SHDN}$ Pins)			0.01	0.1	µA
Ripple Rejection (Note 3)	V_{IN} = 2.72V (Avg), V_{RIPPLE} = 0.5V_{P-P}, f_{RIPPLE} = 120Hz, I_{LOAD} = 50mA		55	65		dB
Current Limit	V_{IN} = 7V, V_{OUT} = 0V			200		mA
	V_{IN} = 2.3V, ΔV_{OUT} = –5%	●	110			mA
Input Reverse Leakage Current	V_{IN} = –20V, V_{OUT} = 0V	●			1	mA
Reverse Output Current (Notes 3,10)	V_{OUT} = 1.22V, V_{IN} < 1.22V			5	10	µA

Note 1: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to any Absolute Maximum Rating condition for extended periods may affect device reliability and lifetime.

Note 2: The LT3023 is tested and specified under pulse load conditions such that $T_J \cong T_A$. The LT3023E is 100% tested at T_A = 25°C. Performance at –40°C and 125°C is assured by design, characterization and correlation with statistical process controls. The LT3023I is guaranteed over the full –40°C to 125°C operating junction temperature range.

Note 3: The LT3023 is tested and specified for these conditions with the ADJ1/ADJ2 pin connected to the corresponding OUT1/OUT2 pin.

Note 4: Operating conditions are limited by maximum junction temperature. The regulated output voltage specification will not apply for all possible combinations of input voltage and output current. When operating at maximum input voltage, the output current range must be limited. When operating at maximum output current, the input voltage range must be limited.

Note 5: To satisfy requirements for minimum input voltage, the LT3023 is tested and specified for these conditions with an external resistor divider (two 250k resistors) for an output voltage of 2.44V. The external resistor divider will add a 5µA DC load on the output.

Note 6: Dropout voltage is the minimum input to output voltage differential needed to maintain regulation at a specified output current. In dropout, the output voltage will be equal to: $V_{IN} – V_{DROPOUT}$.

Note 7: GND pin current is tested with V_{IN} = 2.44V and a current source load. This means the device is tested while operating in its dropout region or at the minimum input voltage specification. This is the worst-case GND pin current. The GND pin current will decrease slightly at higher input voltages.

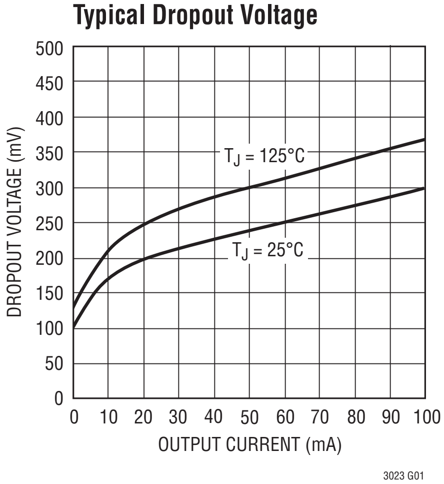
Note 8: ADJ1 and ADJ2 pin bias current flows into the pin.

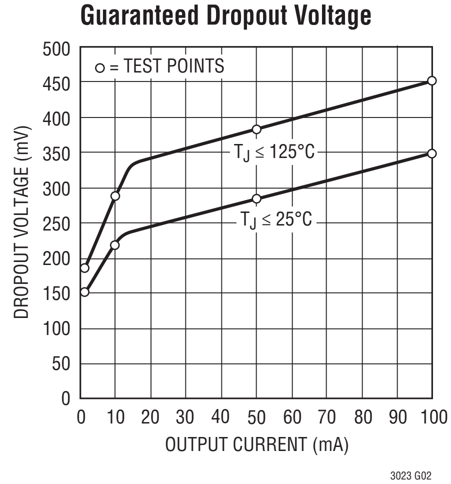
Note 9: $\overline{SHDN1}$ and $\overline{SHDN2}$ pin current flows into the pin.

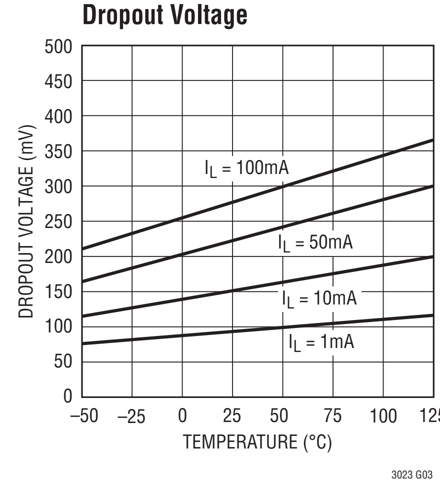
Note 10: Reverse output current is tested with the IN pin grounded and the OUT pin forced to the rated output voltage. This current flows into the OUT pin and out the GND pin.

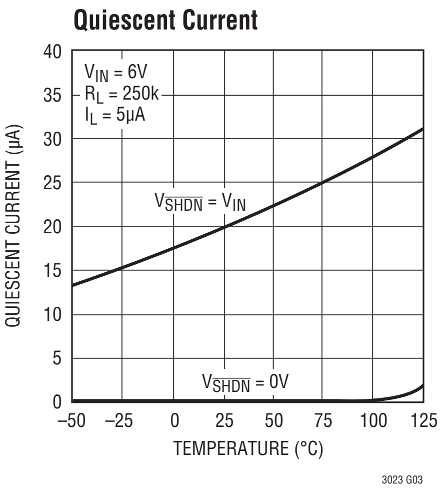
Note 11: For the LT3023 dropout voltage will be limited by the minimum input voltage specification under some output voltage/load conditions. See the curve of Minimum Input Voltage in the Typical Performance Characteristics.

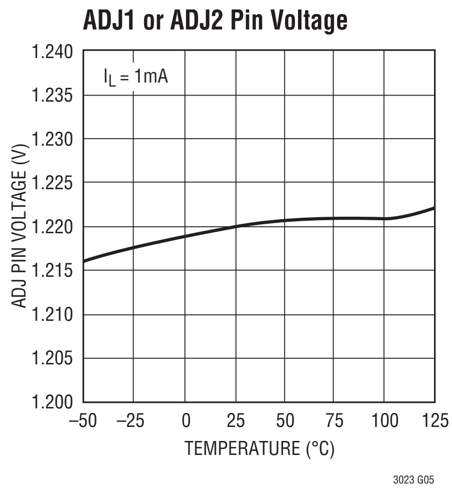
TYPICAL PERFORMANCE CHARACTERISTICS

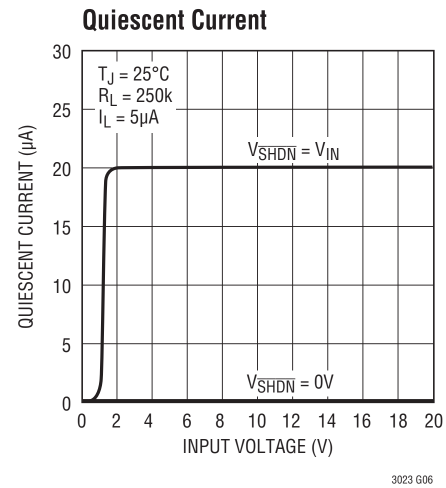


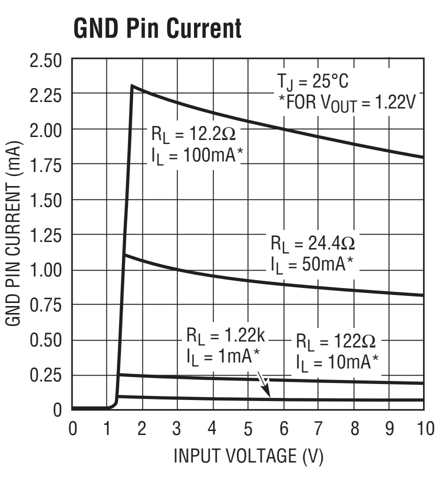


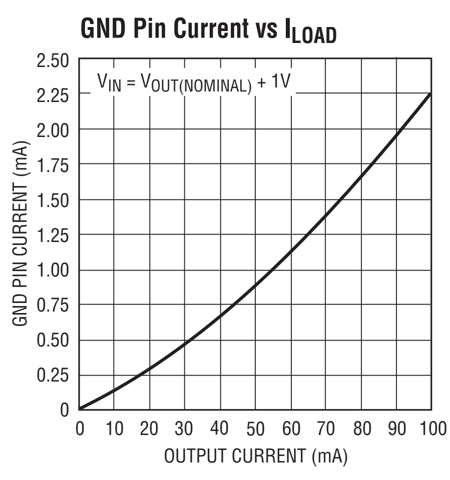


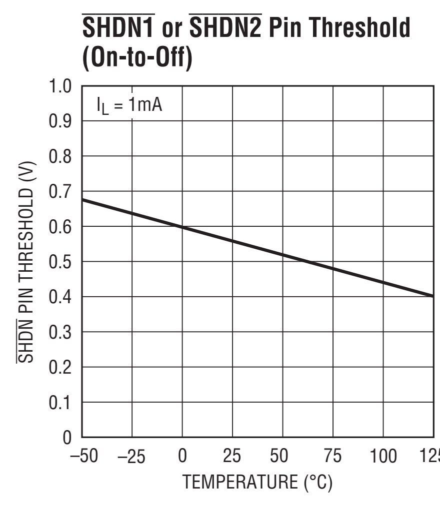






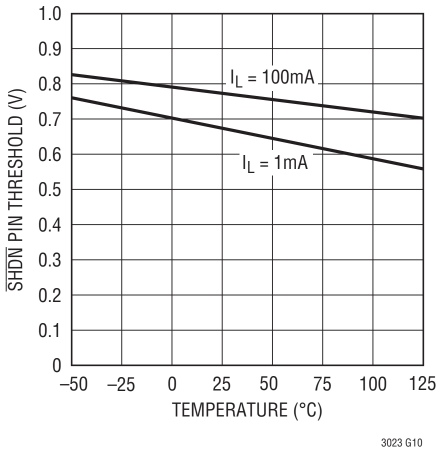




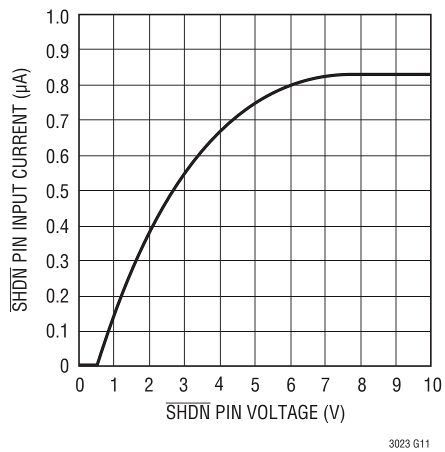


TYPICAL PERFORMANCE CHARACTERISTICS

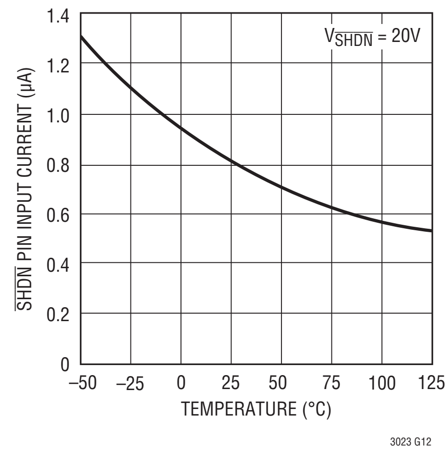
$\overline{SHDN1}$ or $\overline{SHDN2}$ Pin Threshold (Off-to-On)



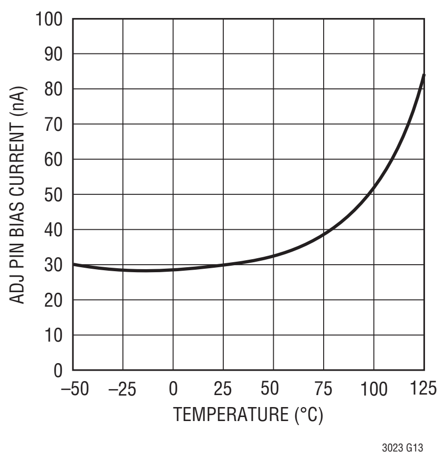
$\overline{SHDN1}$ or $\overline{SHDN2}$ Pin Input Current



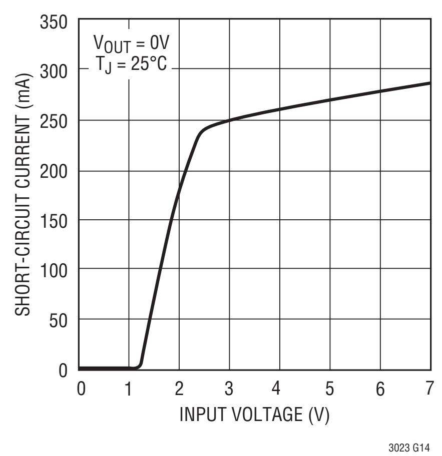
$\overline{SHDN1}$ or $\overline{SHDN2}$ Pin Input Current



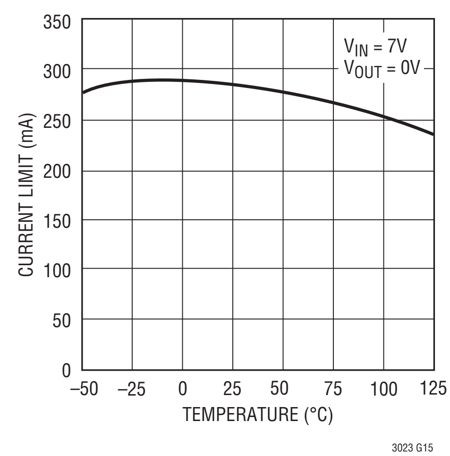
ADJ1 or ADJ2 Pin Bias Current



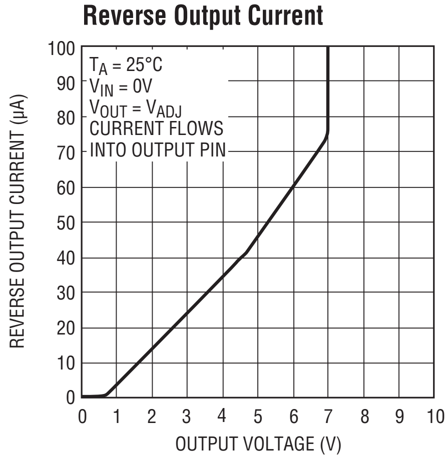
Current Limit



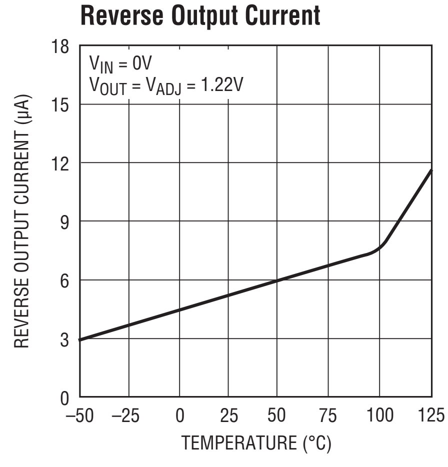
Current Limit



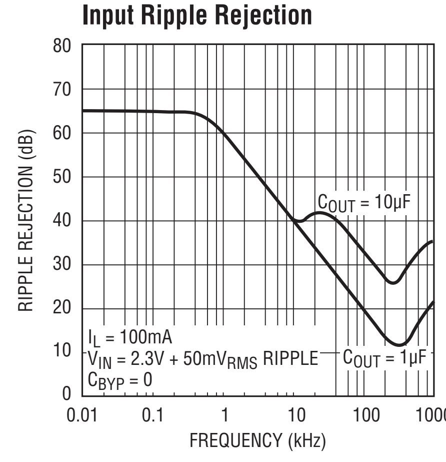
Reverse Output Current



Reverse Output Current

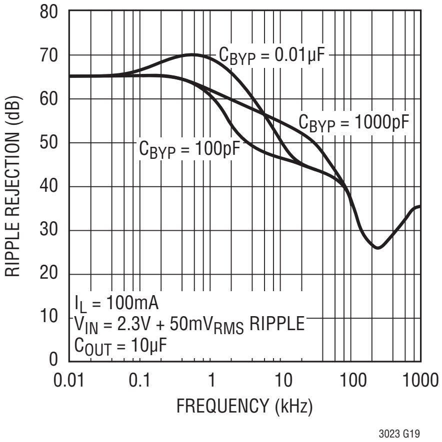


Input Ripple Rejection

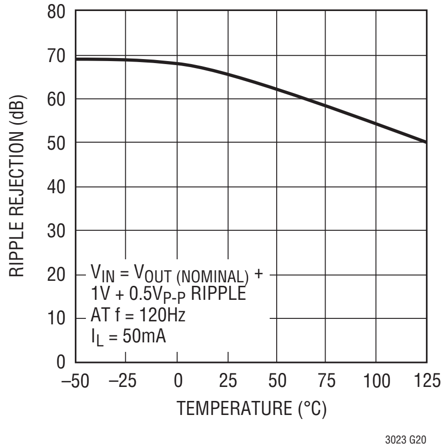


TYPICAL PERFORMANCE CHARACTERISTICS

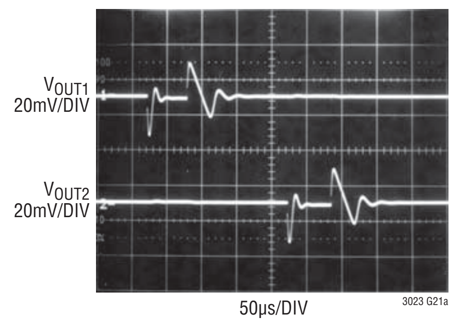
Input Ripple Rejection



Input Ripple Rejection

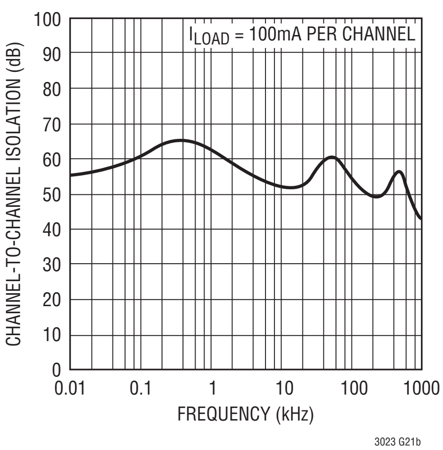


Channel-to-Channel Isolation

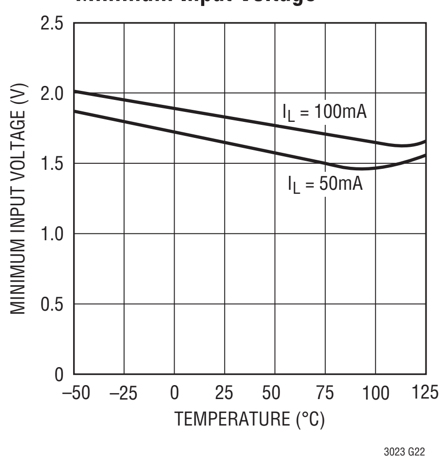


C_{OUT1}, C_{OUT2} = 10µF
C_{BYP1}, C_{BYP2} = 0.01µF
ΔI_{L1} = 10mA to 100mA
ΔI_{L2} = 10mA to 100mA
V_{IN} = 6V, V_{OUT1} = V_{OUT2} = 5V

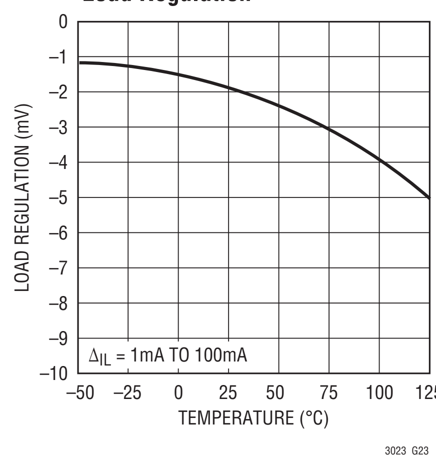
Channel-to-Channel Isolation



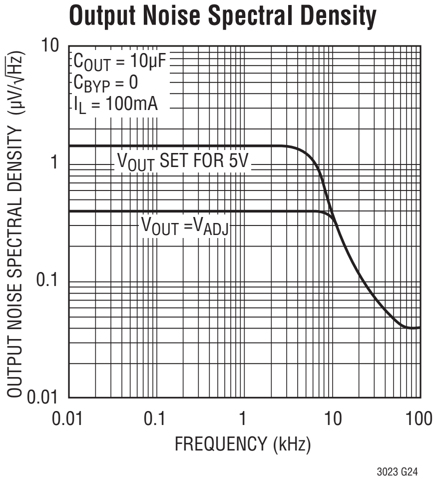
Minimum Input Voltage



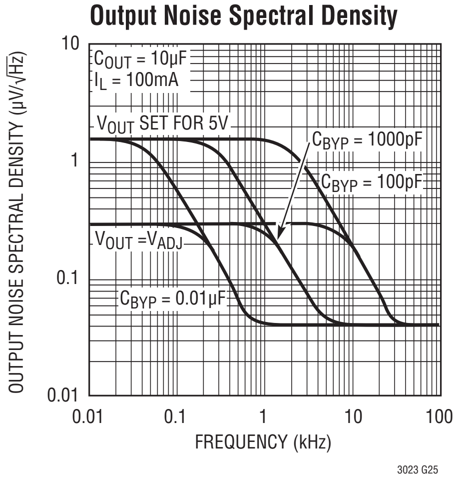
Load Regulation



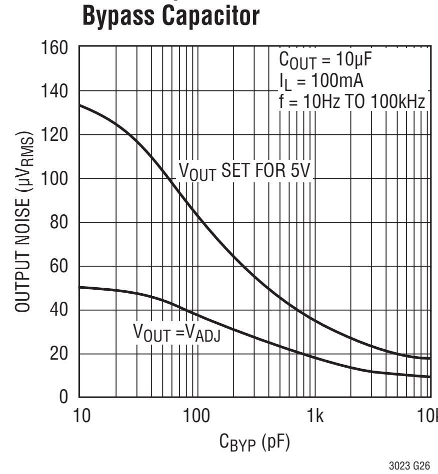
Output Noise Spectral Density



Output Noise Spectral Density

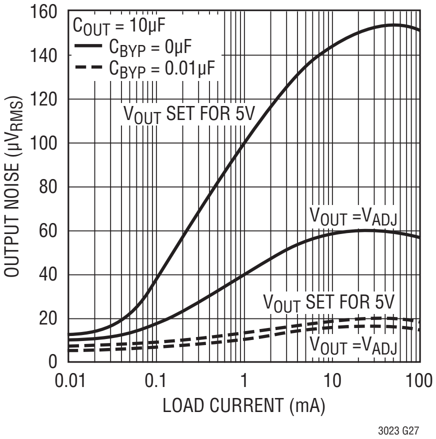


RMS Output Noise vs Bypass Capacitor

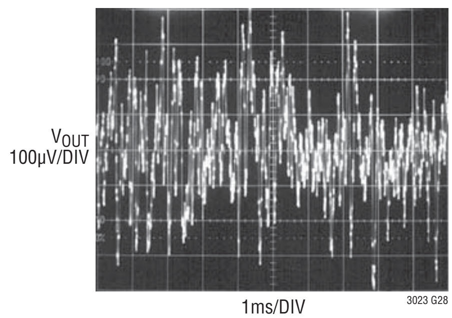


TYPICAL PERFORMANCE CHARACTERISTICS

RMS Output Noise vs Load Current (10Hz to 100kHz)

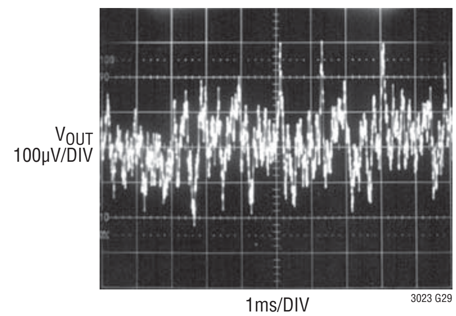


10Hz to 100kHz Output Noise $C_{BYP} = 0$



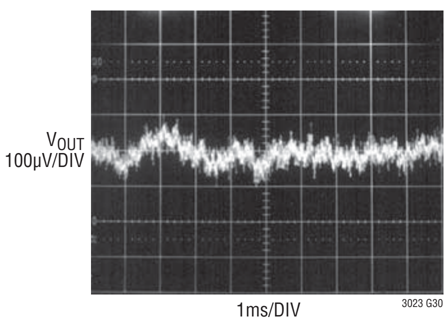
C_{OUT} = 10µF
I_L = 100mA
V_{OUT} SET FOR 5V OUT

10Hz to 100kHz Output Noise C_{BYP} = 100pF



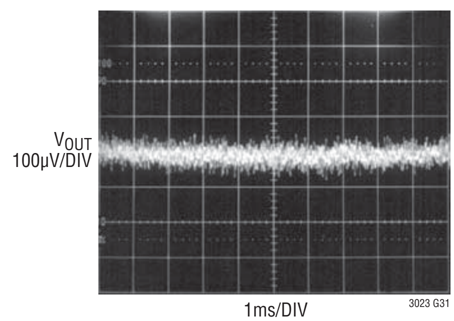
C_{OUT} = 10µF
I_L = 100mA
V_{OUT} SET FOR 5V OUT

10Hz to 100kHz Output Noise C_{BYP} = 1000pF



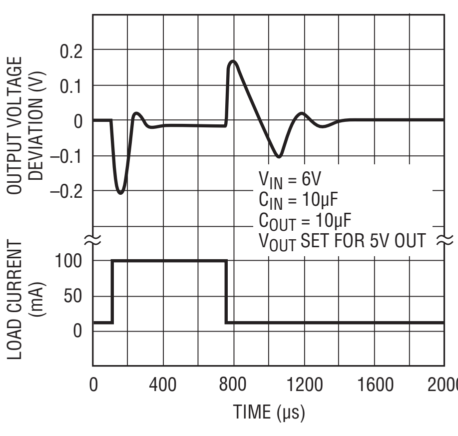
C_{OUT} = 10µF
I_L = 100mA
V_{OUT} SET FOR 5V OUT

10Hz to 100kHz Output Noise C_{BYP} = 0.01µF

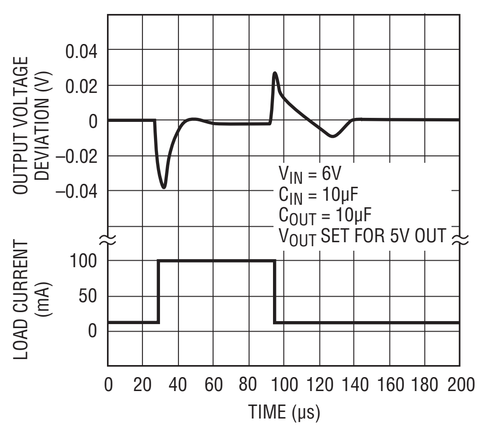


C_{OUT} = 10µF
I_L = 100mA
V_{OUT} SET FOR 5V OUT

Transient Response $C_{BYP} = 0$



Transient Response C_{BYP} = 0.01µF



PIN FUNCTIONS

GND (Pin 3): Ground.

ADJ1/ADJ2 (Pins 4/2): Adjust Pin. These are the inputs to the error amplifiers. These pins are internally clamped to ± 7V. They have a bias current of 30nA which flows into the pin (see curve of ADJ1/ADJ2 Pin Bias Current vs Temperature in the Typical Performance Characteristics section). The ADJ1 and ADJ2 pin voltage is 1.22V referenced to ground and the output voltage range is 1.22V to 20V.

BYP1/BYP2 (Pins 5/1): Bypass. The BYP1/BYP2 pins are used to bypass the reference of the LT3023 regulator to achieve low noise performance from the regulator. The BYP1/BYP2 pins are clamped internally to ±0.6V (one V_{BE}) from ground. A small capacitor from the corresponding output to this pin will bypass the reference to lower the output voltage noise. A maximum value of 0.01µF can be used for reducing output voltage noise to a typical 20µV_{RMS} over a 10Hz to 100kHz bandwidth. If not used, this pin must be left unconnected.

OUT1/OUT2 (Pins 6/10): Output. The outputs supply power to the loads. A minimum output capacitor of 1µF is required to prevent oscillations. Larger output capacitors will be required for applications with large transient loads to limit peak voltage transients. See the Applications Information section for more information on output capacitance and reverse output characteristics.

$\overline{\text{SHDN1}}$/$\overline{\text{SHDN2}}$ (Pins 7/9): Shutdown. The $\overline{\text{SHDN1}}$/$\overline{\text{SHDN2}}$ pins are used to put the corresponding channel of the LT3023 regulator into a low power shutdown state. The output will be off when the pin is pulled low. The $\overline{\text{SHDN1}}$/$\overline{\text{SHDN2}}$ pins can be driven either by 5V logic or open-collector logic with pull-up resistors. The pull-up resistors are required to supply the pull-up current of the open-collector gates, normally several microamperes, and the $\overline{\text{SHDN1}}$/$\overline{\text{SHDN2}}$ pin current, typically 1µA. If unused, the pin must be connected to V_{IN}. The device will not function if the $\overline{\text{SHDN1}}$/$\overline{\text{SHDN2}}$ pins are not connected.

IN (Pin 8): Input. Power is supplied to the device through the IN pin. A bypass capacitor is required on this pin if the device is more than six inches away from the main input filter capacitor. In general, the output impedance of a battery rises with frequency, so it is advisable to include a bypass capacitor in battery-powered circuits. A bypass capacitor in the range of 1µF to 10µF is sufficient. The LT3023 regulator is designed to withstand reverse voltages on the IN pin with respect to ground and the OUT pin. In the case of a reverse input, which can happen if a battery is plugged in backwards, the device will act as if there is a diode in series with its input. There will be no reverse current flow into the regulator and no reverse voltage will appear at the load. The device will protect both itself and the load.

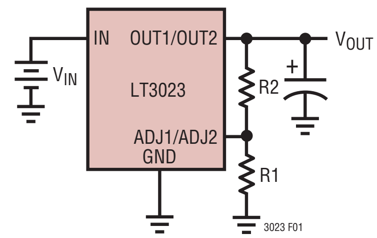
Exposed Pad (Pin 11): Ground. This pin must be soldered to the PCB and electrically connected to ground.

APPLICATIONS INFORMATION

The LT3023 is a dual 100mA low dropout regulator with micropower quiescent current and shutdown. The device is capable of supplying 100mA per channel at a dropout voltage of 300mV. Output voltage noise can be lowered to $20\mu V_{RMS}$ over a 10Hz to 100kHz bandwidth with the addition of a 0.01µF reference bypass capacitor. Additionally, the reference bypass capacitor will improve transient response of the regulator, lowering the settling time for transient load conditions. The low operating quiescent current (20µA per channel) drops to less than 1µA in shutdown. In addition to the low quiescent current, the LT3023 regulator incorporates several protection features which make it ideal for use in battery-powered systems. The device is protected against both reverse input and reverse output voltages. In battery backup applications where the output can be held up by a backup battery when the input is pulled to ground, the LT3023 acts like it has a diode in series with its output and prevents reverse current flow. Additionally, in dual supply applications where the regulator load isreturned to a negative supply, the output can be pulled below ground by as much as 20V and still allow the device to start and operate.

Adjustable Operation

The LT3023 has an output voltage range of 1.22V to 20V. The output voltage is set by the ratio of two external resistors as shown in Figure 1. The device servos the output to maintain the corresponding ADJ1/ADJ2 pin voltage at 1.22V referenced to ground. The current in R1 is then equal to 1.22V/R1 and the current in R2 is the current in R1 plus the ADJ1/ADJ2 pin bias current. The ADJ1/ADJ2 pin bias current, 30nA at 25°C, flows through R2 into the ADJ1/ADJ2 pin. The output voltage can be calculated using the formula in Figure 1. The value of R1 should be no greater than 250k to minimize errors in the output voltage caused by the ADJ1/ADJ2 pin bias current. Note that in shutdown the output is turned off and the divider current will be zero. Curves of ADJ1/ADJ2 Pin Voltage vs Temperature and ADJ1/ADJ2 Pin Bias Current vs Temperature appear in the Typical Performance Characteristics.



$V_{OUT} = 1.22V\left(1+\frac{R2}{R1}\right)+(I_{ADJ})(R2)$

$V_{ADJ} = 1.22V$

$I_{ADJ} = 30nA$ AT 25°C

OUTPUT RANGE = 1.22V TO 20V

Figure 1. Adjustable Operation

The device is tested and specified with the ADJ1/ADJ2 pin tied to the corresponding OUT1/OUT2 pin for an output voltage of 1.22V. Specifications for output voltages greater than 1.22V will be proportional to the ratio of the desired output voltage to 1.22V: V_{OUT}/1.22V. For example, load regulation for an output current change of 1mA to 100mA is –1mV typical at V_{OUT} = 1.22V. At V_{OUT} = 12V, load regulation is:

(12V/1.22V)(–1mV) = –9.8mV

Bypass Capacitance and Low Noise Performance

The LT3023 regulator may be used with the addition of a bypass capacitor from V_{OUT} to the corresponding BYP1/BYP2 pin to lower output voltage noise. A good quality low leakage capacitor is recommended. This capacitor will bypass the reference of the regulator, providing a low frequency noise pole. The noise pole provided by this bypass capacitor will lower the output voltage noise to as low as $20\mu V_{RMS}$ with the addition of a 0.01µF bypass capacitor. Using a bypass capacitor has the added benefit of improving transient response. With no bypass capacitor and a 10µF output capacitor, a 10mA to 100mA load step will settle to within 1% of its final value in less than 100µs. With the addition of a 0.01µF bypass capacitor, the output will stay within 1% for a 10mA to 100mA load step (see Transient Reponse in Typical Performance Characteristics section). However, regulator start-up time is proportional to the size of the bypass capacitor, slowing to 15ms with a 0.01µF bypass capacitor and 10µF output capacitor.

APPLICATIONS INFORMATION

Output Capacitance and Transient Response

The LT3023 regulator is designed to be stable with a wide range of output capacitors. The ESR of the output capacitor affects stability, most notably with small capacitors. A minimum output capacitor of 1µF with an ESR of 3Ω or less is recommended to prevent oscillations. The LT3023 is a micropower device and output transient response will be a function of output capacitance. Larger values of output capacitance decrease the peak deviations and provide improved transient response for larger load current changes. Bypass capacitors, used to decouple individual components powered by the LT3023, will increase the effective output capacitor value. With larger capacitors used to bypass the reference (for low noise operation), larger values of output capacitors are needed. For 100pF of bypass capacitance, 2.2µF of output capacitor is recommended. With a 330pF bypass capacitor or larger, a 3.3µF output capacitor is recommended. The shaded region of Figure 2 defines the region over which the LT3023 regulator is stable. The minimum ESR needed is defined by the amount of bypass capacitance used, while the maximum ESR is 3Ω.

Extra consideration must be given to the use of ceramic capacitors. Ceramic capacitors are manufactured with a variety of dielectrics, each with different behavior across temperature and applied voltage. The most common dielectrics used are specified with EIA temperature characteristic codes of Z5U, Y5V, X5R and X7R. The Z5U and Y5V dielectrics are good for providing high capacitances in a small package, but they tend to have strong voltage and temperature coefficients as shown in Figures 3 and 4. When used with a 5V regulator, a 16V 10µF Y5V capacitor can exhibit an effective value as low as 1µF to 2µF for the DC bias voltage applied and over the operating temperature range. The X5R and X7R dielectrics result in more stable characteristics and are more suitable for use as the output capacitor. The X7R type has better stability across temperature, while the X5R is less expensive and is available in higher values. Care still must be exercised when using X5R and X7R capacitors; the X5R and X7R codes only specify operating temperature range and maximum capacitance change over temperature. Capacitance change due to DC bias with X5R and X7R capacitors is better than Y5V and Z5U capacitors, but can still be significant enough to drop capacitor values below appropriate levels. Capacitor DC bias characteristics tend to improve as component

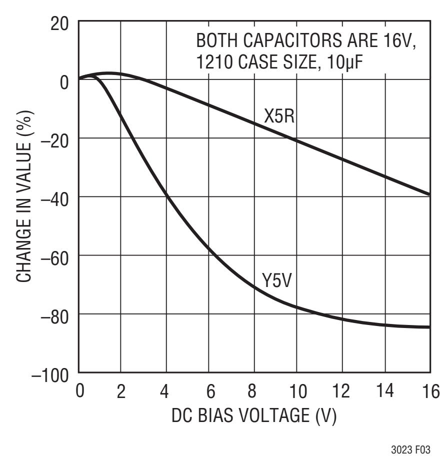


Figure 3. Ceramic Capacitor DC Bias Characteristics

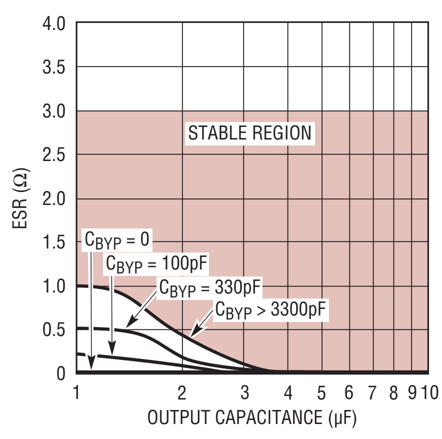


Figure 2. Stability

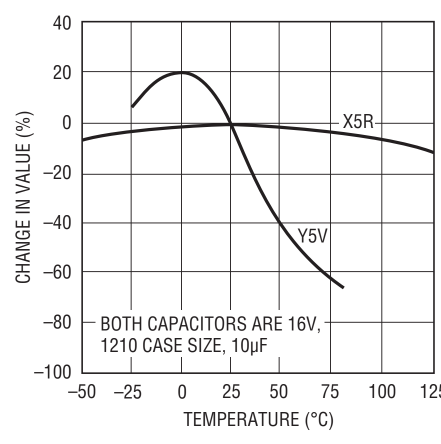


Figure 4. Ceramic Capacitor Temperature Characteristics

APPLICATIONS INFORMATION

case size increases, but expected capacitance at operating voltage should be verified.

Voltage and temperature coefficients are not the only sources of problems. Some ceramic capacitors have a piezoelectric response. A piezoelectric device generates voltage across its terminals due to mechanical stress, similar to the way a piezoelectric accelerometer or microphone works. For a ceramic capacitor the stress can be induced by vibrations in the system or thermal transients. The resulting voltages produced can cause appreciable amounts of noise, especially when a ceramic capacitor is used for noise bypassing. A ceramic capacitor produced Figure 5's trace in response to light tapping from a pencil. Similar vibration induced behavior can masquerade as increased output voltage noise.

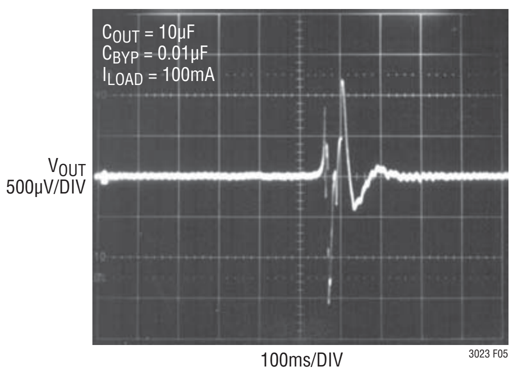


Figure 5. Noise Resulting from Tapping on a Ceramic Capacitor

Thermal Considerations

The power handling capability of the device will be limited by the maximum rated junction temperature (125°C). The power dissipated by the device will be made up of two components (for each channel):

1. Output current multiplied by the input/output voltage differential: $(I_{OUT})(V_{IN} – V_{OUT})$, and
2. GND pin current multiplied by the input voltage: $(I_{GND})(V_{IN})$.

The ground pin current can be found by examining the GND Pin Current curves in the Typical Performance Characteristics section. Power dissipation will be equal to the sum of the two components listed above. Power dissipation from both channels must be considered during thermal analysis.

The LT3023 regulator has internal thermal limiting designed to protect the device during overload conditions. For continuous normal conditions, the maximum junction temperature rating of 125°C must not be exceeded. It is important to give careful consideration to all sources of thermal resistance from junction to ambient. Additional heat sources mounted nearby must also be considered.

For surface mount devices, heat sinking is accomplished by using the heat spreading capabilities of the PC board and its copper traces. Copper board stiffeners and plated through-holes can also be used to spread the heat generated by power devices.

The following tables list thermal resistance for several different board sizes and copper areas. All measurements were taken in still air on 3/32" FR-4 board with one ounce copper.

Table 1. MSE Package, 10-Lead MSOP

COPPER AREA			
TOPSIDE*	BACKSIDE	BOARD AREA	THERMAL RESISTANCE (JUNCTION-TO-AMBIENT)
2500mm^2	2500mm^2	2500mm^2	40°C/W
1000mm^2	2500mm^2	2500mm^2	45°C/W
225mm^2	2500mm^2	2500mm^2	50°C/W
100mm^2	2500mm^2	2500mm^2	62°C/W

*Device is mounted on topside.

Table 2. DD Package, 10-Lead DFN

COPPER AREA			
TOPSIDE*	BACKSIDE	BOARD AREA	THERMAL RESISTANCE (JUNCTION-TO-AMBIENT)
2500mm^2	2500mm^2	2500mm^2	40°C/W
1000mm^2	2500mm^2	2500mm^2	45°C/W
225mm^2	2500mm^2	2500mm^2	50°C/W
100mm^2	2500mm^2	2500mm^2	62°C/W

*Device is mounted on topside.

The thermal resistance juncton-to-case (θ_{JC}), measured at the Exposed Pad on the back of the die is 10°C/W.

APPLICATIONS INFORMATION

Calculating Junction Temperature

Example: Given an output voltage on the first channel of 3.3V, an output voltage of 2.5V on the second channel, an input voltage range of 4V to 6V, output current ranges of 0mA to 100mA for the first channel and 0mA to 50mA for the second channel, with a maximum ambient temperature of 50°C, what will the maximum junction temperature be?

The power dissipated by each channel of the device will be equal to:

$I_{OUT(MAX)}(V_{IN(MAX)} – V_{OUT}) + I_{GND}(V_{IN(MAX)})$

where (for the first channel):

$I_{OUT(MAX)}$ = 100mA
$V_{IN(MAX)}$ = 6V
I_{GND} at (I_{OUT} = 100mA, V_{IN} = 6V) = 2mA

so:

P1 = 100mA(6V – 3.3V) + 2mA(6V) = 0.28W

and (for the second channel):

$I_{OUT(MAX)}$ = 50mA
$V_{IN(MAX)}$ = 6V
I_{GND} at (I_{OUT} = 50mA, V_{IN} = 6V) = 1mA

so:

P2 = 50mA(6V – 2.5V) + 1mA(6V) = 0.18W

The thermal resistance will be in the range of 40°C/W to 60°C/W depending on the copper area. So the junction temperature rise above ambient will be approximately equal to:

(0.28W + 018W)(60°C/W) = 27.8°C

The maximum junction temperature will then be equal to the maximum junction temperature rise above ambient plus the maximum ambient temperature or:

T_{JMAX} = 50°C + 27.8°C = 77.8°C

Protection Features

The LT3023 regulator incorporates several protection features which makes it ideal for use in battery-powered circuits. In addition to the normal protection features associated with monolithic regulators, such as current limiting and thermal limiting, the devices are protected against reverse input voltages, reverse output voltages and reverse voltages from output to input.

Current limit protection and thermal overload protection are intended to protect the device against current overload conditions at the output of the device. For normal operation, the junction temperature should not exceed 125°C.

The input of the device will withstand reverse voltages of 20V. Current flow into the device will be limited to less than 1mA (typically less than 100µA) and no negative voltage will appear at the output. The device will protect both itself and the load. This provides protection against batteries which can be plugged in backward.

The output of the LT3023 can be pulled below ground without damaging the device. If the input is left open circuit or grounded, the output can be pulled below ground by 20V. The output will act like an open circuit; no current will flow out of the pin. If the input is powered by a voltage source, the output will source the short-circuit current of the device and will protect itself by thermal limiting. In this case, grounding the $\overline{SHDN1}$/$\overline{SHDN2}$ pins will turn off the device and stop the output from sourcing the short-circuit current.

The ADJ1 and ADJ2 pins can be pulled above or below ground by as much as 7V without damaging the device. If the input is left open circuit or grounded, the ADJ1 and ADJ2 pins will act like an open circuit when pulled below ground and like a large resistor (typically 100k) in series with a diode when pulled above ground.

In situations where the ADJ1 and ADJ2 pins are connected to a resistor divider that would pull the pins above their 7V clamp voltage if the output is pulled high, the ADJ1/ADJ2 pin input current must be limited to less than 5mA. For example, a resistor divider is used to provide a regulated 1.5V output from the 1.22V reference when the output is forced to 20V. The top resistor of the resistor divider must be chosen to limit the current into the ADJ pin to less than 5mA when the ADJ1/ADJ2 pin is at 7V. The 13V difference between output and ADJ1/ADJ2 pin divided by the 5mA maximum current into the ADJ1/ADJ2 pin yields a minimum top resistor value of 2.6k.

APPLICATIONS INFORMATION

In circuits where a backup battery is required, several different input/output conditions can occur. The output voltage may be held up while the input is either pulled to ground, pulled to some intermediate voltage or is left open circuit. Current flow back into the output will follow the curve shown in Figure 6.

When the IN pin of the LT3023 is forced below the OUT1 or OUT2 pins or the OUT1/OUT2 pins are pulled above the IN pin, input current will typically drop to less than 2μA. This can happen if the input of the device is connected to a discharged (low voltage) battery and the output is held up by either a backup battery or a second regulator circuit. The state of the $\overline{SHDN1}/\overline{SHDN2}$ pins will have no effect on the reverse output current when the output is pulled above the input.

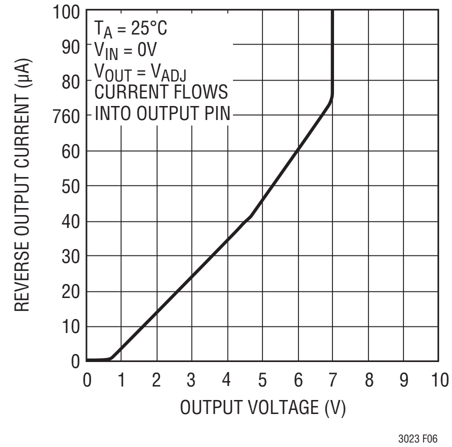
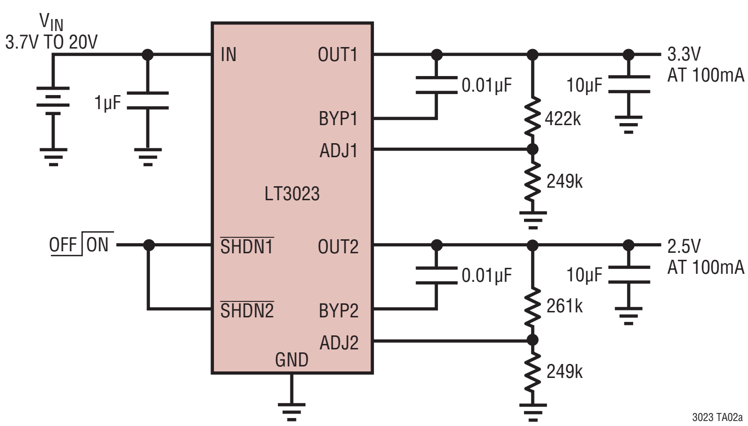
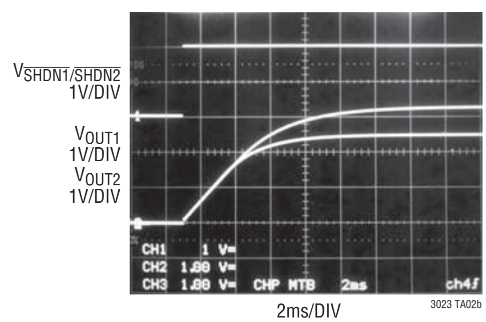


Figure 6. Reverse Output Current

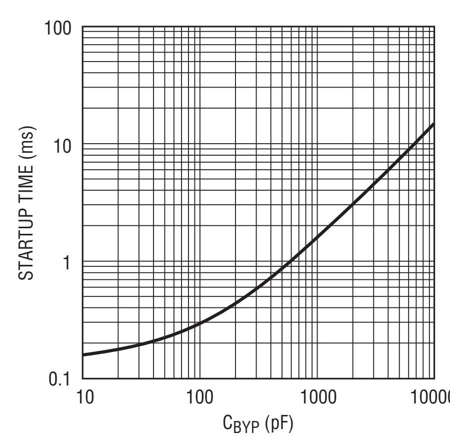
TYPICAL APPLICATIONS

Noise Bypassing Slows Startup, Allows Outputs to Track



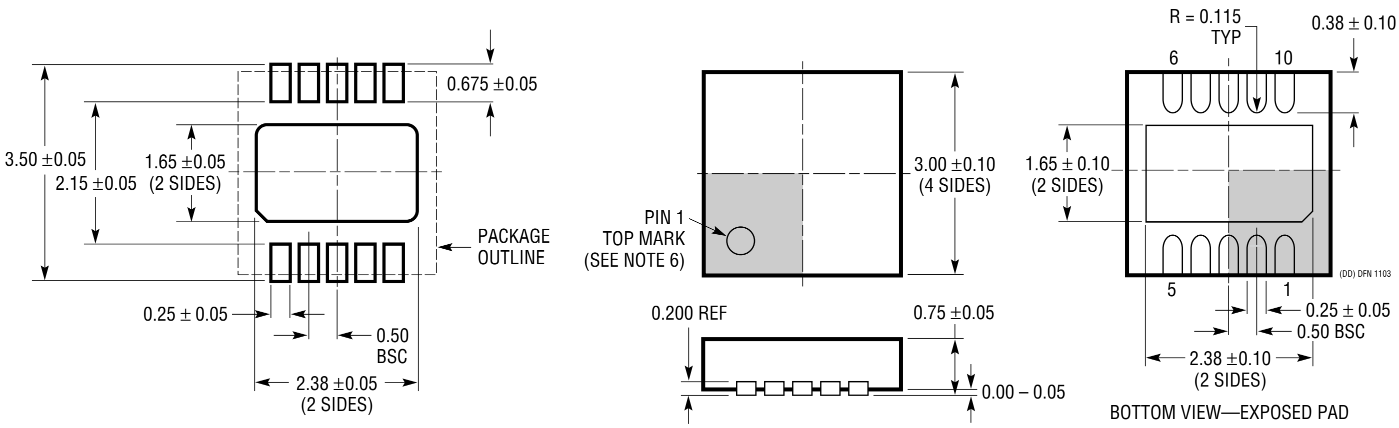


Startup Time



PACKAGE DESCRIPTION

DD Package
10-Lead Plastic DFN (3mm × 3mm)
(Reference LTC DWG # 05-08-1699)

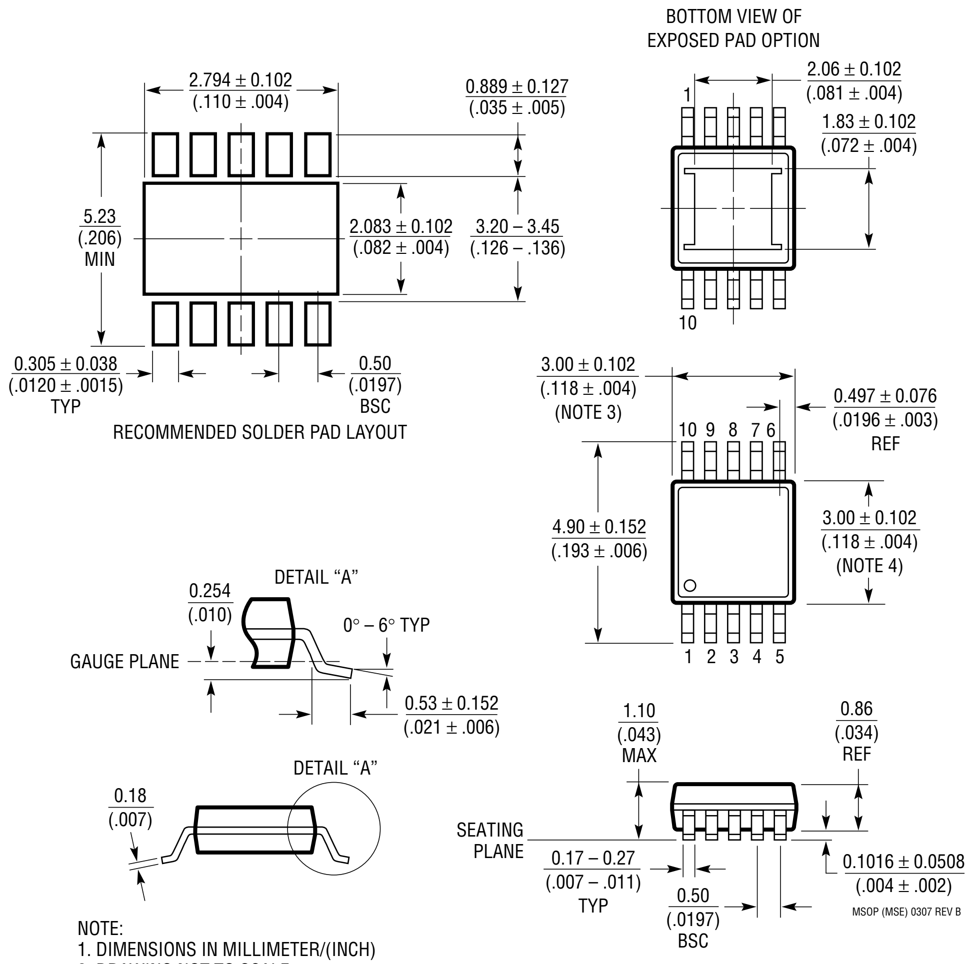


RECOMMENDED SOLDER PAD PITCH AND DIMENSIONS

NOTE:
1. DRAWING TO BE MADE A JEDEC PACKAGE OUTLINE M0-229 VARIATION OF (WEED-2). CHECK THE LTC WEBSITE DATA SHEET FOR CURRENT STATUS OF VARIATION ASSIGNMENT
2. DRAWING NOT TO SCALE
3. ALL DIMENSIONS ARE IN MILLIMETERS
4. DIMENSIONS OF EXPOSED PAD ON BOTTOM OF PACKAGE DO NOT INCLUDE MOLD FLASH. MOLD FLASH, IF PRESENT, SHALL NOT EXCEED 0.15mm ON ANY SIDE
5. EXPOSED PAD SHALL BE SOLDER PLATED
6. SHADED AREA IS ONLY A REFERENCE FOR PIN 1 LOCATION ON THE TOP AND BOTTOM OF PACKAGE

PACKAGE DESCRIPTION

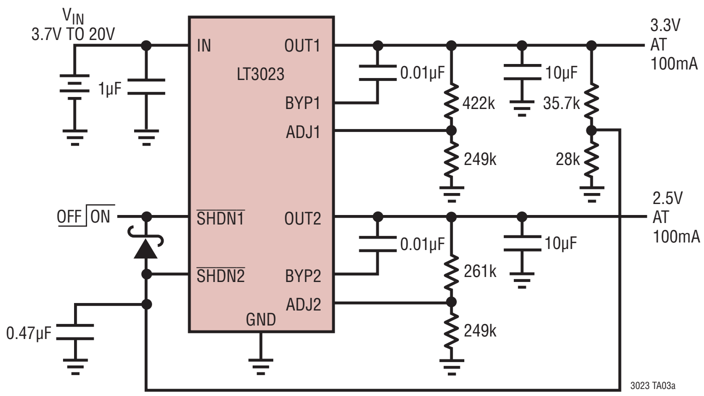
MSE Package
10-Lead Plastic MSOP, Exposed Die Pad
(Reference LTC DWG # 05-08-1664 Rev B)



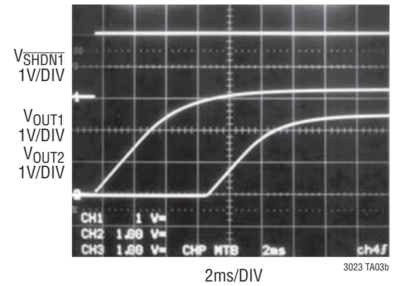
NOTE:
1. DIMENSIONS IN MILLIMETER/(INCH)
2. DRAWING NOT TO SCALE
3. DIMENSION DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS.
MOLD FLASH, PROTRUSIONS OR GATE BURRS SHALL NOT EXCEED 0.152mm (.006") PER SIDE
4. DIMENSION DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSIONS.
INTERLEAD FLASH OR PROTRUSIONS SHALL NOT EXCEED 0.152mm (.006") PER SIDE
5. LEAD COPLANARITY (BOTTOM OF LEADS AFTER FORMING) SHALL BE 0.102mm (.004") MAX

TYPICAL APPLICATION

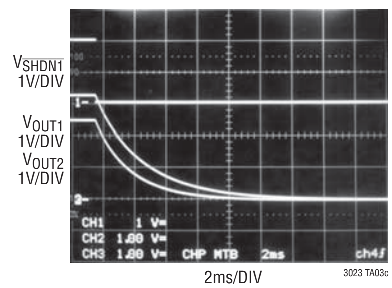
Startup Sequencing



Turn-On Waveforms



Turn-Off Waveforms



RELATED PARTS

PART NUMBER	DESCRIPTION	COMMENTS
LT1129	700mA, Micropower, LDO	V_{IN}: 4.2V to 30V, $V_{OUT(MIN)}$ = 3.75V, I_Q = 50µA, I_{SD} = 16µA, DD, SOT-223, S8,TO220, TSSOP20 Packages
LT1175	500mA, Micropower Negative LDO	Guaranteed Voltage Tolerance and Line/Load Regulation, V_{IN}: –20V to –4.3V, $V_{OUT(MIN)}$ = –3.8V, I_Q = 45µA, I_{SD} = 10µA, DD,SOT-223, S8 Packages
LT1185	3A, Negative LDO	Accurate Programmable Current Limit, Remote Sense, V_{IN}: –35V to –4.2V, $V_{OUT(MIN)}$ = –2.40V, I_Q = 2.5mA, I_{SD} <1µA, TO220-5 Package
LT1761	100mA, Low Noise Micropower, LDO	Low Noise < 20µ$V_{RMS,}$ Stable with 1µF Ceramic Capacitors, V_{IN}: 1.8V to 20V, $V_{OUT(MIN)}$ = 1.22V, I_Q = 20µA, I_{SD} <1µA, ThinSOT Package
LT1762	150mA, Low Noise Micropower, LDO	Low Noise < 20µ$V_{RMS,}$ V_{IN}: 1.8V to 20V, $V_{OUT(MIN)}$ = 1.22V, I_Q = 25µA, I_{SD} <1µA, MS8 Package
LT1763	500mA, Low Noise Micropower, LDO	Low Noise < 20µ$V_{RMS,}$ V_{IN}: 1.8V to 20V, $V_{OUT(MIN)}$ = 1.22V, I_Q = 30µA, I_{SD} <1µA, S8 Package
LT1764/LT1764A	3A, Low Noise, Fast Transient Response, LDO	Low Noise < 40µ$V_{RMS,}$ "A" Version Stable with Ceramic Capacitors, V_{IN}: 2.7V to 20V, $V_{OUT(MIN)}$ = 1.21V, I_Q = 1mA, I_{SD} <1µA, DD, TO220 Packages
LTC1844	150mA, Very Low Drop-Out LDO	Low Noise < 30µV_{RMS}, Stable with 1µF Ceramic Capacitors, V_{IN}: 1.6V to 6.5V, $V_{OUT(MIN)}$ = 1.25V, I_Q = 40µA, I_{SD} <1µA, ThinSOT Package
LT1962	300mA, Low Noise Micropower, LDO	Low Noise < 20µ$V_{RMS,}$ V_{IN}: 1.8V to 20V, $V_{OUT(MIN)}$ = 1.22V, I_Q = 30µA, I_{SD} <1µA, MS8 Package
LT1963/LT1963A	1.5A, Low Noise, Fast Transient Response, LDO	Low Noise < 40µ$V_{RMS,}$ "A" Version Stable with Ceramic Capacitors, V_{IN}: 2.1V to 20V, $V_{OUT(MIN)}$ = 1.21V, I_Q = 1mA, I_{SD} <1µA, DD, TO220, SOT-223, S8 Packages
LT1964	200mA, Low Noise Micropower, Negative LDO	Low Noise < 30µ$V_{RMS,}$ Stable with Ceramic Capacitors, V_{IN}: –0.9V to –20V, $V_{OUT(MIN)}$ = –1.21V, I_Q = 30µA, I_{SD} = 3µA, ThinSOT Package
LTC3407	Dual 600mA. 1.5MHz Synchronous Step Down DC/DC Converter	V_{IN}: 2.5V to 5.5V, $V_{OUT(MIN)}$ = 0.6 V, I_Q = 40µA, I_{SD} <1µA, MSE Package

3023fa

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