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September 2015

FAN2110 — 3-24 V Input, 10 A, High-Efficiency, Integrated Synchronous Buck Regulator

Features

- Wide Input Voltage Range: 3 V-24 V
- Wide Output Voltage Range: 0.8 V to 80% V_{IN}
- 10 A Output Current
- 1% Reference Accuracy Over Temperature
- Over 93% Peak Efficiency
- Programmable Frequency Operation: 200 KHz to 600 KHz
- Fully Synchronous Operation with Integrated Schottky Diode on Low-Side MOSFET Boosts Efficiency
- Internal Bootstrap Diode
- Power-Good Signal
- Starts up on Pre-Bias Outputs
- Accepts Ceramic Capacitors on Output
- External Compensation for Flexible Design
- Programmable Current Limit
- Under-Voltage, Over-Voltage, and Thermal Shutdown Protections
- Internal Soft-Start
- 5x6 mm, 25-Pin, 3-Pad MLP Package

Applications

- Servers & Telecom
- Graphics Cards & Displays
- Computing Systems
- Point-of-Load Regulation
- Set-Top Boxes & Game Consoles

Description

The FAN2110 is a highly efficient, small footprint, constant frequency, 10 A integrated synchronous Buck regulator.

The FAN2110 contains both synchronous MOSFETs and a controller/driver with optimized interconnects in one package, which enables designers to solve high-current requirements in a small area with minimal external components. Integration helps to minimize critical inductances making component layout simpler and more efficient compared to discrete solutions.

The FAN2110 provides for external loop compensation, programmable switching frequency, and current limit. These features allow design flexibility and optimization. High frequency operation allows for all ceramic solutions.

The summing current mode modulator uses lossless current sensing for current feedback and over-current protection. Voltage feedforward helps operation over a wide input voltage range.

Fairchild's advanced BiCMOS power process, combined with low-$R_{DS(ON)}$ internal MOSFETs and a thermally efficient MLP package, provide the ability to dissipate high power in a small package.

Output over-voltage, under-voltage, and thermal shutdown protections help protect the device from damage during fault conditions. FAN2110 also prevents pre-biased output discharge during startup in point-of-load applications.

Related Application Notes

TinyCalc™ Calculator Design Tool

AN-8022 — TinyCalc™ Calculator User Guide

Ordering Information

Part Number	Operating Temperature Range	Package	Packing Method
FAN2110MPX	-40°C to 85°C	Molded Leadless Package (MLP) 5 x 6 mm	Tape and Reel
FAN2110EMPX			

Typical Application

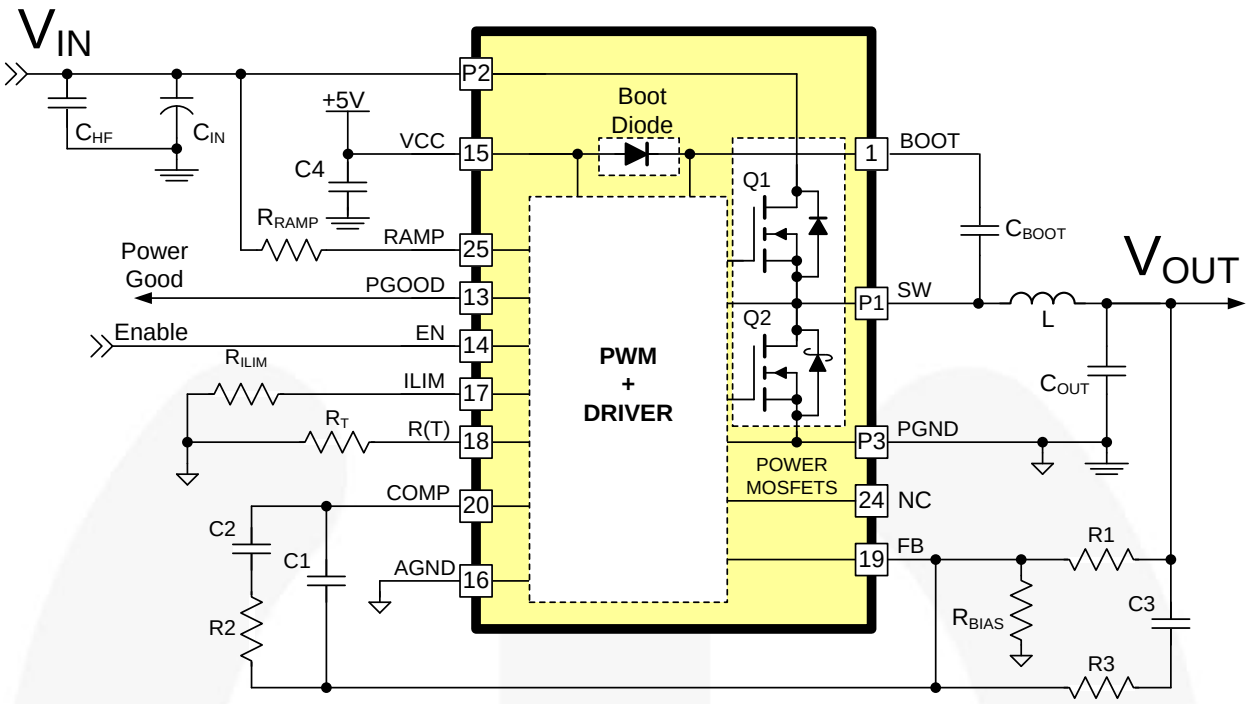


Figure 1. Typical Application Diagram

Block Diagram

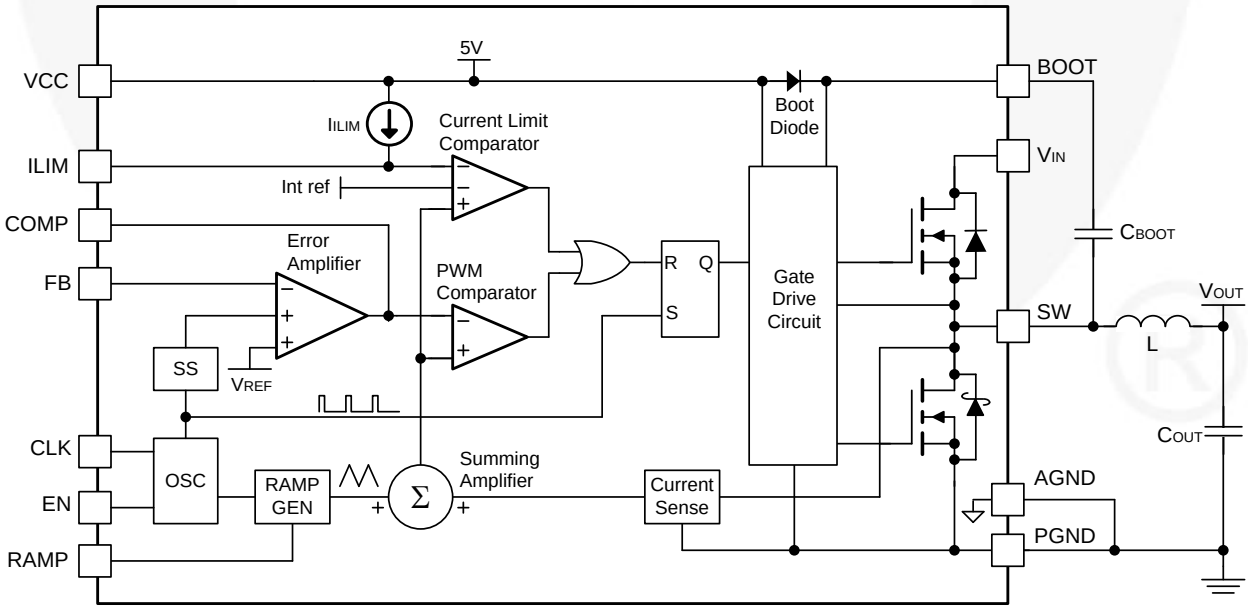


Figure 2. Block Diagram

Pin Configuration

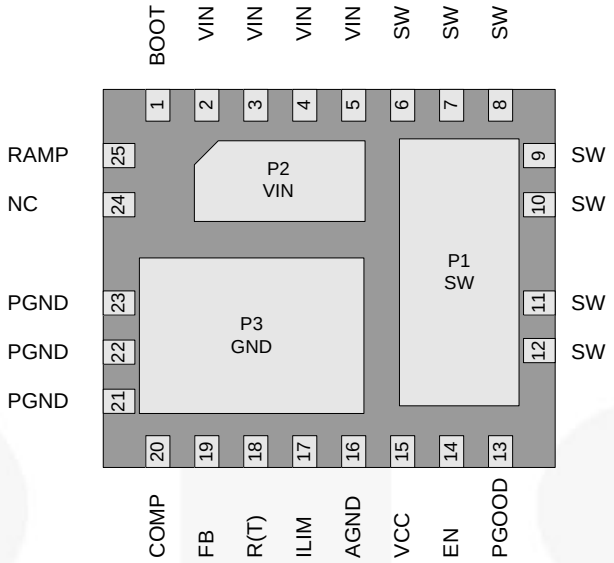


Figure 3. MLP 5 x 6 mm Pin Configuration (Bottom View)

Pin Definitions

Pin #	Name	Description
P1, 6-12	SW	**Switching Node**. Junction of high-side and low-side MOSFETs.
P2, 2-5	VIN	**Power Conversion Input Voltage**. Connect to the main input power source.
P3, 21-23	PGND	**Power Ground**. Power return and Q2 source.
1	BOOT	**High-Side Drive BOOT Voltage**. Connect through capacitor (C_{BOOT}) to SW. The IC includes an internal synchronous bootstrap diode to recharge the capacitor on this pin to V_{CC} when SW is LOW.
13	PGOOD	**Power-Good Flag**. An open-drain output that pulls LOW when FB is outside the limits specified in electrical specs. PGOOD does not assert HIGH until the fault latch is enabled.
14	EN	**ENABLE**. Enables operation when pulled to logic HIGH or left open. Toggling EN resets the regulator after a latched fault condition. This input has an internal pull-up when the IC is functioning normally. When a latched fault occurs, EN is discharged by a current sink.
15	VCC	**Input Bias Supply for IC**. The IC's logic and analog circuitry are powered from this pin. This pin should be decoupled to AGND through a > 2.2 µF X5R / X7R capacitor.
16	AGND	**Analog Ground**. The signal ground for the IC. All internal control voltages are referred to this pin. Tie this pin to the ground island/plane through the lowest impedance connection.
17	ILIM	**Current Limit**. A resistor (R_{ILIM}) from this pin to AGND can be used to program the current-limit trip threshold lower than the internal default setting.
18	R(T)	**Oscillator Frequency**. A resistor (R_T) from this pin to AGND sets the PWM switching frequency.
19	FB	**Output Voltage Feedback**. Connect through a resistor divider to the output voltage.
20	COMP	**Compensation**. Error amplifier output. Connect the external compensation network between this pin and FB.
24	NC	**No Connect**. This pin is not used.
25	RAMP	**Ramp Amplitude**. A resistor (R_{RAMP}) connected from this pin to V_{IN} sets the ramp amplitude and provides voltage feedforward functionality.

Absolute Maximum Ratings

Stresses exceeding the absolute maximum ratings may damage the device. The device may not function or be operable above the recommended operating conditions and stressing the parts to these levels is not recommended. In addition, extended exposure to stresses above the recommended operating conditions may affect device reliability. The absolute maximum ratings are stress ratings only.

Parameter	Conditions	Min.	Max.	Unit
VIN to PGND			28	V
VCC to AGND	AGND=PGND		6	V
BOOT to PGND			35	V
BOOT to SW		-0.5	6.0	V
SW to PGND	Continuous	-0.5	24.0	V
	Transient (t < 20 ns, f ≤ 600 KHz)	-5	30	V
All other pins		-0.3	V_{CC}+0.3	V
ESD	Human Body Model, JEDEC JESD22-A114	2.0		KV
	Charged Device Model, JEDEC JESD22-C101	2.5		

Recommended Operating Conditions

The Recommended Operating Conditions table defines the conditions for actual device operation. Recommended operating conditions are specified to ensure optimal performance to the datasheet specifications. Fairchild does not recommend exceeding them or designing to absolute maximum ratings.

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
V_{CC}	Bias Voltage	VCC to AGND	4.5	5.0	5.5	V
V_{IN}	Supply Voltage	VIN to PGND	3		24	V
T_A	Ambient Temperature		-40		+85	°C
T_J	Junction Temperature				+125	°C
f_{SW}	Switching Frequency		200		600	kHz

Thermal Information

Symbol	Parameter		Min.	Typ.	Max.	Unit
T_{STG}	Storage Temperature		-65		+150	°C
T_L	Lead Soldering Temperature, 10 Seconds				+300	°C
θ_{JC}	Thermal Resistance: Junction-to-Case	P1 (Q2)		4		°C/W
		P2 (Q1)		7		°C/W
		P3		4		°C/W
$\theta_{J\text{-}PCB}$	Thermal Resistance: Junction-to-Mounting Surface[1]			35		°C/W
P_D	Power Dissipation, T_A=25°C[1]				2.8	W

Note:

1. Typical thermal resistance when mounted on a four-layer, two-ounce PCB, as shown in Figure 35. Actual results are dependent on mounting method and surface related to the design.

Electrical Specifications

Electrical specifications are the result of using the circuit shown in Figure 1 with V_{IN}=12 V, unless otherwise noted.

Symbol	*Parameter*	Conditions	Min.	Typ.	Max.	Unit
Power Supplies						
I_{CC}	V_{CC} Current	SW=Open, V_{FB}=0.7 V, V_{CC}=5 V, f_{SW}=600 KHz		8	12	mA
		Shutdown: EN=0, V_{CC}=5 V		7	10	µA
V_{UVLO}	V_{CC} UVLO Threshold	Rising V_{CC}	4.1	4.3	4.5	V
		Hysteresis		300		mV
Oscillator						
f_{SW}	Frequency	R_T=50 KΩ to GND	255	300	345	KHz
		R_T=24 KΩ to GND	540	600	660	KHz
t_{ONmin}	Minimum On-Time(2)			50	65	ns
V_{RAMP}	Ramp Amplitude, Peak-to-Peak	16 V_{IN}, 1.8 V_{OUT}, R_T=30 KΩ, R_{RAMP}=200 KΩ		0.53		V
t_{OFFmin}	Minimum Off-Time(2)			100	150	ns
Reference						
V_{FB}	Reference Voltage (see Figure 4 for Temperature Coefficient)		795	800	805	mV
Error Amplifier						
G	DC Gain(2)	V_{CC}=5 V	80	85		dB
GBW	Gain Bandwidth Product(2)		12	15		MHz
V_{COMP}	Output Voltage(2)		0.4		3.2	V
I_{SINK}	Output Current, Sourcing	V_{CC}=5 V, V_{COMP}=2.2 V	1.5	2.2		mA
I_{SOURCE}	Output Current, Sinking	V_{CC}=5 V, V_{COMP}=1.2 V	0.8	1.2		mA
I_{BIAS}	FB Bias Current	V_{FB}=0.8 V, 25°C	-850	-650	-450	nA
Protection and Shutdown						
I_{LIM}	Current Limit (see Circuit Description)(2)	R_{ILIM}=182 KΩ,, 25°C, f_{SW}=500 KHz, V_{OUT}=1.5 V, R_{RAMP}=243 KΩ, 16 Consecutive Clock Cycles(3)	12	14	16	A
I_{ILIM}	I_{LIM} Current	V_{CC}=5 V, 25°C	-11	-10	-9	µA
T_{TSD}	Over-Temperature Shutdown(2)	Internal IC Temperature		+155		°C
T_{HYS}	Over-Temperature Hysteresis(2)			+30		°C
V_{OVP}	Over-Voltage Threshold	2 Consecutive Clock Cycles(3)	110	115	121	%V_{OUT}
V_{UVSD}	Under-Voltage Shutdown	16 Consecutive Clock Cycles(3)	68	73	78	%V_{OUT}
V_{FLT}	Fault Discharge Threshold	Measured at FB Pin		250		mV
V_{FLT_HYS}	Fault Discharge Hysteresis	Measured at FB Pin (V_{FB} ~500 mV)		250		mV
Soft-Start						
t_{SS}	V_{OUT} to Regulation (T0.8)	f_{SW}=500 KHz		5.3		ms
t_{EN}	Fault Enable/SSOK (T1.0)(2)			6.7		ms

Continued on the following page…

Electrical Specifications (Continued)

Electrical specifications are the result of using the circuit shown in Figure 1 with V_{IN}=12 V, unless otherwise noted.

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
Control Functions						
V_{EN}	EN Threshold, Rising	V_{CC}=5 V		1.35	2.00	V
V_{EN_HYS}	EN Hysteresis	V_{CC}=5 V		250		mV
R_{EN}	EN Pull-Up Resistance	V_{CC}=5 V		800		KΩ
I_{EN_DISC}	EN Discharge Current	Auto-Restart Mode, V_{CC}=5 V		1		µA
R_{FBok}	FB OK Drive Resistance				800	Ω
V_{PGTH_LO}	PGOOD LOW Threshold	FB < V_{REF}, 2 Consecutive Clock Cycles(3)	-14	-11	-8	%V_{REF}
V_{PGTH_UP}		FB > V_{REF}, 2 Consecutive Clock Cycles(3)	+7.0	+10.0	+13.5	
V_{PG_LO}	PGOOD Output Low	$I_{OUT} \leq$ 2 mA			0.4	V
I_{PG_LK}	PGOOD Leakage Current	V_{PGOOD}=5 V		0.2	1.0	µA

Notes:
2. Specifications guaranteed by design and characterization; not production tested.
3. Delay times are not tested in production. Guaranteed by design.

Typical Characteristics

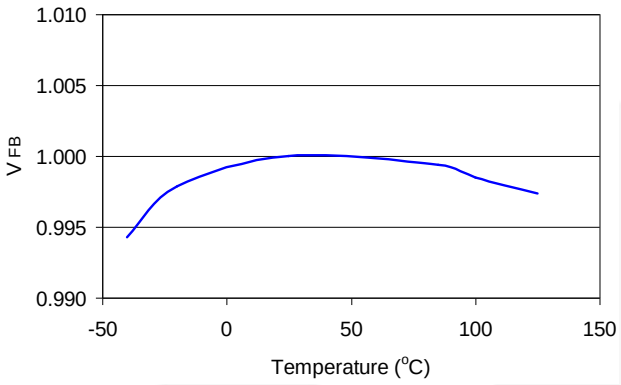


Figure 4. Reference Voltage (V_{FB}) vs. Temperature, Normalized

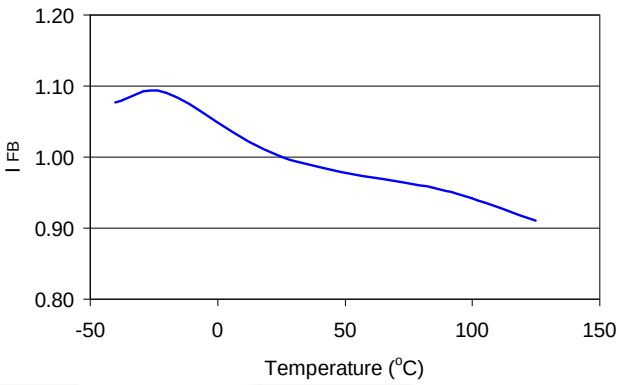


Figure 5. Reference Bias Current (I_{FB}) vs. Temperature, Normalized

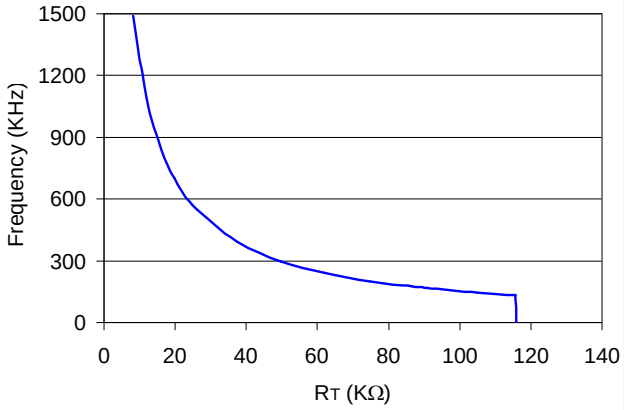


Figure 6. Frequency vs. R_T

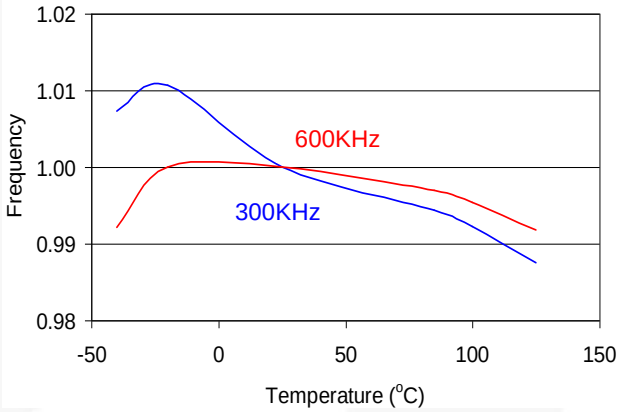


Figure 7. Frequency vs. Temperature, Normalized

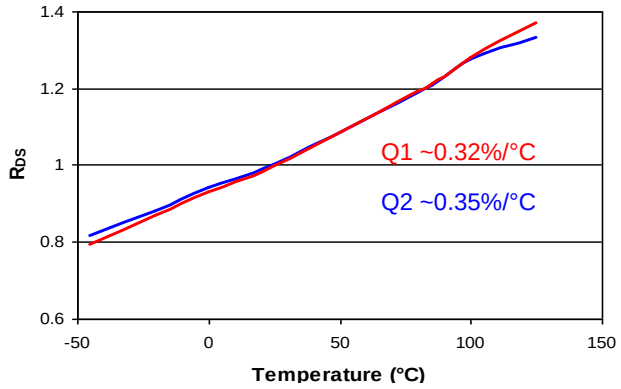


Figure 8. R_{DS} vs. Temperature, Normalized (V_{CC}=V_{GS}=5 V), Figure 1

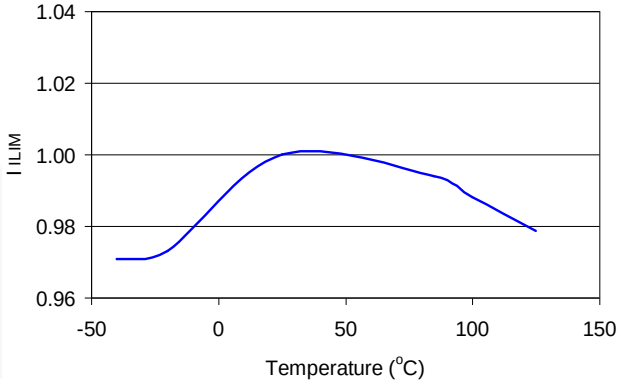


Figure 9. I_{LIM} Current (I_{ILIM}) vs. Temperature, Normalized

Application Circuits

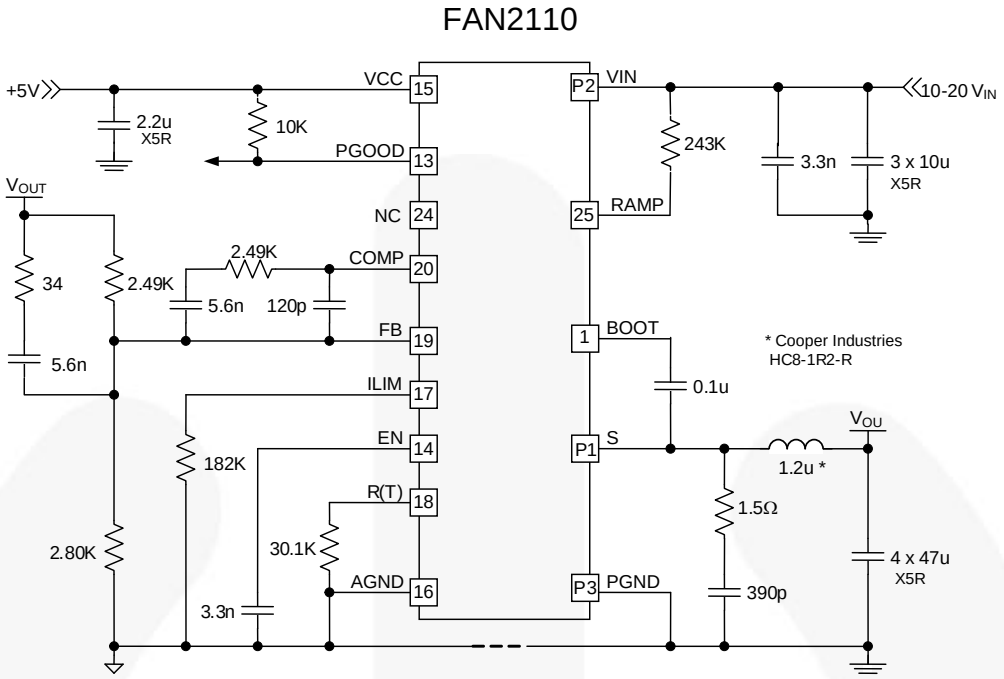


Figure 10. Application Circuit: 1.5 V_{OUT}, 10 A, 500 KHz (10 V-20 V_{IN})

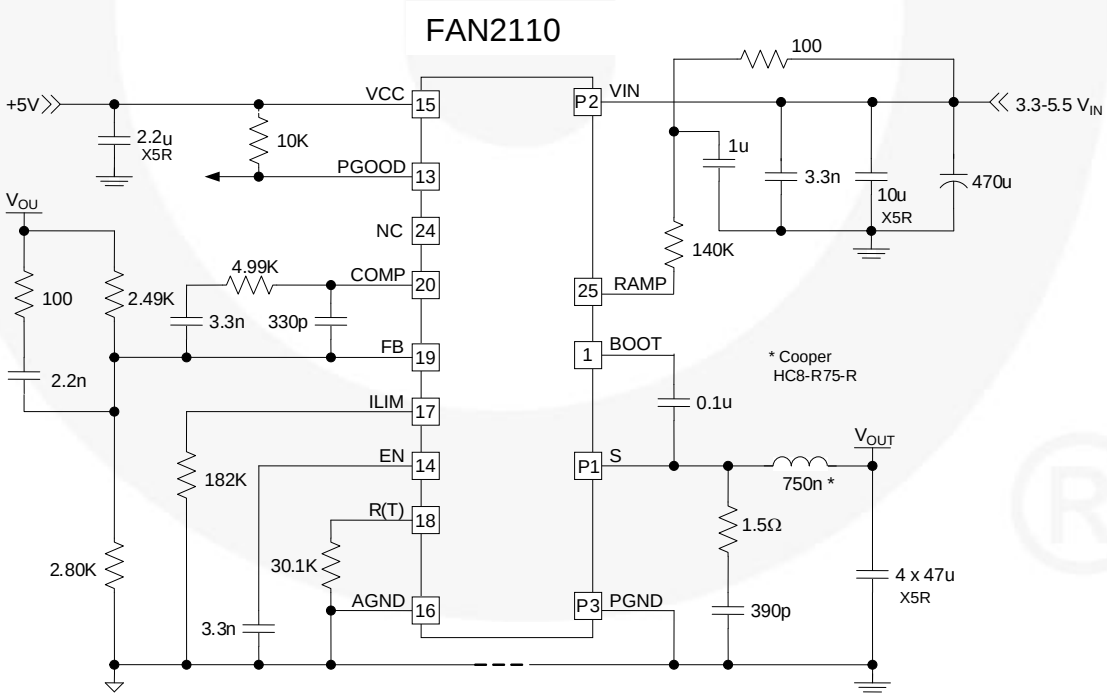


Figure 11. Application Circuit: 1.5 V_{OUT}, 10 A, 500 KHz (3.3 V-5.5 V_{IN})

Typical Performance Characteristics

Typical operating characteristics using the circuit in Figure 10. V_{IN}=12 V, V_{CC}=5 V, T_A=25°C, unless otherwise specified.

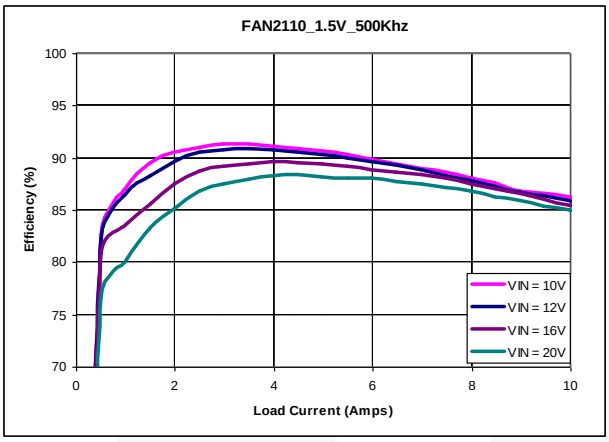


Figure 12. 1.5 V_{OUT} Efficiency, 500 KHz

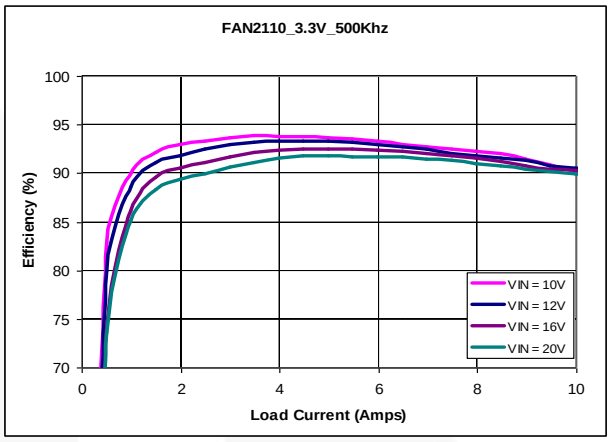


Figure 13. 3.3 V_{OUT} Efficiency, 500 KHz(4)

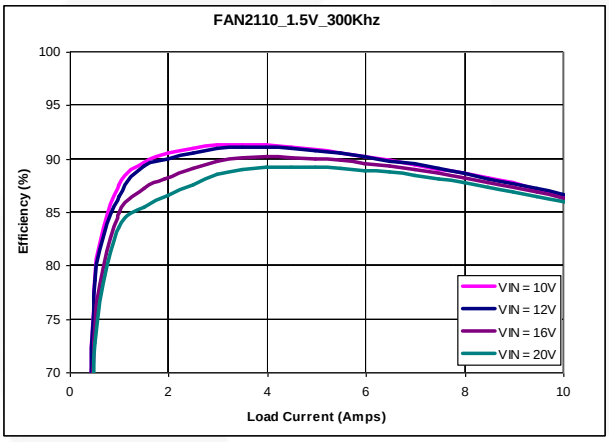


Figure 14. 1.5 V_{OUT} Efficiency, 300 KHz

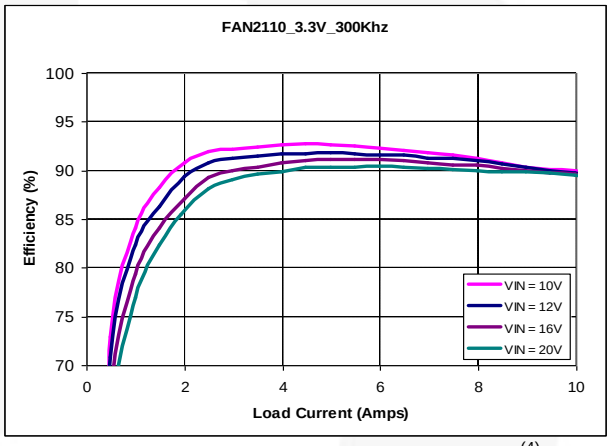


Figure 15. 3.3 V_{OUT} Efficiency, 300 KHz(4)

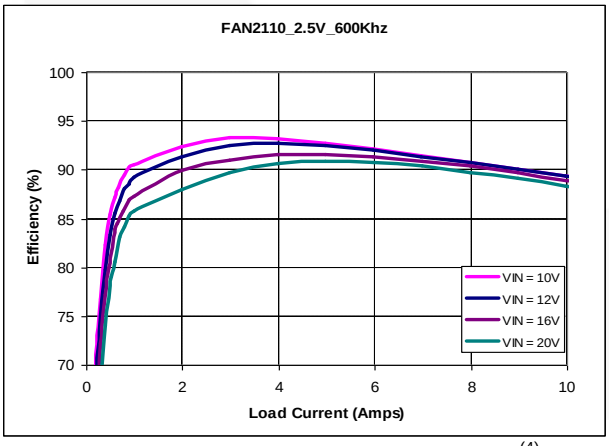


Figure 16. 2.5 V_{OUT} Efficiency ,600 KHz(4)

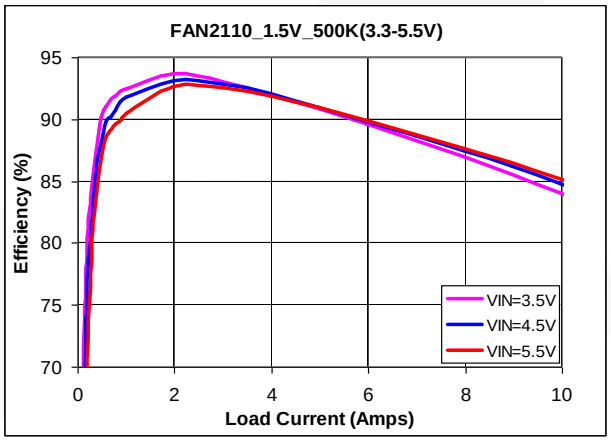


Figure 17. 1.5 V_{OUT} Efficiency, 500 KHz (V_{IN}=3.3 V to 5 V), Figure 11

Note:

4. Circuit values for this configuration change in Figure 10.

Typical Performance Characteristics (Continued)

Typical operating characteristics using the circuit in Figure 10. V_{IN}=12 V, V_{CC}=5 V, T_A=25°C unless otherwise specified.

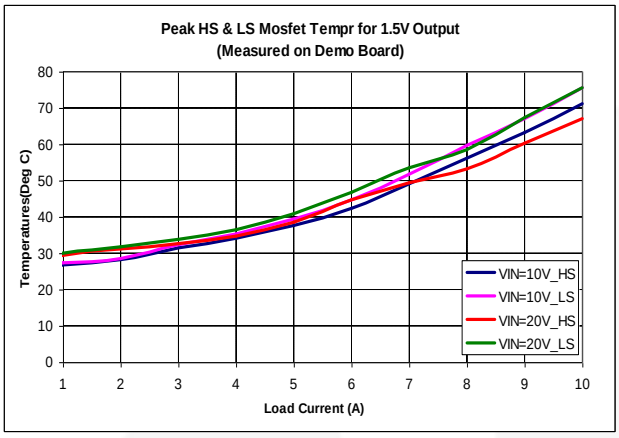


Figure 18. Peak MOSFET Temperatures, Figure 10

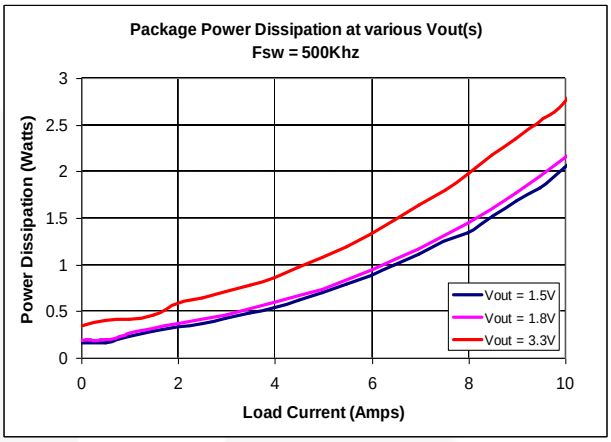


Figure 19. Device Dissipation Over V_{OUT} vs. Load

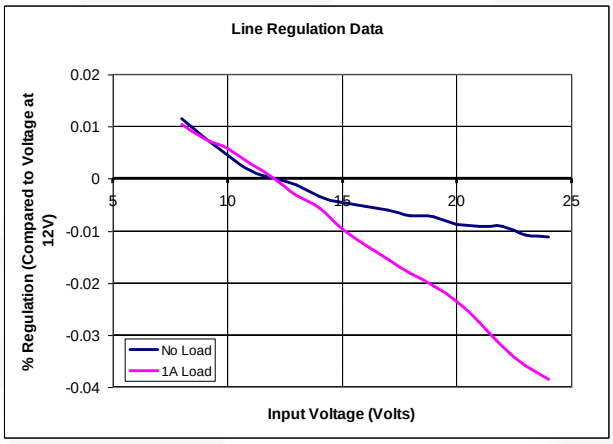


Figure 20. 1.5 V_{OUT} Line Regulation

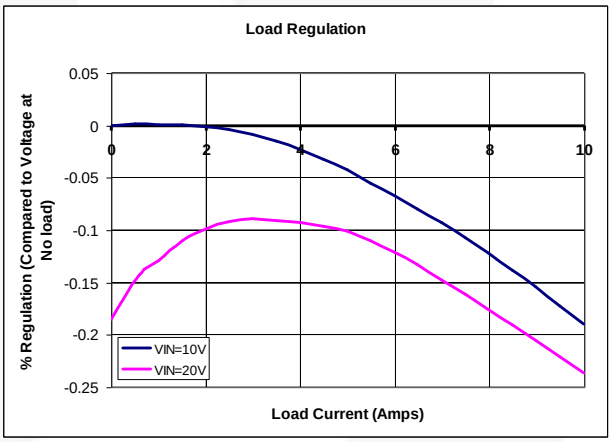


Figure 21. 1.5 V_{OUT} Load Regulation

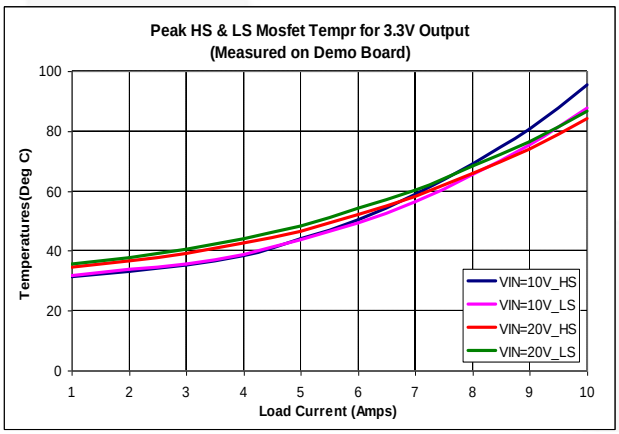


Figure 22. Peak MOSFET Temperatures, 3.3 V Output(5)

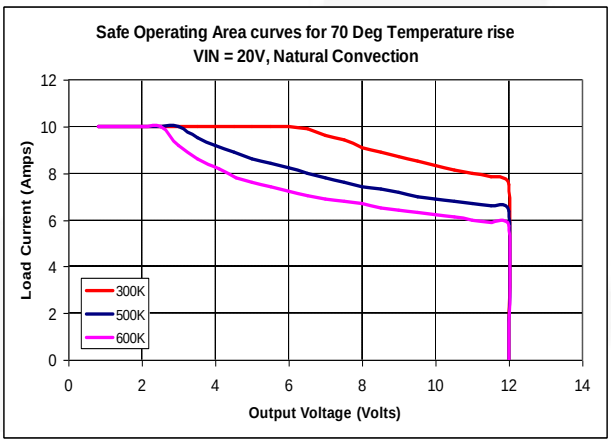


Figure 23. Typical 20 V_{IN} Safe Operation Area (SOA), 70°C Ambient Temperature, Natural Convection

Note:

5. Circuit values for this configuration change in Figure 10.

Typical Performance Characteristics (Continued)

Typical operating characteristics using the circuit in Figure 10. V_{IN}=12 V, V_{CC}=5 V, T_A=25°C unless otherwise specified.

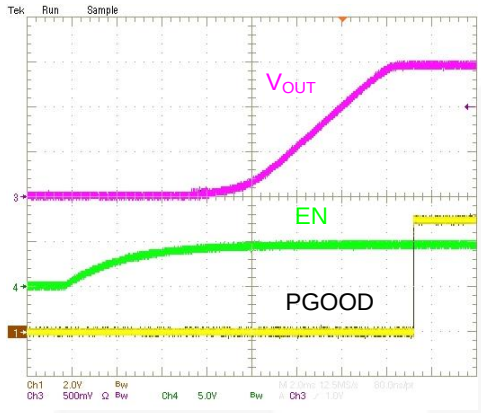


Figure 24. Startup, 10 A Load

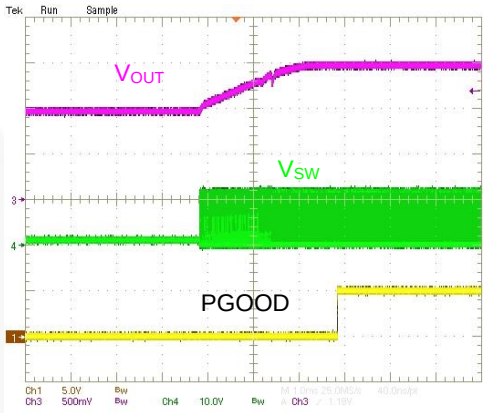


Figure 25. Startup with 1.0 V Pre-Bias on V_{OUT}

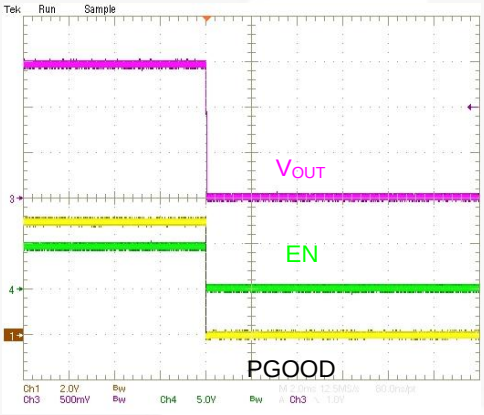


Figure 26. Shutdown, 10 A Resistive Load

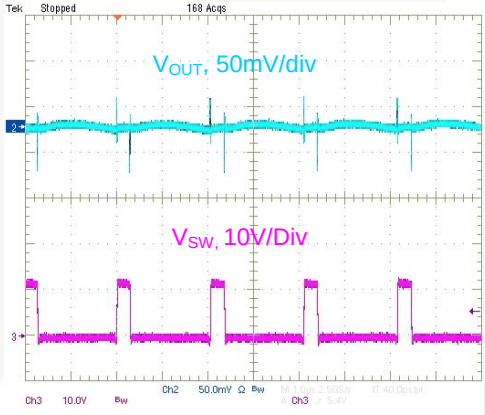


Figure 27. V_{OUT} Ripple and SW Voltage, 10 A Load

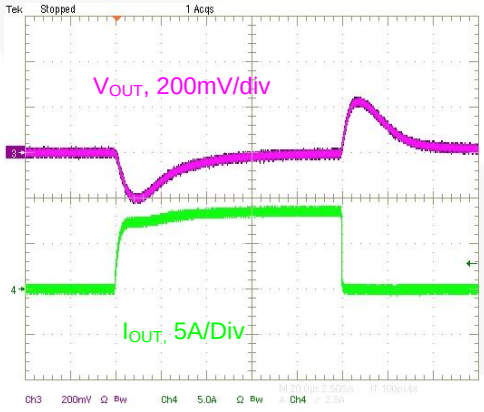


Figure 28. Transient Response, 0-8 A Load, 5 A / µs Slew Rate

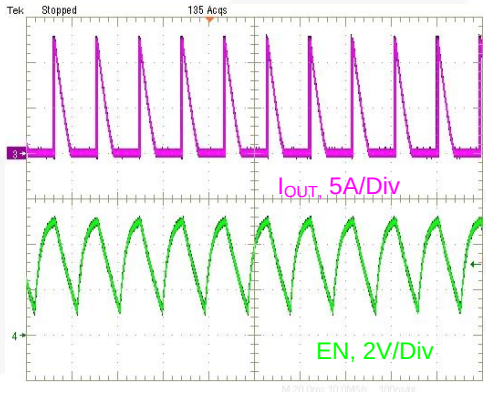


Figure 29. Restart on Short Circuit (Fault)

Circuit Description

PWM Generation

Refer to Figure 2 for the PWM control mechanism. FAN2110 uses the summing-mode method of control to generate the PWM pulses. An amplified current-sense signal is summed with an internally generated ramp and the combined signal is compared with the output of the error amplifier to generate the pulse width to drive the high-side MOSFET. Sensed current from the previous cycle is used to modulate the output of the summing block. The output of the summing block is also compared against a voltage threshold set by the R_{LIM} resistor to limit the inductor current on a cycle-by-cycle basis. R_{RAMP} resistor helps set the charging current for the internal ramp and provides input voltage feed-forward function. The controller facilitates external compensation for enhanced flexibility.

Initialization

Once V_{CC} exceeds the UVLO threshold and EN is HIGH, the IC checks for a shorted FB pin before releasing the internal soft-start ramp (SS).

If the parallel combination of R1 and R_{BIAS} is $\leq$ 1 KΩ, the internal SS ramp is not released and the regulator does not start.

Enable

FAN2110 has an internal pull-up to the enable (EN) pin so that the IC is enabled once V_{CC} exceeds the UVLO threshold. Connecting a small capacitor across EN and AGND delays the rate of voltage rise on the EN pin. The EN pin also serves for the restart whenever a fault occurs *(refer to the Auto-Restart section)*. If the regulator is enabled externally, the external EN signal should go HIGH only after V_{CC} is established. For applications where such sequencing is required, FAN2110 can be enabled (after the V_{CC} comes up) with external control, as shown in Figure 30.

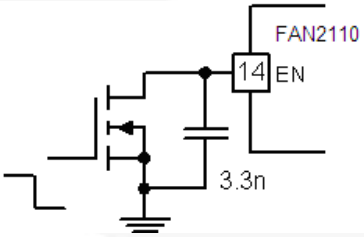


Figure 30. Enabling with External Control

Soft-Start

Once internal SS ramp has charged to 0.8 V (T0.8), the output voltage is in regulation. Until SS ramp reaches 1.0 V (T1.0), the fault latch is inhibited.

To avoid skipping the soft-start cycle, it is necessary to apply V_{IN} before V_{CC} reaches its UVLO threshold. Normal sequence for powering up would be VIN→VCC→EN.

Soft-start time is a function of oscillator frequency.

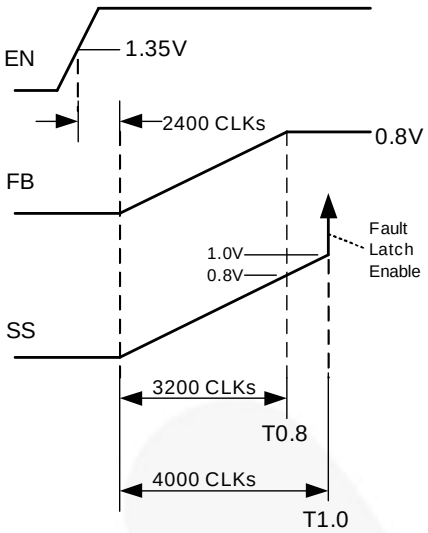


Figure 31. Soft-Start Timing Diagram

V_{CC} UVLO or toggling the EN pin discharges the internal SS and resets the IC. In applications where external EN signal is used, V_{IN} and V_{CC} should be established before the EN signal comes up to prevent skipping the soft-start function.

Startup on Pre-Bias

The regulator does not allow the low-side MOSFET to operate in full synchronous mode until SS reaches 95% of V_{REF} (~0.76 V). This enables the regulator to startup on a pre-biased output and ensures that pre-biased outputs are not discharged during the soft-start cycle.

Protections

The converter output is monitored and protected against extreme overload, short-circuit, over-voltage, under-voltage, and over-temperature conditions.

Under-Voltage Shutdown

If voltage on the FB pin remains below the under-voltage threshold for 16 consecutive clock cycles, the fault latch is set and the converter shuts down. This protection is not active until the internal SS ramp reaches 1.0 V during soft-start.

Over-Voltage Protection

If voltage on the FB pin exceeds 115% of V_{REF} for two consecutive clock cycles, the fault latch is set and shutdown occurs.

A shorted high-side MOSFET condition is detected when SW voltage exceeds ~0.7 V while the low-side MOSFET is fully enhanced. The fault latch is set immediately upon detection.

The OV/UV fault protection circuits above are active all the time, including during soft-start.

Over-Temperature Protection (OTP)

The chip incorporates an over-temperature protection circuit that sets the fault latch when a die temperature of about 150°C is reached. The IC restarts when the die temperature falls below 125°C.

Auto-Restart

After a fault, EN pin is discharged by a 1 µA current sink to a 1.1 V threshold before the internal 800 KΩ pull-up is restored. A new soft-start cycle begins when EN charges above 1.35 V.

Depending on the external circuit, the FAN2110 can be configured to remain latched-off or to automatically restart after a fault.

Table 1. Fault / Restart Configurations

EN Pin	Controller / Restart State
Pull to GND	OFF (Disabled)
Pull-up to V_{CC} with 100K	No Restart – Latched OFF (After V_{CC} Comes Up)
Open	Immediate Restart After Fault
Cap. to GND	New Soft-Start Cycle After: t_{DELAY} (ms)=3.9 • C(nf)

When EN is left open, restart is immediate.

If auto-restart is not desired, tie the EN pin to the VCC pin or pull it HIGH after V_{CC} comes up with a logic gate to keep the 1 µA current sink from discharging EN to 1.1V. Figure 32 shows one method to pull up EN to V_{CC} for a latch configuration.

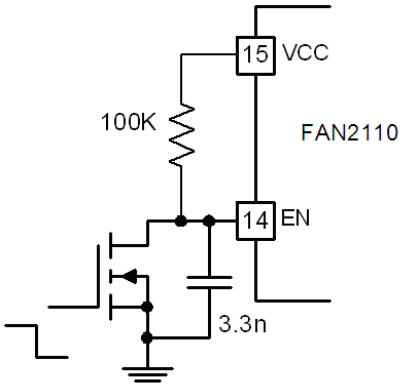


Figure 32. Enable Control with Latch Option

Power-Good (PGOOD) Signal

PGOOD is an open-drain output that asserts LOW when V_{OUT} is out of regulation, as measured at the FB pin. Thresholds are specified in the Electrical Specifications section. PGOOD does not assert HIGH until the fault latch is enabled (T1.0) *(see Figure 31)*.

Application Information

Bias Supply

The FAN2110 requires a 5 V supply rail to bias the IC and provide gate-drive energy. Connect a ≥ 2.2 µf X5R or X7R decoupling capacitor between VCC and AGND.

Since V_{CC} is used to drive the internal MOSFET gates, supply current is frequency and voltage dependent. Approximate V_{CC} current (I_{CC}) is calculated by:

$$I_{CC(mA)} = 4.58 + [(\frac{V_{CC} - 5}{227} + 0.013) \bullet (f - 128)] \quad (1)$$

where frequency (f) is expressed in KHz.

Setting the Output Voltage

The output voltage of the regulator can be set from 0.8V to 80% of V_{IN} by an external resistor divider (R1 and R_{BIAS} in Figure 1). For output voltages >3.3V, output current rating may need to be de-rated depending on the ambient temperature, power dissipated in the package and the PCB layout. *(Refer to Thermal Information table on page 4, Figure 22, and Figure 23.)*

The external resistor divider is calculated using:

$$\frac{0.8V}{R_{BIAS}} = \frac{V_{OUT} - 0.8V}{R1} + 650nA \quad (2)$$

Connect R_{BIAS} between FB and AGND.

If R1 is open *(see Figure 1),* the output voltage is not regulated and a latched fault occurs after the SS is complete (T1.0).

If the parallel combination of R1 and R_{BIAS} is ≤ 1KΩ, the internal SS ramp is not released and the regulator does not start.

Setting the Clock Frequency

Oscillator frequency is determined by an external resistor, R_T, connected between the R_T pin and AGND. Resistance is calculated by:

$$R_{T(K\Omega)} = \frac{(10^6 / f) - 135}{65} \quad (3)$$

where R_T is in KΩ and frequency (f) is in KHz.

The regulator cannot start if R_T is left open.

Calculating the Inductor Value

Typically the inductor value is chosen based on ripple current (ΔI_L), which is chosen between 10 to 35% of the maximum DC load. Regulator designs that require fast transient response use a higher ripple-current setting, while regulator designs that require higher efficiency keep ripple current on the low side and operate at a lower switching frequency. The inductor value is calculated by the following formula:

$$L = \frac{V_{OUT} \bullet (1 - \frac{V_{OUT}}{Vin})}{\Delta IL \bullet f} \quad (4)$$

where f is the oscillator frequency.

Setting the Ramp Resistor Value

R_{RAMP} resistor plays a critical role in the design by providing charging current to the internal ramp capacitor and also serving as a means to provide input voltage feedforward.

R_{RAMP} is calculated by the following formula:

$$R_{RAMP(K\Omega)} = \frac{(V_{IN} - 1.8) \bullet V_{OUT}}{(31 - 2.05 \bullet I_{OUT}) \bullet V_{IN} \bullet f \bullet 10^{-6}} - 2 \quad (5)$$

where frequency (f) is expressed in KHz.

For wide input operation, first calculate R_{RAMP} for the minimum and maximum input voltage conditions and use larger of the two values calculated.

In all applications, current through the R_{RAMP} pin must be greater than 10 µA from the equation below for proper operation:

$$\frac{V_{IN} - 1.8}{R_{RAMP} + 2} \geq 10\mu A \quad (6)$$

If the calculated R_{RAMP} values in Equation (5) result in a current less than 10 µA, use the R_{RAMP} value that satisfies Equation (6). In applications with large Input ripple voltage, the R_{RAMP} resistor should be adequately decoupled from the input voltage to minimize ripple on the ramp pin. For example, see Figure 11.

Setting the Current Limit

The current limit system involves two comparators. The MAX I_{LIMIT} comparator is used with a V_{ILIM} fixed-voltage reference and represents the maximum current limit allowable. This reference voltage is temperature compensated to reflect the R_{DSON} variation of the low-side MOSFET. The ADJUST I_{LIMIT} comparator is used where the current limit needs to be set lower than the V_{ILIM} fixed reference. The 10 µA current source does not track the R_{DSON} changes over temperature, so change is added into the equations for calculating the ADJUST I_{LIMIT} comparator reference voltage, as is shown below. Figure 33 shows a simplified schematic of the over-current system.

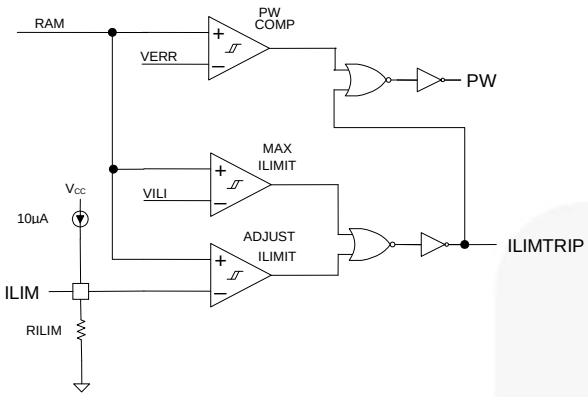


Figure 33. Current-Limit System Schematic

Since the I_{LIM} voltage is set by a 10 µA current source into the R_{ILIM} resistor, the basic equation for setting the reference voltage is:

$$V_{RILIM} = 10\mu A * R_{ILIM} \quad (7)$$

To calculate R_{ILIM}:

$$R_{ILIM} = V_{RILIM} / 10\mu A \quad (8)$$

The voltage V_{RILIM} is made up of two components, V_{BOT} (which relates to the current through the low-side MOSFET) and V_{RMPEAK} (which relates to the peak current through the inductor). Combining those two voltage terms results in:

$$R_{ILIM} = (V_{BOT} + V_{RMPEAK}) / 10\mu A \quad (9)$$

$$R_{ILIM} = \{0.96 + (I_{LOAD} * R_{DSON} * K_T * 8)\} + \{D*(V_{IN} - 1.8)/(f_{SW}*0.03*10\text{^-}3*R_{RAMP})\}/10\ \mu A \quad (10)$$

where:

$V_{BOT} = 0.96 + (I_{LOAD} * R_{DSON} * K_T * 8)$;

$V_{RMPEAK} = D*(V_{IN} - 1.8)/(f_{SW}*0.03*10\text{^-}3*R_{RAMP})$;

I_{LOAD} = the desired maximum load current;

R_{DSON} = the nominal R_{DSON} of the low-side MOSFET;

K_T = the normalized temperature coefficient for the low-side MOSFET (on datasheet graph);

$D = V_{OUT}/V_{IN}$ duty cycle;

f_{SW} = Clock frequency in kHz; and

R_{RAMP} = chosen ramp resistor value in kΩ.

After 16 consecutive, pulse-by-pulse, current-limit cycles, the fault latch is set and the regulator shuts down. Cycling V_{CC} or EN restores operation after a normal soft-start cycle *(refer to the Auto-Restart section)*.

The over-current protection fault latch is active during the soft-start cycle. Use 1% resistor for R_{ILIM}.

Always use an external resistor R_{ILIM} to set the current limit at the desired level. When R_{ILIM} is not connected, the IC's internal default current limit is fairly high. This could lead to operation at high load currents, causing overheating of the regulator. For a given R_{ILIM} and R_{RAMP} setting, the current limit point varies slightly in an inverse relationship with respect to input voltage (V_{IN}).

Loop Compensation

The loop is compensated using a feedback network around the error amplifier. Figure 34 shows a complete type-3 compensation network. For type-2 compensation, eliminate R3 and C3.

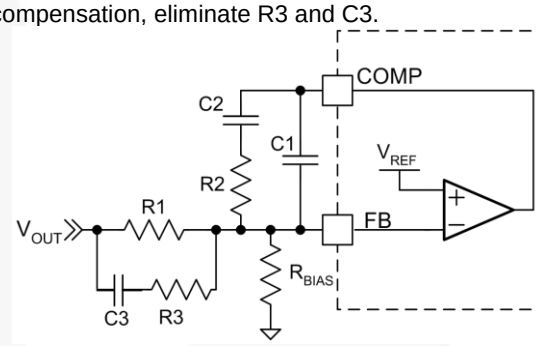


Figure 34. Compensation Network

Since the FAN2110 employs summing current-mode architecture, type-2 compensation can be used for many applications. For applications that require wide loop bandwidth and/or use very low-ESR output capacitors, type-3 compensation may be required.

R_{RAMP} also provides feedforward compensation for changes in V_{IN}. With a fixed R_{RAMP} value, the modulator gain increases as V_{IN} is reduced, which could make it difficult to compensate the loop. For low-input-voltage-range designs (3 V to 8 V), R_{RAMP} and the compensation component values are different compared to designs with V_{IN} between 8 V and 24 V.

Recommended PCB Layout

Good PCB layout and careful attention to temperature rise is essential for reliable operation of the regulator. Four-layer PCB with two-ounce copper on the top and bottom side and thermal vias connecting the layers is recommended. Keep power traces wide and short to minimize losses and ringing. Do not connect AGND to PGND below the IC. Connect the AGND pin to PGND at the output OR to the PGND plane.

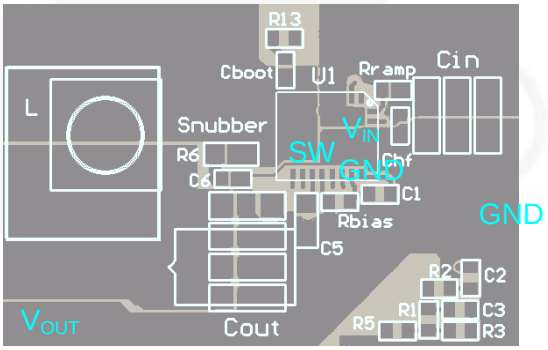
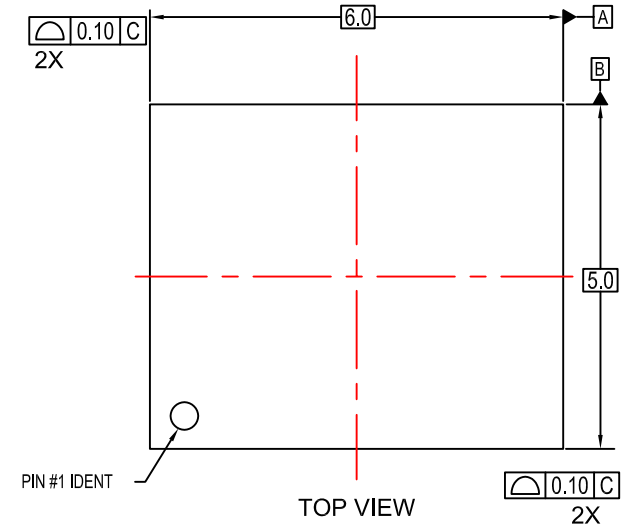
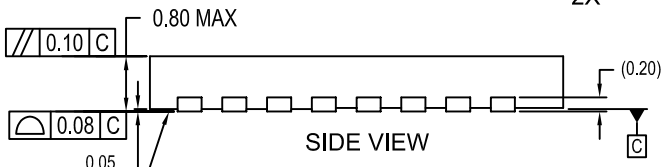


Figure 35. Recommended PCB Layout

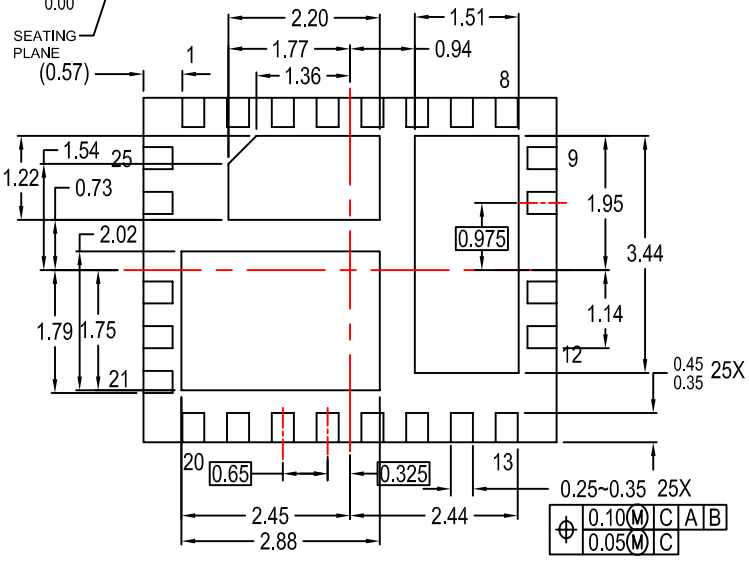
REVISIONS			
LTR	DESCRIPTION	DATE	BY/SITE
1	RELEASE TO DOCUMENT CONTROL	12-Jul-2007	J Chan/FSPM
2	ADDED DIMENSIONS TO BOTTOM VIEW AND LANDPATTERN RECOMMENDATION	7-SEPT-2007	H.ALLEN/FSME
3	CHAMFERED LANDPATTERN PAD 1	17-JUN-2009	H.ALLEN/FSME



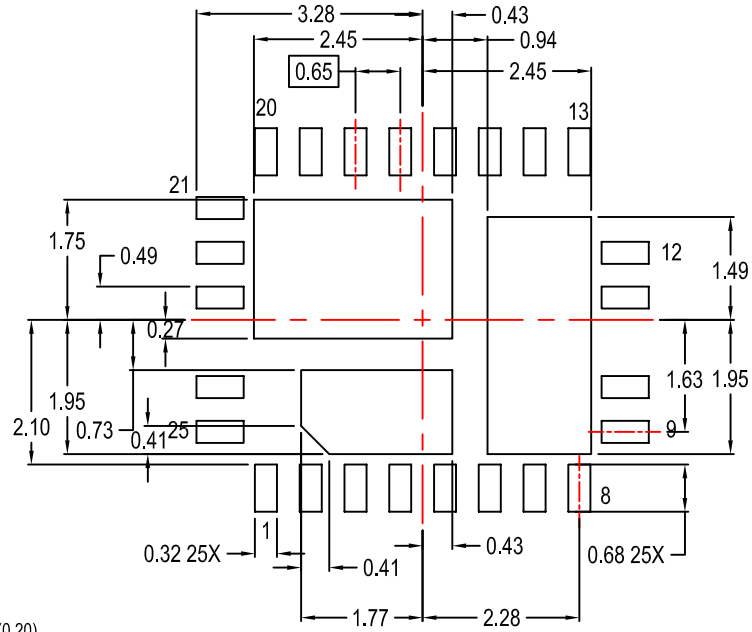
TOP VIEW



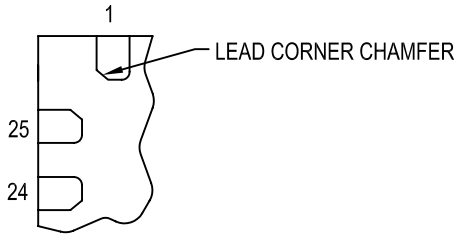
SIDE VIEW



BOTTOM VIEW



RECOMMENDED LAND PATTERN
ALL VALUES TYPICAL EXCEPT WHERE NOTED



OPTIONAL LEAD DESIGN
(LEADS# 1, 24 & 25 ONLY)
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NOTES: UNLESS OTHERWISE SPECIFIED

A) DIMENSIONS ARE IN MILLIMETERS.

B) DIMENSIONS AND TOLERANCES PER ASME Y14.5M, 1994

C) DIMENSIONS DO NOT INCLUDE MOLD FLASH OR BURRS.

D) DESIGN BASED ON JEDEC MO-220 VARIATION WJHC

E) TERMINALS ARE SYMMETRICAL AROUND THE X & Y AXIS EXCEPT WHERE DEPOPULATED.

F) DRAWING FILENAME: MKT-MLP25AREV3

APPROVALS	DATE
DRAWN H.ALLEN	7-SEPT-07
DFTG. CHK. S.MARTIN	7-SEPT-07
ENGR. CHK.	

FAIRCHILD SEMICONDUCTOR
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PROJECTION
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