1. General description

The 74LV04 is a hex inverter. Inputs include clamp diodes. This enables the use of current limiting resistors to interface inputs to voltages in excess V_{CC} .

2. Features and benefits

- Wide supply voltage range from 1.0 to 5.5 V
- CMOS low power dissipation
- Latch-up performance exceeds 100 mA per JESD 78 Class II Level B
- Optimized for low voltage applications: 1.0 V to 3.6 V
- Accepts TTL input levels between V_{CC} = 2.7 V and V_{CC} = 3.6 V
- Typical output ground bounce < 0.8 V at V_{CC} = 3.3 V and T_{amb} = 25 °C
- Typical HIGH-level output voltage (V_{OH}) undershoot: > 2 V at V_{CC} = 3.3 V and T_{amb} = 25 °C
- Complies with JEDEC standards:
 - JESD8-7 (1.65 V to 1.95 V)
 - JESD8-5 (2.3 V to 2.7 V)
 - JESD8C (2.7 V to 3.6 V)
 - JESD36 (4.5 V to 5.5 V)
- ESD protection:
 - HBM JESD22-A114E exceeds 2000 V
 - MM JESD22-A115-A exceeds 200 V
- Multiple package options
- Specified from -40 °C to +85 °C and from -40 °C to +125 °C

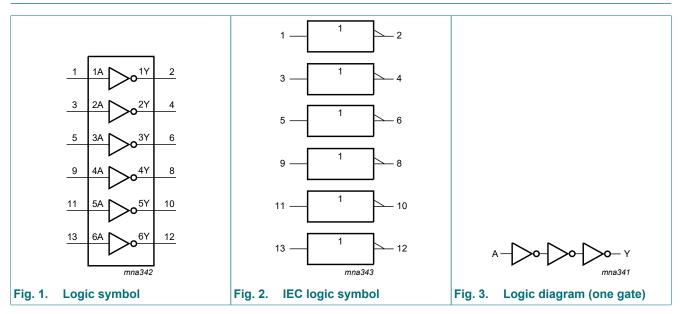
3. Ordering information

Table 1. Ordering information

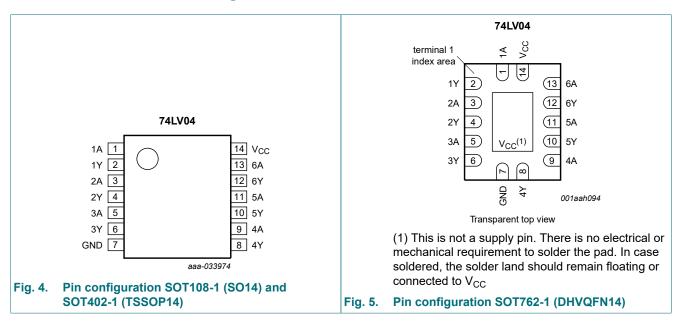
Type number	Package						
	Temperature range	Name	Description	Version			
74LV04D	-40 °C to +125 °C	SO14	plastic small outline package; 14 leads; body width 3.9 mm	SOT108-1			
74LV04PW	-40 °C to +125 °C	TSSOP14	plastic thin shrink small outline package; 14 leads; body width 4.4 mm	SOT402-1			
74LV04BQ	-40 °C to +125 °C	DHVQFN14	plastic dual in-line compatible thermal enhanced very thin quad flat package; no leads; 14 terminals; body 2.5 × 3 × 0.85 mm	SOT762-1			

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4. Functional diagram



5. Pinning information



5.1. Pinning

5.2. Pin description

Table 2. Pin description					
Symbol	Pin	Description			
1A, 2A, 3A, 4A, 5A, 6A	1, 3, 5, 9, 11, 13	data input			
1Y, 2Y, 3Y, 4Y, 5Y, 6Y	2, 4, 6, 8, 10, 12	data output			
GND	7	ground (0 V)			
V _{CC}	14	supply voltage			

6. Functional description

Table 3. Function table

H = HIGH voltage level; L = LOW voltage level.

Input nA	Output nY
L	Н
Н	L

7. Limiting values

Table 4. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134). Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions		Min	Max	Unit
V _{CC}	supply voltage			-0.5	+7.0	V
I _{IK}	input clamping current	$V_{\rm I}$ < -0.5 V or $V_{\rm I}$ > $V_{\rm CC}$ + 0.5 V	[1]	-	±20	mA
I _{OK}	output clamping current	$V_{\rm O}$ < -0.5 V or $V_{\rm O}$ > $V_{\rm CC}$ + 0.5 V	[1]	-	±50	mA
I _O	output current	$V_{O} = -0.5 \text{ V to} (V_{CC} + 0.5 \text{ V})$		-	±25	mA
I _{CC}	supply current			-	50	mA
I _{GND}	ground current			-50	-	mA
T _{stg}	storage temperature			-65	+150	°C
P _{tot}	total power dissipation	T_{amb} = -40 °C to +125 °C	[2]	-	500	mW

[1] The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

[2] For SOT108-1 (SO14) package: P_{tot} derates linearly with 10.1 mW/K above 100 °C.

For SOT402-1 (TSSOP14) package: P_{tot} derates linearly with 7.3 mW/K above 81 °C.

For SOT762-1 (DHVQFN14) package: P_{tot} derates linearly with 9.6 mW/K above 98 °C.

8. Recommended operating conditions

Table 5. Recommended operating conditions

Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	Min	Тур	Max	Unit
V _{CC}	supply voltage	[1]	1.0	3.3	5.5	V
VI	input voltage		0	-	V _{CC}	V
Vo	output voltage		0	-	V _{CC}	V
T _{amb}	ambient temperature		-40	+25	+125	°C

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Symbol	Parameter	Conditions	Min	Тур	Max	Unit
Δt/ΔV	input transition rise and fall rate	V _{CC} = 1.0 V to 2.0 V	-	-	500	ns/V
		V _{CC} = 2.0 V to 2.7 V	-	-	200	ns/V
		V _{CC} = 2.7 V to 3.6 V	-	-	100	ns/V
		V _{CC} = 3.6 V to 5.5 V	-	-	50	ns/V

[1] The static characteristics are guaranteed from V_{CC} = 1.2 V to V_{CC} = 5.5 V, but LV devices are guaranteed to function down to V_{CC} = 1.0 V (with input levels GND or V_{CC}).

9. Static characteristics

Table 6. Static characteristics

Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	ameter Conditions		-40 °C to +85 °C			-40 °C to +125 °C	
			Min	Typ[1]	Max	Min	Мах	-
V _{IH}	HIGH-level input voltage	V _{CC} = 1.2 V	0.9	-	-	0.9	-	V
		V _{CC} = 2.0 V	1.4	-	-	1.4	-	V
		V _{CC} = 2.7 V to 3.6 V	2.0	-	-	2.0	-	V
		V _{CC} = 4.5 V to 5.5 V	0.7V _{CC}	-	-	0.7V _{CC}	-	V
V _{IL}	LOW-level input voltage	V _{CC} = 1.2 V	-	-	0.3	-	0.3	V
		V _{CC} = 2.0 V	-	-	0.6	-	0.6	V
		V _{CC} = 2.7 V to 3.6 V	-	-	0.8	-	0.8	V
		V _{CC} = 4.5 V to 5.5 V	-	-	0.3V _{CC}	-	0.3V _{CC}	V
V _{OH}	HIGH-level output voltage	$V_{I} = V_{IH} \text{ or } V_{IL}$						
		I _O = -100 μA; V _{CC} = 1.2 V	-	1.2	-	-	-	V
		I _O = -100 μA; V _{CC} = 2.0 V	1.8	2.0	-	1.8	-	V
		I _O = -100 μA; V _{CC} = 2.7 V	2.5	2.7	-	2.5	-	V
		I _O = -100 μA; V _{CC} = 3.0 V	2.8	3.0	-	2.8	-	V
		I _O = -100 μA; V _{CC} = 4.5 V	4.3	4.5	-	4.3	-	V
		I_{O} = -6 mA; V_{CC} = 3.0 V	2.4	2.82	-	2.2	-	V
		l _O = -12 mA; V _{CC} = 4.5 V	3.6	4.2	-	3.5	-	V
V _{OL}	LOW-level output voltage	$V_{I} = V_{IH}$ or V_{IL}						
		I_{O} = 100 µA; V_{CC} = 1.2 V	-	0	-	-	-	V
		I_{O} = 100 µA; V_{CC} = 2.0 V	-	0	0.2	-	0.2	V
		I_{O} = 100 µA; V_{CC} = 2.7 V	-	0	0.2	-	0.2	V
		I_{O} = 100 µA; V_{CC} = 3.0 V	-	0	0.2	-	0.2	V
		I_{O} = 100 µA; V_{CC} = 4.5 V	-	0	0.2	-	0.2	V
		I_{O} = 6 mA; V_{CC} = 3.0 V	-	0.25	0.40	-	0.50	V
		I_0 = 12 mA; V_{CC} = 4.5 V	-	0.35	0.55	-	0.65	V
lı	input leakage current	V_{I} = V_{CC} or GND; V_{CC} = 5.5 V	-	-	1.0	-	1.0	μA
I _{CC}	supply current	$V_{I} = V_{CC}$ or GND; $I_{O} = 0$ A; $V_{CC} = 5.5$ V	-	-	20.0	-	40	μA
ΔI _{CC}	additional supply current	per input; $V_1 = V_{CC} - 0.6 V$; $V_{CC} = 2.7 V$ to 3.6 V	-	-	500	-	850	μA
CI	input capacitance		-	3.5	-	-	-	pF

[1] Typical values are measured at T_{amb} = 25 °C.

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10. Dynamic characteristics

Table 7. Dynamic characteristics

GND = 0 V; For test circuit see Fig. 7.

Symbol Parameter		Conditions		-40 °C to +85 °C			-40 °C to +125 °C		Unit
				Min	Typ[1]	Max	Min	Мах	
t _{pd}	propagation delay	nA to nY; see Fig. 6	[2]						
		V _{CC} = 1.2 V		-	40	-	-	-	ns
		V _{CC} = 2.0 V		-	14	20	-	25	ns
		V _{CC} = 2.7 V		-	10	15	-	19	ns
		V _{CC} = 3.0 V to 3.6 V; C _L = 15 pF	[3]	-	6	-	-	-	ns
		V _{CC} = 3.0 V to 3.6 V	[3]	-	8	12	-	15	ns
		V_{CC} = 4.5 V to 5.5 V		-	-	9	-	11	ns
C _{PD}	power dissipation capacitance	C_L = 50 pF; f _i = 1 MHz; V _I = GND to V _{CC}	[4]	-	21	-	-	-	pF

All typical values are measured at T_{amb} = 25 °C. [1]

[2]

 t_{pd} is the same as t_{PLH} and t_{PHL} . Typical values are measured at nominal supply voltage (V_{CC} = 3.3 V). [3]

 C_{PD} is used to determine the dynamic power dissipation (P_D in μ W). [4]

 $P_D = C_{PD} \times V_{CC}^2 \times f_i \times N + \Sigma (C_L \times V_{CC}^2 \times f_o)$ where:

f_i = input frequency in MHz, f_o = output frequency in MHz

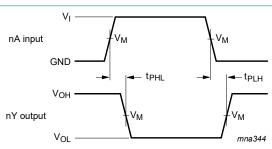
C_L = output load capacitance in pF

V_{CC} = supply voltage in V

N = number of inputs switching

 $\Sigma(C_L \times V_{CC}^2 \times f_o)$ = sum of the outputs.

10.1. Waveform and test circuit



Measurement points are given in Table 8.

 V_{OL} and V_{OH} are typical voltage output levels that occur with the output load.

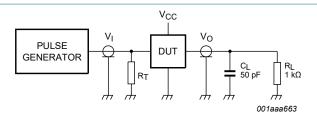
The input (nA) to output (nY) propagation delays Fig. 6.

Table 8. Measurement points

Supply voltage	Input	Output
V _{cc}	V _M	V _M
< 2.7 V	0.5V _{CC}	0.5V _{CC}
2.7 V to 3.6 V	1.5 V	1.5 V
≥ 4.5 V	0.5V _{CC}	0.5V _{CC}

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Test data is given in Table 9.

Definitions test circuit:

 R_{T} = Termination resistance should be equal to output impedance Z_{o} of the pulse generator.

R_L = Load resistance.

 C_L = Load capacitance including jig and probe capacitance.

Fig. 7. Test circuit for measuring switching times

Table 9. Test data

Supply voltage	nput		
V _{cc}	Vi	t _r , t _f	
< 2.7 V	V _{CC}	≤ 2.5 ns	
2.7 V to 3.6 V	2.7 V	≤ 2.5 ns	
≥ 4.5 V	V _{CC}	≤ 2.5 ns	

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11. Package outline

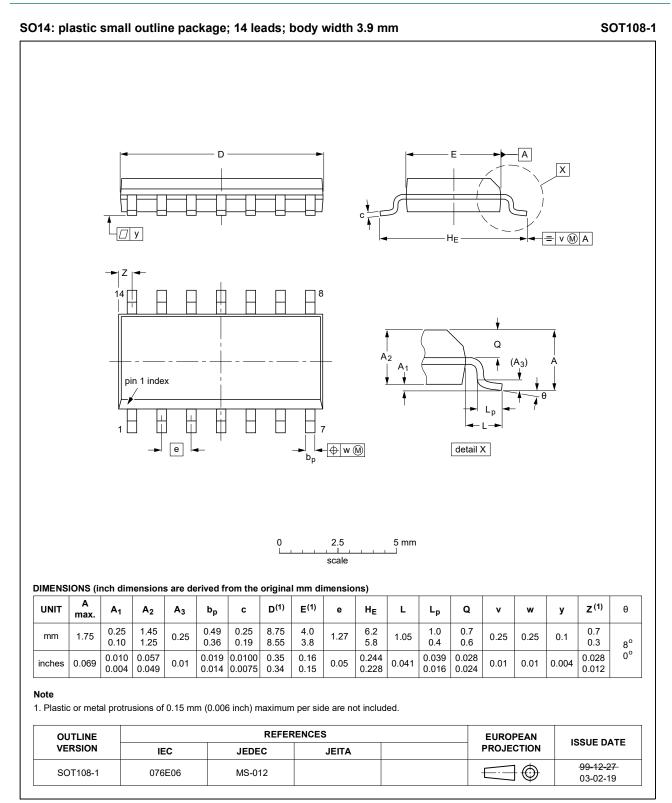


Fig. 8. Package outline SOT108-1 (SO14)

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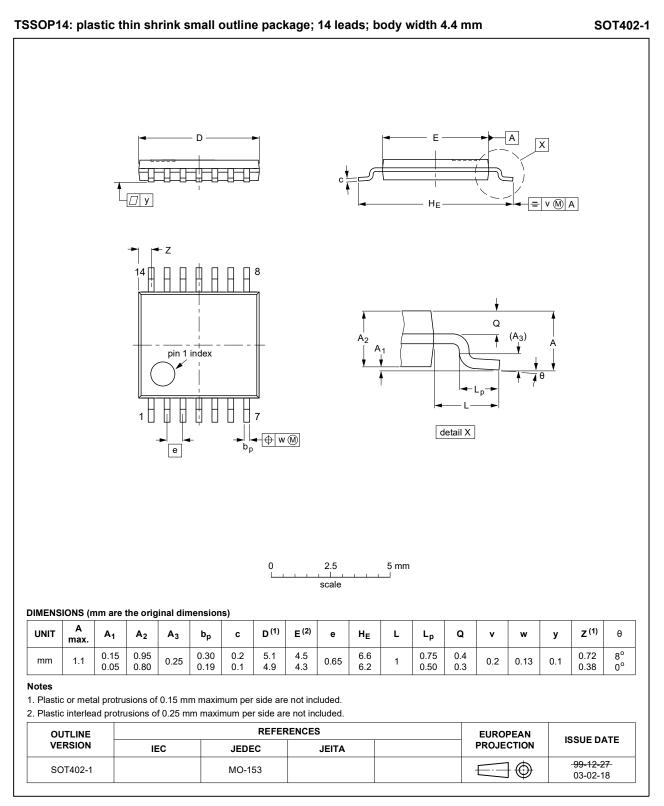


Fig. 9. Package outline SOT402-1 (TSSOP14)

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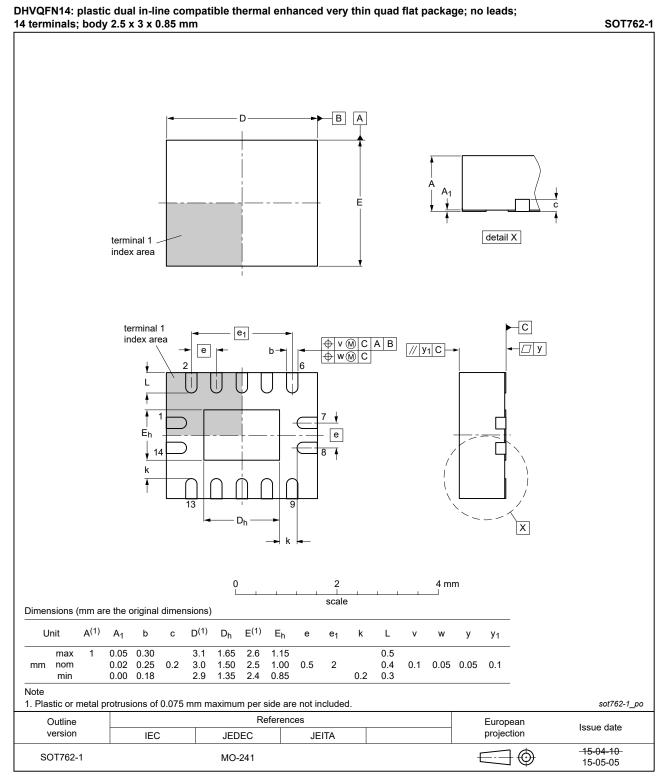


Fig. 10. Package outline SOT762-1 (DHVQFN14)

12. Abbreviations

Acronym	Description
CMOS	Complementary Metal Oxide Semiconductor
DUT	Device Under Test
ESD	ElectroStatic Discharge
HBM	Human Body Model
MM	Machine Model
TTL	Transistor-Transistor Logic

13. Revision history

Table 11. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes		
74LV04 v.5	20210913	Product data sheet	-	74LV04 v.4		
Modifications:	 Nexperia. Legal texts have bee Type number 74LV0 Section 1 and Section 	ata sheet has been redesion on adapted to the new con 4DB (SOT337-1/SSOP14 on <u>2</u> updated. values for P _{tot} total power	mpany name where appr I) removed.	opriate.		
74LV04 v.4	20151208	Product data sheet	-	74LV04 v.3		
Modifications:	Type number 74LV0	4N (SOT27-1) removed.				
74LV04 v.3	20071204	Product data sheet	-	74LV04 v.2		
Modifications:	 The format of this data sheet has been redesigned to comply with the new identity guidelines of NXP Semiconductors. Legal texts have been adapted to the new company name where appropriate. <u>Section 3</u>: DHVQFN14 package added. <u>Section 7</u>: derating values added for DHVQFN14 package. <u>Section 11</u>: outline drawing added for DHVQFN14 package. 					
74LV04 v.2	19980420	Product specification	-	74LV04 v.1		
74LV04 v.1	19970203	Product specification	-	-		

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14. Legal information

Data sheet status

Document status [1][2]	Product status [3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

 Please consult the most recently issued document before initiating or completing a design.

- [2] The term 'short data sheet' is explained in section "Definitions".
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